

SUPPORTED BY  
**ANR**

Ir fu  
cea  
saclay



# GET

Emanuel Pollacco IRFU/SPhN  
For the GET collaboration

## Systems for Nuclear Physics Today

1. Number of Channels Approx. 1,000
2. Short & Reconfigurable Experimental Setups with variety of Detector Types
3. Human & Financial Resources Low

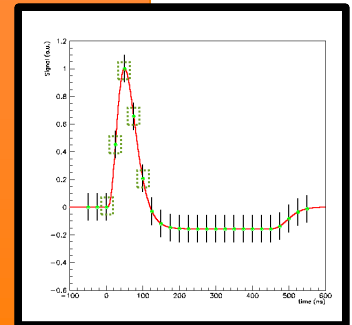
## Systems for Nuclear Physics Tomorrow

1. Number of Channels Approx. 20,000
2. Short & Reconfigurable ....
3. Human & ...

### Measure

1. TPC, Si, CsI ... (E & T via Charge Sampling),
2. Efficient Trigger
3. 1000 events/sec (TPC like)

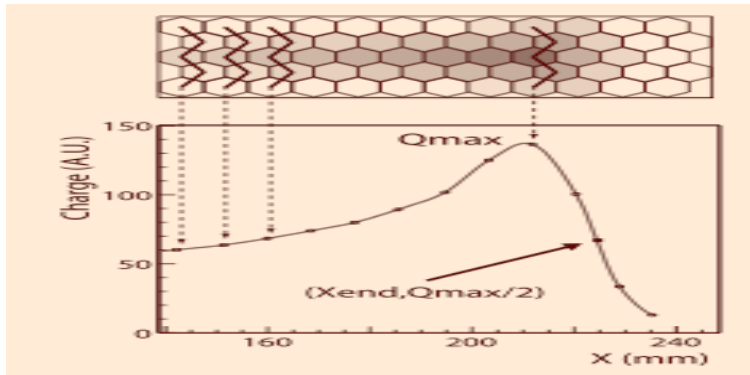
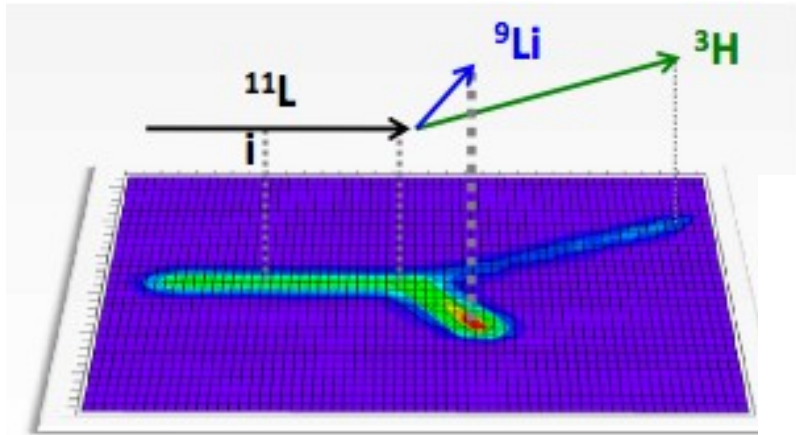
**Adapting Part. Phys. Techniques**



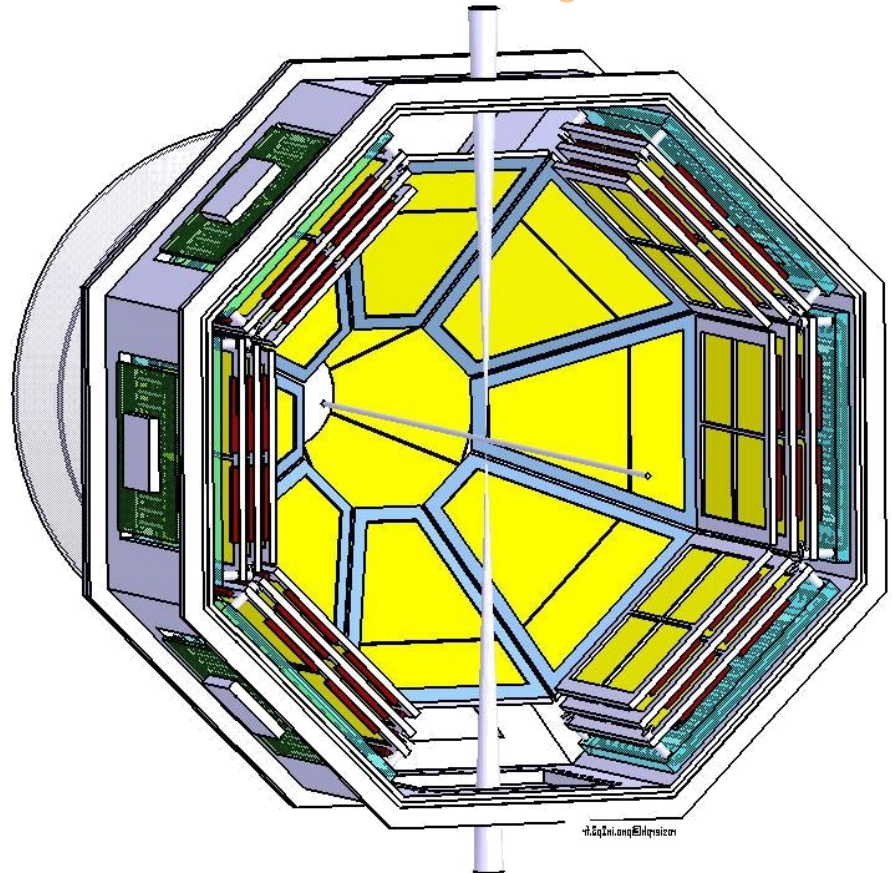
# Active Target - 20Kch

&

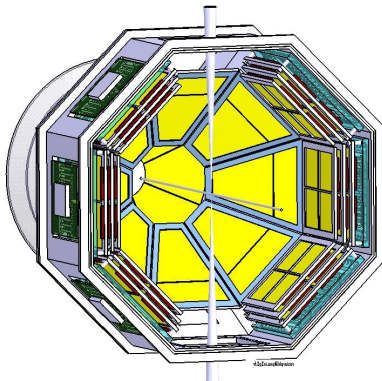
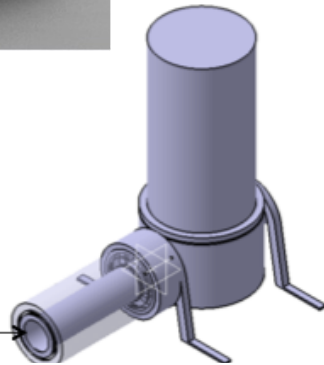
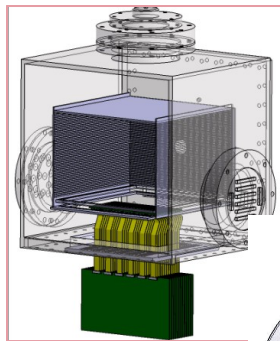
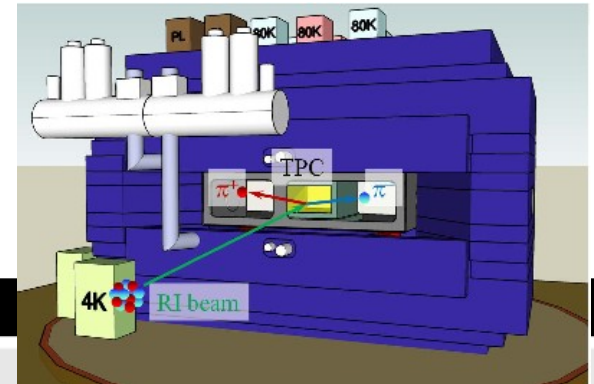
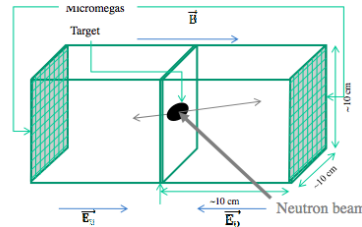
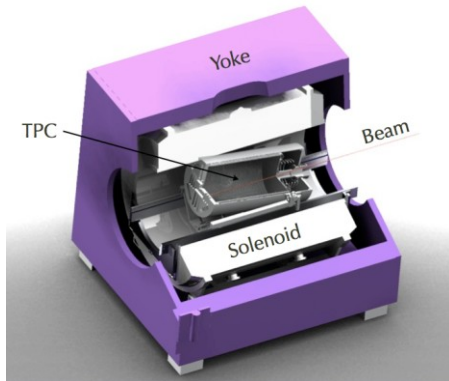
Si 4pi - 12K ch



Bragg trace measure



# Systems to be covered by GET



## Projects employing GET

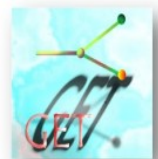
- ACTAR (GANIL, IRFU, IPNO, SFTC, ...) – Micromegas + Si – 20k channels
- 2p-TPC (CENBG) – GEM/Micromegas – 20k channels
- AT-TPC (MSU, LBL ...) – Micromegas – 12k channels
- GASPARD (GANIL, IRFU, IPNO, ...) – Si & CsI – 15k channels
- BTD (IRFU & GANIL) – 100 channels
- SAMURAI-TPC (RIKEN) – Micromegas -15k channels
- FORFIRE – IRFU – Industry
- Test system - IRFU

## Under Study use of GET/ GET modules

- S3 – (SPIRAL2+IRFI+...) – Si/gas tracker - 500 channels
- MINOS → (p;2p,  $\gamma$ ) - (IRFU)– Micromegas - 8k channels
- FIDIAS (IRFU) – Micromegas 5K Channels (IRFU)

**100 K  
Channels  
Gas, Si & CsI**

**→ GENERIC**

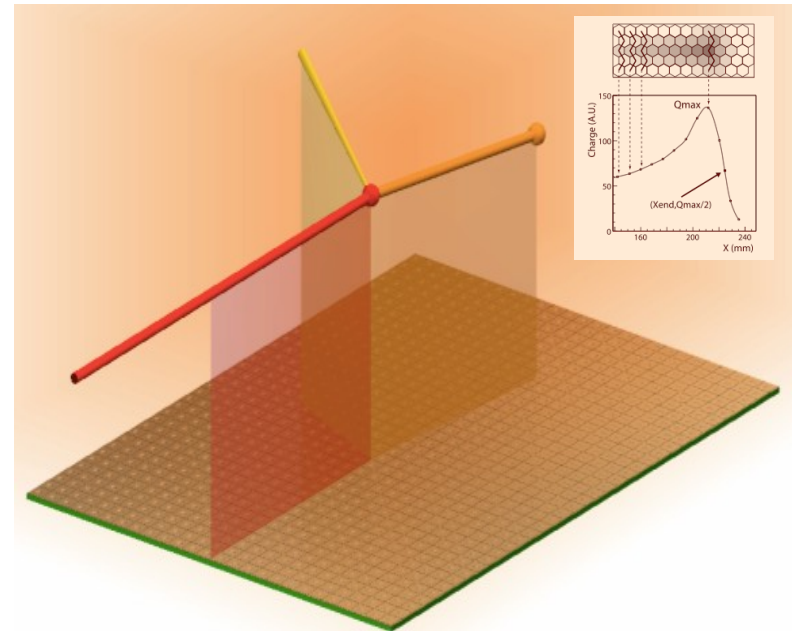


# GET Project Objectives

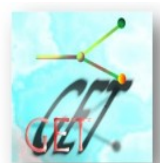
- Develop for Nucl. Physics :- Full Data Acquisition system for
  - Active Targets(Target = Gas). → Nucl. Spec & Astrophys. with Radio active Beams
  - TPC → Exotique Decay & EoS with RABs

Require

- **Low detection thresholds (A,Z, E, The, Phi)**  
**for slow ions** ( below 300KeV),
  - **Dynamic range ( $\sim Z^2$ ),**
  - High Luminosity & Solid Angle,
  - Effective Internal TPC Trigger,
  - Gas & pressure ( $H_2, D_2, ^3He, He \dots$  )
  - Different detector Systems,
  - Pad density (25-100 pads/cm<sup>2</sup>)
- Opportunity to develop a **generic /reconfigurable** system approach for Nucl. Phys. to cover **medium size systems** (256 – 32K channels).



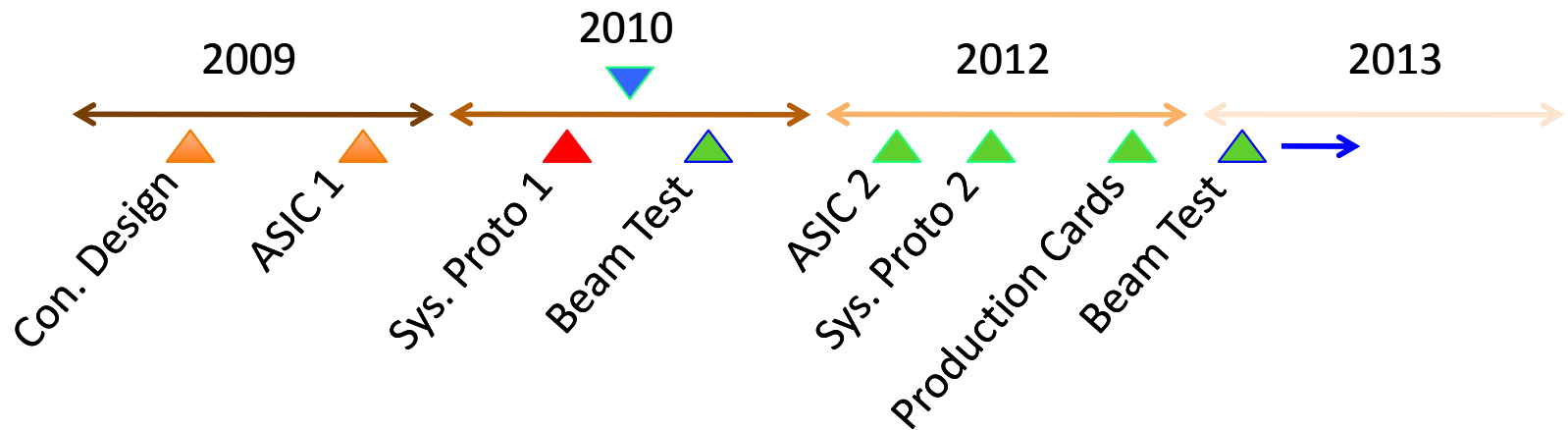
→ **This is an experimental system**





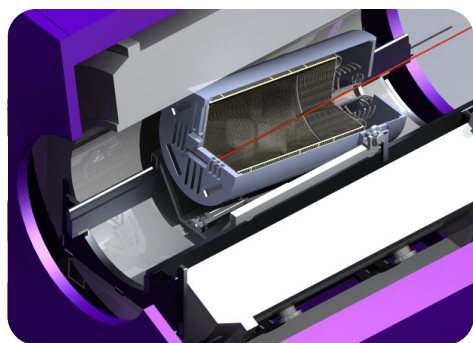
# GET Project

R&D Financed 75% (France)  
25% (US)

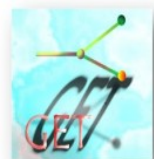
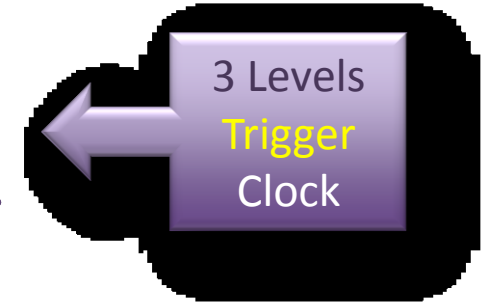
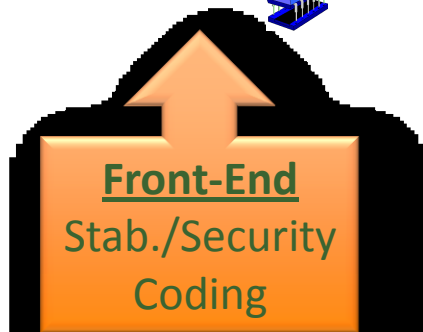
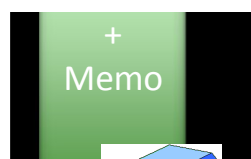
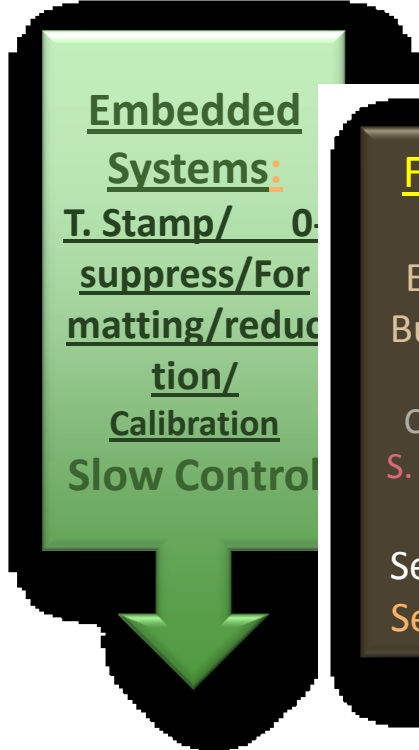


# SYSTEM GET

## Conceptuel Design

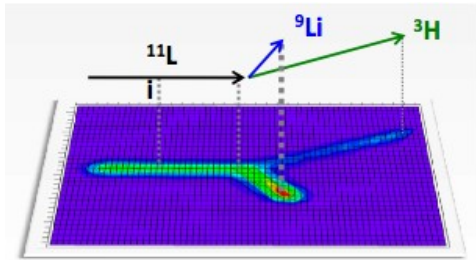


AT-TPC



# SYSTEM GET

## Conceptuel Design



irfu  
cea  
saclay-

irfu  
cea  
saclay

irfu  
cea  
saclay

GANIT  
Laboratoire commun CEA/IRFU/SPHn

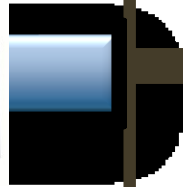
ZAP-PAC

**AsAd**  
ASIC  
ADC  
FPGA  
PULSER  
T/μ

NSCL

**CoBo**  
FPGA

**Mutant**  
Trigger  
FPGA



irfu  
cea  
saclay



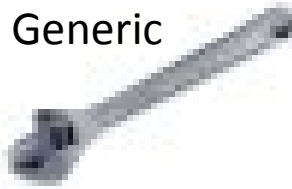
GANIT  
Laboratoire commun CEA/IRFU/SPHn

GANIT  
Laboratoire commun CEA/IRFU/SPHn

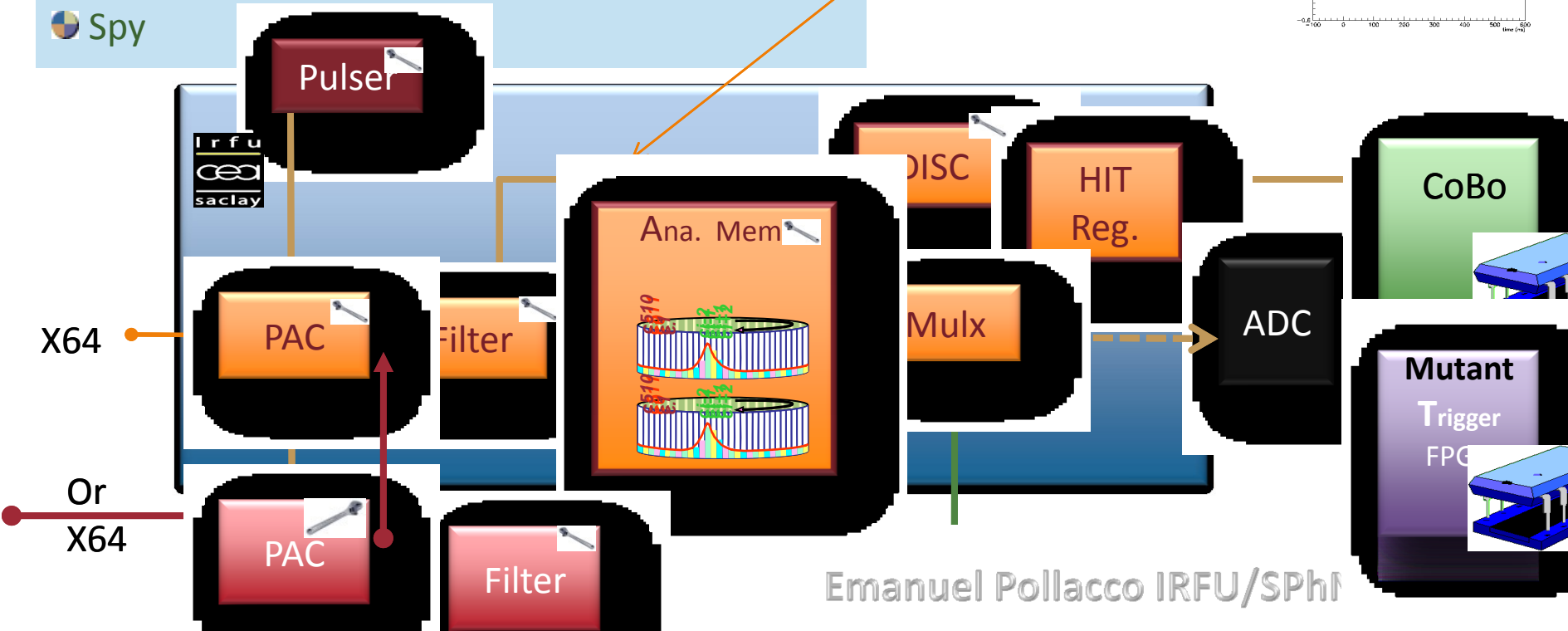
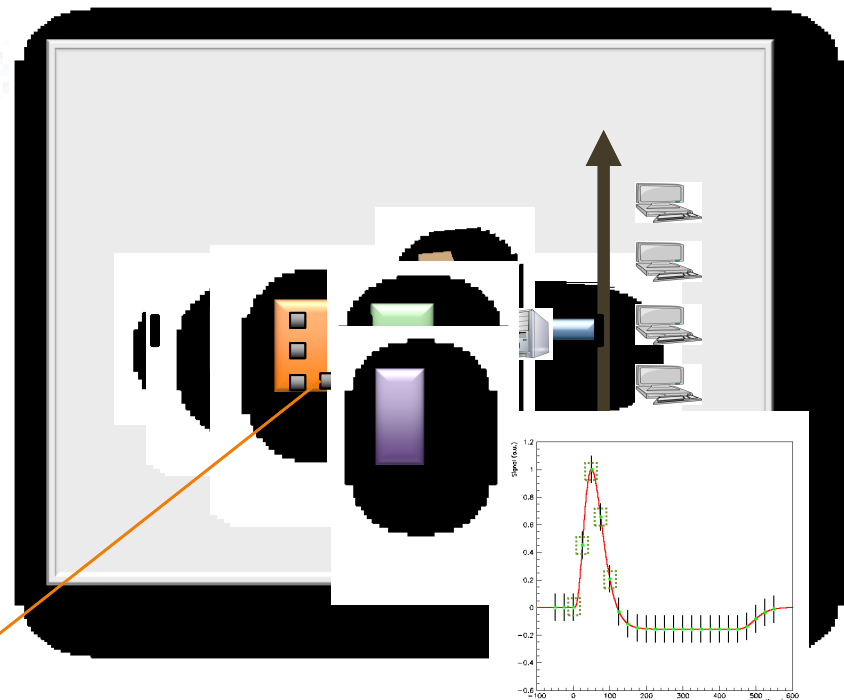


# Asic AGET

Generic



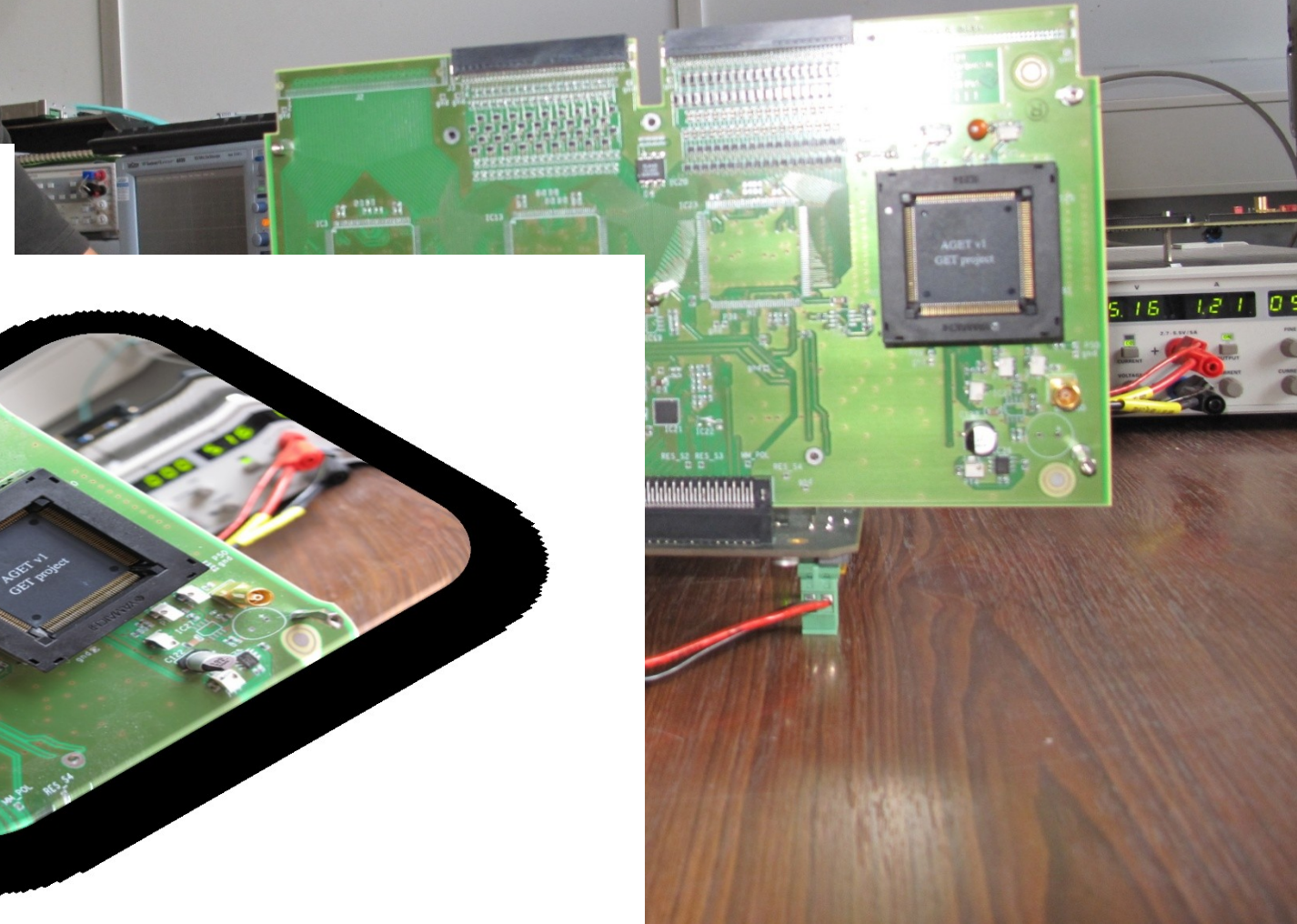
- CMOS 0.35 $\mu$ m
- Int./Ext. PAC &/or Filter
- Gain & Disc/channel  $\rightarrow$  120, 240 fC, 1, 10 pC.
- Shaping 50-1000 nsec
- Sampling rate 1-100MHz  $\rightarrow$  25MHz ADC 12/14bits
- Selective Readout – Hit Reg.
- Windowed SCA readout  $\rightarrow$  128/256/512 or variable
- 2 fast time- consecutive SCA windows
- Pulser facilities
- Spy



Emanuel Pollacco IRFU/SPhI



Pascal Baron  
IRFU/SeDi

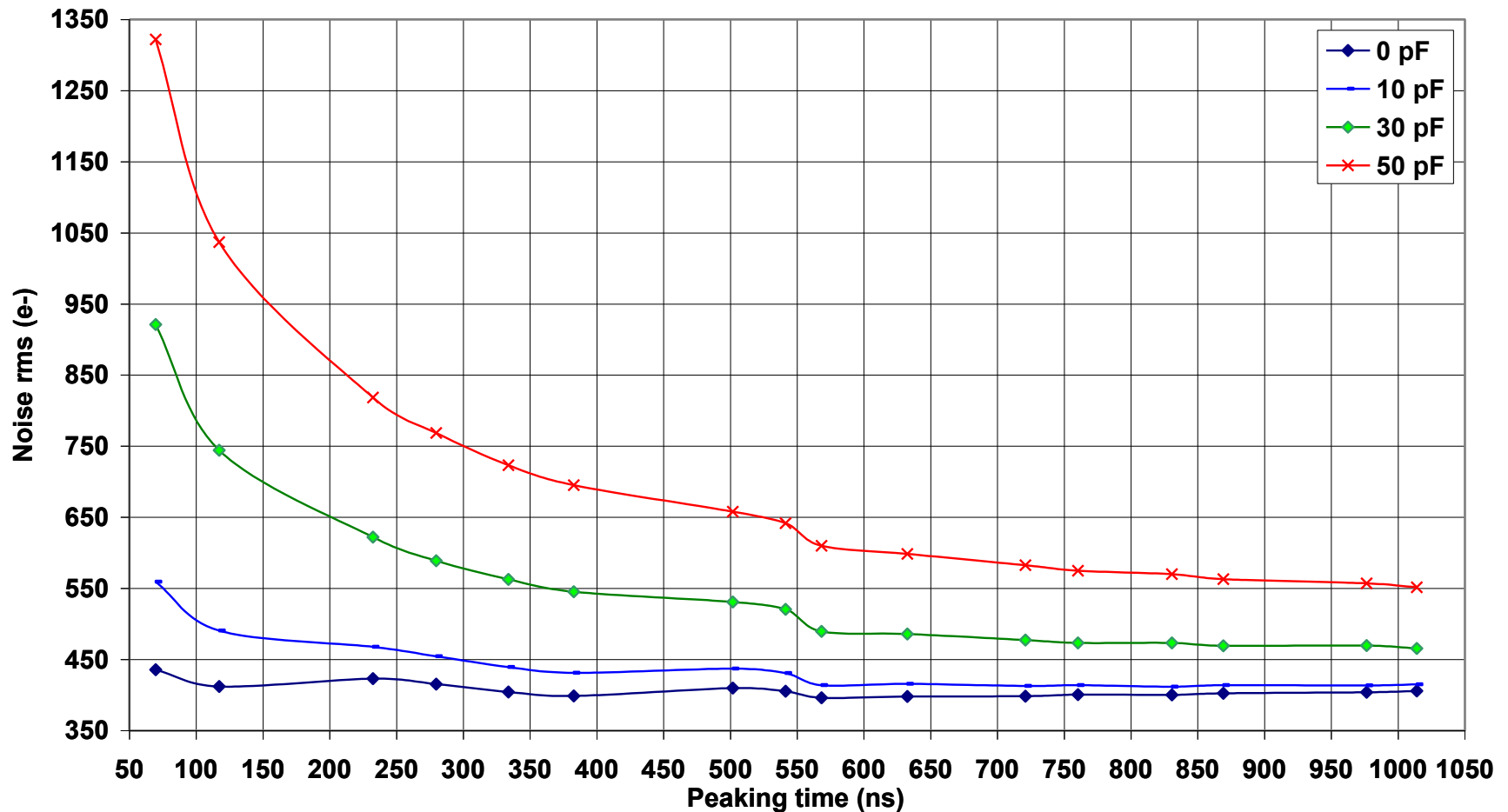


# AGET: Charge Channel

- Some numbers: Simulation results

**Charge resolution:** versus input capacitor and peaking time

120 fC range



**ANALYSIS**

Stored Cell Number: 7  
Stored Cell Width: 512  
Processed Cell Number: 7  
Processed Cell Width: 512

**ASIC To Study**

- ASIC 0
- ASIC 1
- ASIC 2
- ASIC 3

**Data Process**

ON

Instr Nbr: 33

ASIC Nbr: 0  
Begin Canal: 2  
End Canal: 69

**DAC values to change generator amplitude**

Levels Array: 0 3FFF  
Incr/Array: Incr  
Begin Level: 3FFF End Level: 0  
Index: 1000

**Init values for first script**

Start Value of DAC: BFFF End Value of DAC: 8A11

**TRIGGER WINDOW**

Threshold: 231  
First Cell Number: 7  
Cell Width: 508

**Acquisition**

ON

Stop Trigger: OFF

Trigger Running...  
 RUNNING....

```

pokes 0x1A 0x0080
fem 0
fec 0
aget 0 write 1 0x3A 0x45FD
aget 0 write 2 0x28 0xA100
aget 0 write 3 0x3 0xFFFF 0xFFFF
aget 0 write 4 0x3 0xFFFF 0xFFFF
aget 0 write 6 0x0 0x0 0x0
aget 0 write 7 0x0 0x0 0x0
aget 0 write 8 0xFFFF 0xFFFF 0xFFFF 0xFFFF 0xFFFF 0xFFFF
0xFFFF 0xFFFF 0xFFFF
aget 0 write 9 0xFFFF 0xFFFF 0xFFFF 0xFFFF 0xFFFF
0xFFFF 0xFFFF 0xFFFF
aget 0 write 10 0x0 0x0 0x0 0x0
aget 0 write 11 0x0 0x0 0x0 0x0
aget 0 write 12 0x0
pokeb 0x5 0x0001
pokeb 0x4 0x00FE
pokes 0x14 0x0000
pokes 0x8 0x4000
pulser delay 0x091E
ped 0 0 2 0xC8
ped 0 0 3 0xC8
ped 0 0 4 0xC8
ped 0 0 5 0xC8
ped 0 0 6 0xC8
ped 0 0 7 0xC8
ped 0 0 8 0xC8
ped 0 0 9 0xC7
  
```

hitRegisterRead:  ON

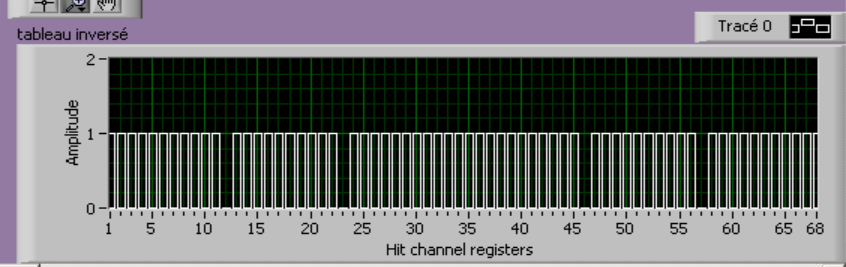
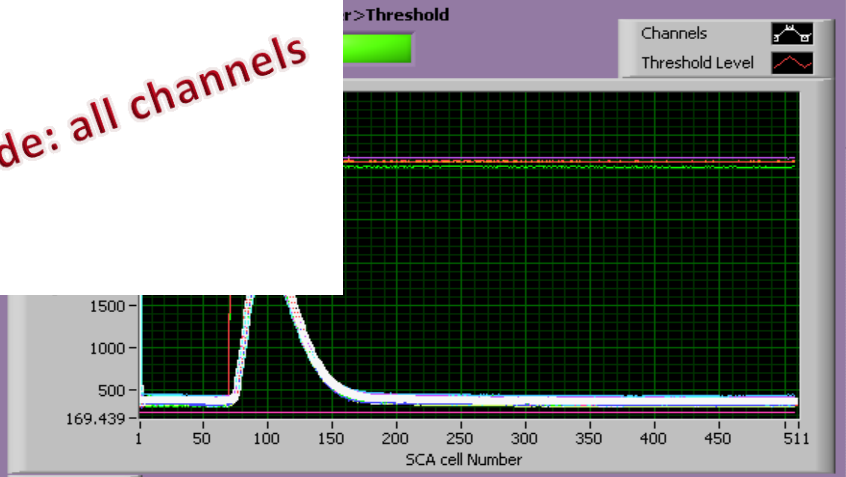
SAVE OF DATAS

**XML file path**: F:\perturb.xml

**rawdata file**: D:\DAQSOFT\TestBench\ProgTest\Result\Essai\_xml4asic.csv

**File with processed data**: <Pas un chemin>

**Functional mode: all channels**



**XML Error Log**

état	code	source
✓	0	





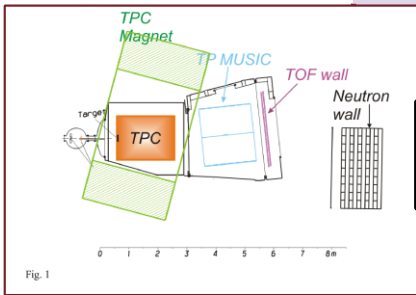
# EMC, Connectors, Cables, Temp. Monitoring & Security



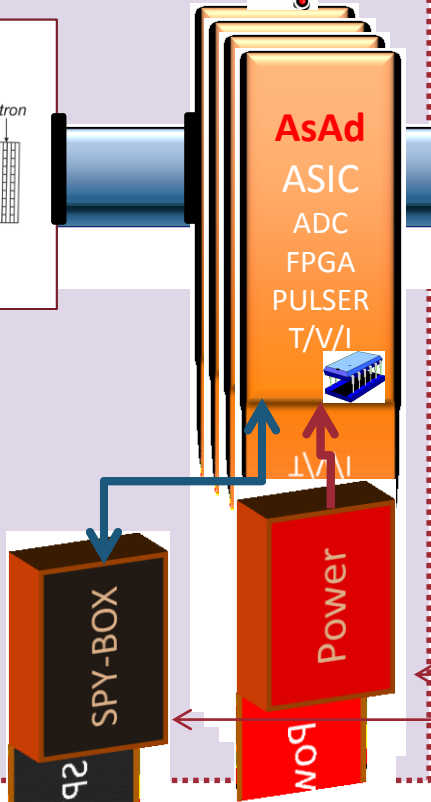
Cooling Study

CEM Study

SAMURAI-TPC



Power Supplies Stud

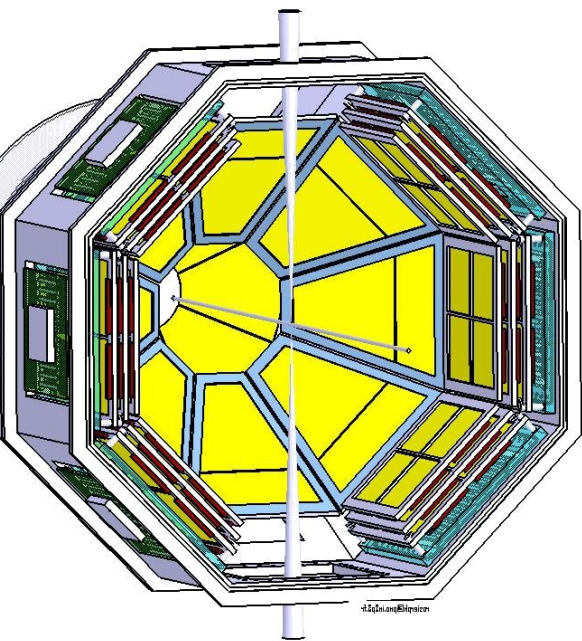


Emanuel Pollacco IRFU/SPhN

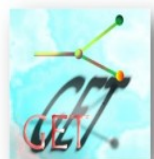
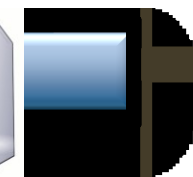
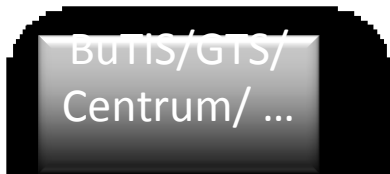
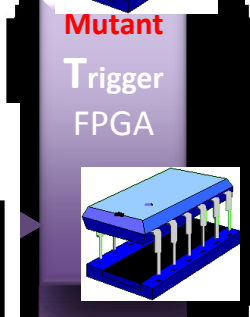
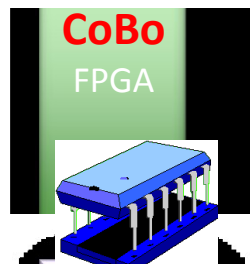
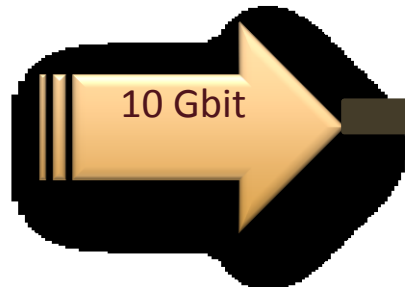
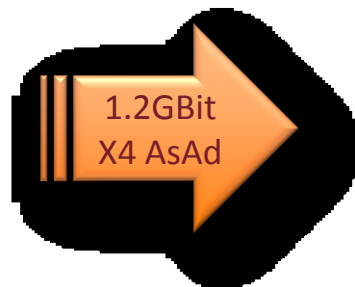
# Band Width & Trigger

**Common Dead Time  
Or  
Individual AsAd Dead-Time**

$10^{-12}$



**GASPARD**





# MUTANT (Multiplicity Trigger and Time stamp)

Nucl. Phys. Have Limited Experience → Scenarios/Simul.

## 4-level triggers

L0: External trigger

L1: Time dependent Multip. trigger

→ Self Trigger, ...

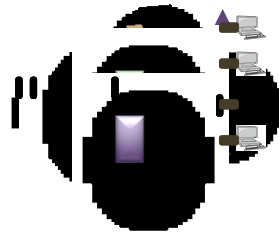
L2: Hit Pattern trigger → Self Trigger, calculated read pattern ...

L3: Soft trigger

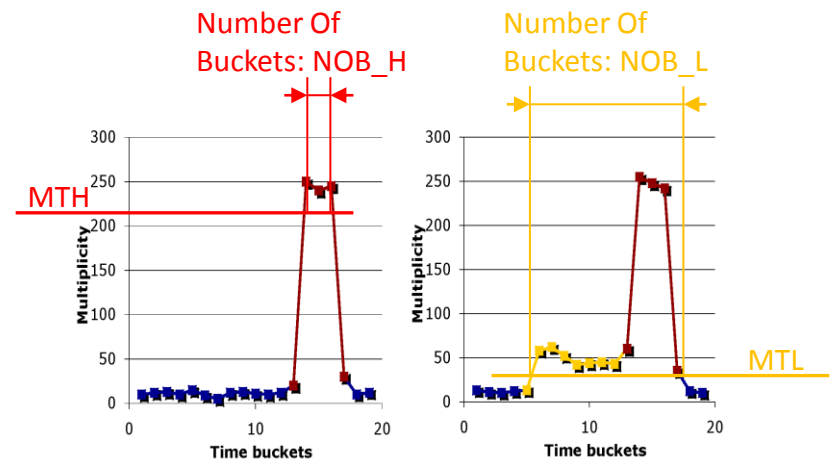
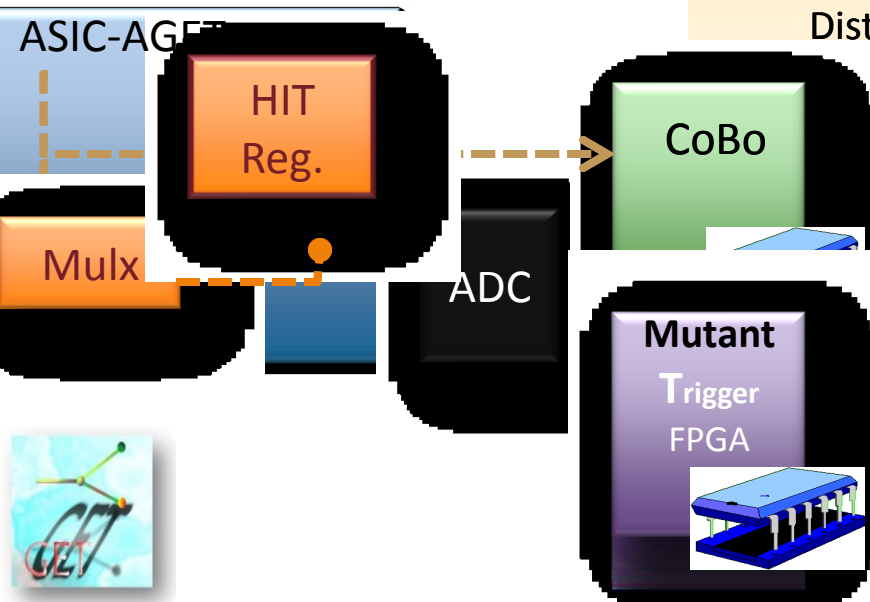
Compute the digital trigger from CoBos (25MHz)

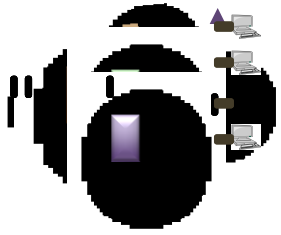
Time stamp (48b, 10ns) and event N° (32b)

Distribute the 100MHz clock for the synchronisation

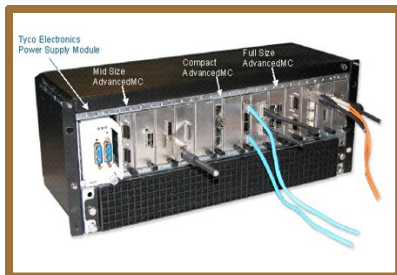
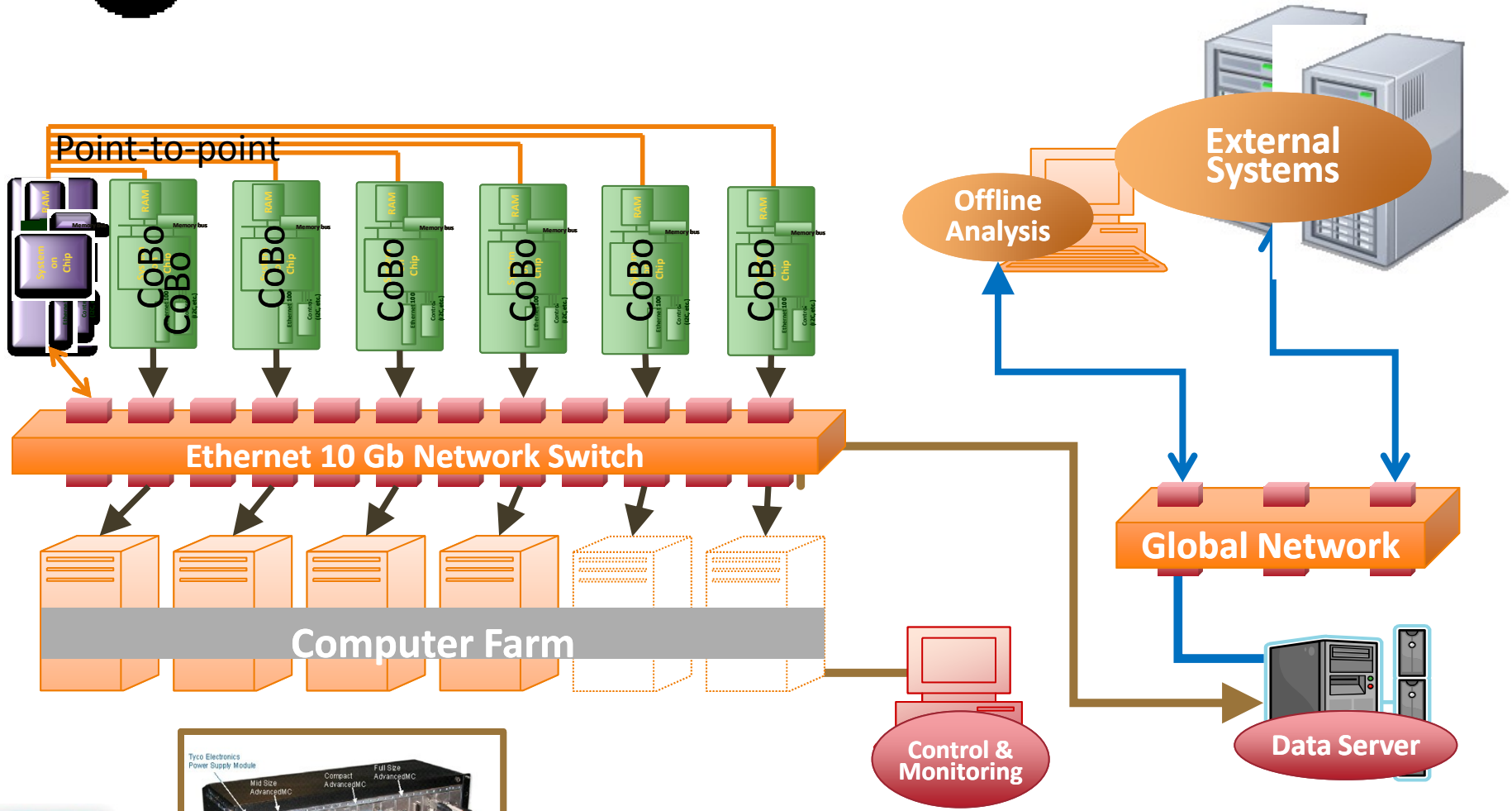


Trigger Building  
Data Transfer

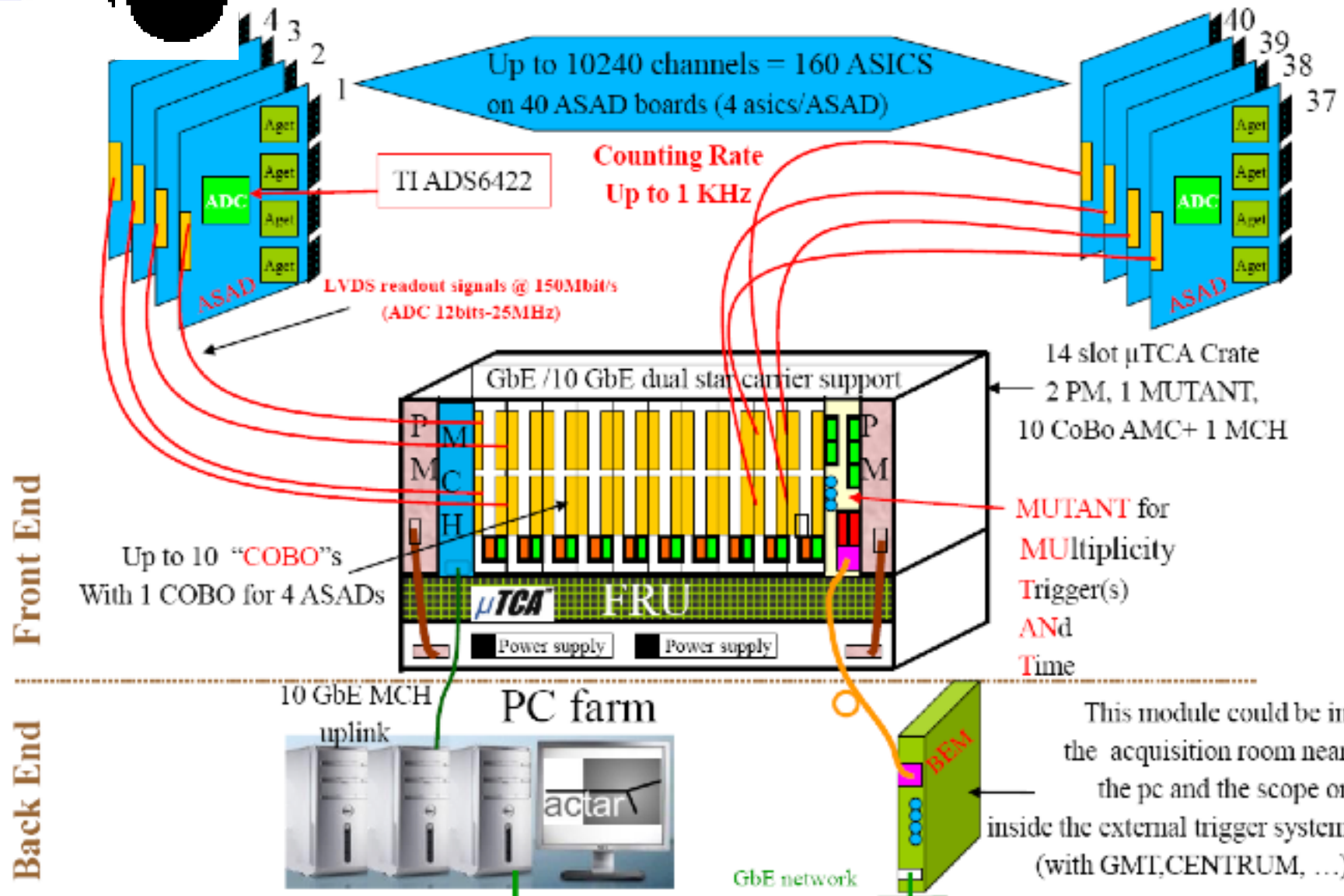




# Global View of DAQ Hardware Infrastructure



# 1 $\mu$ TCA shelf typical architecture

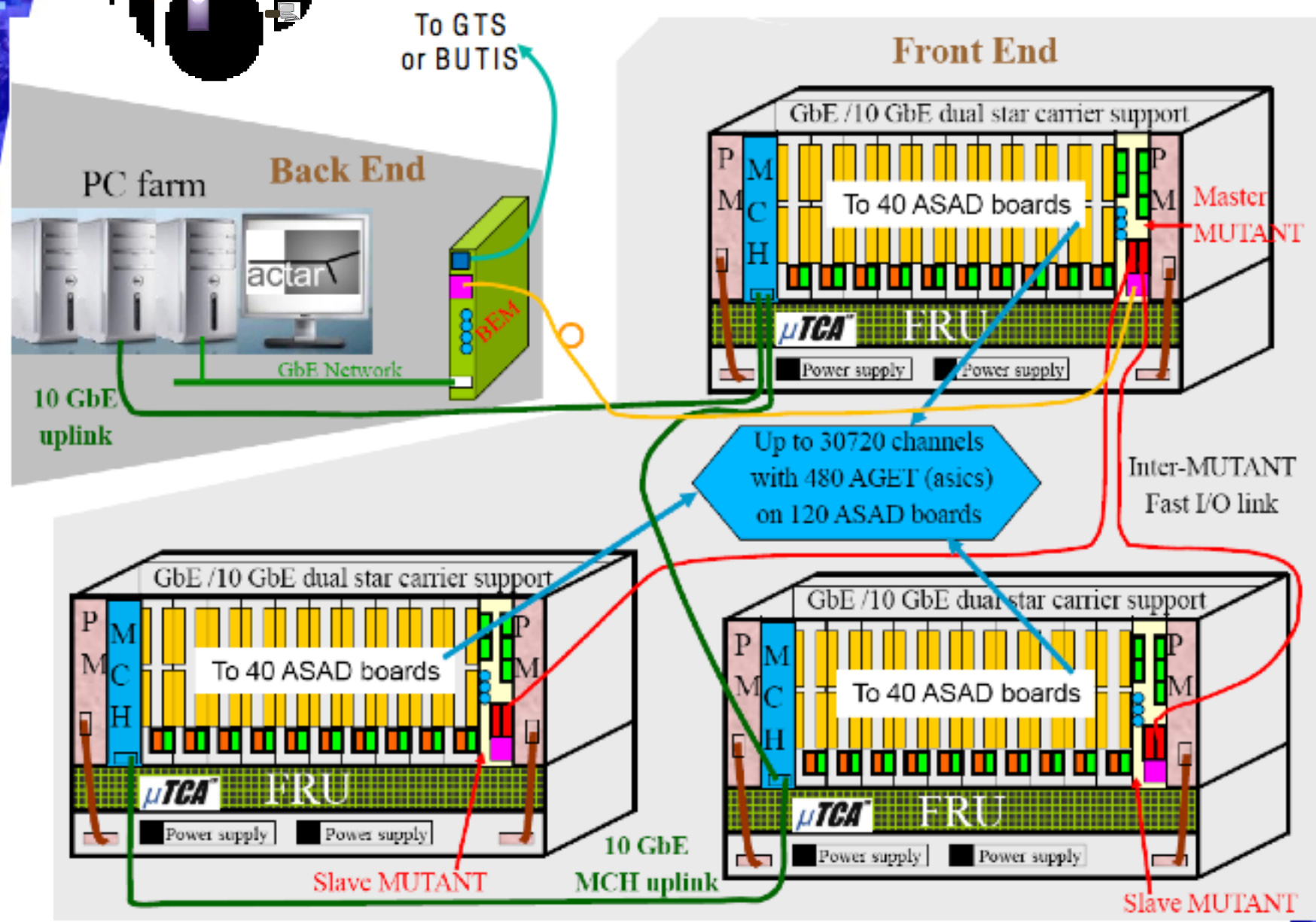
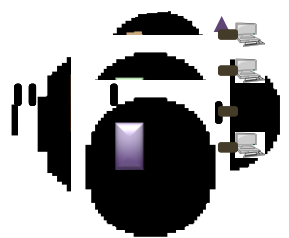


Front End

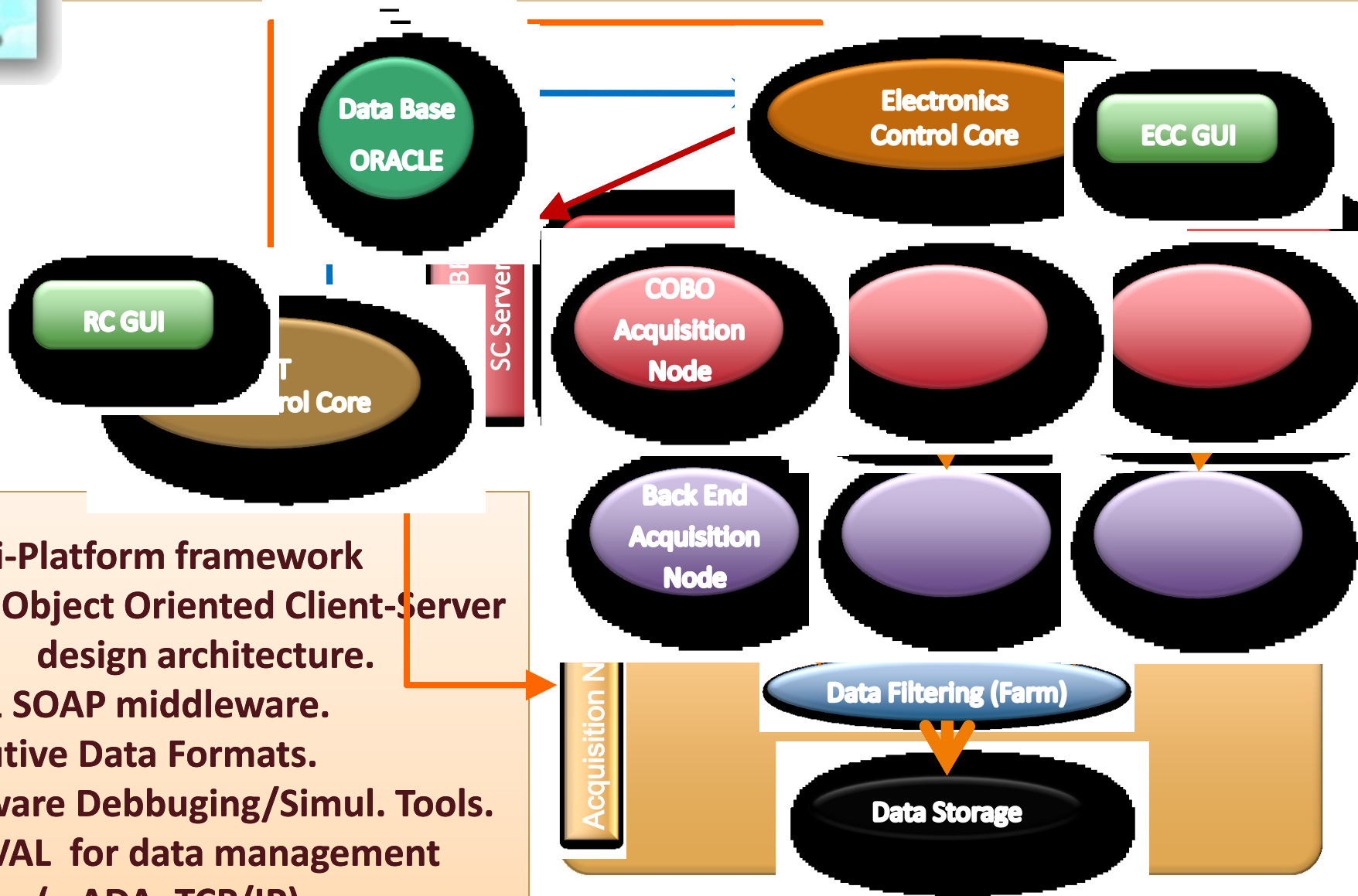
Back End

This module could be in the acquisition room near the pc and the scope or inside the external trigger system (with GMT, CENTRUM, ...)

# Full architecture – 3 $\mu$ TCA shelves



# Software/Firmware developments



- Multi-Platform framework
- Fully Object Oriented Client-Server design architecture.
- ICE & SOAP middleware.
- Evolutive Data Formats.
- Software Debbing/Simul. Tools.
- NARVAL for data management (- ADA, TCP/IP).

# Reconfigurable Approach

Via:- Hardware - Software Architecture  
*Documentation & Simulation tools*

Genericity → Multi-Platform (Linux, VxWorks,  
Windows, Mac) framework

Fully Object Oriented Client-Server design architecture.

ICE & SOAP middleware.

Evolutionary Data Formats.

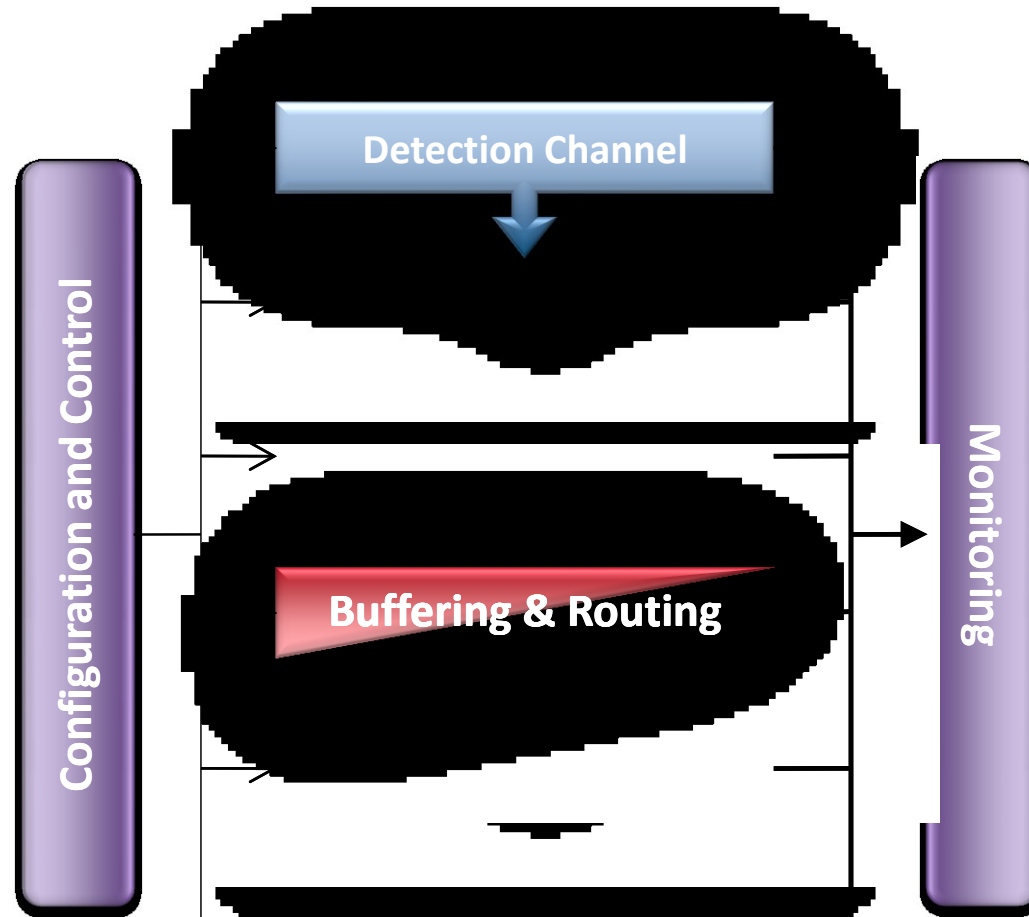
Software Développement /Debugging/Simulation Tools.

NARVAL for data management (NARVAL – ADA, TCP/IP).



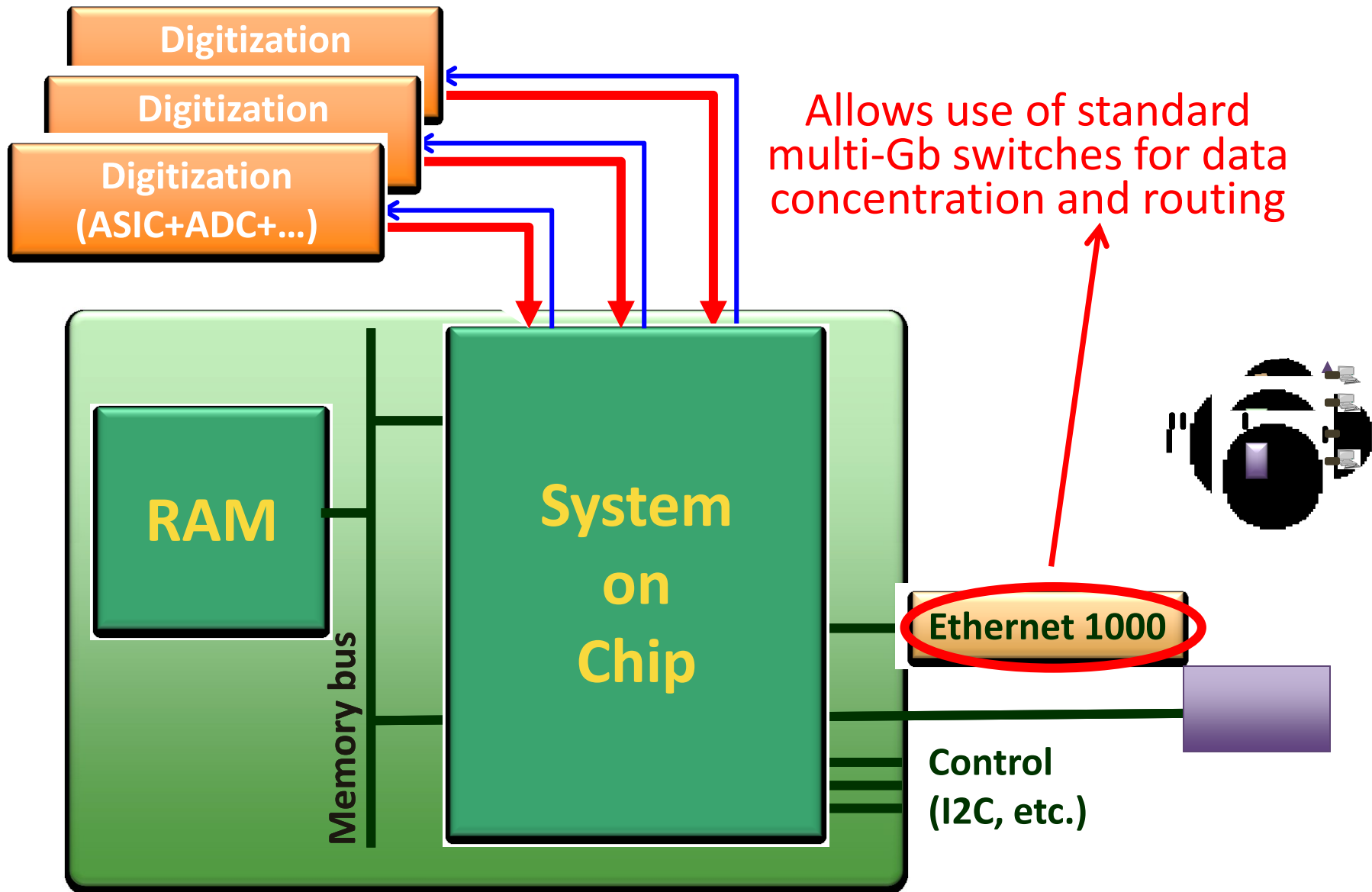
**END**

# Control, Acquisition & Online Processing



Hardware  
Firmware  
Software

# Embedded Implementation (Upstream)



Polarity of detector signal	Negative or Positive
External Preamplifier	Yes; access to the filter or SCA inputs
<b>Charge measurement</b>	
Input dynamic range	120 fC; 1 pC; 10 pC
Output dynamic range	2V p-p
Resolution	< 850 e- (Charge range: 120fC; Peaking Time: 200ns; Cinchannel. < 30pF)
<b>Sampling</b>	
Peaking time value	50 ns to 1 $\mu$ s (16 values) [new]
Sampling Frequency	1 MHz to 100 MHz
<b>Time resolution</b>	
Jitter	60 ps rms
<b>Trigger</b>	
Discriminator solution	L.E.D
Dynamic range	5% of input charge range
Threshold value	4-bit DAC/channel + (3-bit + polarity bit) common DAC
<b>Readout</b>	
Readout frequency	20 MHz to 25 MHz
SCA Readout mode	512 cells; 256 cells; 128 cells
<b>Test</b>	
calibration	1 channel / 64; external test capacitor
functional	1, few or 64 channels; internal test capacitor/channel
<b>Counting rate</b>	< 1 kHz
Power consumption	< 10 mW / channel

# Number Channelling

1 - 32,000

256

TRIG

10240

PAC

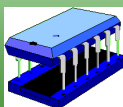
AsAd

ASIC  
ADC  
FPGA  
PULSER  
T/V/I

1M1  
b02EB

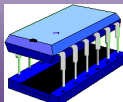
CoBo

FPGA

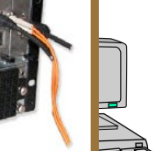


Mutant

Trigger  
FPGA

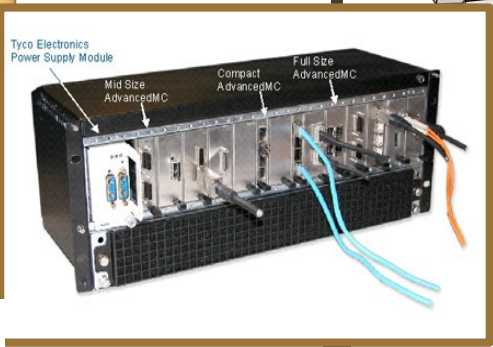


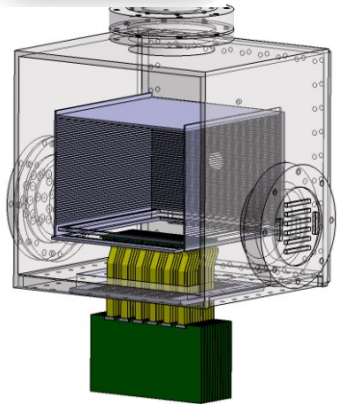
μ - T C A



AT-TPC

Channel Number –  
can be increased

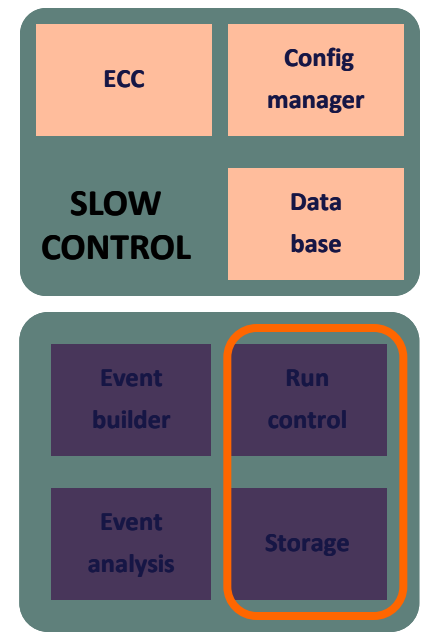
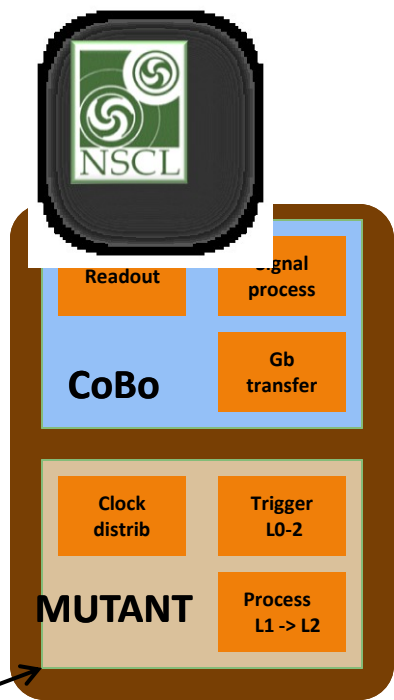




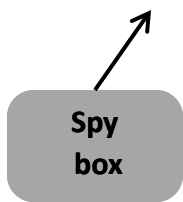
**Front-end boards**  
 Asic+ADC  
 HV, I, T monitoring

**Data Readout & Trig**  
 Zero suppress  
 Time stamp  
 3-Level trigger

**DAQ & Slow control**  
 Run control  
 Online analysis  
 Electronics control

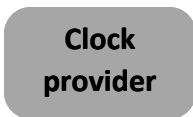


Inspection box  
 time alignment  
 (Riken)



**ASAD**

Time reference  
 (GSI Butis)



Micro-TCA standard