SUPPORTED BY ANR

Irfu  
CEA  
saclay

NSCL

Riken Nishina Center

Emanuel Pollacco IRFU/SPhN
For the GET collaboration
Systems for Nuclear Physics Today

1. Number of Channels Approx. 1,000
2. Short & Reconfigurable Experimental Setups with variety of Detector Types
3. Human & Financial Resources Low

Systems for Nuclear Physics Tomorrow

1. Number of Channels Approx. 20,000
2. Short & Reconfigurable ...
3. Human & ...

Measure

1. TPC, Si, CsI ... (E & T via Charge Sampling),
2. Efficient Trigger
3. 1000 events/sec (TPC like)

Adapting Part. Phys. Techniques
Active Target - 20Kch

&

Si 4pi - 12K ch

Bragg trace measure
Projects employing GET

- ACTAR (GANIL, IRFU, IPNO, SFTC, ...) – Micromegas + Si – 20k channels
- 2p-TPC (CENBG) – GEM/Micromegas – 20k channels
- AT-TPC (MSU, LBL ...) – Micromegas – 12k channels
- GASPARD (GANIL, IRFU, IPNO, ...) – Si & CsI – 15k channels
- BTD (IRFU & GANIL) – 100 channels
- SAMURAI-TPC (RIKEN) – Micromegas -15k channels
- FORFIRE – IRFU – Industry
- Test system - IRFU

Under Study use of GET/GET modules

- S3 – (SPIRAL2+IRFI+) – Si/gas tracker - 500 channels
- MINOS \( \rightarrow \) \( (p;2p, \gamma) \) - (IRFU) – Micromegas - 8K channels
- FIDIAS (IRFU) – Micromegas 5K Channels (IRFU)
GET Project Objectives

• Develop for **Nucl. Physics** :- Full Data Acquisition system for
  – Active Targets (Target = Gas). → Nucl. Spec & Astrophys. with Radio active Beams
  – TPC → Exotique Decay & EoS with RABs

Require
  – Low detection thresholds \((A,Z, E, \text{The, Phi})\) for slow ions (below 300KeV),
  – Dynamic range \((\sim Z^2)\),
  – High Luminosity & Solid Angle,
  – Effective Internal TPC Trigger,
  – Gas & pressure \((H_2, D_2, {}^3\text{He}, \text{He} \ldots)\)
  – Different detector Systems,
  – Pad density \((25-100 \text{ pads/cm}^2)\)

• Opportunity to develop a **generic /reconfigurable** system approach for Nucl. Phys. to cover medium size systems \((256 – 32K \text{ channels})\).

→ This is an experimental system
GET Project

R&D Financed 75% (France)
25% (US)
SYSTEM GET
Conceptual Design

Embedded Systems:
- T. Stamp/
- 0:
- suppress/Formatting/reduction/
- Calibration
- Slow Control

FARM
- L-3
- Event-Building
- Data
- Control
- S. Control
- Web
- Services
- Security

Very FE
- Pre-amp/
- Protection

Front-End
- Stab./Security
- Coding

3 Levels
- Trigger
- Clock

Emmanuel Pollacco IRFU/SPhN
SYSTEM GET
Conceptuel Design

ACTAR

ZAP-PAC

AsAd
ASIC
ADC
FPGA
PULSER
T/V/I

CoBo
FPGA

Mutant
Trigger
FPGA

Emanuel Pollacco IRFU/SPhN
Asic AGET

- CMOS 0.35µm
- Int./Ext. PAC &/or Filter
- Gain & Disc/channel → 120, 240 fC, 1, 10 pC.
- Shaping 50-1000 nsec
- Sampling rate 1-100Mhz → 25MHz ADC 12/14bits
- Selective Readout – Hit Reg.
- Windowed SCA readout → 128/256/512 or variable
- 2 fast time-consecutive SCA windows
- Pulser facilities
- Spy
Pascal Baron
IRFU/SeDi
Some numbers: Simulation results

**Charge resolution:** versus input capacitor and peaking time

120 fC range

![Graph showing charge resolution versus peaking time for different input capacitors](image-url)
Functional mode: all channels
EMC, Connectors, Cables, Temp. Monitoring & Security
Band Width & Trigger

Common Dead Time
Or
Individual AsAd Dead-Time

GASPARD

BuTIS/GTS/Centrum/...

Emanuel Pollacco IRFU/SPhN
MUTANT (Multiplicity Trigger and Time stamp)


4-level triggers

L0: External trigger
L1: Time dependent Multip. trigger ➔ Self Trigger, ...
L2: Hit Pattern trigger ➔ Self Trigger, calculated
  read pattern ...
L3: Soft trigger

Compute the digital trigger from CoBos (25MHz)

Time stamp (48b, 10ns) and event N° (32b)

Distribute the 100MHz clock for the synchronisation
Global View of DAQ Hardware Infrastructure

Point-to-point

Ethernet 10 Gb Network Switch

Computer Farm

External Systems

Offline Analysis

Global Network

Control & Monitoring

Data Server

Shebli ANVAR, CEA Irfu
1 µTCA shelf typical architecture

Up to 10240 channels = 160 ASICs on 40 ASAD boards (4 asics/ASAD)

Counting Rate
Up to 1 KHz

LVDS readout signals @ 150Mbit/s
(ADC 12bits-25MHz)

14 slot µTCA Crate
2 PM, 1 MUTANT,
10 CoBo AMC + 1 MCH

MUTANT for
MULTiplicity
Trigger(s)
AND
Time

Up to 10 "COBO"s
With 1 COBO for 4 ASADs

PC farm

10 GbE MCH uplink

GbE network

This module could be in the acquisition room near the pc and the scope or inside the external trigger system (with GMT, CENTRUM, …)
- Multi-Platform framework
- Fully Object Oriented Client-Server design architecture.
- ICE & SOAP middleware.
- Evolutive Data Formats.
- NARVAL for data management (ADA, TCP/IP).
Reconfigurable Approach

Via:- Hardware - Software Architecture
Documentation & Simulation tools

Genericity ➔ Multi-Platform (Linux, VxWorks, Windows, Mac) framework
Fully Object Oriented Client-Server design architecture.
ICE & SOAP middleware.
Evolutive Data Formats.
Software Développement /Debbuging/Simulation Tools.
NARVAL for data management (NARVAL – ADA, TCP/IP).
END
Control, Acquisition & Online Processing

Control Flow

Data Flow

Detection Channel

Buffering & Routing

Configuration and Control

Monitoring

Hardware

Firmware

Software

Shebli ANVAR, CEA Irfu
Embedded Implementation (Upstream)

Digitization
Digitization
Digitization (ASIC+ADC+...)

System on Chip

RAM

Ethernet 1000

Control (I2C, etc.)

Allows use of standard multi-Gb switches for data concentration and routing

Shebli ANVAR, CEA Irfu
<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polarity of detector signal</td>
<td>Negative or Positive</td>
</tr>
<tr>
<td>External Preamplifier</td>
<td>Yes; access to the filter or SCA inputs</td>
</tr>
<tr>
<td>Charge measurement</td>
<td></td>
</tr>
<tr>
<td>Input dynamic range</td>
<td>120 fC; 1 pC; 10 pC</td>
</tr>
<tr>
<td>Output dynamic range</td>
<td>2V p-p</td>
</tr>
<tr>
<td>Resolution</td>
<td>&lt; 850 e- (Charge range: 120fC; Peaking Time: 200ns; Cinchannel. &lt; 30pF)</td>
</tr>
<tr>
<td>Sampling</td>
<td></td>
</tr>
<tr>
<td>Peaking time value</td>
<td>50 ns to 1 µs (16 values)</td>
</tr>
<tr>
<td>New</td>
<td></td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>1 MHz to 100 MHz</td>
</tr>
<tr>
<td>Time resolution</td>
<td></td>
</tr>
<tr>
<td>Jitter</td>
<td>60 ps rms</td>
</tr>
<tr>
<td>Trigger</td>
<td></td>
</tr>
<tr>
<td>Discriminator solution</td>
<td>L.E.D</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>5% of input charge range</td>
</tr>
<tr>
<td>Threshold value</td>
<td>4-bit DAC/channel + (3-bit + polarity bit) common DAC</td>
</tr>
<tr>
<td>Readout</td>
<td></td>
</tr>
<tr>
<td>Readout frequency</td>
<td>20 MHz to 25 MHz</td>
</tr>
<tr>
<td>SCA Readout mode</td>
<td>512 cells; 256 cells; 128 cells</td>
</tr>
<tr>
<td>Test</td>
<td></td>
</tr>
<tr>
<td>calibration</td>
<td>1 channel / 64; external test capacitor</td>
</tr>
<tr>
<td>functional</td>
<td>1, few or 64 channels; internal test capacitor/channel</td>
</tr>
<tr>
<td>Counting rate</td>
<td>&lt; 1 kHz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt; 10 mW/channel</td>
</tr>
</tbody>
</table>
Number Channelling

1 – 32,000

AT-TPC

Channel Number – can be increased

Emanuel Pollacco IRFU/SPhN
Front-end boards
Asic+ADC
HV, I, T monitoring

Data Readout & Trig
Zero suppress
Time stamp
3-Level trigger

DAQ & Slow control
Run control
Online analysis
Electronics control

---

Inspection box
time alignment
(Riken)

Clock provider

Clock
provider

Spy
box

Time reference
(GSI Butis)

---

DAQ & Slow control

DAQ & Slow control

Event builder
Run control

Event analysis
Storage

---

Micro-TCA standard