Recent developments of HEP pixel detector readout chips

TIPP 2011

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LBNL
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Overview

- Pixel Detectors
  - Task and Design Principles
  - Hybrid Pixel Detectors at LHC
- Front-End Electronics for Hybrid Pixel Detectors
  - First generation at LHC: PSI46 and FEI3
  - Second generation: FEI4
  - R&D: 65nm technology
- Conclusion
Pixel Detector Task

- High precision tracking close to the interaction point to allow for reconstruction of primary vertex and secondary vertices of long lived particles
- This requires detectors with high spatial resolution, high granularity and minimum material
**Design Principles**

### CCD

- **MAPS design**
- **Charge collection method:** diffusion (conventional) & drift (new)

### Monolithic Pixel and DEPFET (many variants)

#### Charge collection method:
- diffusion (conventional)
- drift (new)

#### Applications:
- **SLD@SLAC, R&D for pixels@ILC**
- **STAR@RHIC (MAPS), BELLE@SuperKEKB (DEPFET), R&D for pixels@ILC**
- **CMS, ATLAS, ALICE@LHC, CMS, ATLAS, ALICE & LHCb upgrade, NA46 GTK@SPS**

### Hybrid Pixel

#### Charge collection method: drift

#### Radiation hardness:
- **< 50 krad**
- **< 20 Mrad**
- **> 250 Mrad**

#### Pixel area:
- **25 µm²**
- **400 µm²**
- **10000 µm²**

#### Speed:
- **< 1 kHz**
- **kHz - MHz**
- **> 10 MHz**

#### Applications:
- **SLD@SLAC, R&D for pixels@ILC**
- **STAR@RHIC (MAPS), BELLE@SuperKEKB (DEPFET), R&D for pixels@ILC**
- **CMS, ATLAS, ALICE@LHC, CMS, ATLAS, ALICE & LHCb upgrade, NA46 GTK@SPS**
Hybrid Pixel Detectors at LHC

• LHC is a challenging environment for pixel detectors
  – High bunch crossing rate (40MHz)
  – Large particle fluence due to high luminosity (1MHz/mm² at r=4cm for pp collisions at L=10^{34}cm^{-2}s^{-1})
  – High radiation levels (lifetime dose of 50Mrad)

• ALICE pixel detector designed for heavy-ion collisions
  – Lower luminosity and bunch crossing frequency but higher particle multiplicity (dN/dy/BX = 8000)

<table>
<thead>
<tr>
<th></th>
<th>ATLAS</th>
<th>CMS</th>
<th>ALICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mechanics</td>
<td>3 layers+ 6 disks</td>
<td>3 layers+ 4 disks</td>
<td>2 layers</td>
</tr>
<tr>
<td>Radius of L0</td>
<td>5 cm</td>
<td>4.4 cm</td>
<td>3.9 cm</td>
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<tr>
<td>Active area</td>
<td>1.7 m²</td>
<td>1 m²</td>
<td>0.24 m²</td>
</tr>
<tr>
<td>Number of channels</td>
<td>80M</td>
<td>66M</td>
<td>10M</td>
</tr>
<tr>
<td>Pixel size</td>
<td>50x400 μm²</td>
<td>100x150 μm²</td>
<td>50x425 μm²</td>
</tr>
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</table>
Performance of ATLAS and CMS Pixel Detectors

- Pixel detectors at LHC show excellent performance
  - 98.3% (CMS), 96.9% (ATLAS) of channels fully operational
- Reliable operation resulting in high data taking efficiency
- Detector response well described by simulation
- Hit efficiency > 99%
- Resolution
  - ATLAS: $\sigma_x \sim 15\mu m$, $\sigma_y \sim 115\mu m$. CMS: $\sigma_x \sim 13\mu m$, $\sigma_y \sim 28\mu m$

$\rightarrow$ CMS: Morris Swartz’s talk
$\rightarrow$ ATLAS: Markus Keil’s talk

![Graphs showing performance metrics for ATLAS and CMS Pixel Detectors]
Upgrade Plans of LHC Pixel Detectors

• Performance of innermost layer degrades with higher pile-up
  – Need replacement to maintain/improve tracking performance
• Build innermost layer closer to interaction point and less material
• LHC luminosity upgrade (Phase I) targets to $L=2\times10^{34}\text{cm}^{-2}\text{s}^{-1}$ by 2020
  – Need fast front-end electronics to reduce dead-time
  – Improve radiation hardness of readout electronics and sensors

ATLAS: upgrade in 2 steps
IBL (2013): Add 4th pixel layer at 3.2cm to existing pixel detector
Pixel replacement (2017/18) being studied

CMS pixel upgrade (2017/18)
Build new 4 layer pixel system.
Innermost layer at 3cm.

LHCb VELO upgrade (2017/18)
26 stations of pixel
Closest pixel 7.5mm from IP
HEP Pixel Detector FE Electronics

• Task of pixel readout chip
  – Charge amplification
  – Signal discrimination
  – Temporary hit storage during trigger latency
  – Retrieval and readout according to trigger selection

• Requirements for LHC pixel detector FEs
  – Fast signal rise time (<25ns), longer fall time (<2μs)
  – Allow for low threshold operation (≤ 3000 e)
  – Ensure uniformity of pixel matrix (threshold dispersion < noise)
  – Radiation hard technology (expected dose 50Mrad → 250Mrad → 500Mrad )
Design: PSI46 and FEI3

- **CMS**: smaller volume, operated in high magnetic field (3.8T)
  - Improve resolution making use of charge sharing → analog pulse height measurement, need low threshold
  - Similar resolution in rφ and z → square pixels

- **ATLAS**: larger volume, smaller magnetic field (2T)
  - Optimize resolution in transverse plain → rectangular pixels
  - Charge digitization: time-over-threshold (ToT) measurement

<table>
<thead>
<tr>
<th></th>
<th>PSI46</th>
<th>FEI3</th>
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<tbody>
<tr>
<td>Year</td>
<td>2005</td>
<td>2003</td>
</tr>
<tr>
<td>Technology</td>
<td>250nm</td>
<td>250nm</td>
</tr>
<tr>
<td>Chip size</td>
<td>7.9x9.9mm²</td>
<td>7.6x10.8mm²</td>
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<tr>
<td>Active area</td>
<td>81%</td>
<td>74%</td>
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<tr>
<td>Array</td>
<td>80x52 (4160)</td>
<td>18x160 (2880)</td>
</tr>
<tr>
<td>Pixel size</td>
<td>100x150μm²</td>
<td>50x400μm²</td>
</tr>
<tr>
<td>Number of transistors</td>
<td>1.3M</td>
<td>3.5M</td>
</tr>
<tr>
<td>Data rate</td>
<td>40Mb/s</td>
<td>40Mb/s</td>
</tr>
<tr>
<td>Wafer yield</td>
<td>74%</td>
<td>80%</td>
</tr>
</tbody>
</table>
Key Features of FEI4

- New ATLAS pixel detector readout chip to be used in IBL and outer layers for upgrade pixel detector

- Designed to cope with higher hit rate
  - Regional architecture
  - Smaller pixel size

- Improved cost effectiveness
  - Large chip with large active area

- Lower power
  - Improved design and architecture

- Increased radiation tolerance (up to 250Mrad)
  - 130nm technology

- Submission of FEI4A (July 2010) was successful. Chip was thoroughly tested. Only minor modification needed before submission of production version FEI4B in summer 2011.

<table>
<thead>
<tr>
<th></th>
<th>FEI4A</th>
<th>FEI3</th>
</tr>
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<tbody>
<tr>
<td>Year</td>
<td>2010</td>
<td>2003</td>
</tr>
<tr>
<td>Technology</td>
<td>130nm</td>
<td>250nm</td>
</tr>
<tr>
<td>Chip size</td>
<td>20x19mm²</td>
<td>7.6x10.8mm²</td>
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<tr>
<td>Active area</td>
<td>89%</td>
<td>74%</td>
</tr>
<tr>
<td>Array</td>
<td>80x336 (26880)</td>
<td>18x160 (2880)</td>
</tr>
<tr>
<td>Pixel size</td>
<td>50x250μm²</td>
<td>50x400μm²</td>
</tr>
<tr>
<td>Number of transistors</td>
<td>87M</td>
<td>3.5M</td>
</tr>
<tr>
<td>Data rate</td>
<td>320 Mb/s</td>
<td>40Mb/s</td>
</tr>
<tr>
<td>Wafer yield</td>
<td>65% *</td>
<td>80%</td>
</tr>
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</table>

*based on 9 wafers, loose criteria
PSI46 Analog Readout

- 2 stage preamp/shaper
- Comparator with global and local threshold adjustment (4 trim bits +1 mask bit)
- Analog pulse height information and pixel address are sent to periphery
- No clock in PUC, runs asynchronous with periphery
FEI3 charge digitization

• Two-stage amplification
• Time stamp distributed to all pixels to allow for Time-over-Threshold measurement (ToT)
  - ToT proportional to charge due to linear return-to-baseline
• Timestamp LE/TE together with pixel address sent to periphery
Threshold and Noise from LHC Collision Data

- Mean threshold well above noise level
  - CMS: 2500e threshold and <150e noise
  - ATLAS: 3500e threshold and ~170e noise
- In-time threshold is higher due to time-walk
  - CMS: 3200e, ATLAS: 3700e
  - FEI3 does on-chip hit doubling to recover small hits in later BX (cost of 10% data volume increase), PSI46 reads out only one BX
Readout Architecture of PSI46 and FEI3

• Pixel array organized in double columns (DC)

• Column drain mechanism:
  – Fast transfer of hits data to DC periphery
  – Buffers to store data during L1 latency at periphery
  – Trigger verification performed at periphery

• Data is marked for readout if triggered, otherwise discarded

• Triggered hit data is sent out serially

• FEI3/PSI46 share the concept of transferring hits to DC periphery, but differ in the implementation
Column Drain: Limitations at High Rate

• Column drain architecture saturates at high rate
  – All pixel hits are sent to periphery
  – Column based readout induces dead-time (during data transfer to periphery and column readout)

• ATLAS solutions for higher rate
  → Development of regional architecture in FEI4

![ATLAS simulation graph](image)
CMS ROC for Phase I: PSI46dig

- DC in PSI46 have lower occupancy (factor ~ 9/26)
  - Inefficiency wall at significantly higher rate than in FEI3
  - Can keep present architecture (with modifications) for Phase I

- Limitations of PSI46 at Phase I
  1) Buffer size for L1 latency (dominant)
     → increase number of LV1 buffers ✔
  2) Readout related dead time at high rate
     → additional readout buffer stage ★
  3) Need increased bandwidth due to higher module count
     → 320 MHz digital readout
        - On chip 8-bit ADC ✔
        - New fast digital readout links ✔
        - PLL to provide higher frequencies ✔
        - Modification to control logic ★

- Lower operation threshold (~2500e)
- Chip submission in fall 2011
Regional Memories in FEI4

- FEI4 is organized in digital regions serving 4 analog pixels
- Hits are stored locally during L1 latency
  - 5 ToT memories per pixel, 5 latency counters per region
- Hits are not moved unless triggered
  - only 0.25% of hits are sent to periphery
- Lower digital power consumption (6µW/pixel at IBL occupancy)
FEI4 Analog Pixel

- Similar design of analog pixel in FEI3/FEI4
- Two-stage amplification
- Clock is distributed to all digital pixel region
- ToT counters within pixel digital region
- ToT together with pixel address sent to periphery
Time-walk Correction in FEI4

- Small hits are associated to big hits based on position rather than on time information
- PDR triggers on “big” hits and uses a time window of 2 BX to look for “small” hits
- Allows for lower power operation since digital logic corrects for reduced analog performance
FEI4: Threshold and Noise

- FEI4 bump-bonded to planar and 3D sensors have been successfully operated in lab test, test beams and cosmic data taking
- Tuned threshold dispersion ~30e
  → Philippe Grenier’s talk
- FEI4 low threshold operation (~700e) shows promising results with reasonable dispersion
- Irradiation tests with bare chips show no effect on threshold dispersion and 20% increase in noise
Power Consumption

• **PSI46**
  - **Analog:** $26\text{mA} \times 1.7\text{V} = 44\text{mW/chip}$  =>  $11\mu\text{W/pixel}$
  - **Digital:** $29\text{mA} \times 2.5\text{V} = 73\text{mW/chip}$  =>  $17\mu\text{W/pixel}$
  - Fluence dependent contribution $0.1\mu\text{A/pixel} \times \text{fluence [MHz/cm}^2\text{]}$

• **FEI3**
  - **Analog:** $75\text{mA} \times 1.6\text{V} = 120\text{mW/chip}$  =>  $42\mu\text{W/pixel}$
  - **Digital:** $49\text{mA} \times 2.0\text{V} = 98\text{mW/chip}$  =>  $34\mu\text{W/pixel}$

• **FEI4**
  - **Analog:** $350\text{mA} \times 1.2\text{V} = 420\text{mW/chip}$  =>  $16\mu\text{W/pixel}$
  - **Digital:** $110\text{mA} \times 1.5\text{V} = 165\text{mW/chip}$  =>  $6\mu\text{W/pixel}$
  - Reduced analog current in FEI4 (reduced analog performance is recovered by adding digital functionality)
  - Reduced digital current due to improved architecture
The Future

• Still higher rate needed for coverage of small radii at HL-LHC (peak luminosity of $10^{35}\text{cm}^{-2}\text{s}^{-1}$, 230 pile-up events)

• Need increased radiation hardness (up to 500Mrad)

• Aim for smaller, faster pixels and more memory per pixel
  – Reduce occupancy
  – Improve resolution
  – Reduce readout inefficiencies

• 2 directions being explored
  – High density: 65nm technology
  – 3D integration: Tezzaron-Chartered 130nm technology

⇒ Carl Grace’s talk
⇒ Satellite meeting on Tuesday
Prototype Analog Chip in 65nm

- Factor of 4 in area reduction for digital circuits compared to 130nm
- Idea: reduce analog complexity/performance and compensate with digital signal processing
- Prototype analog chip submitted on June 2, 2011
  - 25µm pitch in rφ, 50µm bump spacing
  - z length to be adjusted as needed for digital logic (expect 150µm)
Simulation Results: Noise

- Noise increases slowly as current decreases
- Non-limiting factor
Simulation Results: Rise Time

Q = 2000e                   Preamp Current: 0.25 → 5.25 µA

IFF = 50nA

IFF = 100nA

IFF = 200nA
Conclusion

- First generation of pixel detectors show excellent performance during LHC data taking and substantially improve physics potential of the experiments.

- FEI4 presents a new chip for upgrade projects. It includes real innovation and reduces the cost of module production thanks to its size and reasonable wafer yield. Submission of FEI4A was a success.

- R&D of readout electronics for HL-LHC is ongoing. Newly available technologies like 65nm feature size and 3D technology are being exploited.
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SLAC: Martin Kocian
Backup
Cluster Size and Cluster Charge in ATLAS/CMS

**ATLAS**

ATLAS Preliminary

\( s = 7 \text{ TeV} \)

<table>
<thead>
<tr>
<th>Fraction of pixel clusters</th>
<th>Size</th>
<th>Cluster Charge</th>
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</thead>
<tbody>
<tr>
<td>0.2</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0.16</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>0.14</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>0.12</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>0.1</td>
<td>20</td>
<td></td>
</tr>
</tbody>
</table>

**CMS**

CMS preliminary 2010 \( \sqrt{s} = 7 \text{ TeV} \)

- **Pixel Barrel**
  - MC
  - DATA

- **Number of clusters / 1**

**dE/dx Pixel**

- **Number of Pixel clusters**
  - Data 900 GeV
  - MC 900 GeV

**Normalized cluster charge [ke]**

- **Number of clusters / 1 [ke]**
PSI46 readout architecture

Data buffer
Depth: 32

Marker bits indicate start of new event

Depth: 12

Pixel unit cells: 2x80

Column drain mechanism

Fast double column OR

Sketch of a double column

Time-stamp buffer
Depth: 12
Data loss mechanisms

Pixel busy:
0.04% / 0.08% / 0.21%
pixel insensitiv until hit transferred to data buffer (column drain mechanism)

Double column busy:
0.004% / 0.02% / 0.25%
Column drain transfers hits from pixels to data buffer. Maximum 3 pending column drain requests accepted

Data Buffer full:
0.07% / 0.08% / 0.17%

1xLHC: \(10^{34} \text{ cm}^{-2} \text{s}^{-1}\)
11 cm / 7 cm / 4 cm layer
Total data loss @ 100kHz L1A:
- 0.8%
- 1.2%
- 3.8%

Timestamp Buffer full:
0 / 0.001% / 0.17%

Readout losses:
0.7% / 1% / 3.0%
for 100kHz L1 trigger rate
Column is blocked after L1A and reset when read out
FEI3 Column Drain: Limitations at high rate

- r=5cm at L=10^{34}cm^{-2}s^{-1}
- r=3.7cm at L=2x10^{34}cm^{-2}s^{-1}
FEI4 4-pixel digital region with neighbor logic
**FEI4 Digital Column Simulation vs Measurement**

**Simulation @1.2V**

Average power for 4-pixel region at IBL occupancy (MC hits)

<table>
<thead>
<tr>
<th>Simulation type</th>
<th>Power (avg) [uW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>ETS¹</td>
<td>42.28</td>
</tr>
<tr>
<td>Spectre²</td>
<td>25.19</td>
</tr>
<tr>
<td>Ultrasim(s)²</td>
<td>24.69</td>
</tr>
<tr>
<td>Ultrasim(a)²</td>
<td>24.73</td>
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<tr>
<td>Ultrasim(ms)²</td>
<td>35.12</td>
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<tr>
<td>HSIM</td>
<td>27.64</td>
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<tr>
<td>HSIM</td>
<td>30.98</td>
</tr>
</tbody>
</table>

**Measurement @1.2V**

Occupancy faked with periodic charge injection

Parasitic extraction done width ¹PEX

---

**Diagram**

- Graph showing power per region (uW) vs fraction of occupied counters.
- Different markers represent different rad levels: 0Mrad, 6Mrad, 75Mrad, 200Mrad.
- Approx. IBL range indicated.
65nm Simulation Results: ENC vs CDET

IBP = 0.5μA

IBP = 1μA

IBP = 2μA

IBP = 5μA

ENC [e]

CDET [pF]
DEPFET – Depleted P-channel Field Effect Transistor

- Each pixel is p-channel FET on completely depleted bulk
- Charge collection by drift
- Signal electrons accumulate in internal gate and modulate transistor current
- Accumulated charge removed by clear contact
- Internal amplification
- Readout on demand