Recent developments of HEP pixel detector readout chips

TIPP 2011

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LBNL

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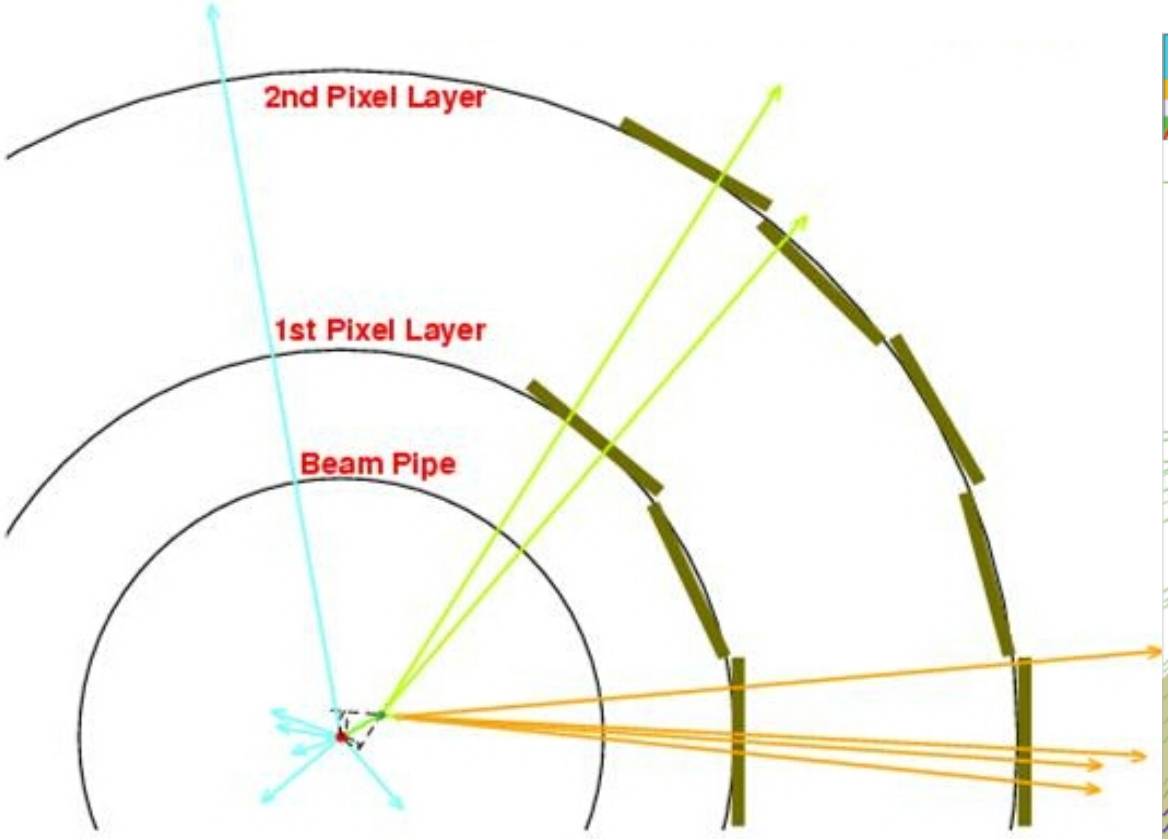
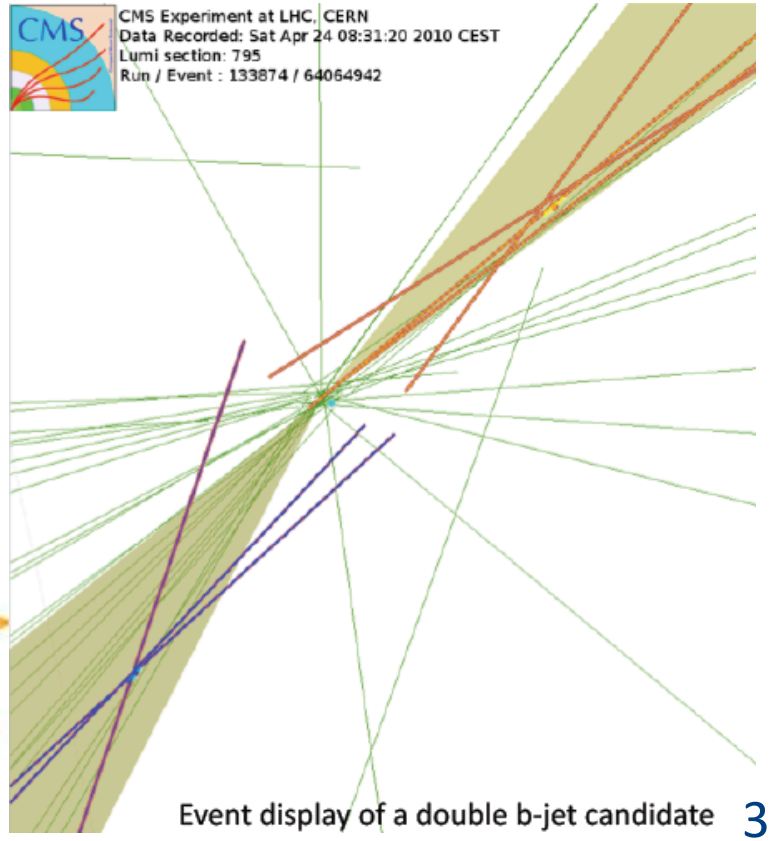
Overview

- Pixel Detectors
  - Task and Design Principles
  - Hybrid Pixel Detectors at LHC
- Front-End Electronics for Hybrid Pixel Detectors
  - First generation at LHC: PSI46 and FEI3
  - Second generation: FEI4
  - R&D: 65nm technology
- Conclusion

Pixel Detector Task

- High precision tracking close to the interaction point to allow for reconstruction of primary vertex and secondary vertices of long lived particles
- This requires detectors with high spatial resolution, high granularity and minimum material

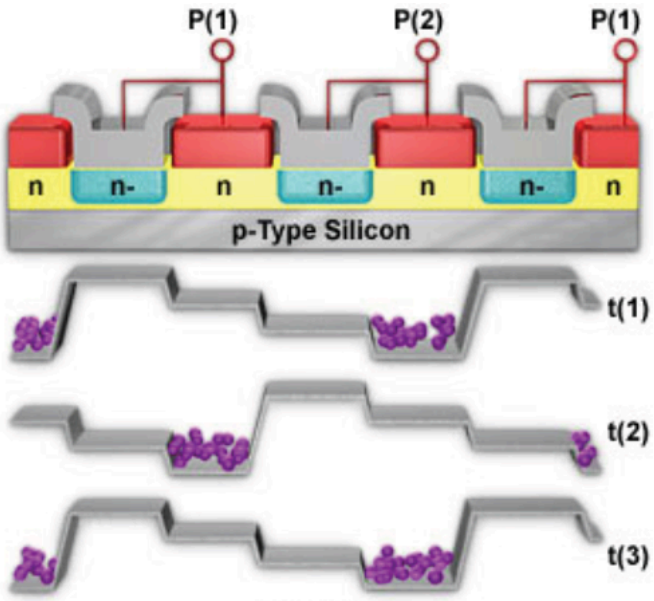




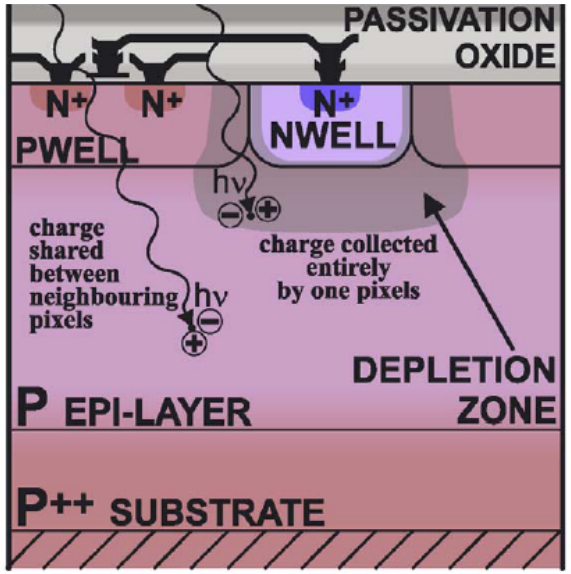
Event display of a double b-jet candidate

Design Principles

CCD

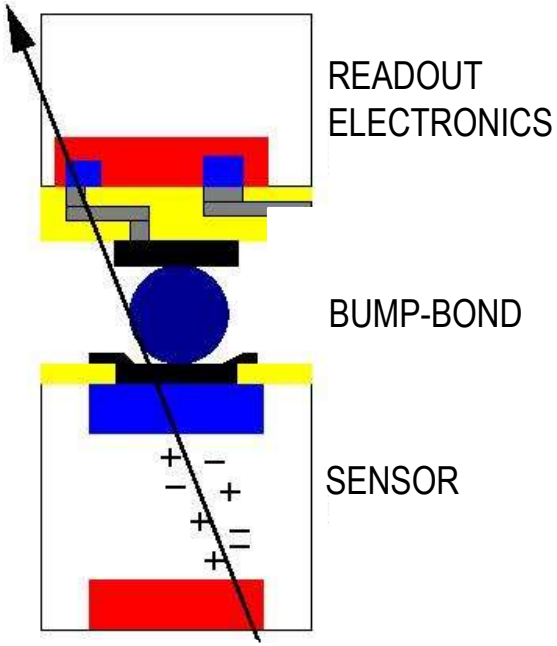


Monolithic Pixel and DEPFET (many variants)



MAPS design

Hybrid Pixel



Charge collection method: diffusion (conventional) & drift (new) drift

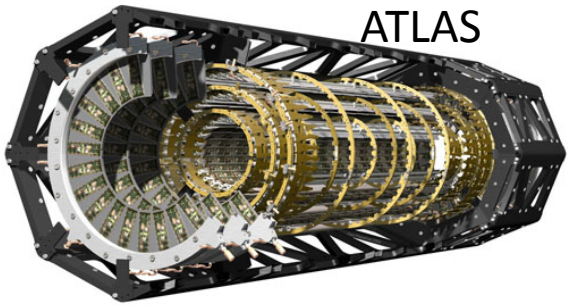
Pixel area	25 μm²	400 μm²	10000 μm²
Speed	< 1 kHz	kHz - MHz	> 10 MHz
Radiation hardness	< 50 krad	< 20 Mrad	> 250 Mrad

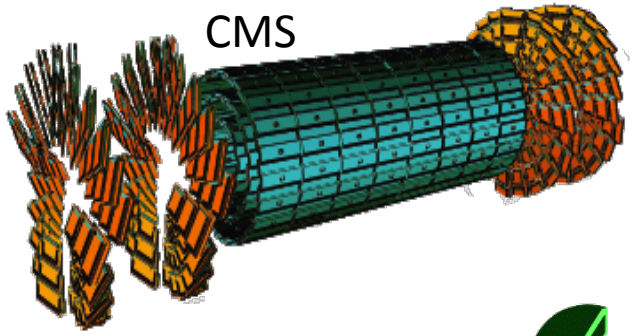
Applications:

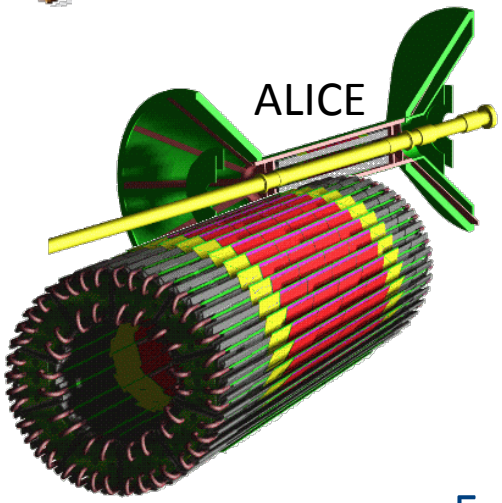
- SLD@SLAC, R&D for pixels@ILC
- STAR@RHIC (MAPS), BELLE@SuperKEKB (DEPFET), R&D for pixels@ILC
- CMS,ATLAS&ALICE@LHC, CMS,ATLAS,ALICE&LHCb upgrade NA46 GTK@SPS

Hybrid Pixel Detectors at LHC

- LHC is a challenging environment for pixel detectors
  - High bunch crossing rate (40MHz)
  - Large particle fluence due to high luminosity ($1MHz/mm^2$ at r=4cm for pp collisions at $L=10^{34}cm^{-2}s^{-1}$)
  - High radiation levels (lifetime dose of 50Mrad)
- ALICE pixel detector designed for heavy-ion collisions
  - Lower luminosity and bunch crossing frequency but higher particle multiplicity (dN/dy/BX = 8000)





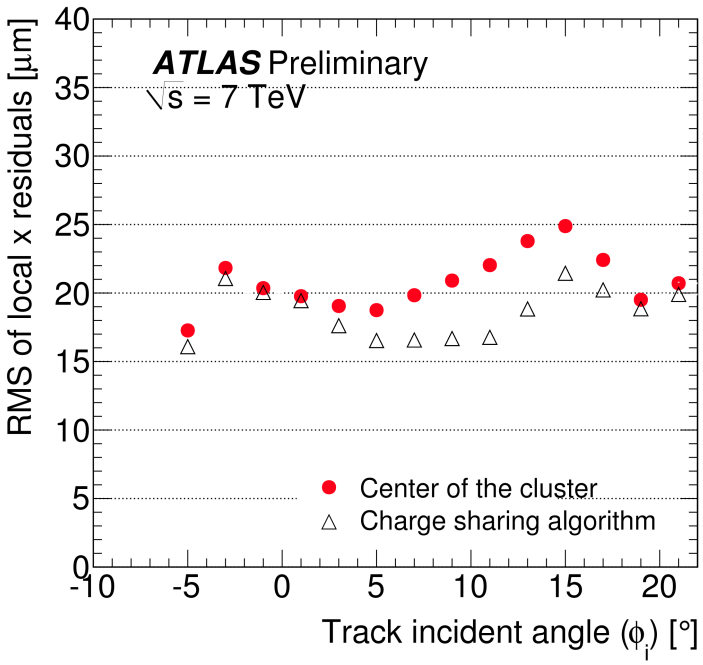


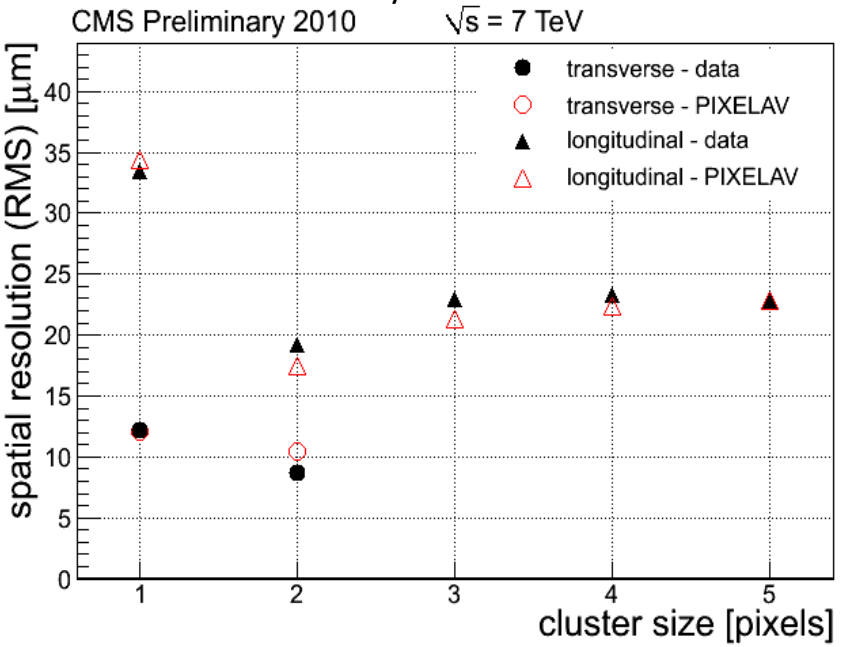
	ATLAS	CMS	ALICE
Mechanics	3 layers+ 6 disks	3 layers+ 4 disks	2 layers
Radius of L0	5 cm	4.4 cm	3.9 cm
Active area	1.7 m^2	1 m^2	0.24 m^2
Number of channels	80M	66M	10M
Pixel size	50x400 μm^2	100x150 μm^2	50x425 μm^2

Performance of ATLAS and CMS Pixel Detectors

- Pixel detectors at LHC show excellent performance
  - 98.3% (CMS), 96.9% (ATLAS) of channels fully operational
- Reliable operation resulting in high data taking efficiency
- Detector response well described by simulation
- Hit efficiency > 99%
- Resolution
  - ATLAS: σ_x ~ 15µm, σ_y ~ 115µm. CMS: σ_x ~ 13µm, σ_y ~ 28µm

→CMS: Morris Swartz's talk
→ATLAS: Markus Keil's talk

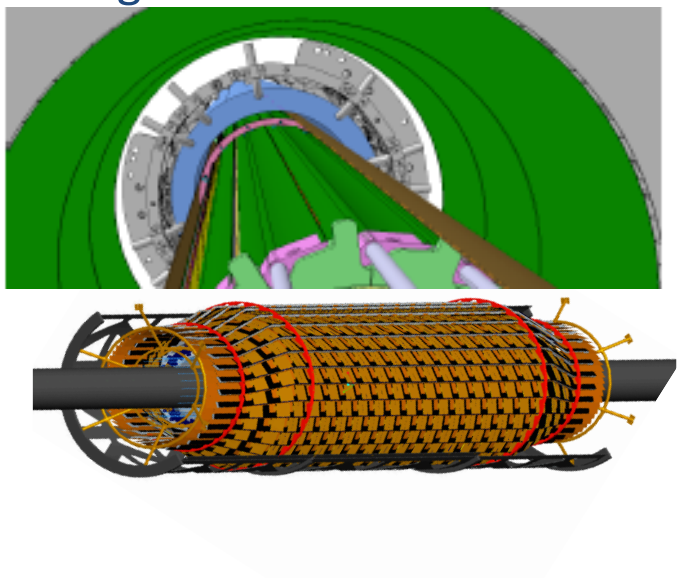




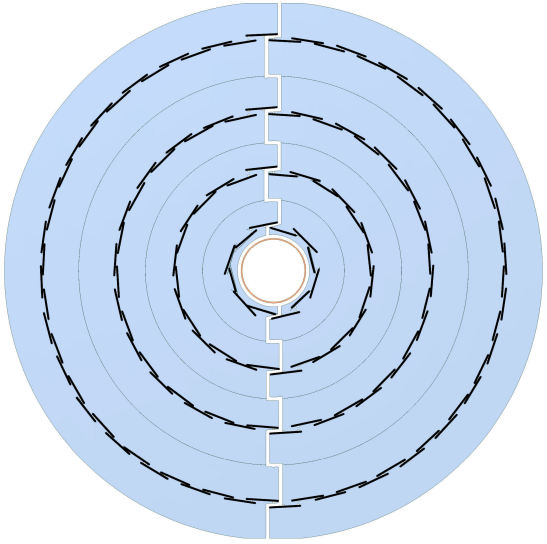
Upgrade Plans of LHC Pixel Detectors

- Performance of innermost layer degrades with higher pile-up
  - Need replacement to maintain/improve tracking performance
- Build innermost layer closer to interaction point and less material
- LHC luminosity upgrade (Phase I) targets to $L=2x10^{34}cm^{-2}s^{-1}$ by 2020
  - Need fast front-end electronics to reduce dead-time
  - Improve radiation hardness of readout electronics and sensors

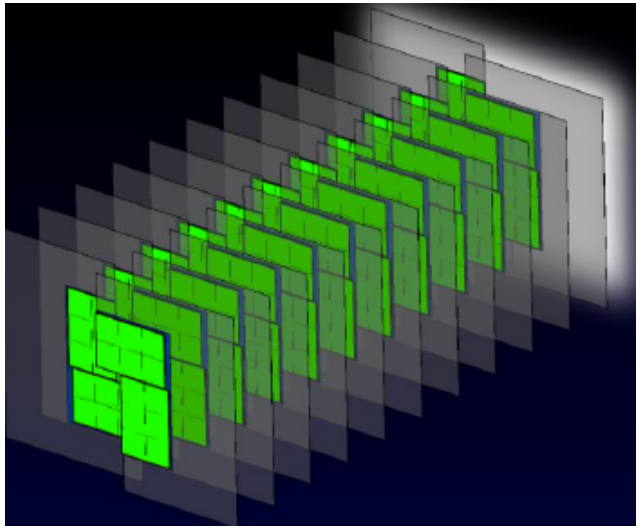
ATLAS: upgrade in 2 steps
IBL (2013): Add 4th pixel layer at 3.2cm to existing pixel detector
Pixel replacement (2017/18) being studied



CMS pixel upgrade (2017/18)
Build new 4 layer pixel system.
Innermost layer at 3cm.

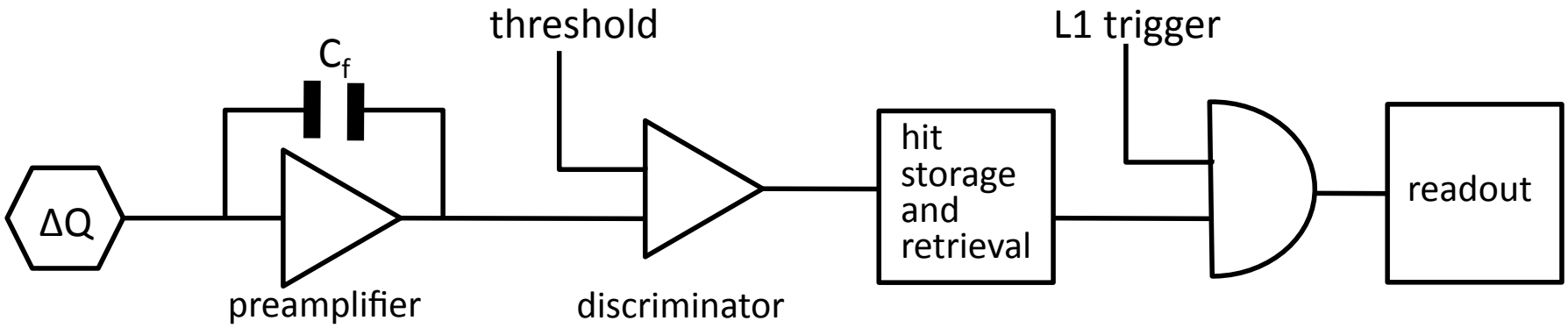


LHCb VELO upgrade(2017/18)
26 stations of pixel
Closest pixel 7.5mm from IP



HEP Pixel Detector FE Electronics

- Task of pixel readout chip
  - Charge amplification
  - Signal discrimination
  - Temporary hit storage during trigger latency
  - Retrieval and readout according to trigger selection
- Requirements for LHC pixel detector FEs
  - Fast signal rise time (<25ns), longer fall time (<2µs)
  - Allow for low threshold operation (≤ 3000 e)
  - Ensure uniformity of pixel matrix (threshold dispersion < noise)
  - Radiation hard technology (expected dose 50Mrad → 250Mrad → 500Mrad)



Design: PSI46 and FEI3

- CMS: smaller volume, operated in high magnetic field (3.8T)
  - Improve resolution making use of charge sharing → analog pulse height measurement, need low threshold
  - Similar resolution in rϕ and z → square pixels
- ATLAS: larger volume, smaller magnetic field (2T)
  - Optimize resolution in transverse plain → rectangular pixels
  - Charge digitization: time-over-threshold (ToT) measurement

	PSI46	FEI3
Year	2005	2003
Technology	250nm	250nm
Chip size	7.9x9.9mm^2	7.6x10.8mm^2
Active area	81%	74%
Array	80x52 (4160)	18x160 (2880)
Pixel size	100x150µm^2	50x400µm^2
Number of transistors	1.3M	3.5M
Data rate	40Mb/s	40Mb/s
Wafer yield	74%	80%

Key Features of FEI4

- New ATLAS pixel detector readout chip to be used in IBL and outer layers for upgrade pixel detector

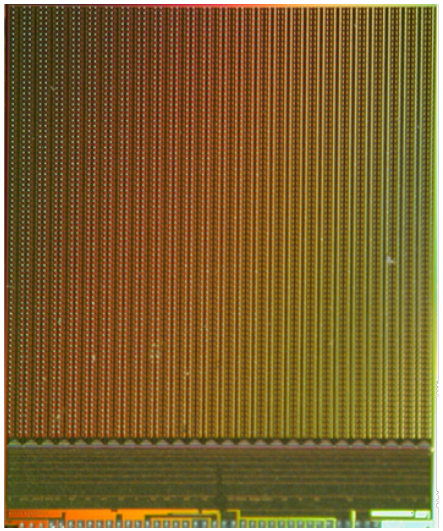
- Designed to cope with higher hit rate
  - Regional architecture
  - Smaller pixel size
- Improved cost effectiveness
  - Large chip with large active area
- Lower power
  - Improved design and architecture
- Increased radiation tolerance (up to 250Mrad)
  - 130nm technology

	FEI4A	FEI3
Year	2010	2003
Technology	130nm	250nm
Chip size	20x19mm^2	7.6x10.8mm^2
Active area	89%	74%
Array	80x336 (26880)	18x160 (2880)
Pixel size	50x250µm^2	50x400µm^2
Number of transistors	87M	3.5M
Data rate	320 Mb/s	40Mb/s
Wafer yield	65% *	80%

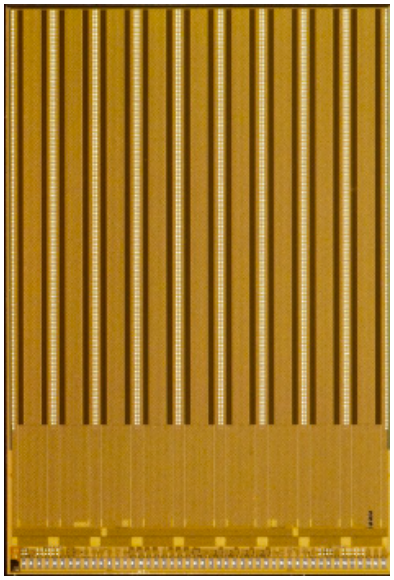
*based on 9 wafers, loose criteria

- Submission of FEI4A (July 2010) was successful. Chip was thoroughly tested. Only minor modification needed before submission of production version FEI4B in summer 2011.

PSI46

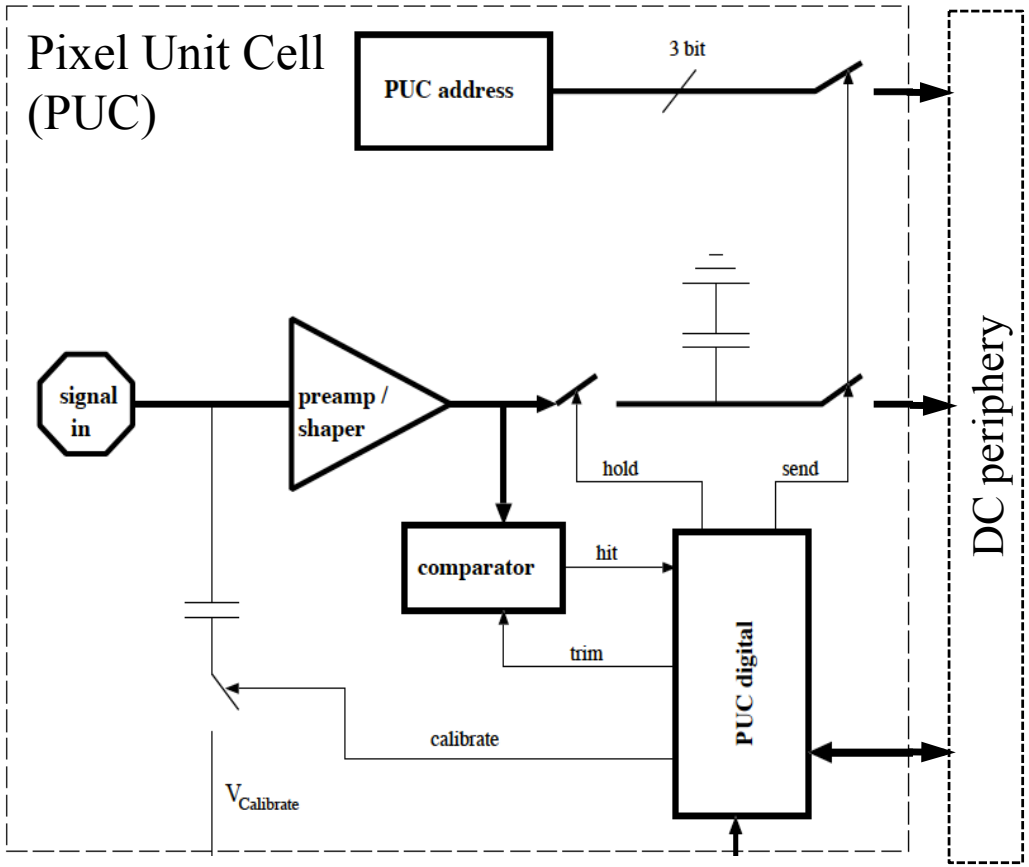


FEI3



FEI4

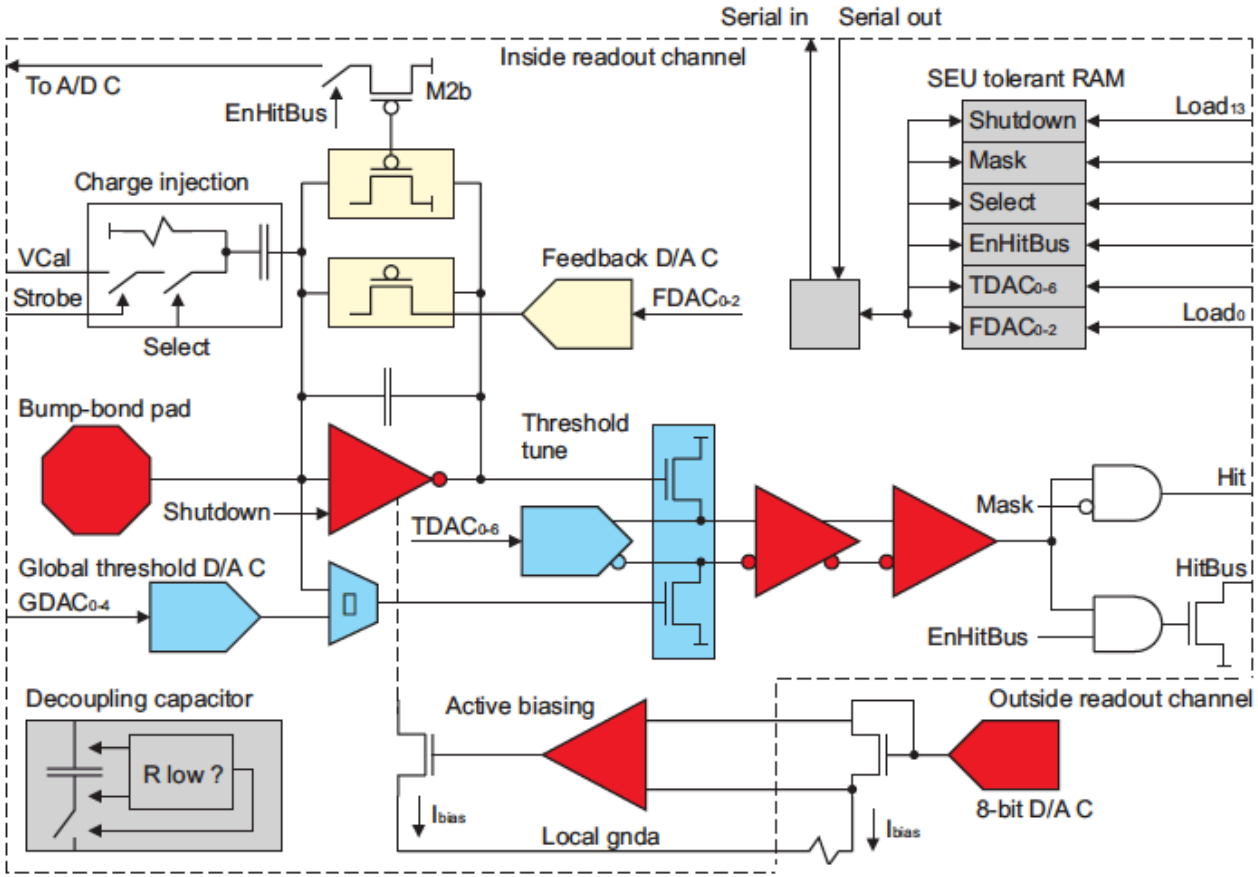
PSI46 Analog Readout



- 2 stage preamp/shaper
- Comparator with global and local threshold adjustment (4 trim bits +1 mask bit)
- Analog pulse height information and pixel address are sent to periphery
- No clock in PUC, runs asynchronous with periphery

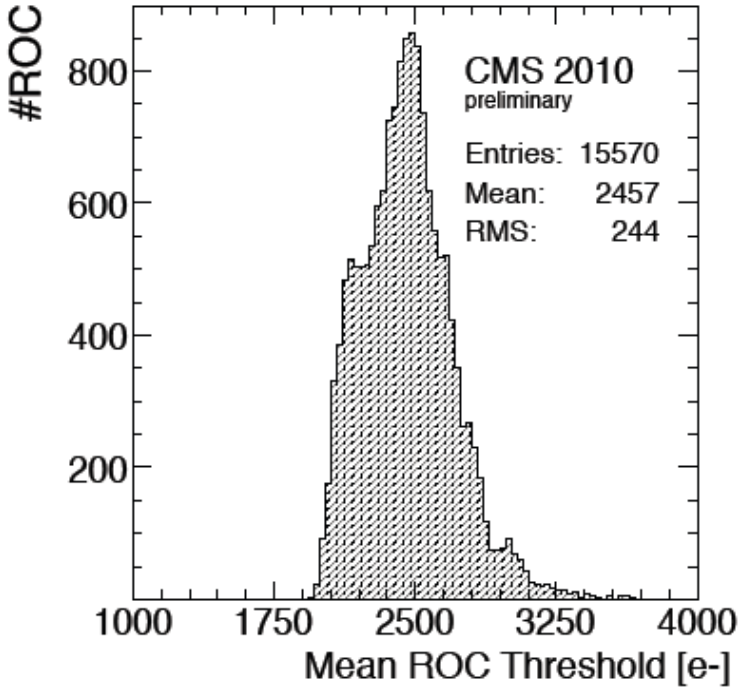
FEI3 charge digitization

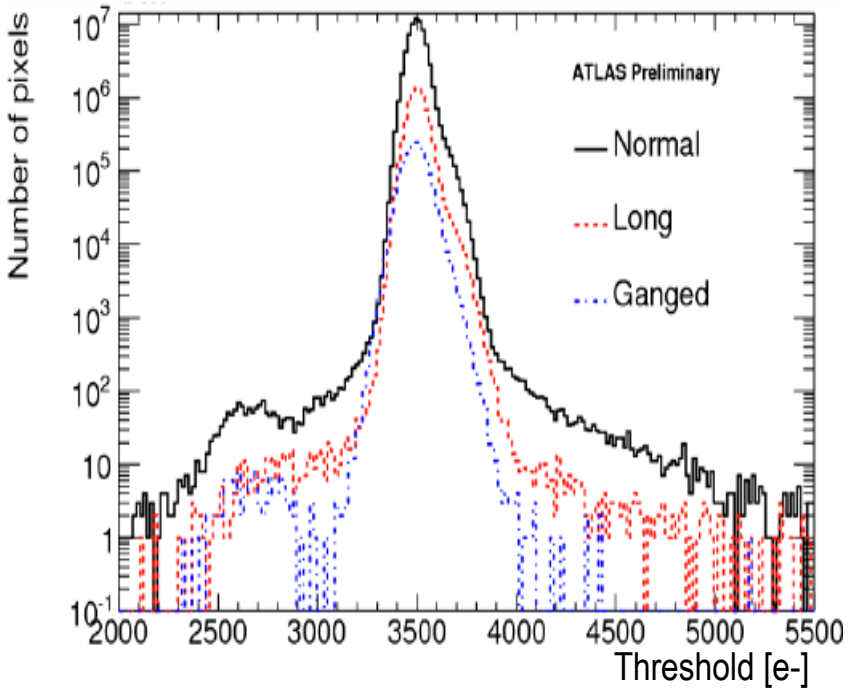
- Two-stage amplification
- Time stamp distributed to all pixels to allow for Time-over-Threshold measurement (ToT)
  - ToT proportional to charge due to linear return-to-baseline
- Timestamp LE/TE together with pixel address sent to periphery



Threshold and Noise from LHC Collision Data

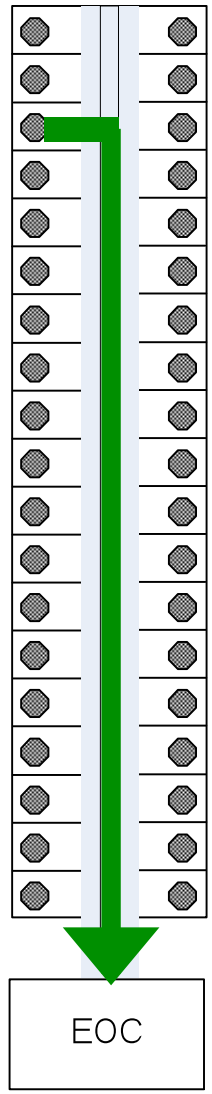
- Mean threshold well above noise level
  - CMS: 2500e threshold and <150e noise
  - ATLAS: 3500e threshold and ~170e noise
- In-time threshold is higher due to time-walk
  - CMS: 3200e, ATLAS: 3700e
  - FEI3 does on-chip hit doubling to recover small hits in later BX (cost of 10% data volume increase), PSI46 reads out only one BX





Readout Architecture of PSI46 and FEI3

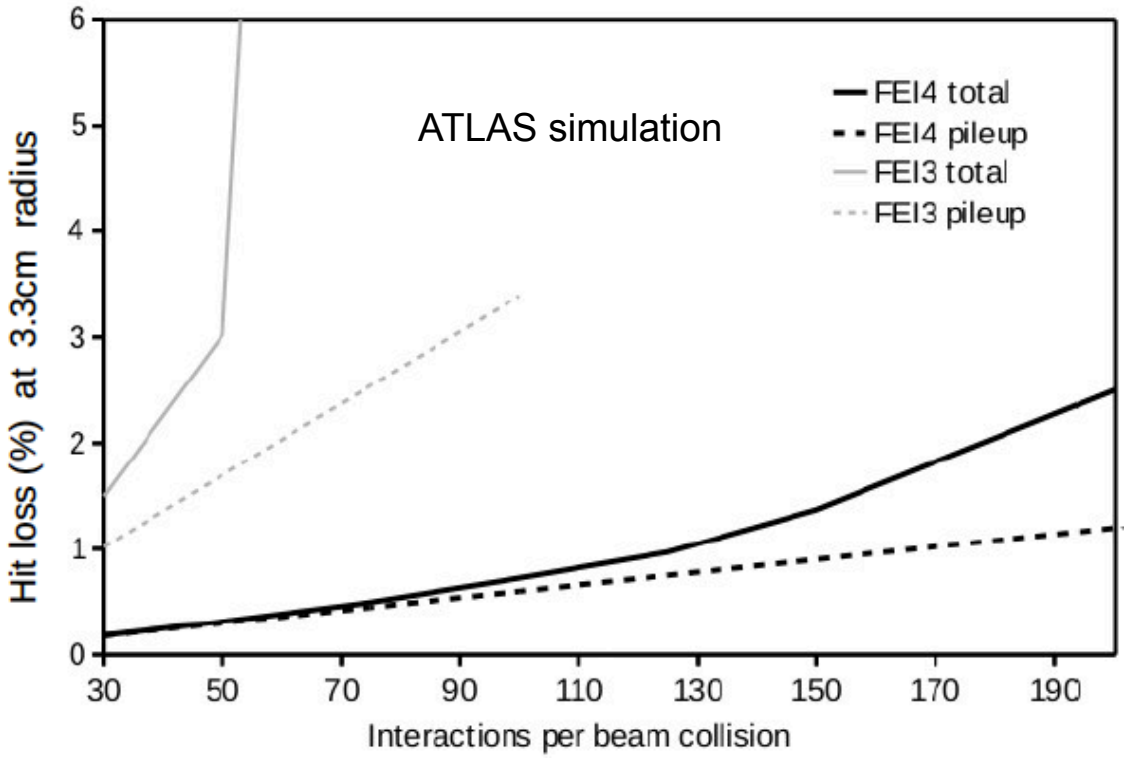
- Pixel array organized in double columns (DC)
- Column drain mechanism:
  - Fast transfer of hits data to DC periphery
  - Buffers to store data during L1 latency at periphery
  - Trigger verification performed at periphery
- Data is marked for readout if triggered, otherwise discarded
- Triggered hit data is sent out serially
- FEI3/PSI46 share the concept of transferring hits to DC periphery, but differ in the implementation



Column Drain: Limitations at High Rate

- Column drain architecture saturates at high rate
  - All pixel hits are sent to periphery
  - Column based readout induces dead-time (during data transfer to periphery and column readout)
- ATLAS solutions for higher rate

  → Development of regional architecture in FEI4



CMS ROC for Phase I: PSI46dig

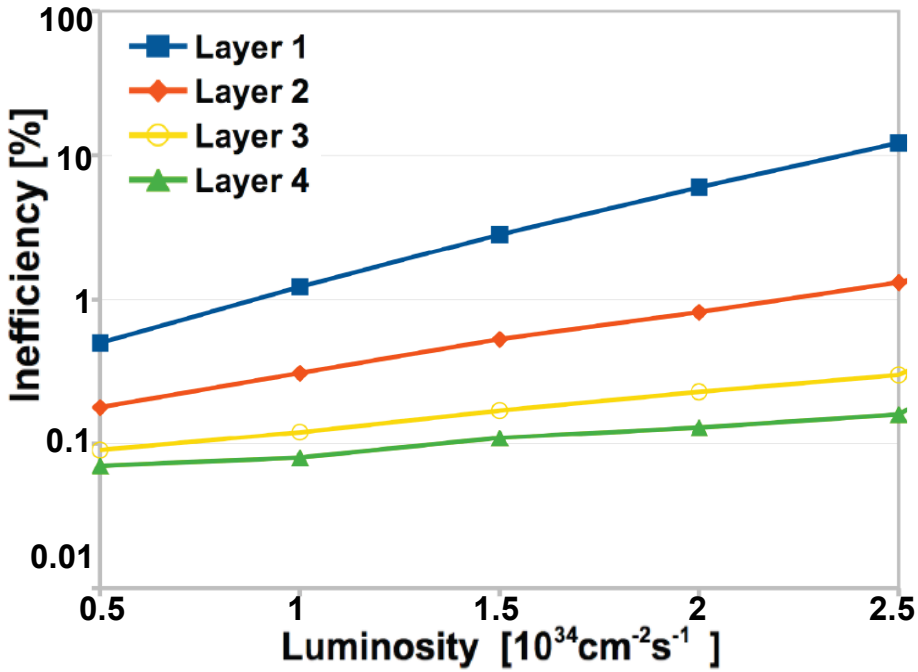
- DC in PSI46 have lower occupancy (factor ~ 9/26)
  - Inefficiency wall at significantly higher rate than in FEI3
  - Can keep present architecture (with modifications) for Phase I
- Limitations of PSI46 at Phase I

✔ done
★ in progress

1) Buffer size for L1 latency (dominant)
   → increase number of LV1 buffers ✔
2) Readout related dead time at high rate
   → additional readout buffer stage ★
3) Need increased bandwidth due to higher module count
   → 320 MHz digital readout
   - On chip 8-bit ADC ✔
   - New fast digital readout links ✔
   - PLL to provide higher frequencies ✔
   - Modification to control logic ★

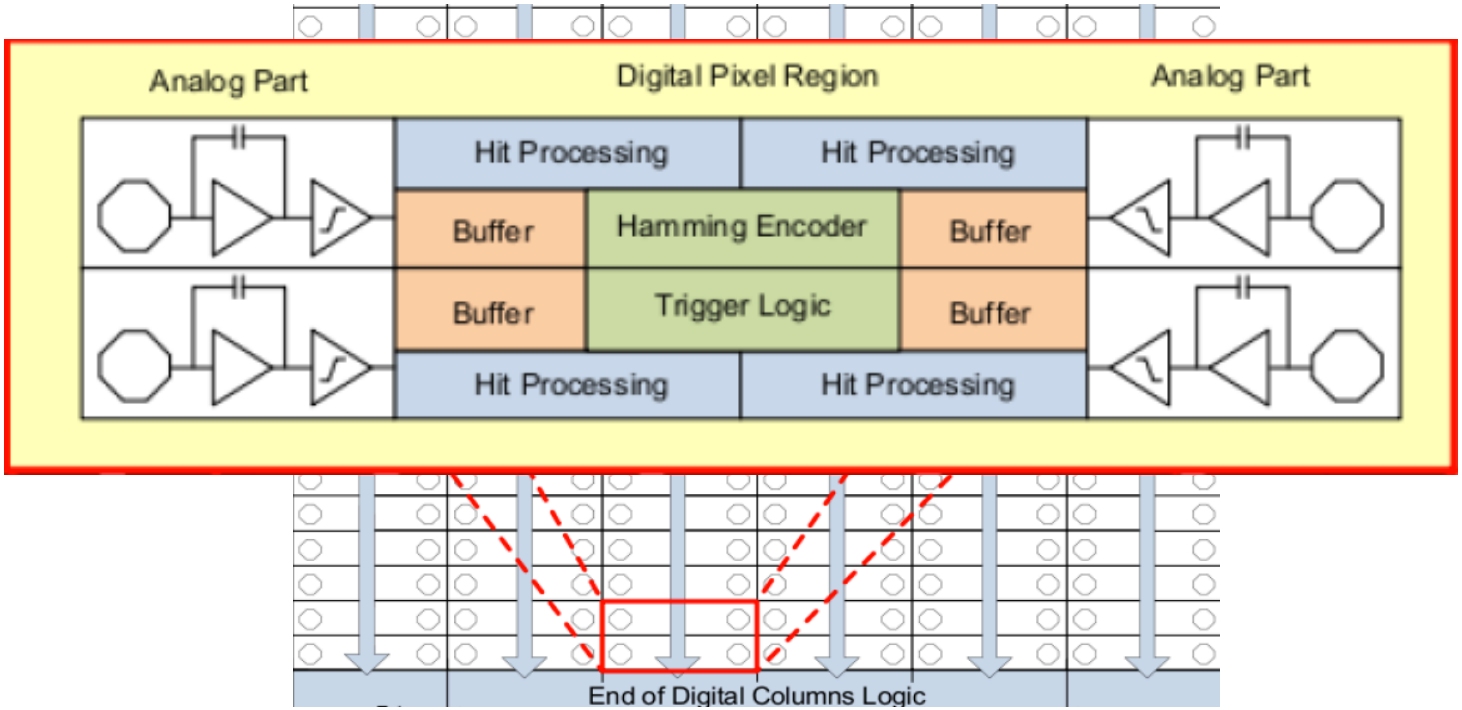
- Lower operation threshold (~2500e)
- Chip submission in fall 2011

H. C. Kästli



Regional Memories in FEI4

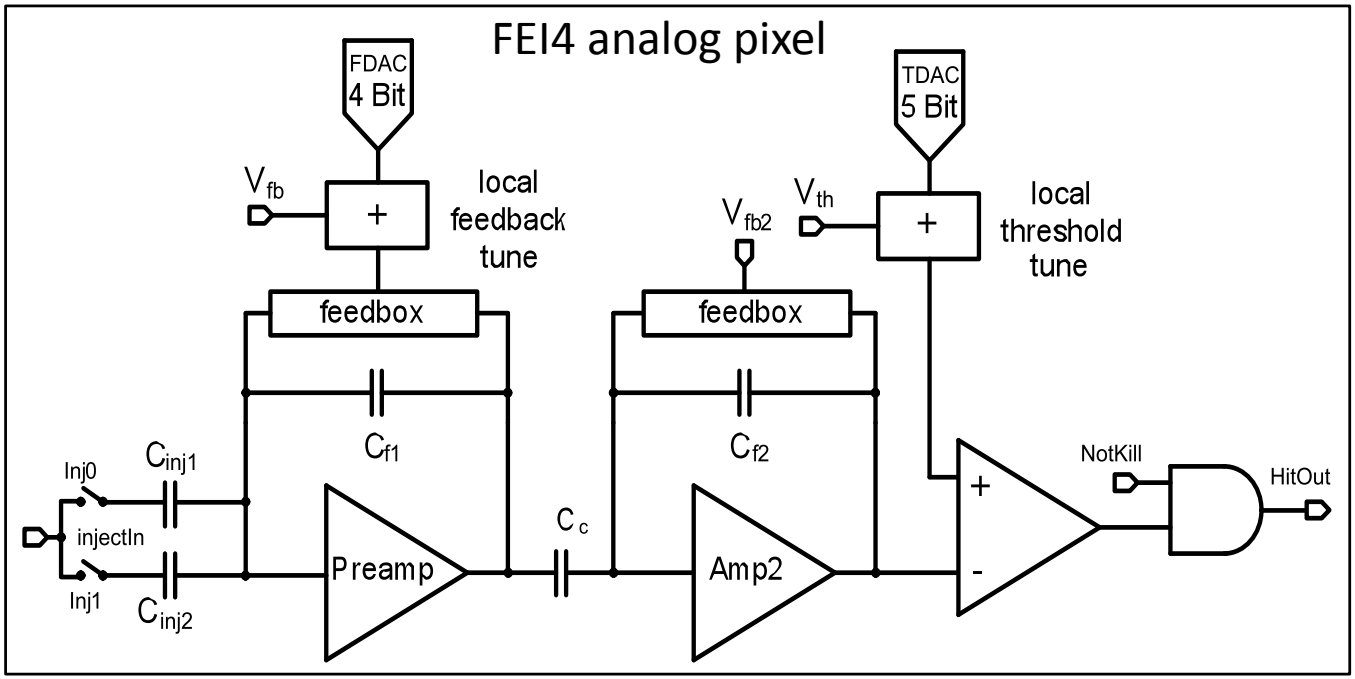
- FEI4 is organized in digital regions serving 4 analog pixels
- Hits are stored locally during L1 latency
  - 5 ToT memories per pixel, 5 latency counters per region
- Hits are not moved unless triggered
  - only 0.25% of hits are sent to periphery
- Lower digital power consumption (6µW/pixel at IBL occupancy)



FEI4 Analog Pixel

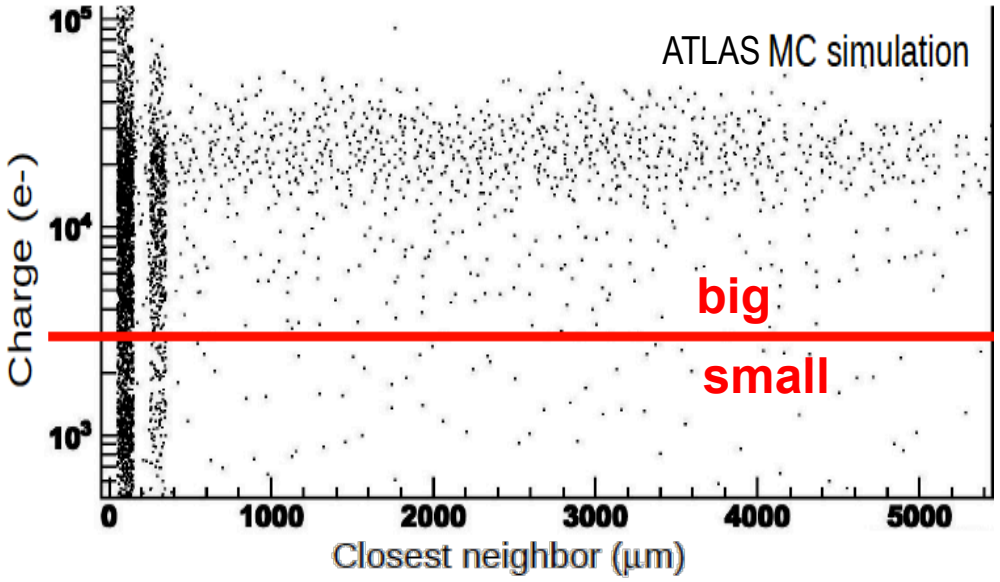
- Similar design of analog pixel in FEI3/FEI4
- Two-stage amplification
- Clock is distributed to all digital pixel region
- ToT counters within pixel digital region
- ToT together with pixel address sent to periphery

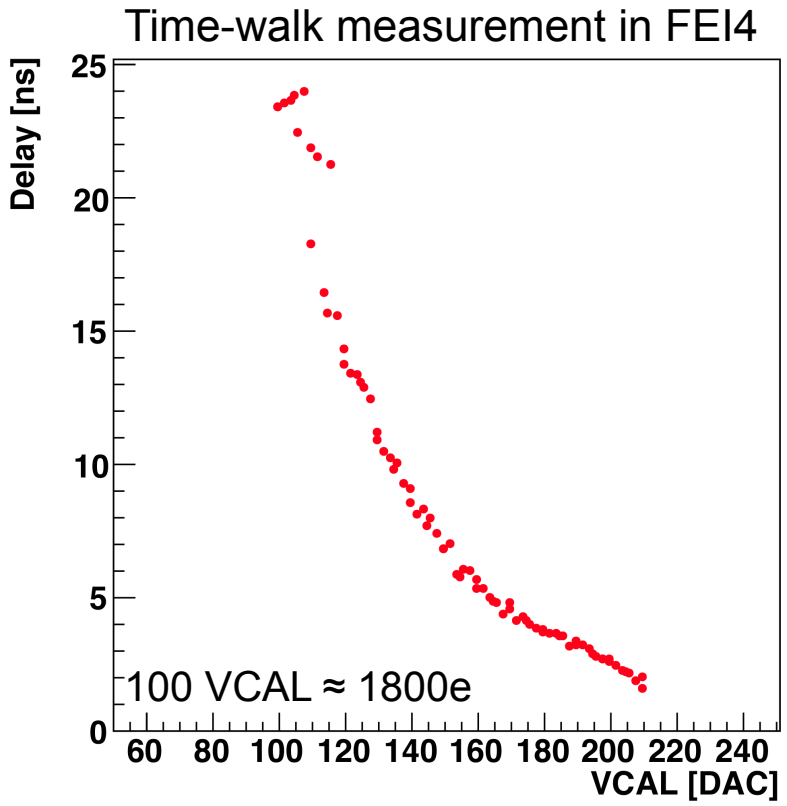
	FEI3	FEI4
ToT	8 bit	4 bit
TDAC	7 bit	5 bit
FDAC	3 bit	4 bit



Time-walk Correction in FEI4

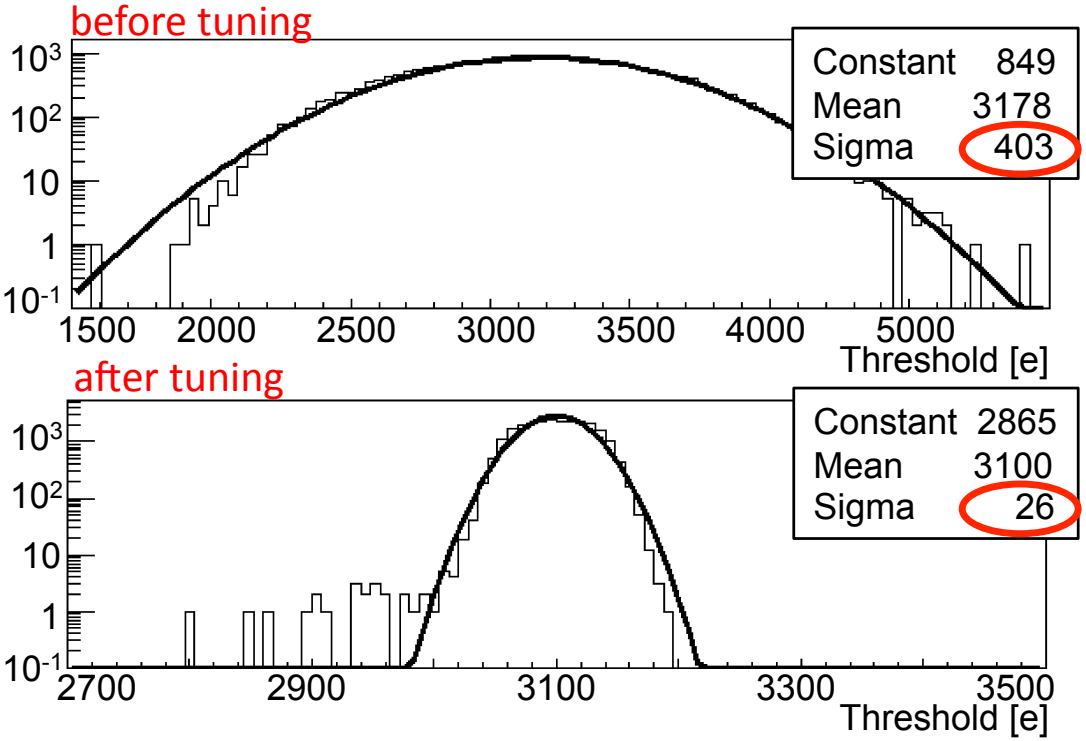
- Small hits are associated to big hits based on position rather than on time information
- PDR triggers on “big” hits and uses a time window of 2 BX to look for “small” hits
- Allows for lower power operation since digital logic corrects for reduced analog performance

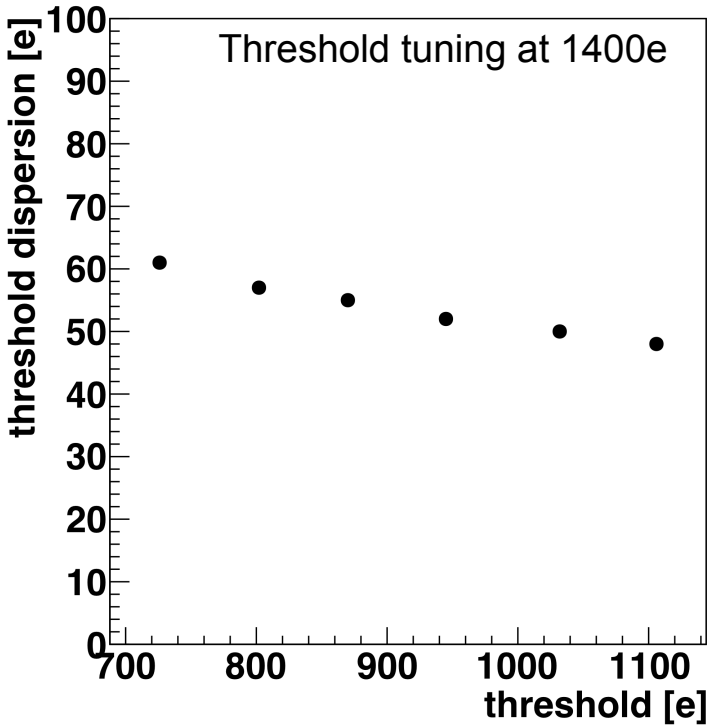




FEI4: Threshold and Noise

- FEI4 bump-bonded to planar and 3D sensors have been successfully operated in lab test, test beams and cosmic data taking
- Tuned threshold dispersion ~30e → Philippe Grenier's talk
- FEI4 low threshold operation (~700e) shows promising results with reasonable dispersion
- Irradiation tests with bare chips show no effect on threshold dispersion and 20% increase in noise





Power Consumption

- PSI46
  - Analog: 26mA x 1.7V = 44mW/chip => 11µW/pixel
  - Digital: 29mA x 2.5V = 73mW/chip => 17µW/pixel
  - Fluence dependent contribution 0.1µA/pixel*fluence [MHz/cm^2]
- FEI3
  - Analog: 75mA x 1.6V = 120mW/chip => 42µW/pixel
  - Digital: 49mA x 2.0V = 98mW/chip => 34µW/pixel
- FEI4
  - Analog: 350mA x 1.2V = 420mW/chip => 16µW/pixel
  - Digital: 110mA x 1.5V = 165mW/chip => 6µW/pixel
  - Reduced analog current in FEI4 (reduced analog performance is recovered by adding digital functionality)
  - Reduced digital current due to improved architecture

The Future

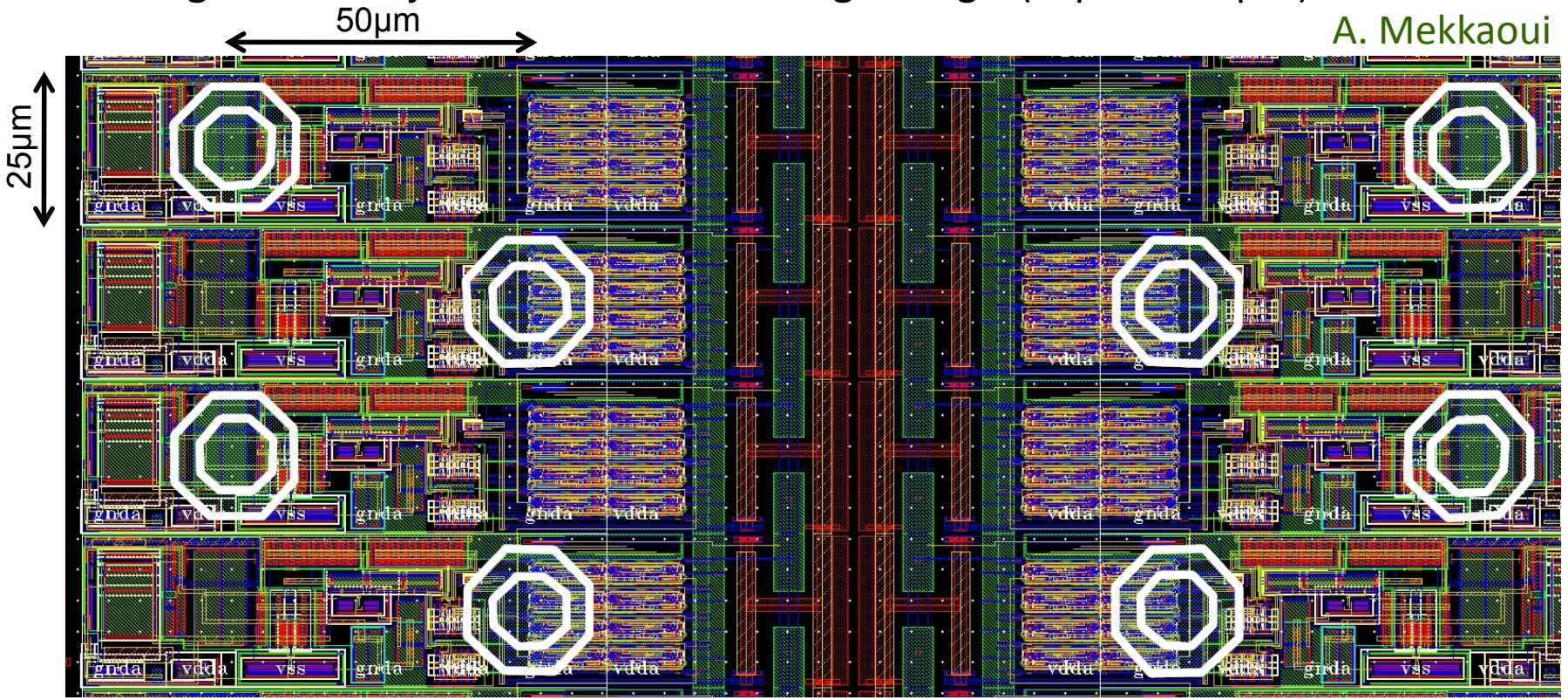
- Still higher rate needed for coverage of small radii at HL-LHC (peak luminosity of $10^{35}cm^{-2}s^{-1}$, 230 pile-up events)
- Need increased radiation hardness (up to 500Mrad)
- Aim for smaller, faster pixels and more memory per pixel
  - Reduce occupancy
  - Improve resolution
  - Reduce readout inefficiencies
- 2 directions being explored
  - High density: 65nm technology →Carl Grace's talk
  - 3D integration: Tezzaron-Chartered 130nm technology

→Satellite meeting on Tuesday

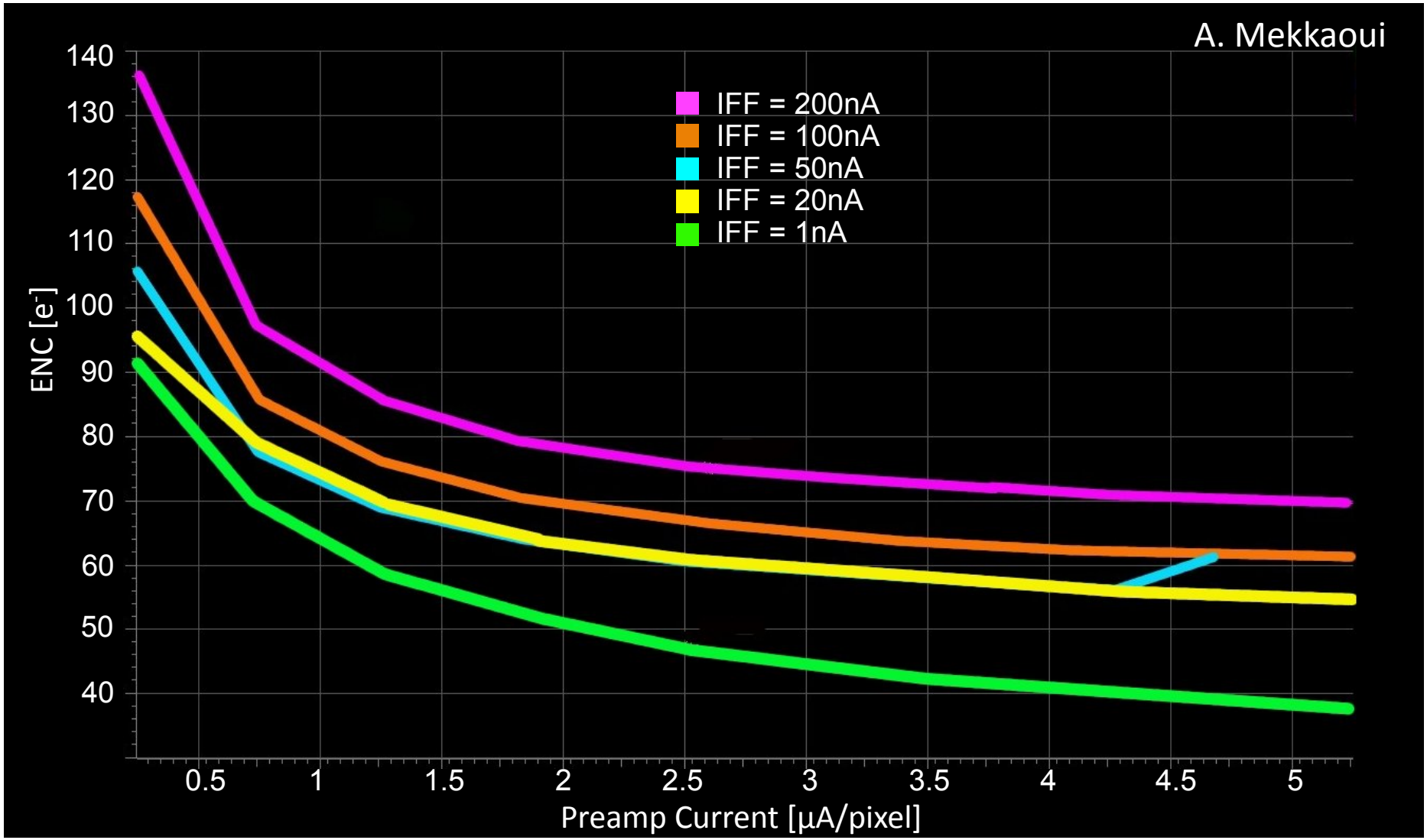
Prototype Analog Chip in 65nm

- Factor of 4 in area reduction for digital circuits compared to 130nm
- Idea: reduce analog complexity/performance and compensate with digital signal processing
- Prototype analog chip submitted on June 2, 2011
  - 25µm pitch in rϕ, 50µm bump spacing
  - z length to be adjusted as needed for digital logic (expect 150µm)

A. Mekkaoui

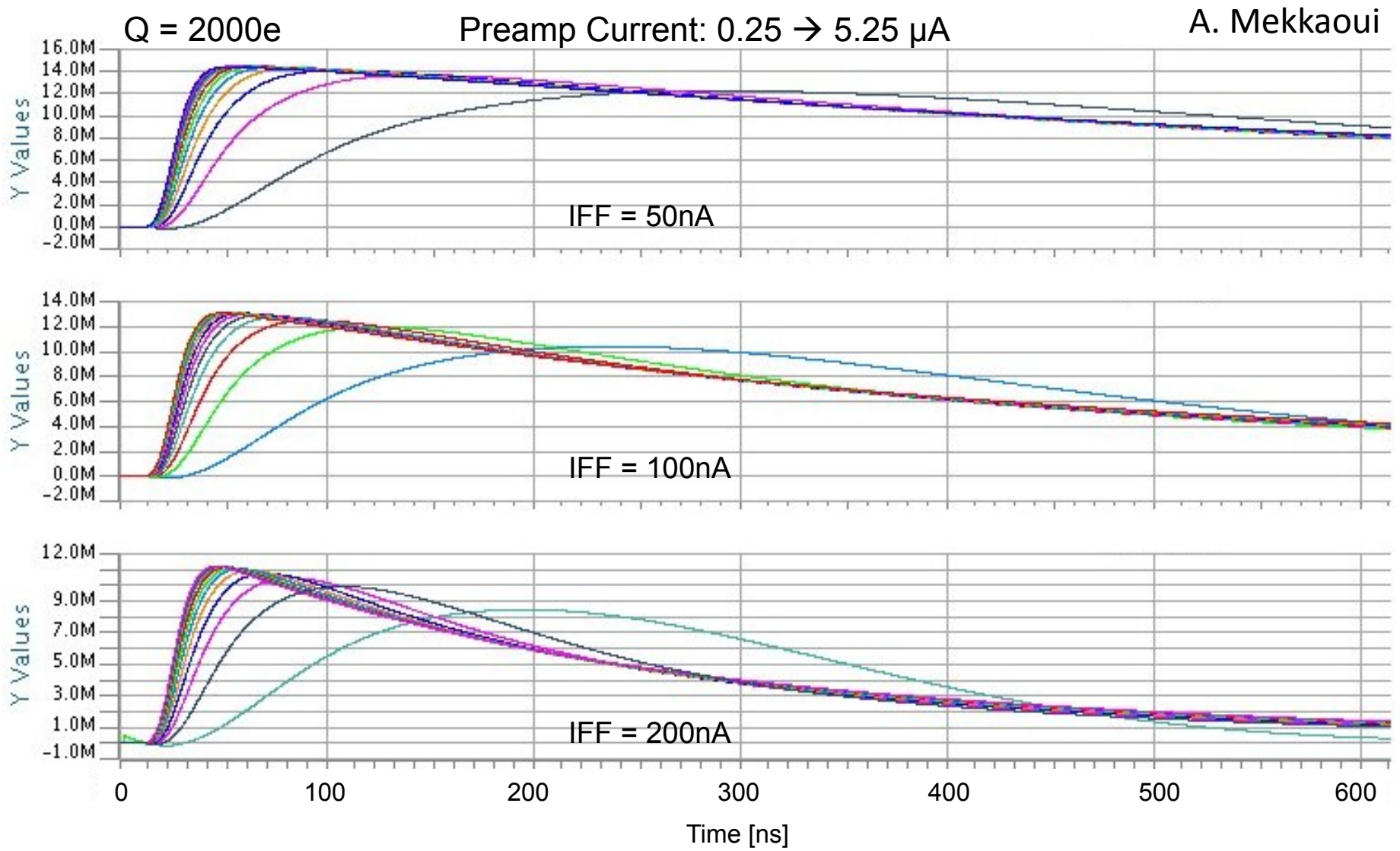


Simulation Results: Noise



- Noise increases slowly as current decreases
- Non-limiting factor

Simulation Results: Rise Time



Conclusion

- First generation of pixel detectors show excellent performance during LHC data taking and substantially improve physics potential of the experiments.

- FEI4 presents a new chip for upgrade projects. It includes real innovation and reduces the cost of module production thanks to its size and reasonable wafer yield. Submission of FEI4A was a success.

- R&D of readout electronics for HL-LHC is ongoing. Newly available technologies like 65nm feature size and 3D technology are being exploited.

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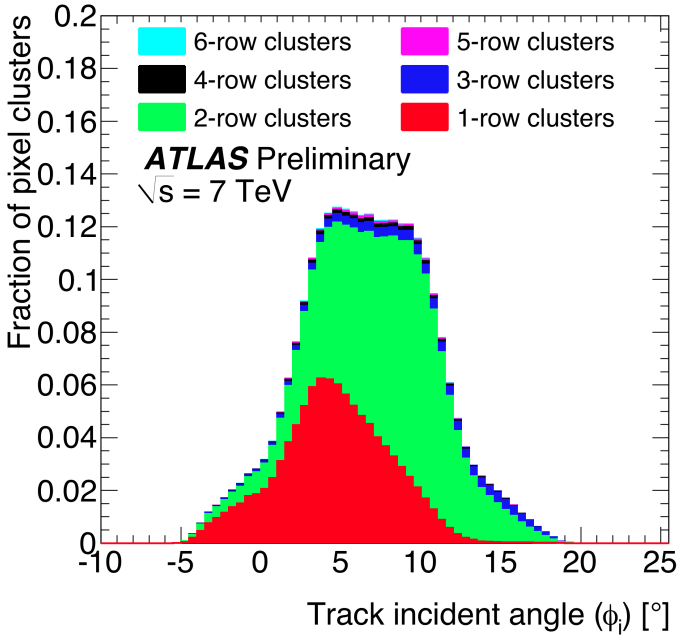
Goettingen: Joern Grosse-Knetter, Jens Weingarten

SLAC: Martin Kocian

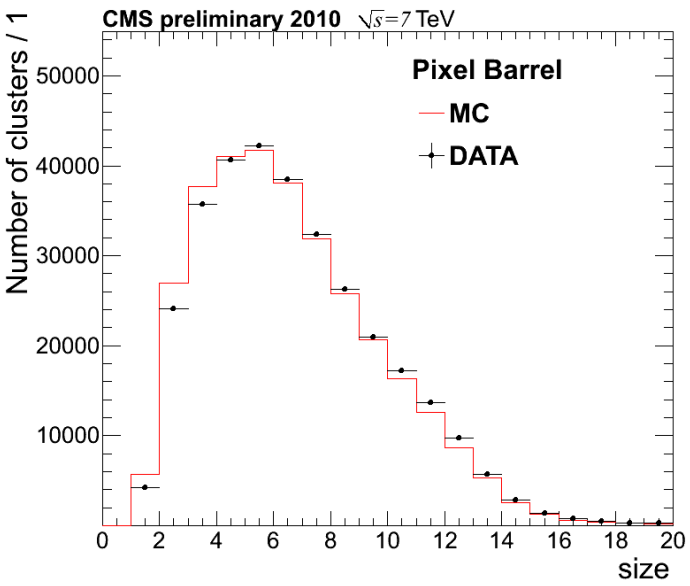
Backup

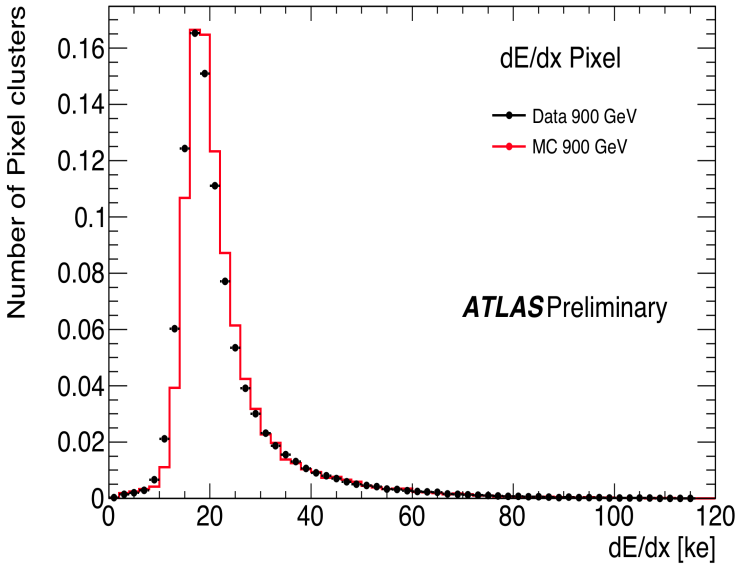
Cluster Size and Cluster Charge in ATLAS/CMS

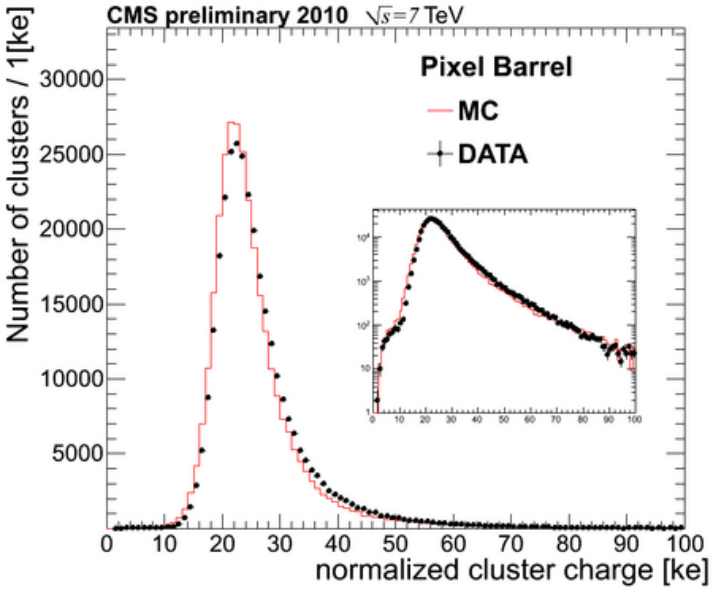
ATLAS



CMS

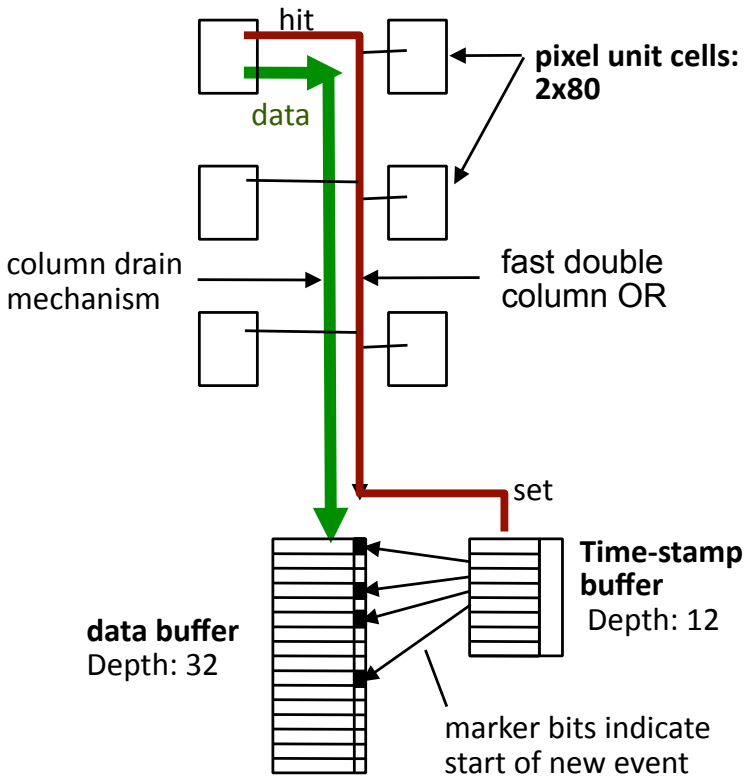


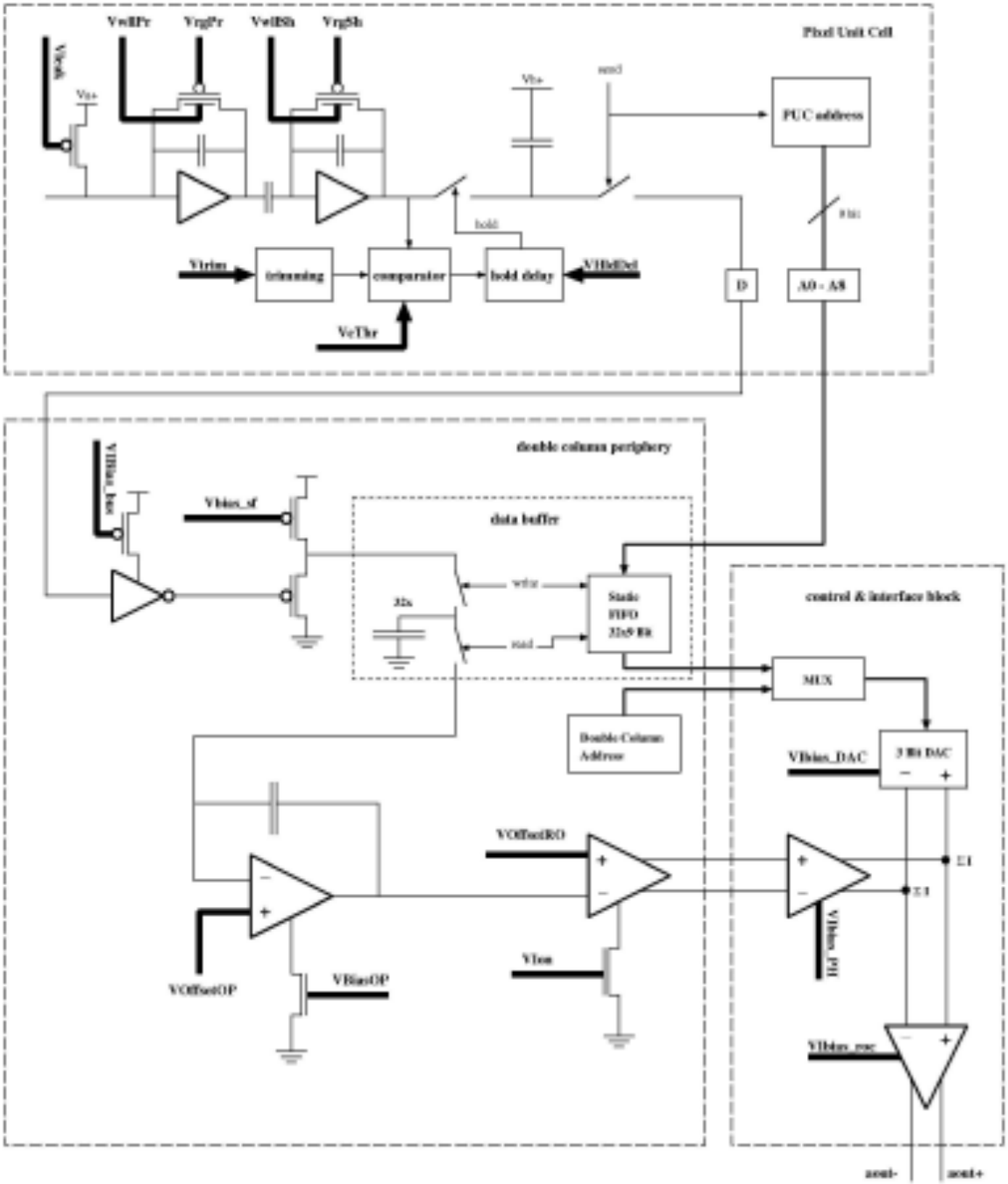




PSI46 readout architecture

sketch of a double column

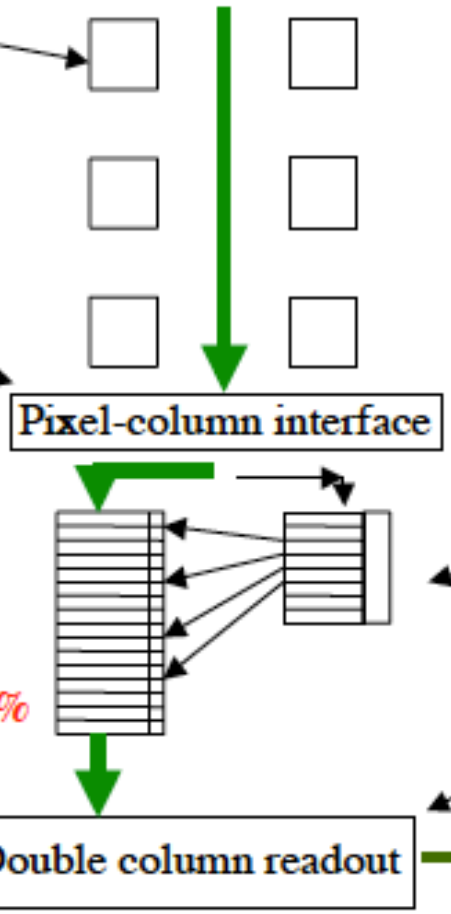




Data loss mechanisms

Pixel busy:
0.04% / 0.08% / 0.21%
pixel insensitiv until hit transferred to data buffer (column drain mechanism)

Double column busy:
0.004% / 0.02% / 0.25%
Column drain transfers hits from pixels to data buffer. Maximum 3 pending column drain requests accepted



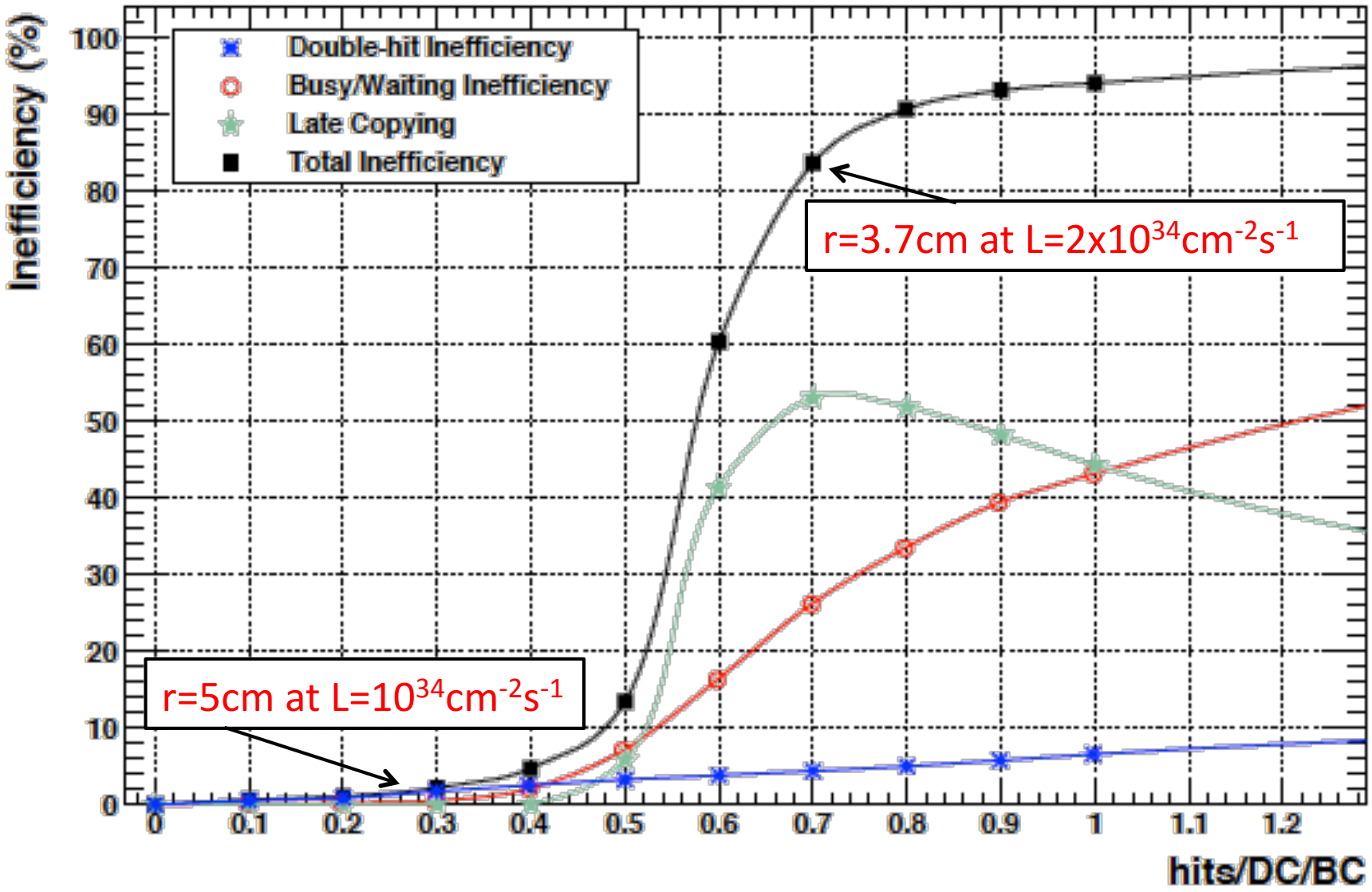
- 1xLHC: $10^{34}cm^{-2}s^{-1}$
- 11 cm / 7 cm / 4 cm layer
- total data loss @ 100kHz L1A:
  - 0.8%
  - 1.2%
  - 3.8%

Timestamp Buffer full:
0 / 0.001% / 0.17%

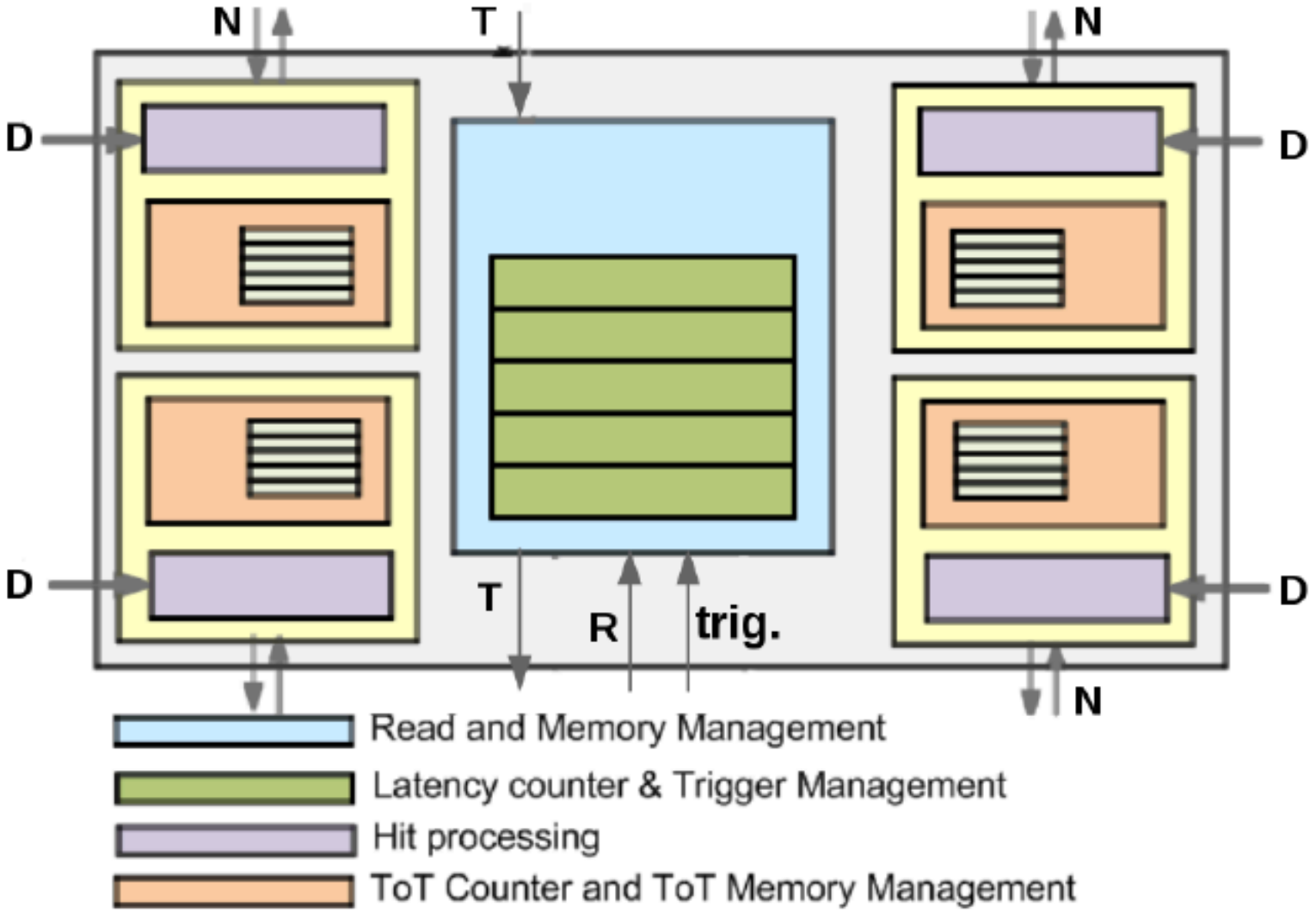
Data Buffer full:
0.07% / 0.08% / 0.17%

Readout losses:
0.7% / 1% / 3.0%
for 100kHz L1 trigger rate
Column is blocked after L1A and reset when read out

FEI3 Column Drain: Limitations at high rate



FEI4 4-pixel digital region with neighbor logic



FEI4 Digital Column Simulation vs Measurement

Simulation @1.2V

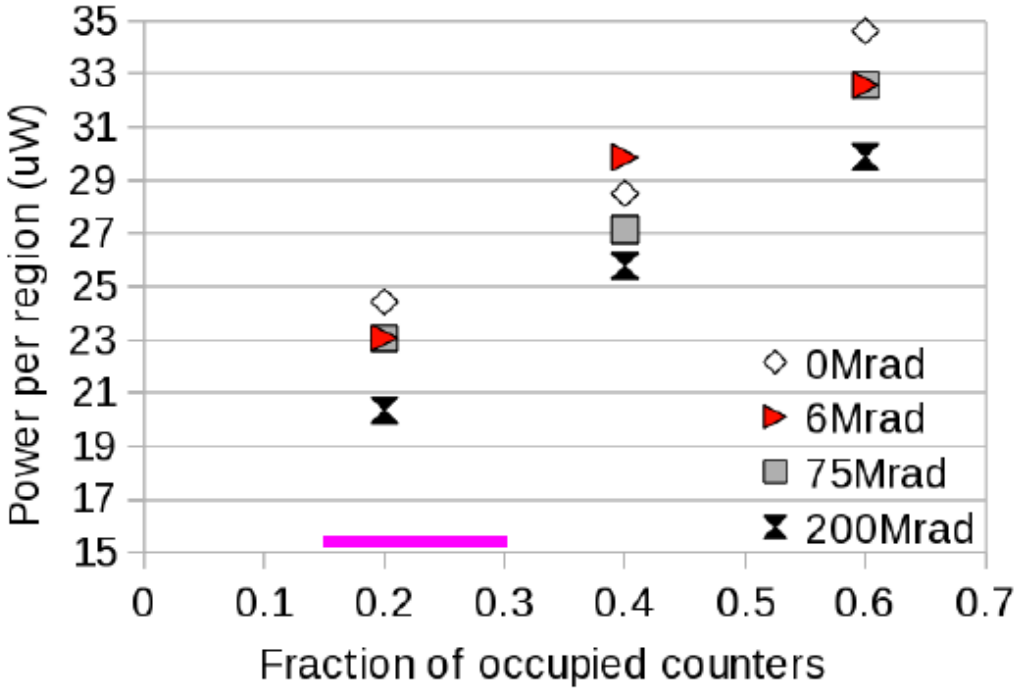
Average power for 4-pixel region at IBL occupancy (MC hits)

Simulation type	Power (avg) [uW]
ETS[1]	42.28
Spectre[2]	25.19
Ultarasim(s)[2]	24.69
Ultarasim(a)[2]	24.73
Ultarasim(ms)[2]	35.12
HSIM[1]	27.64
HSIM[2]	30.98

Parasitic extraction done width [1]PEX

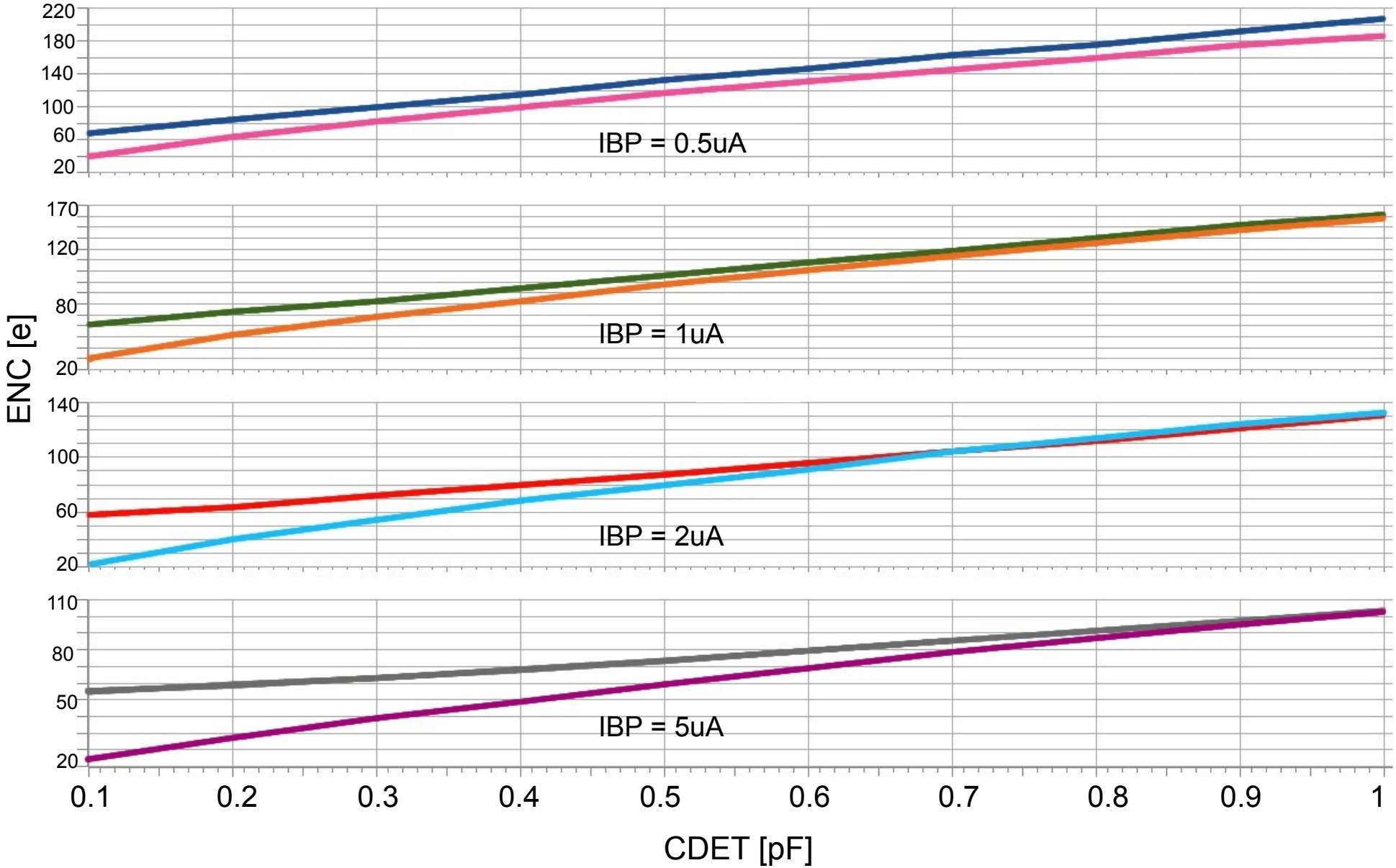
Measurement @1.2V

Occupancy faked with periodic charge injection



Approx. IBL range

65nm Simulation Results: ENC vs CDET



DEPFET – Depleted P-channel Field Effect Transistor

- Each pixel is p-channel FET on completely depleted bulk
- Charge collection by drift
- Signal electrons accumulate in internal gate and modulate transistor current
- Accumulated charge removed by clear contact
- Internal amplification
- Readout on demand