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Recent developments of HEP pixel detector readout chips

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We cover development of readout integrated circuits for hybrid pixel particle physics detectors. We compare the 250nm feature size chips in the presently operating ATLAS and CMS experiments with the current state of the art in 130nm feature size represented by the FE-I4 chip that will be used to add a new beam pipe layer for the ATLAS experiment in 2013 and the upgrade options of the CMS pixel readout chip. We discuss array and pixel size, analog performance, readout architecture, power consumption, power distribution options and radiation hardness. Finally, we present recent work in 65nm feature size as a means to continue the evolution of readout chip technology towards smaller feature size, higher rate, and lower power.

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