A tracker/trigger design for an upgraded CMS Tracker

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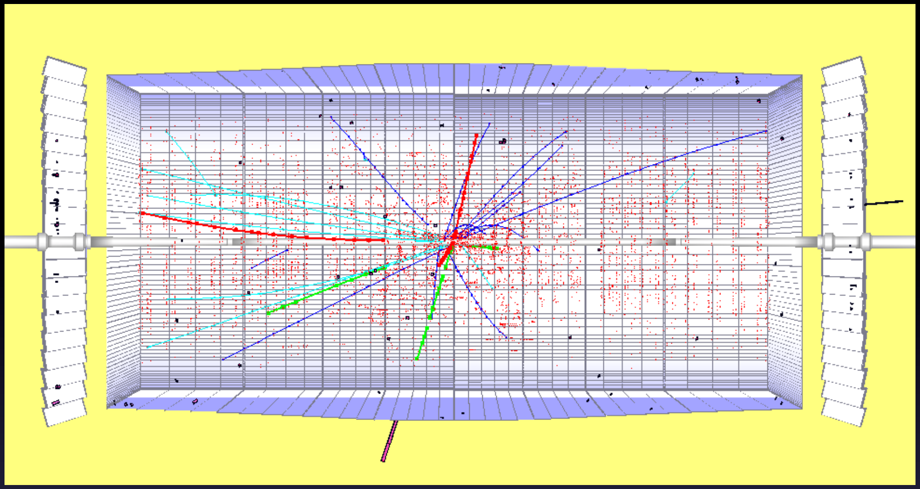
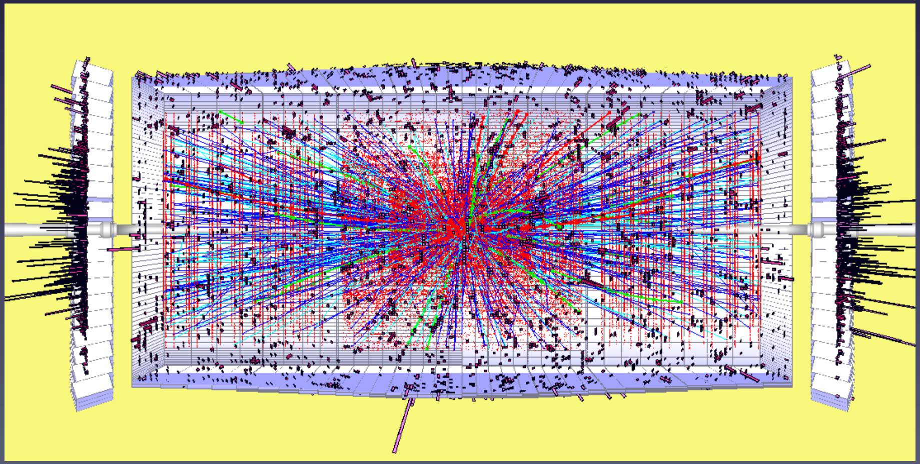
for the CMS tracker/trigger R&D group

Pile-up at LHC/HL-SLHC



10^{33} cm^{-2} s^{-1}
(now)

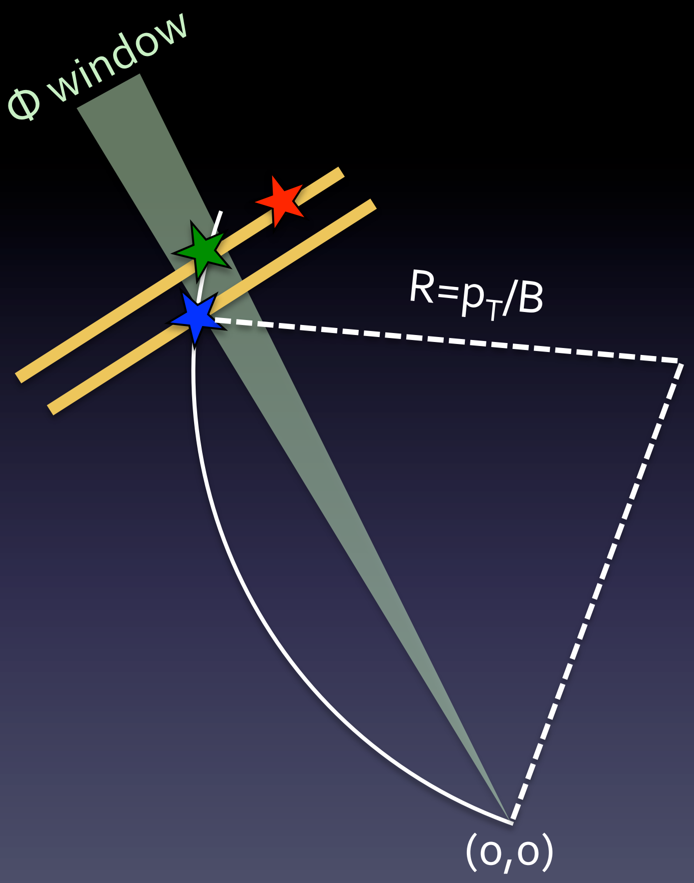


10^{35} cm^{-2} s^{-1}
(2x HL_LHC)

- At 200 pile-up events per 25ns beam crossing L1 triggers will start to saturate.
  - The L1 maximum accept rate is expected to remain unchanged at 100 kHZ
- An upgraded CMS Tracker, with its fine granularity, is a natural candidate for augmenting the existing L1 trigger.
- However, the challenge is to process the 200 pile-up Tracker data well within the data-hold period of the CMS detectors.
- There are a few ideas being considered for including an upgraded Tracker in the L1 trigger.

One Idea

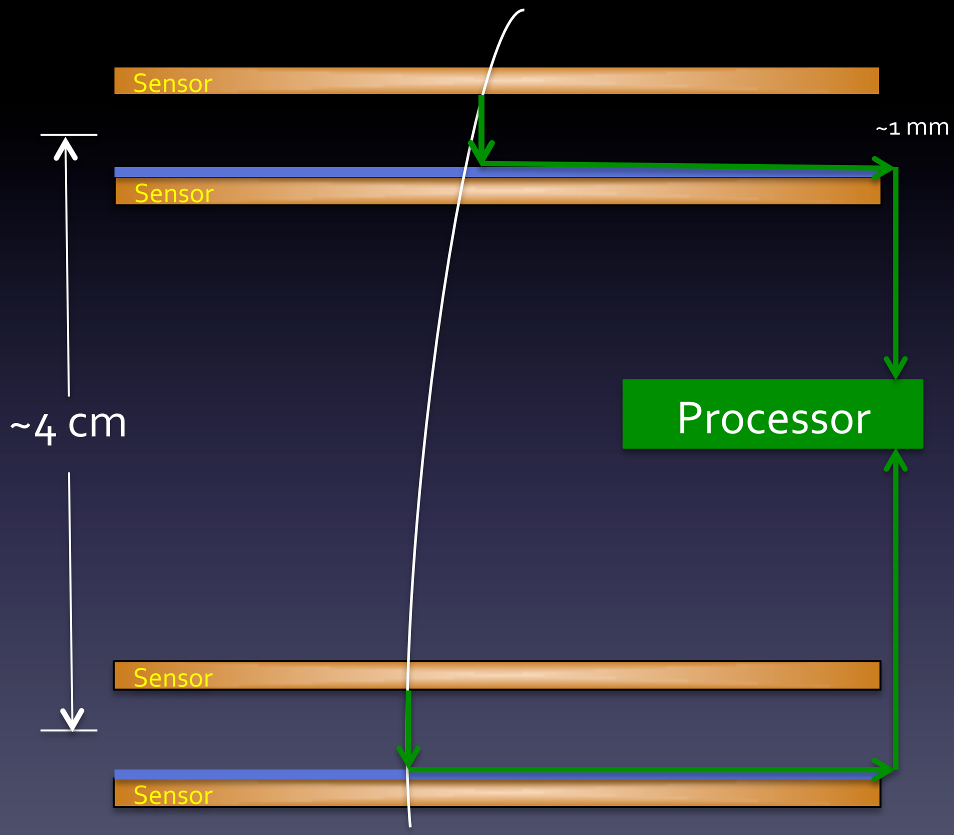
- At 200 interactions/crossing
  - $3\text{x}10^{13}$ bits/second
  - Too much data to move off detectors
- Trigger on p_T by looking for pointing coincidences in planes separated by ~1mm
  - Infinite $p_T \Rightarrow 90°$
  - 2 GeV/c $\Rightarrow 83°$



Push only data of interest off detectors

Double Stack Concept

- A stack consists of two detectors separated radially by about 1 mm
- A double stack consists of two stacks separated by about 4 cm.
- Pass stack correlated hits to an off-detector processor to form final trigger decision.
  - stub
  - tracklet



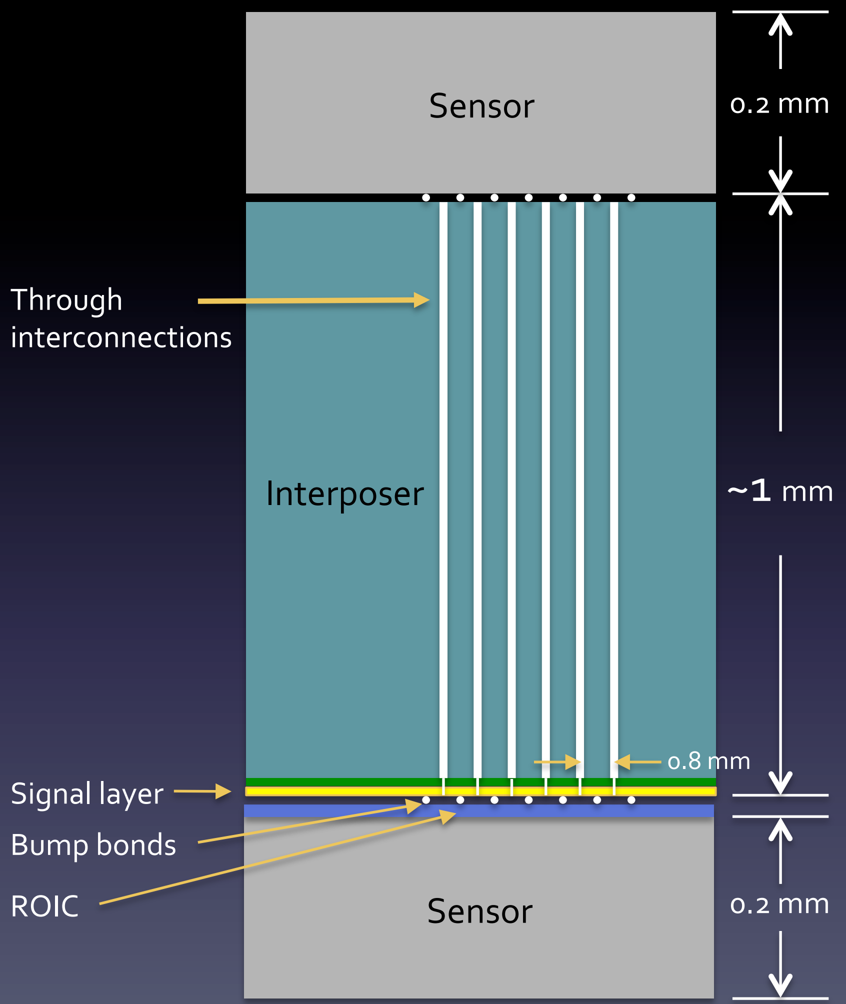
A group of CMS institutes* has been engaged in an R&D effort to explore the use of tracker elements incorporating 3D technology with the idea of establishing an on-detector trigger based on high transverse momentum tracks in HL-LHC. To complement the 3D development work the group has been pursuing

- Interposer design and bump bonding
- Mechanical prototyping of rods based tracker/trigger modules
- Layout studies based on a barrel geometry
- Asynchronous pipelining of on-detector data
- An off-detector FPGA based processor
- Protocols for data transmission
- Material budget and thermal performance studies
- Simulation studies
- Large area array considerations (edgeless sensors)

There are other ideas for triggering on tracker elements that are currently being explored within the CMS upgrade framework and the expectation is that R&D efforts will eventually coalesce into a unified approach.

*Boston, Brown, CERN, Cornell, UC Davis, FNAL, UC Riverside, Rochester, UC Santa Barbara, Texas A&M, Vanderbilt.

Stack Details



- Vertical information flow from outer to inner stack layers
- Readout chip (ROIC) connected to inner sensor
  - Oxide bonding
- Low mass interposer
  - transmits analog signals from upper sensor
  - bump bond connections
  - silicon? Arlon? kapton?
- Through Silicon Vias used to connect ROIC to bonding pads

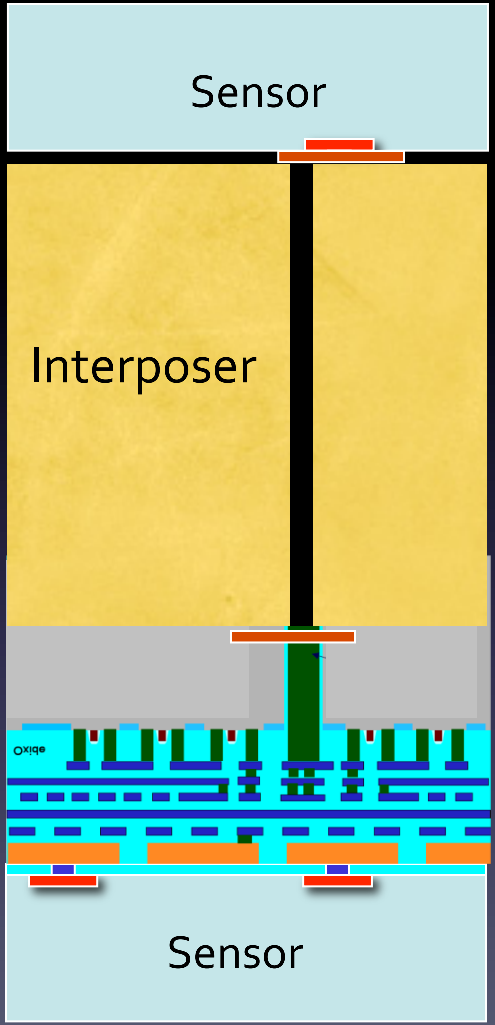
Vertically Interconnected Stack

Assembly process

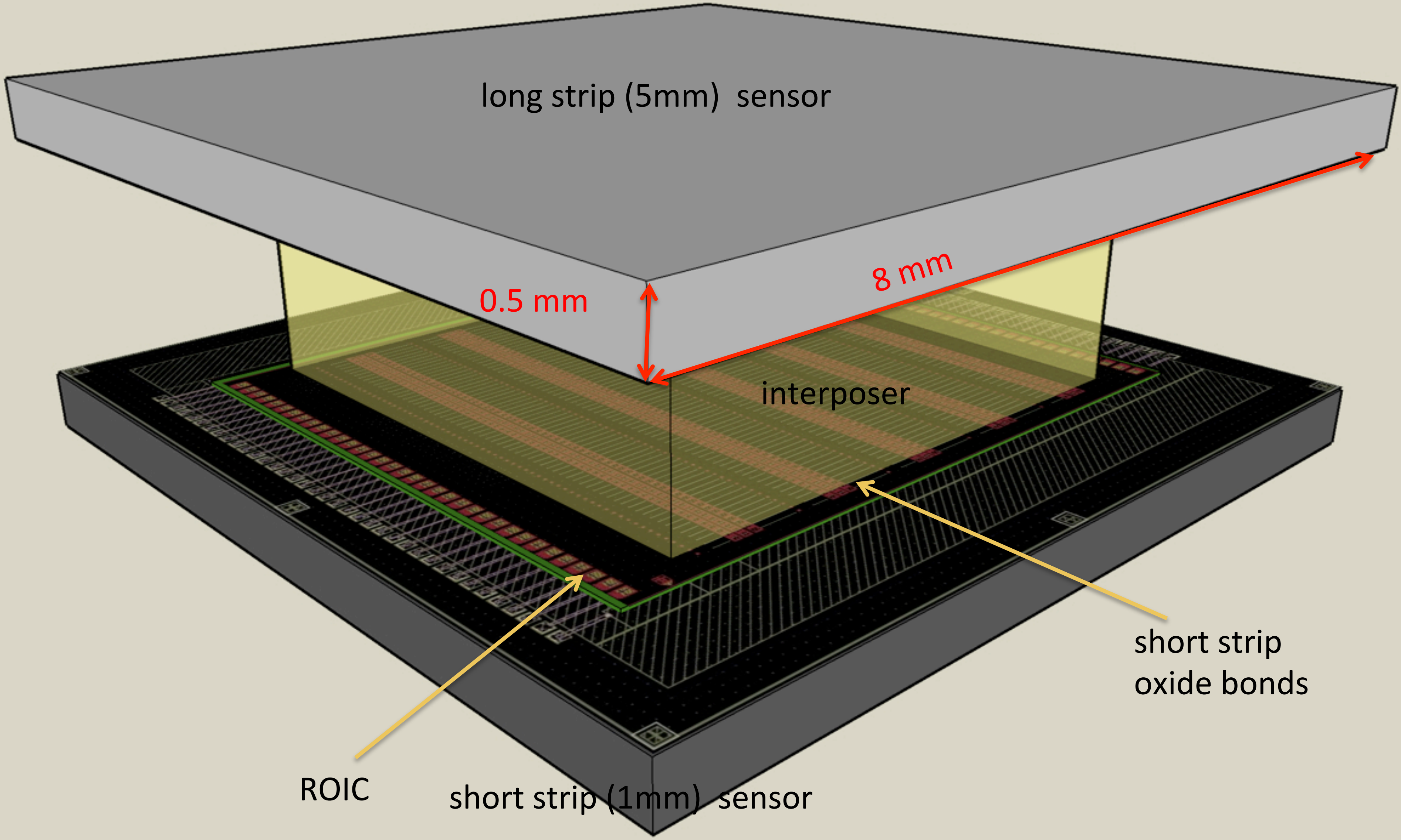
- oxide bond ROIC to inner sensor
- thin carrier to expose through silicon vias
- add contact pads
- bump bond interposer
- bump bond outer sensor

Work closely with vendors

- Tezzaron (ROIC)
- Ziptronix (DBI)



Demonstration Model



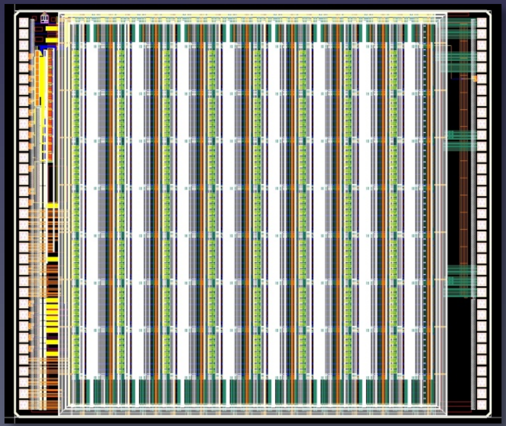
VICTR

Vertically Integrated CMS Tracker ASIC

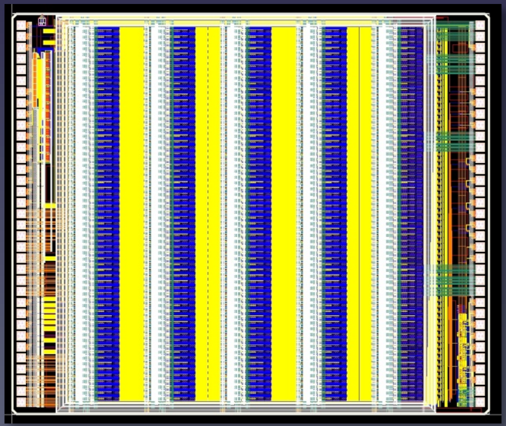
- Included with recent Fermilab-sponsored 3D multi-project run
- Simplified design for demonstrating the basic technique of vertical interconnections
- 3D chip with Through Silicon Vias
- ATLAS front-end (FE-14) design
- Top and bottom connections designed for long strip and short strip stack combinations.

long strip sensor ←

Top tier



Bottom tier

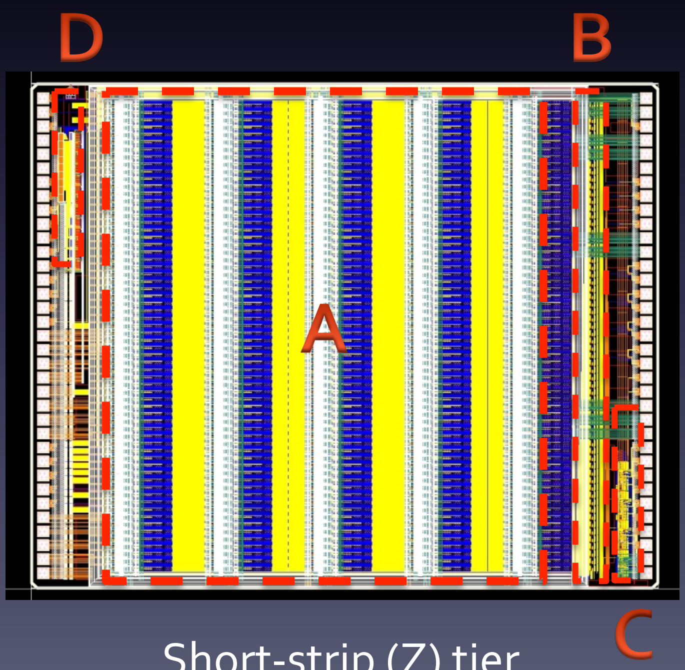


→ short strip sensor

Initial VICTR Testing

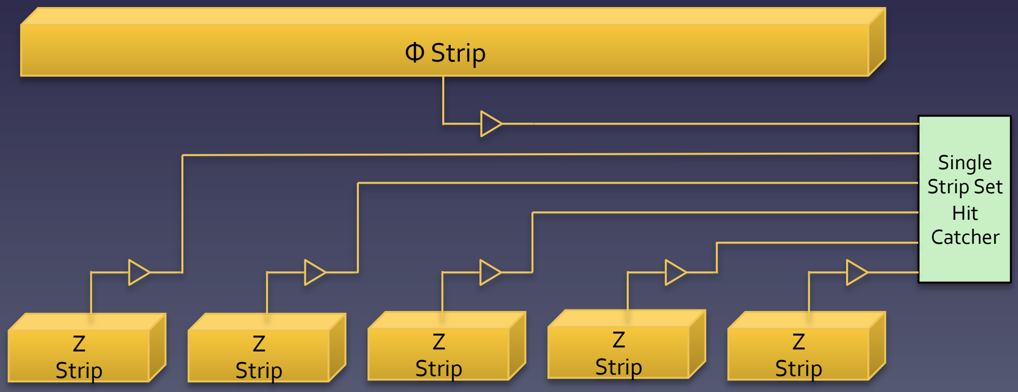
Testing underway at FNAL of short-strip (Z) tier

- inject charge and measure front-end amplifier response
- front-end bias adjusted via on-board slow controller



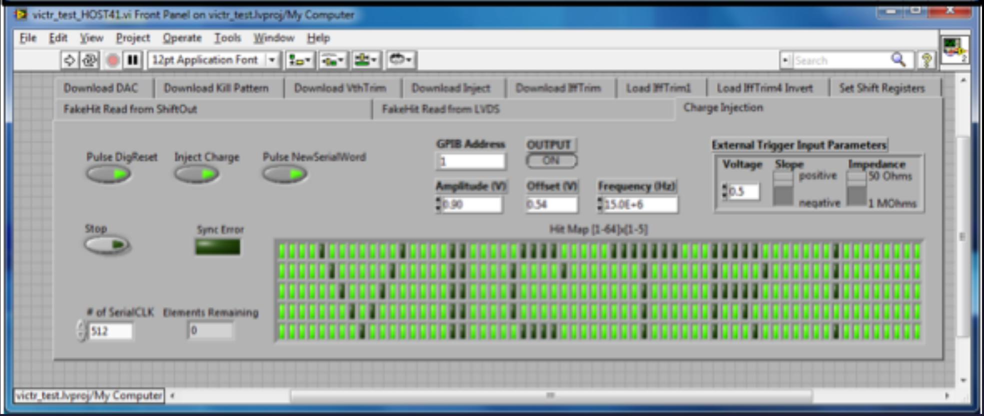
Short-strip (Z) tier

A: 320 (5x54) front-ends
B: back-end readout
C: LVDS drivers for readout output
D: DACs providing front-end bias



VICTR test results

Hit Map from Charge Injection (consistent with kill map)



GPIB Address 1

Amplitude (V) 0.90

Offset (V) 0.54

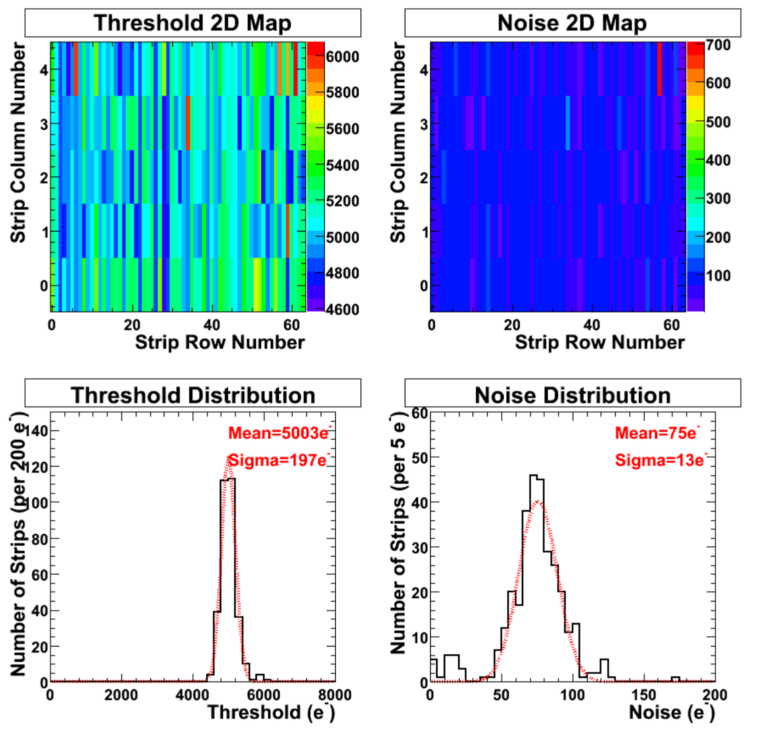
Frequency (Hz) 15.0E+6

Voltage 0.5

# of SerialCLK 512

Elements Remaining 0

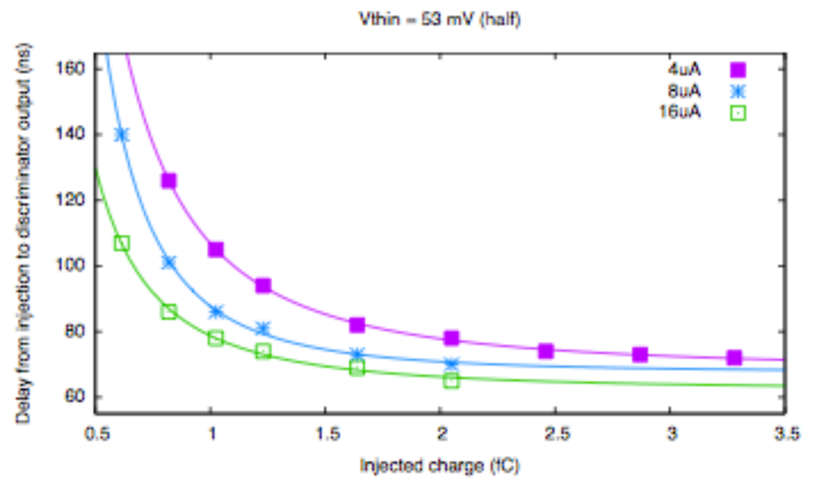
- ➢ downloading chip register
- ➢ control of front-end bias
- ➢ front-end response
- ➢ back-end readout
- ➢ DAQ system



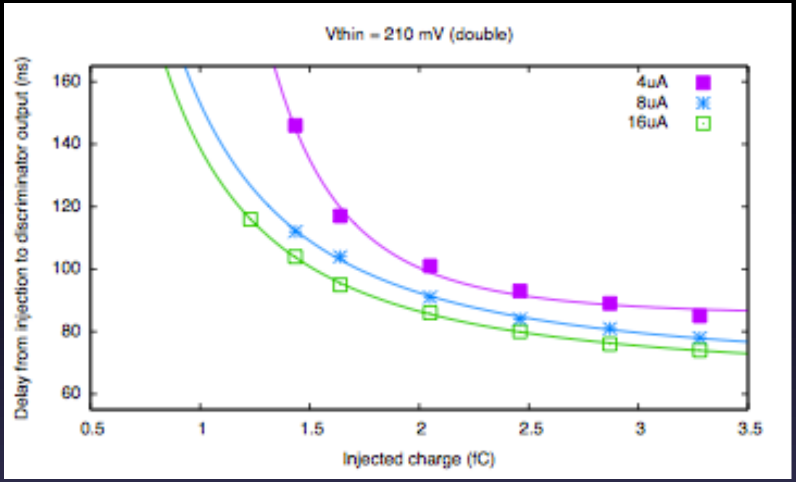

test pulse

VICTR time-walk results

Half default value



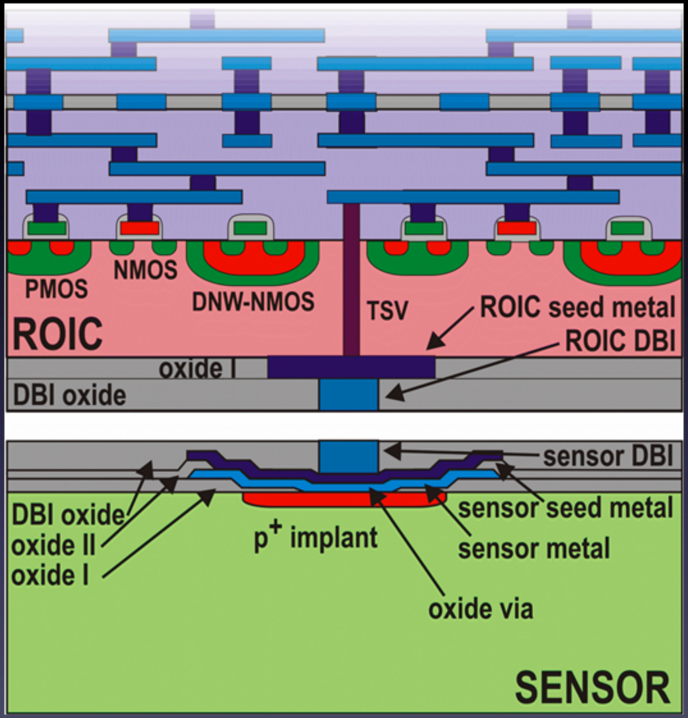
Twice default value



Our best estimate is that the power density for a stack will be around 35mW/cm^2 (not including GBT power and sensor currents). However, this will eventually need to be studied with prototypes that are closer to the final design and take into consideration requirements such as minimal time walk. The 35mW/cm^2 , which has important implications for the material budget, may prove to be optimistic.

DBI® – direct bonded interconnect

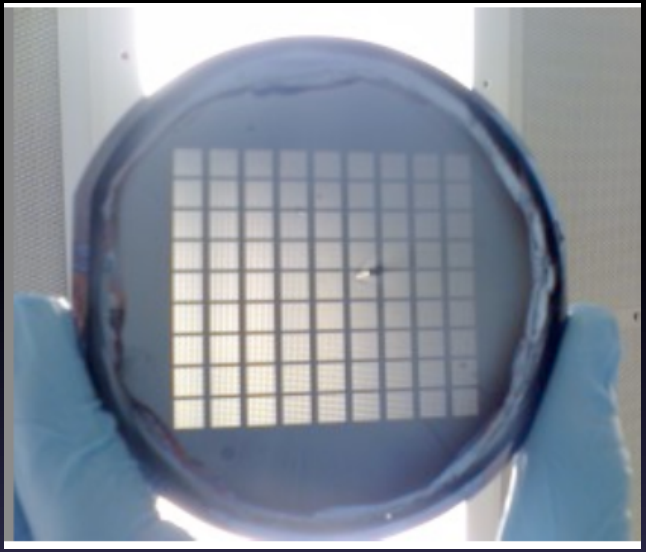
- Developed by Ziptronix
  - www.ziptronix.com
- Oxide bonds between activated SiO_2 surfaces with integrated metal
- Alternative to bump bonding
  - Permits a much finer pitch (down to a few microns).
- Initial bonding at room temperature
  - Cure at 350°C
- <u>Requires tight flatness tolerance</u>

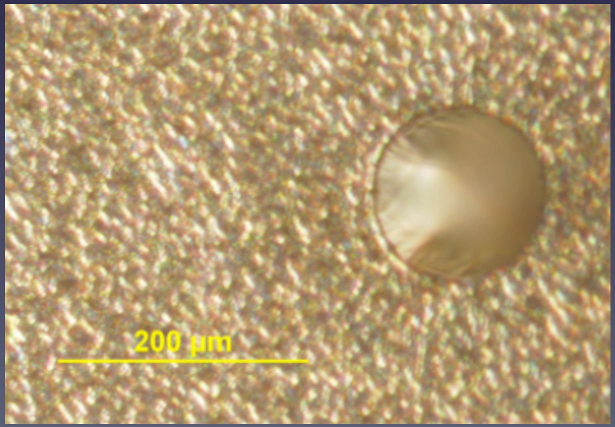


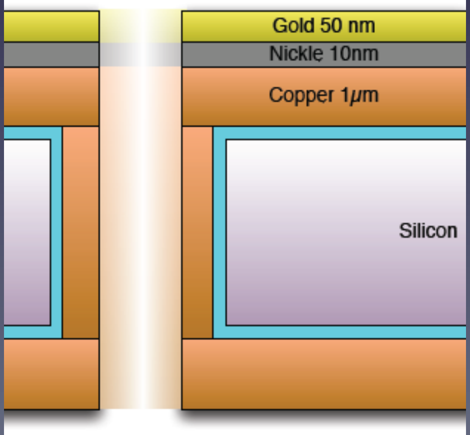
Have not yet attempted with VICTR chip

Interposer Development

- Cornell fabrication laboratory
- Silicon used for the initial approach
  - Good CTE match with sensors
  - Form vias by deep silicon etching
  - Oxidize and create conductive connections by metal sputtering
  - Evaporate on bonding pads







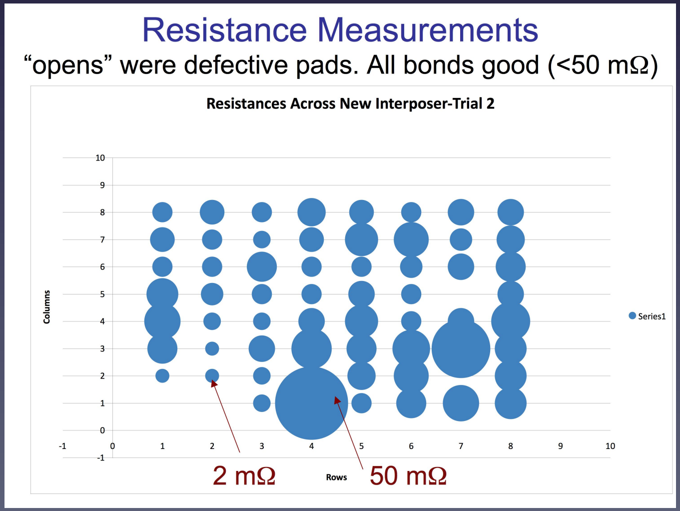
Interposer-Sensor bonding

Gold-stud bonding at UC Davis

Arlon interposer (mechanical model from FNAL) bonded to sensor provided by BNL.

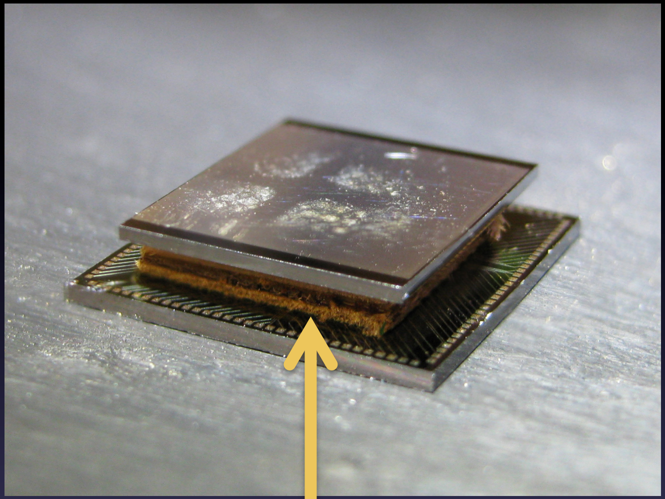
Test chip provided by Cornell.

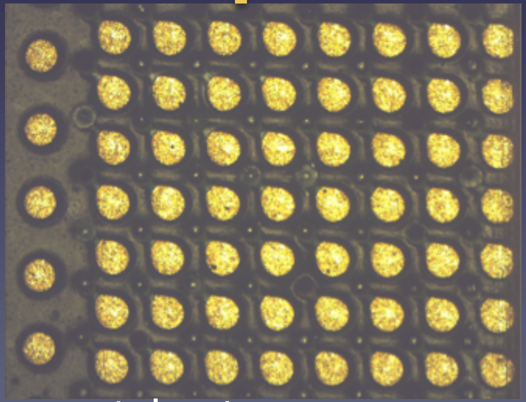
Some defective pads but all bonds good.



Resistance Measurements

“opens” were defective pads. All bonds good (<50 mΩ)

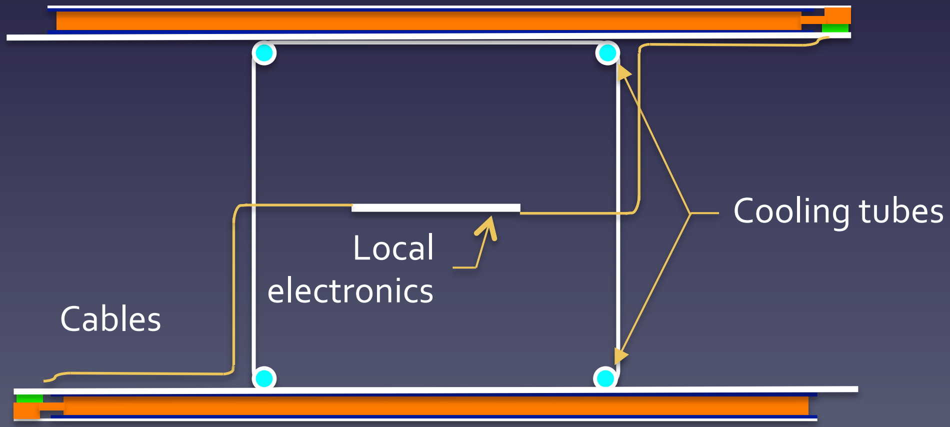




Arlon interposer

Mechanical Design/Prototyping

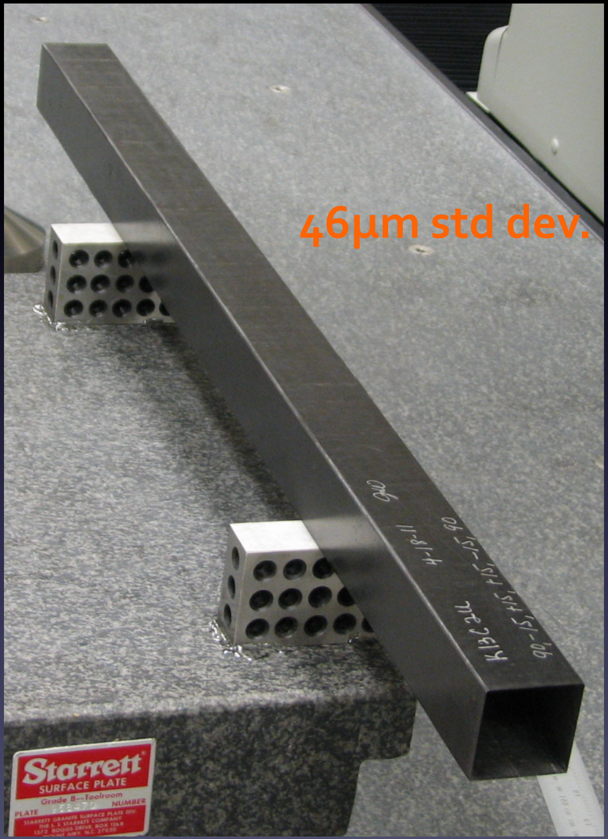
- Box beam used to separate stacks by ~4cm
- Low mass
  - Carbon Fiber
  - CO_2 cooling
- Electrical conductivity through co-cured copper mesh (technique developed for D0 L0)



Cooling tubes

Local electronics

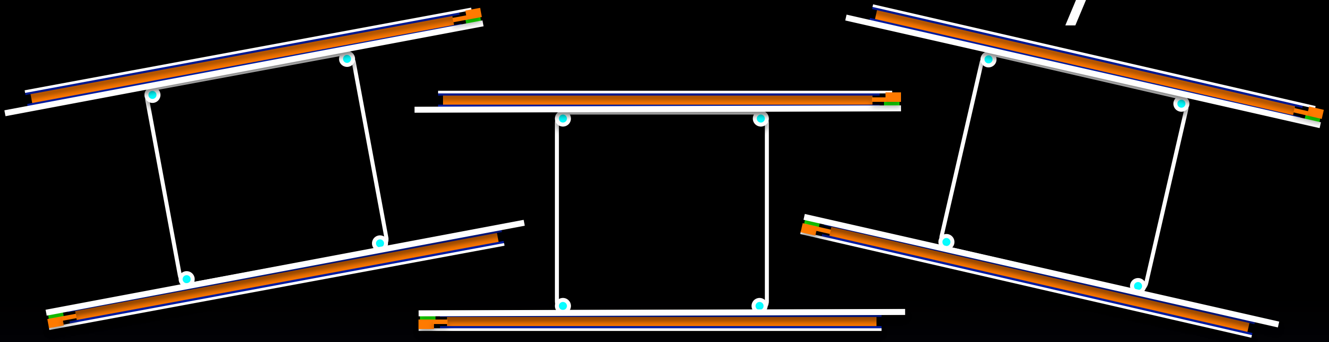
Cables



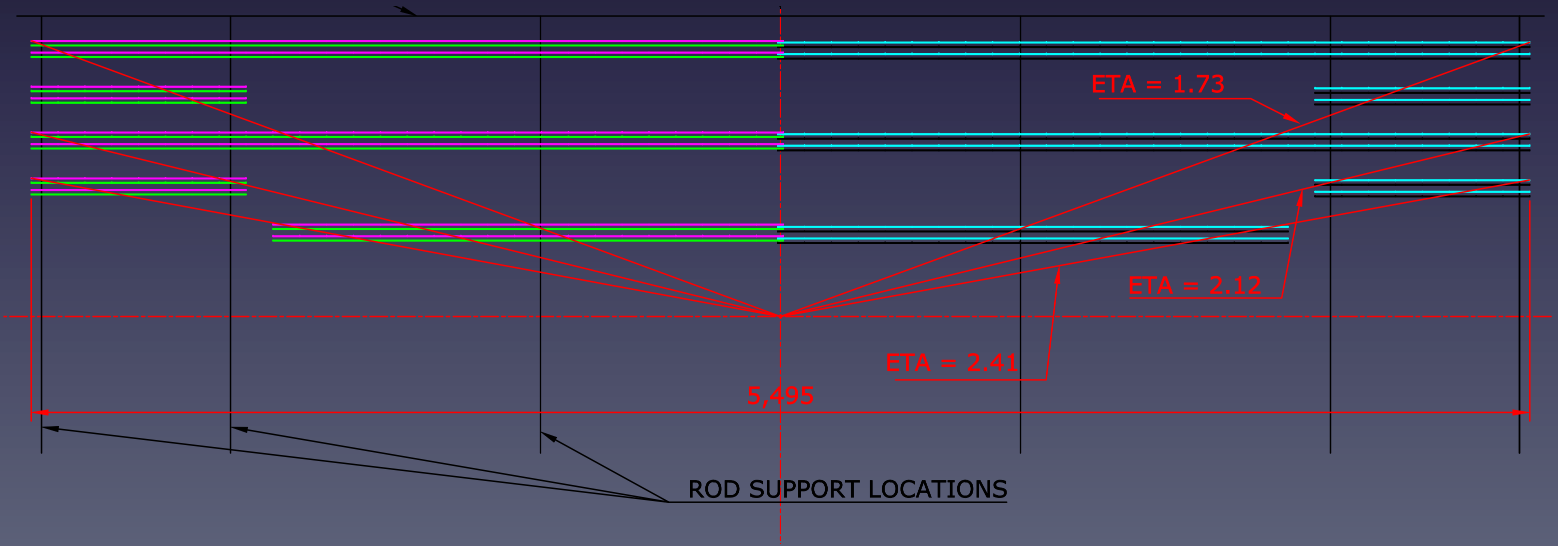
46µm std dev.

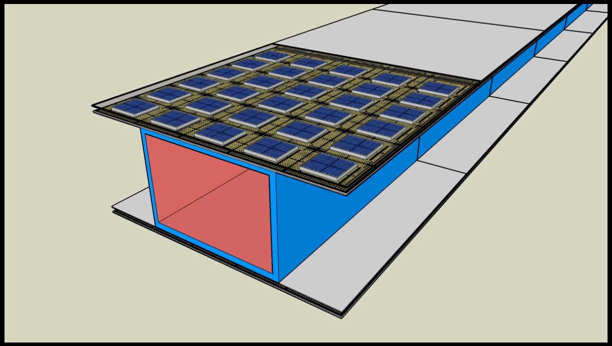
73 cm long prototype CF box, one of two at the FNAL Silicon Detector lab

Barrel Geometry



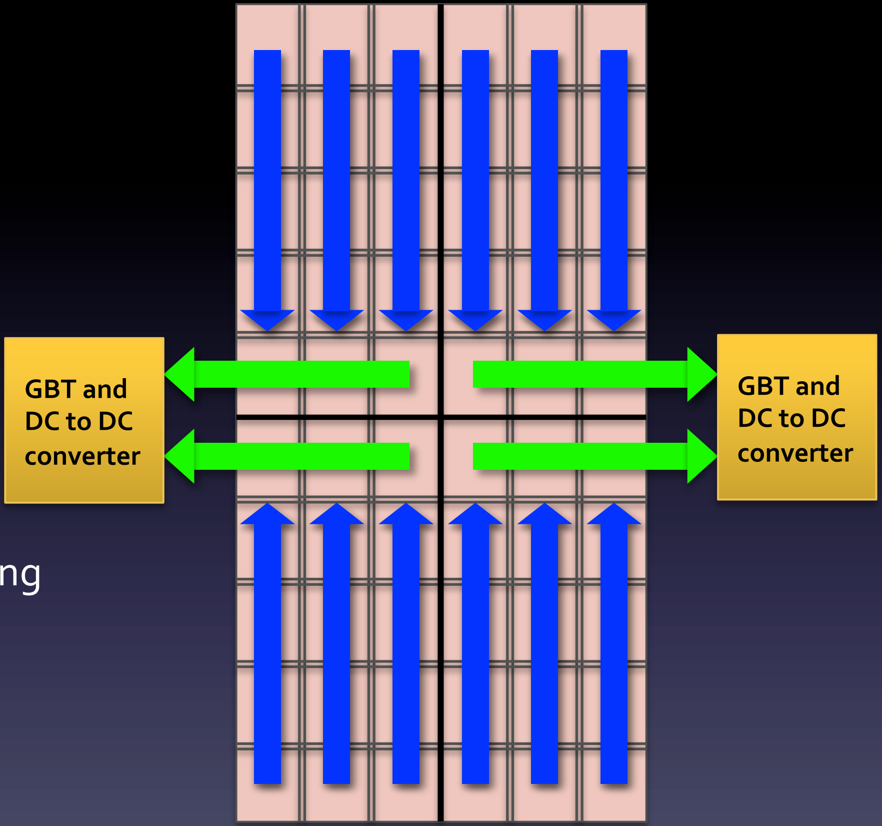
5 layer barrel layout (including short barrels)
One of many scenarios under consideration for HL_CMS
Assumes an inner pixel system (not shown)





Data Flow

- 30 chips/10x10 cm² sensor
- ROIC
  - Correlates hits from outer and inner sensors
  - Sends edge data to neighbor chips
  - Forms data clusters for readout
  - Stores clusters for trigger latency time
  - Forms high pT stubs for off-detector processing
  - Run asynchronously with minimal clocking
- GBT
  - Fiber optic driver
  - 5 GB/sec bandwidth (unidirectional to save power?)
  - Handles both trigger and event streams



GBT and DC to DC converter

GBT and DC to DC converter

Conceptual work at FNAL

Data Flow Issues

- Thin sensors (200μm thick silicon)
  - small signal-to-noise, some degradation with radiation damage
  - shielding?
- High data rates (~4 GHz/half sensor)
  - data spread out across 15 chips
  - pipelining required for chip readout
- Large variations in chip rates
  - asynchronous design using micro pipeline
  - each chip sets up a pipeline only as long as its data
  - synchronous – asynchronous transition every 25 ns
    - race conditions
- Redundancy
  - must be robust against the failure of a single chip ⇒ material budget conflict

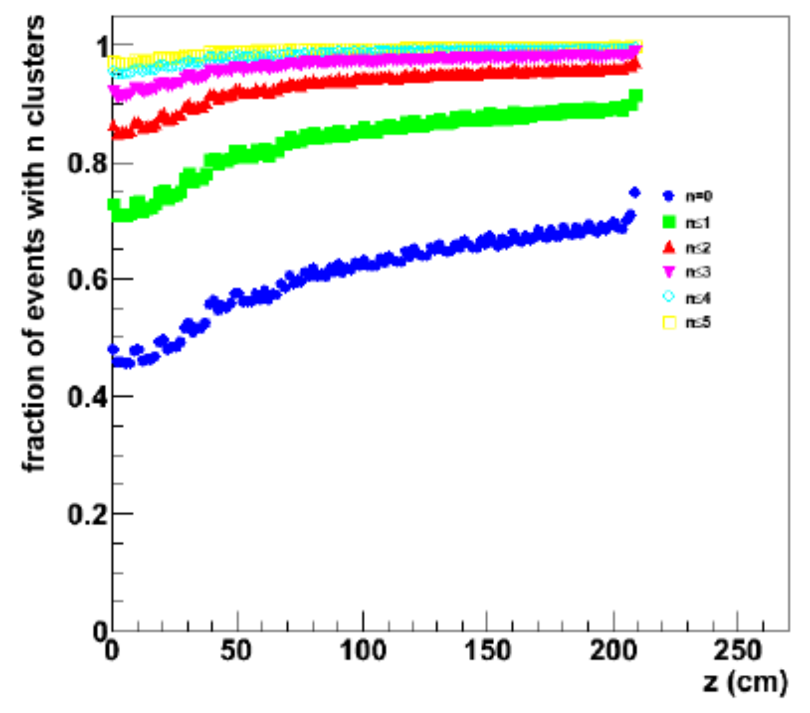
Simulation

Fast simulation based on 200 minbias Pythia events

Study done at Boston University

Z = 0

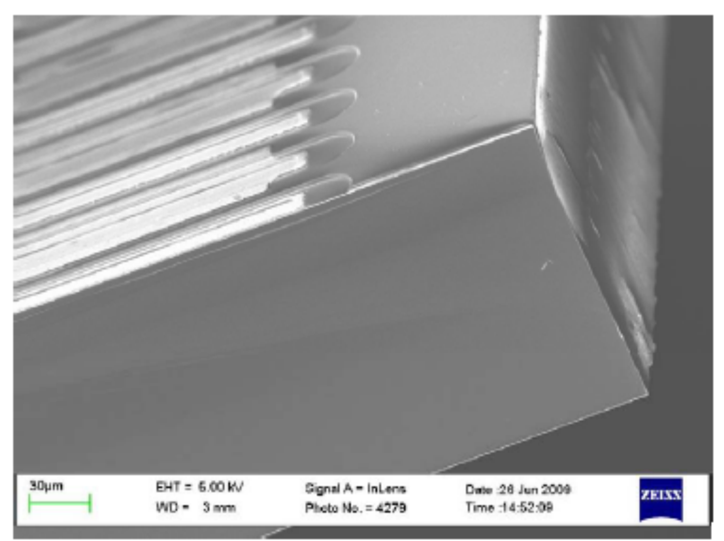
N clusters	Fraction of chips
0	46%
≤1	71%
≤2	85%
≤3	91%
≤4	95%
≤5	97%



Save on material budget by lowering density of GBTs/DC-DC converters at high |Z|?

Large Area Arrays

- 200 m^2 of silicon in present CMS tracker
  - 10cm x 10cm sensors (2) in outer barrel modules
- IC dies are limited to 2x2 cm^2
- Die-to-wafer bonding
  - Use 10x10 cm^2 sensor
  - Select good dies bond die to wafer
  - Cost and yield are an issue
- Wafer-to-wafer bonding
  - Dice and select after bonding
  - Edges/dead space are an issue

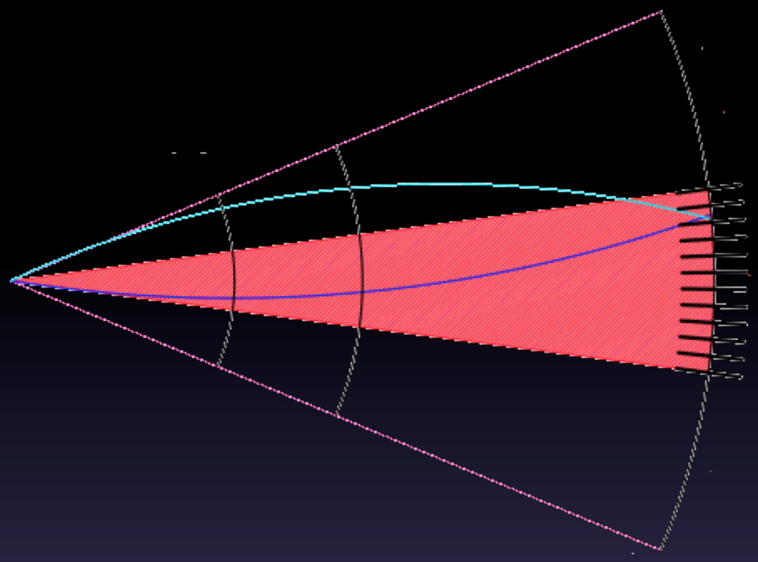


VTT photo

- Edgeless sensors
  - Process exists
  - Edge implantation while on carrier wafer
  - Inactive region < 1µm

Trigger Considerations

- 15° sectors
- 3 layers
  - Must for layer inefficiencies!
- pT min ≈2.5 GeV
- Need to include adjacent sectors to get all tracks



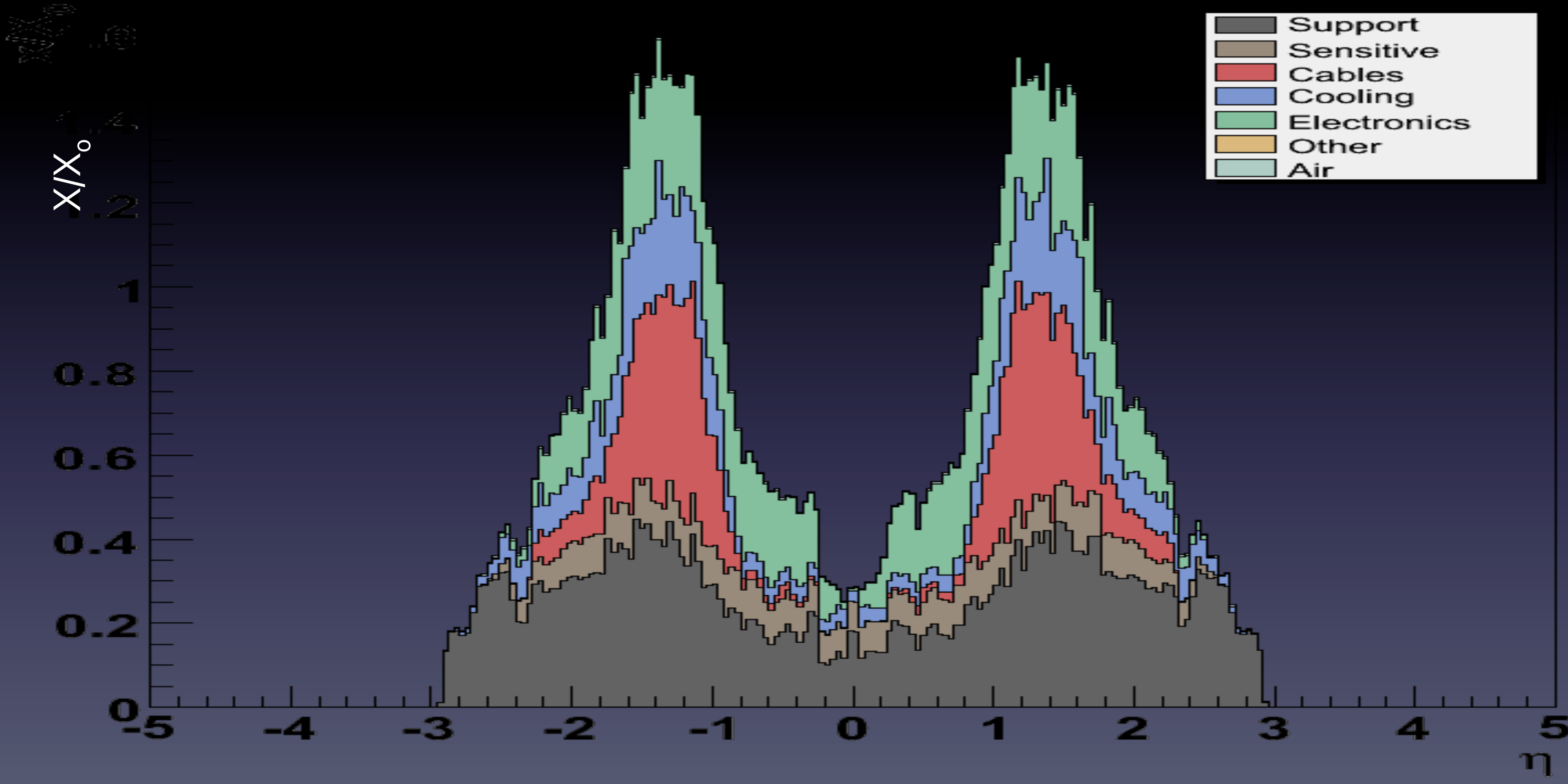
Conceptual development work underway at based on in group experience with Do FPGA trigger processor system.

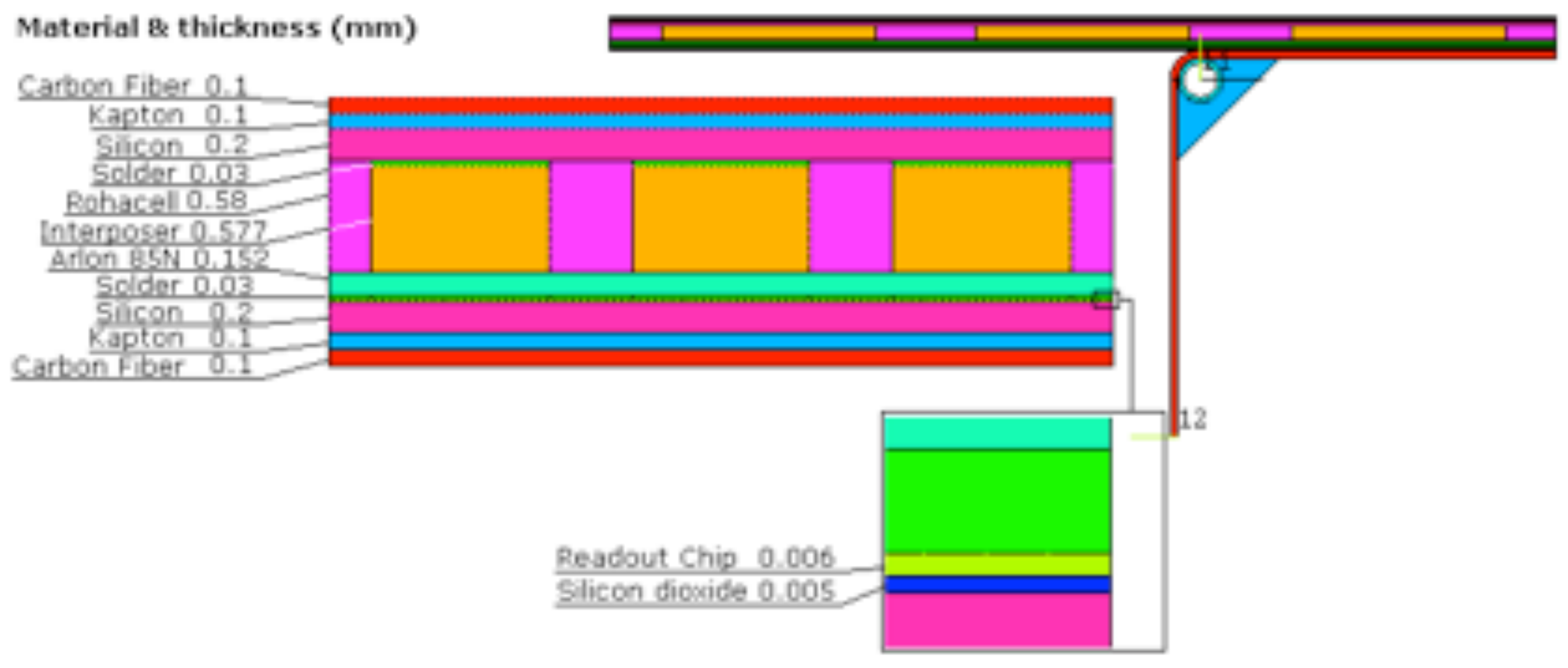
Summary

- R&D effort proceeding on many fronts for an L1 tracker trigger
  - 3D chip development
  - Interposer design and bump bonding studies
  - Mechanical design
  - Chip-to-chip data flow and off-detector processing
  - Large array considerations
  - Simulations, material budget estimates
- Still many challenges
  - Electronic design
  - Chip-sensor bonding
  - Interposer
  - Large area array production yield
- Many thanks to W. Cooper, U. Heintz M. Johnson, R. Lipton, M. Tripathi, M. Woods, Z. Ye

Backup

CMS Material Budget




Material & thickness (mm)
Carbon Fiber 0.1
Kapton 0.1
Silicon 0.2
Solder 0.03
Rohacell 0.58
Interposer 0.577
Arlon 85N 0.152
Solder 0.03
Silicon 0.2
Kapton 0.1
Carbon Fiber 0.1
12
Readout Chip 0.006
Silicon dioxide 0.005