Continuous Acquisition Pixel 12: Hexagonal Pixels

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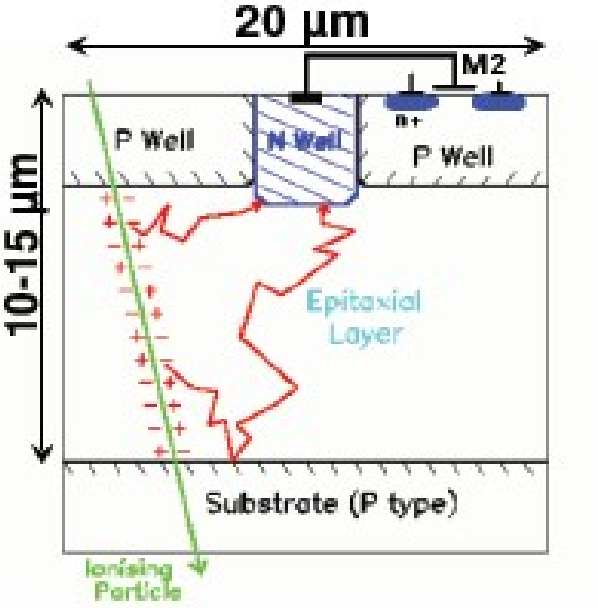
Motivation

- Initial Belle II vertex detector will need to be upgraded to handle full design luminosity of upgraded Belle II
- Researching an upgraded pixel detector for Belle II
  - Handle high luminosity

Introduction

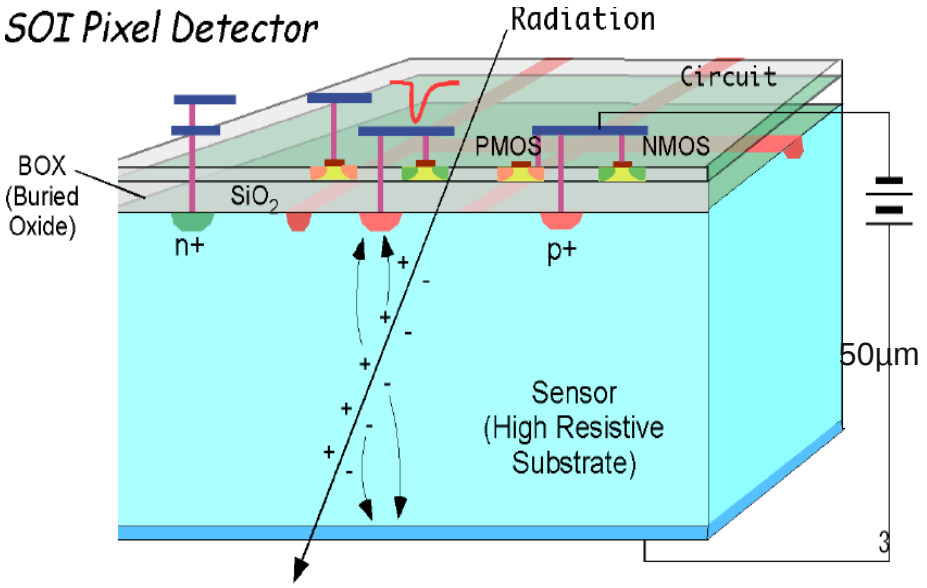
- Pixel R&D in Hawaii for ~7 years
- Three phases:
  - Dr. G. Varner:
    - CAP1, CAP2, CAP3
  - Dr. E. Martin:
    - CAP4, CAP5
  - M. Cooney:
    - CAP6, CAP7, CAP9, CAP11
      CAP12



Charge collection mechanism in bulk CMOS process

Process: Silicon on Insulator

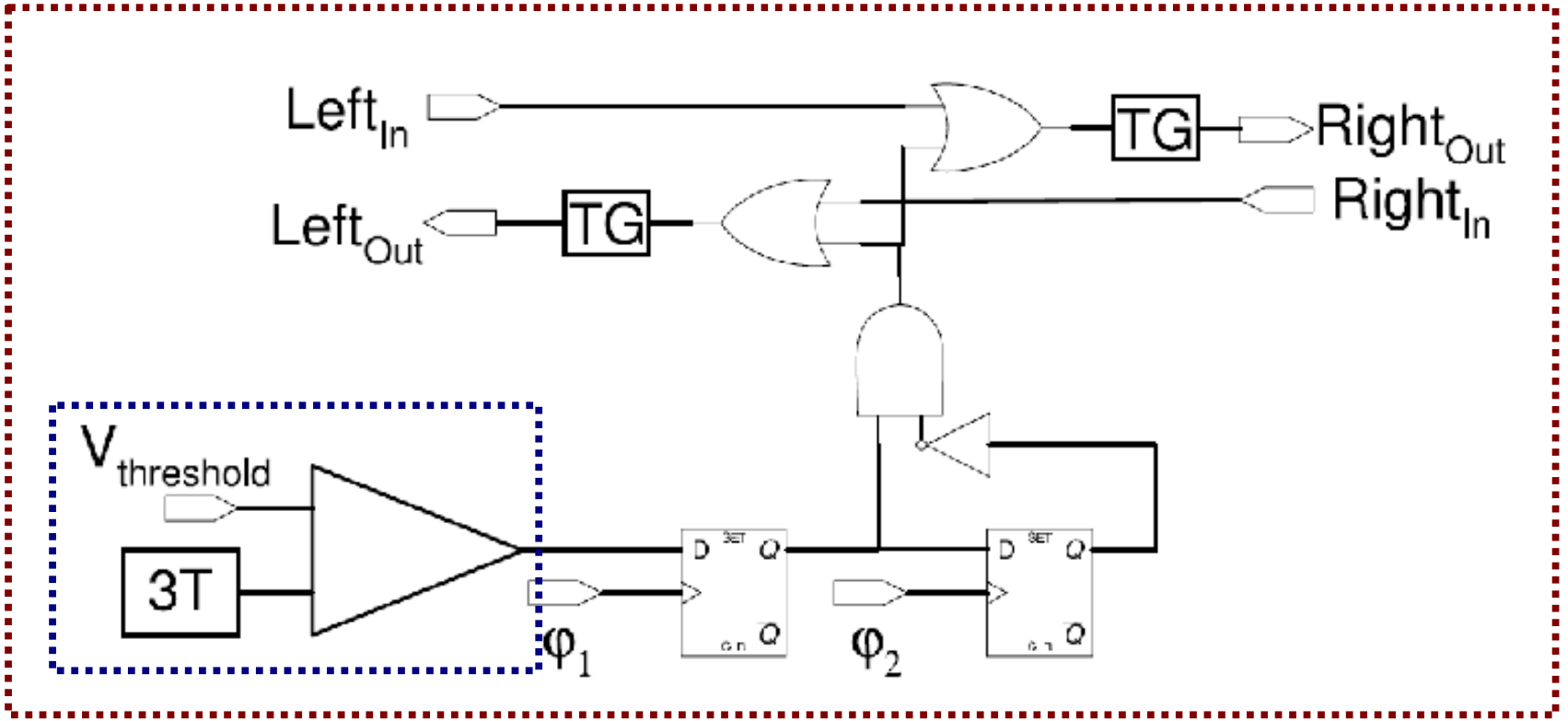
- ROHM Semiconductor
  - 0.2µm
- Designs include:
  - CAP5, CAP7, CAP9, CAP11, CAP12
  - Process actively researched
  - Designed for detectors by ROHM/OKI Semiconductor
  - Continued development with collaborators:
    - KEK, ROHM/OKI, FNAL, LBNL, UH



Charge collection mechanism in SOI process.

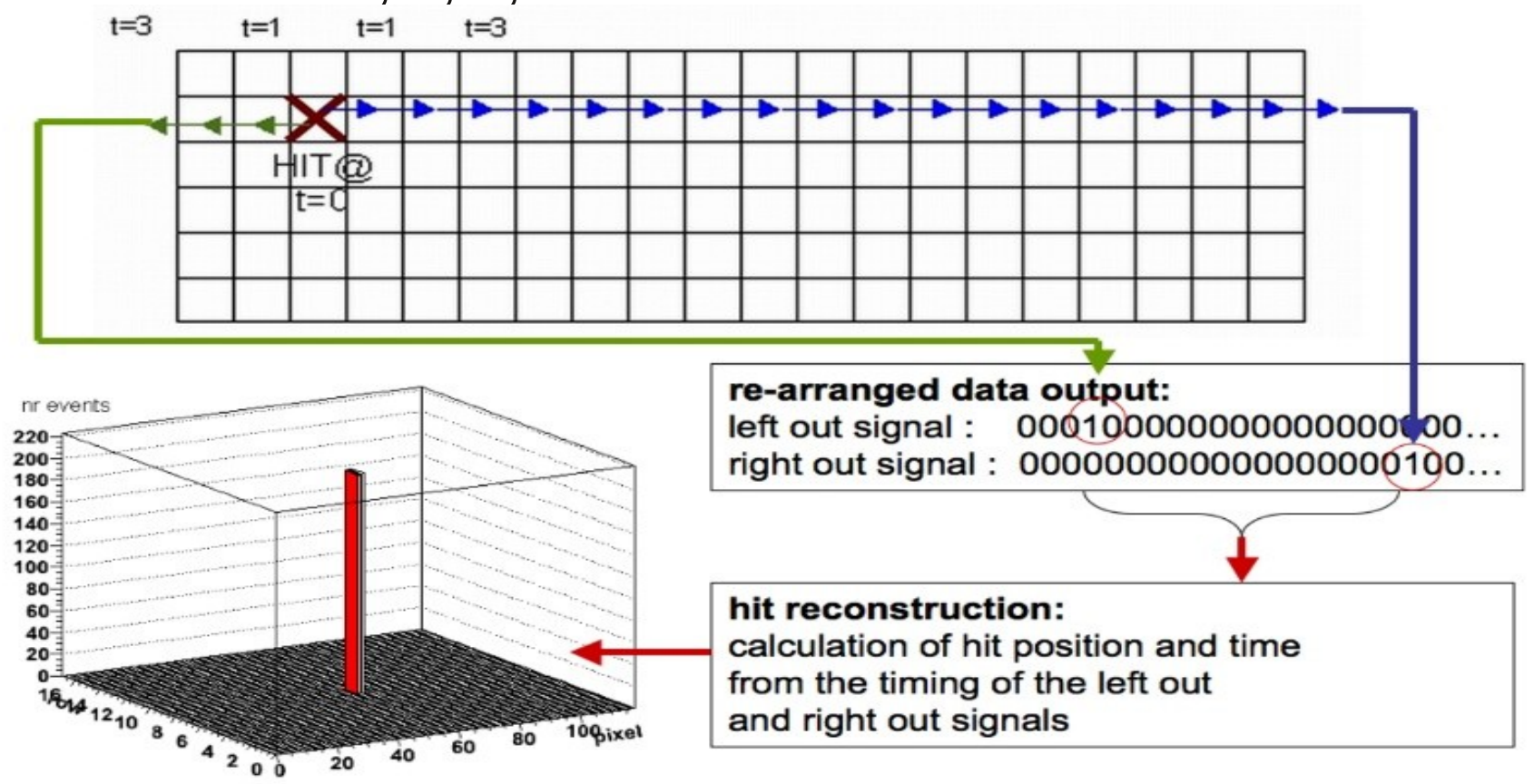
Readout Type: Binary Shifting

- Binary shifting logic all in pixel
- Hexagonal shifting logic is at periphery



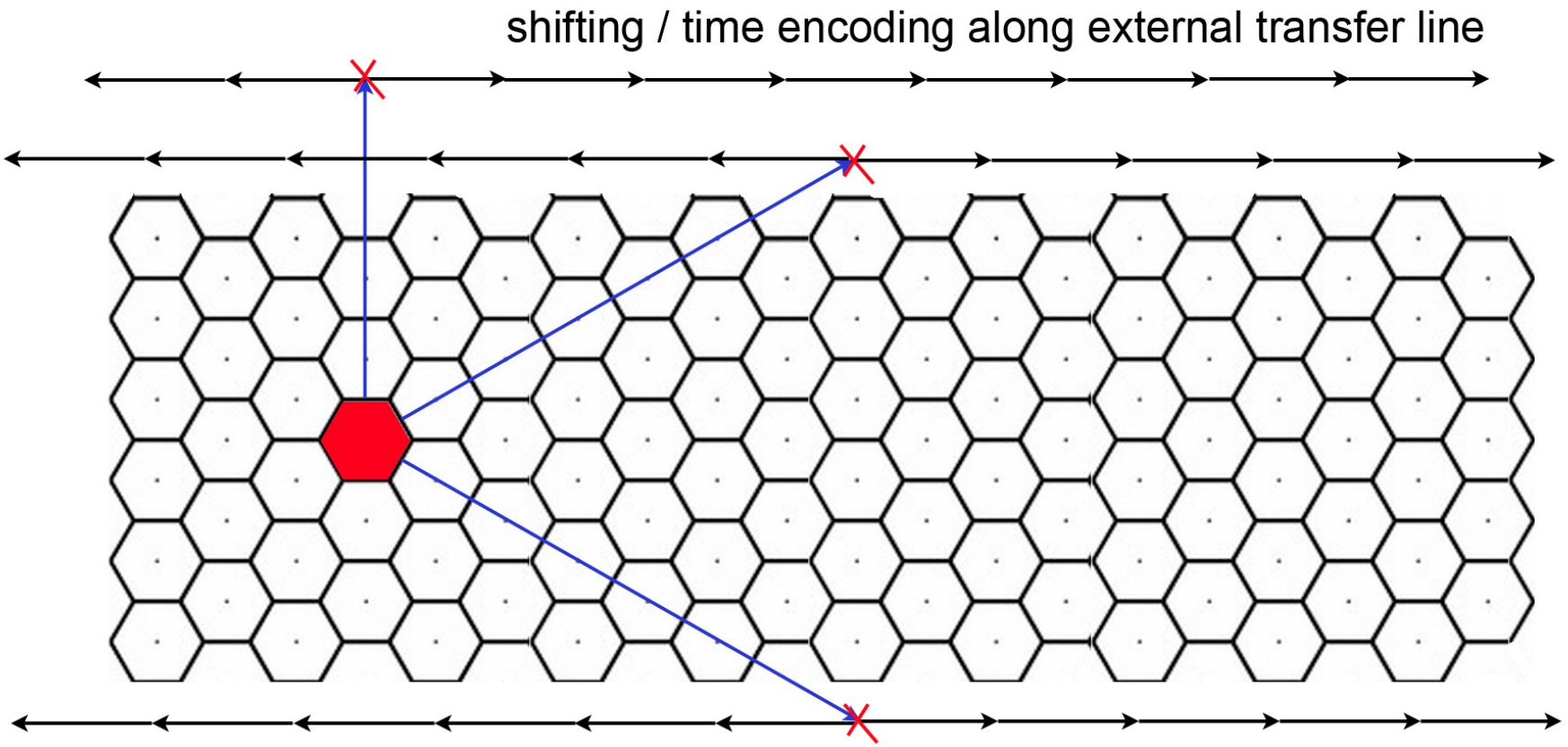
Readout Type: Binary Shifting

- Space-time hit correlation
  - Used in CAP4, 5, 7, 11



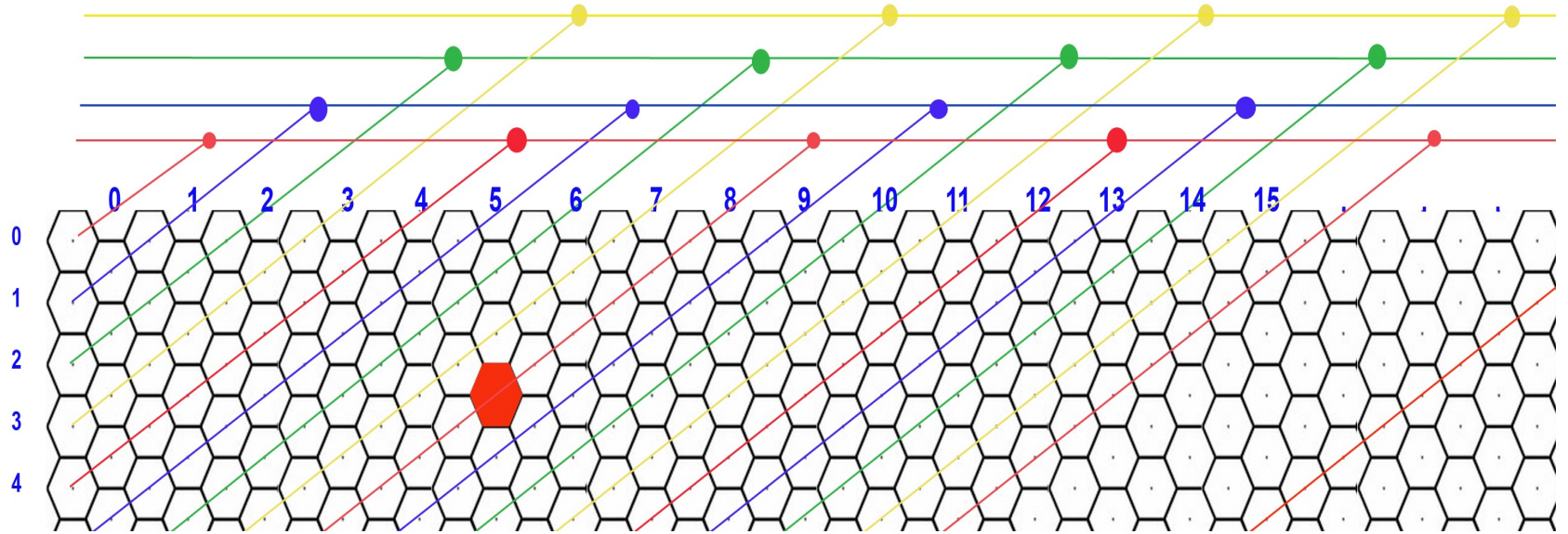
Readout Type: Hexagonal

- Three outputs per pixel



Readout Type: Hexagonal

- Each pixel outputs binary signal in three directions to periphery (CAP9)
- Multiple rows of shifting logic (TLM)
  - More transfer lines = higher readout speed



Readout Type: Hexagonal

Lower occupancy

- 1.6e-2 (Analog) vs 5.2e-5 (TLM=12)

Fewer channels (compared to 2 bit binary)

- 72 channels for 230,000 pixels (TLM=12)

High speed readout

- 100MHz readout vs. ~50MHz analog

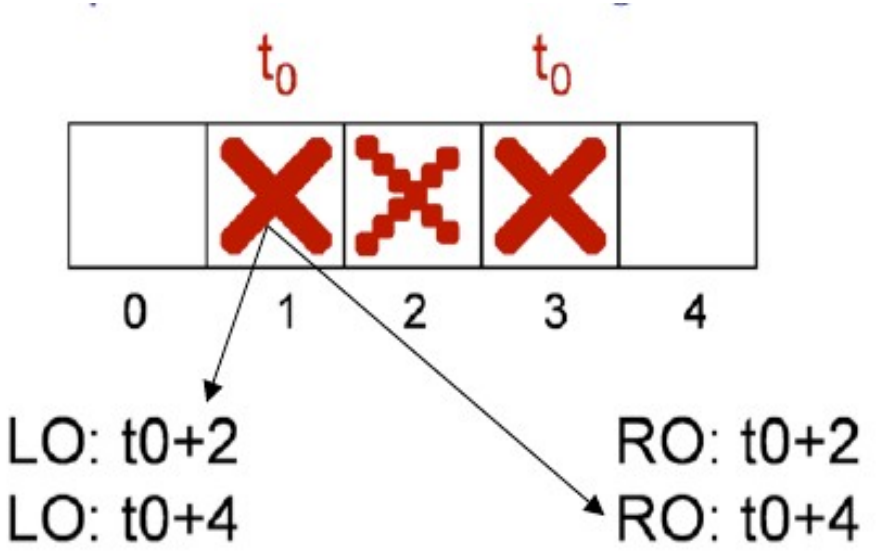
Fewer ghost hits reconstructed

- 4-50x less than 2bit binary shifting readout

Ghost Hits

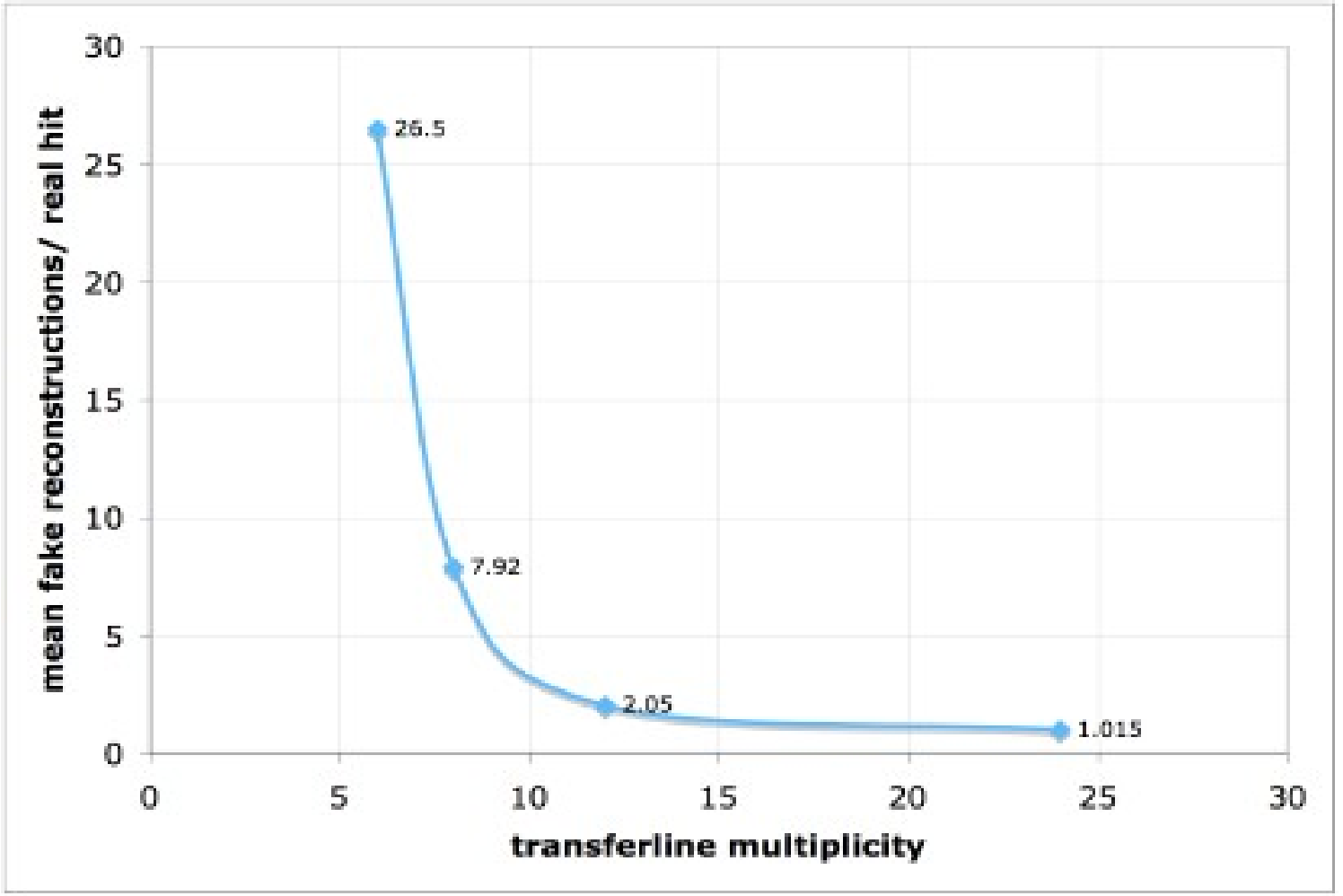
If multiple hits occur, left going signals from one pixel get paired with right going signal from another pixel

If triggering is included, many ghost hits can be eliminated by pairing up the hit signals



for example: wrong pairing of signals from two simultaneous hits leads to reconstruction of two fakes however not at t0, so they can be rejected by trigger

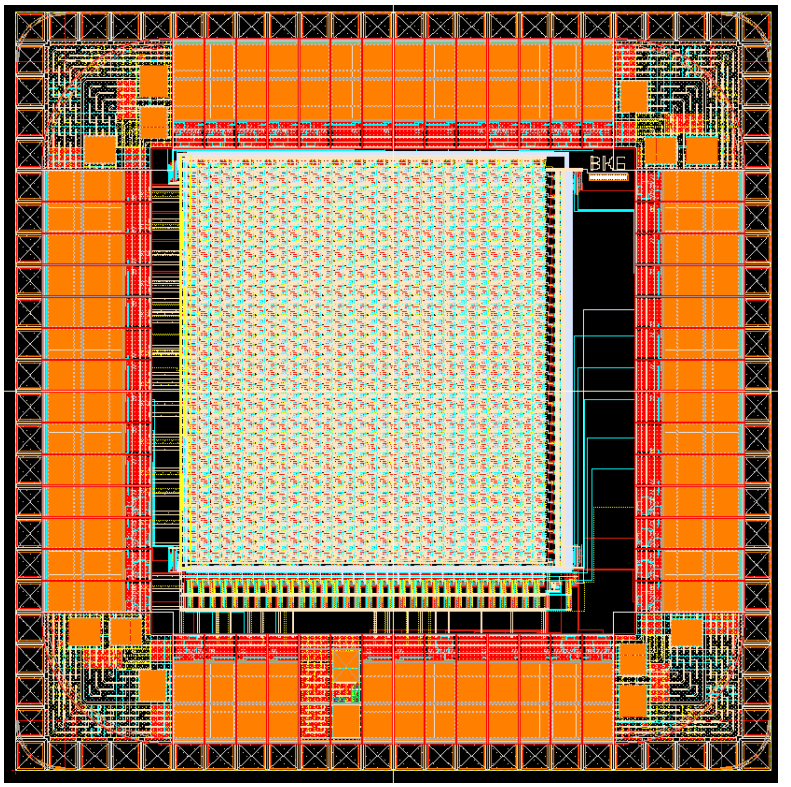
TLM Effectiveness



detector	matrix	pitch	shift clock	outputs	(effective) occupancy
binary	800x240	25 µm square	2 MHz (internal lines)	480	0.124
binary	800x240	25 µm square	10 MHz (internal lines)	480	0.005
binary hexagonal TM = 8	960x240	25 µm hexagonal	100 MHz (external lines)	48	2.2E-04
binary hexagonal TM = 12	960x240	25 µm hexagonal	100 MHz (external lines)	72	5.2E-05
binary hexagonal TM =24	960x240	25 µm hexagonal	100 MHz (external lines)	144	2.7E-05
analog rolling shutter	420x120	50 µm square	9 µs integration time	120	0.016

CAP12: Overview

- Hixel Readout
- 2.4mm x 2.4mm
  - 1296 pixels
- Simulated 500ns integration time
  - 500MHz+ periphery logic operation



Top level layout view of CAP12.

CAP12: Design Goals

- Attempted to fix previous issues with CAP11:
  - Voltage drop across comparator threshold:
    - CAP11: ~125mV across chip
      - Comparators turn on at different voltages
    - Solution: Independent DAC for each column.
  - Backside depletion only worked up to 17V
    - Changed 3T layout, added protection structures
  - Attempted to improve leakage currents
    - 10x - 100x less leakage each submission
      - Learning layout techniques + process manufacturing improvements

CAP12: Pixel Cell

- 1296 pixels
  - 33µm (W) x 31.38µm (H)
- Output is active low (wire OR, entire bus line)

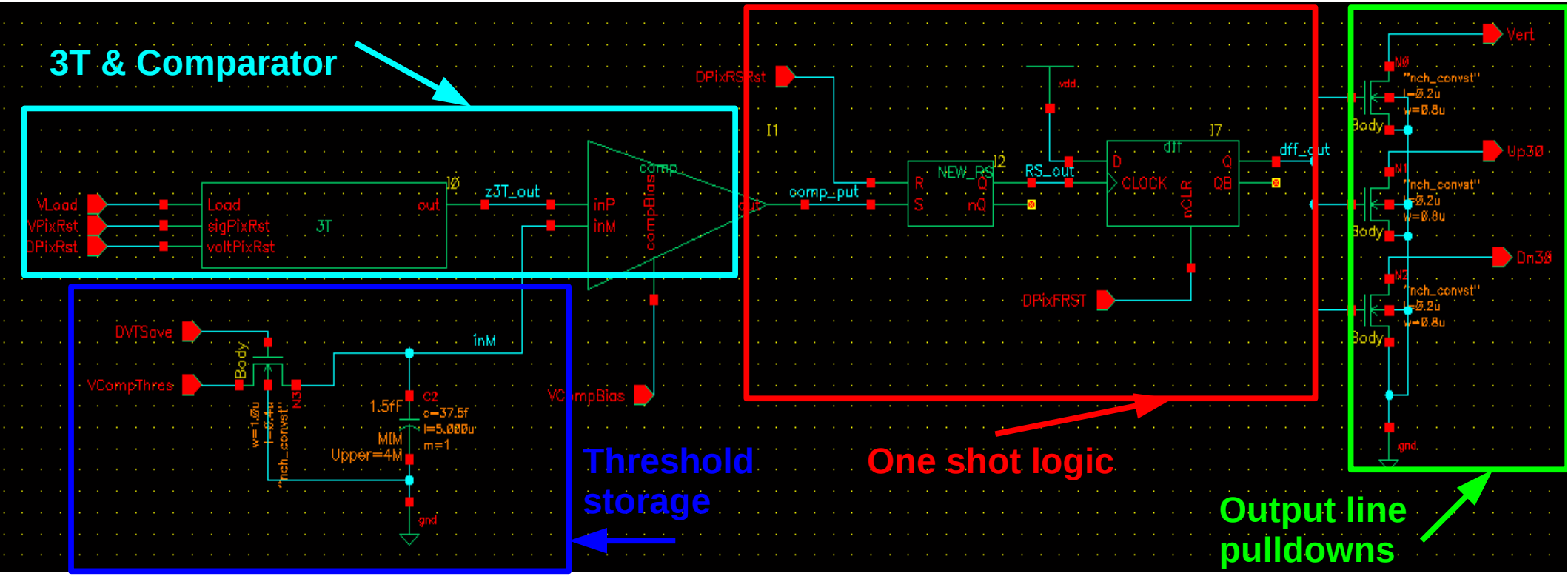
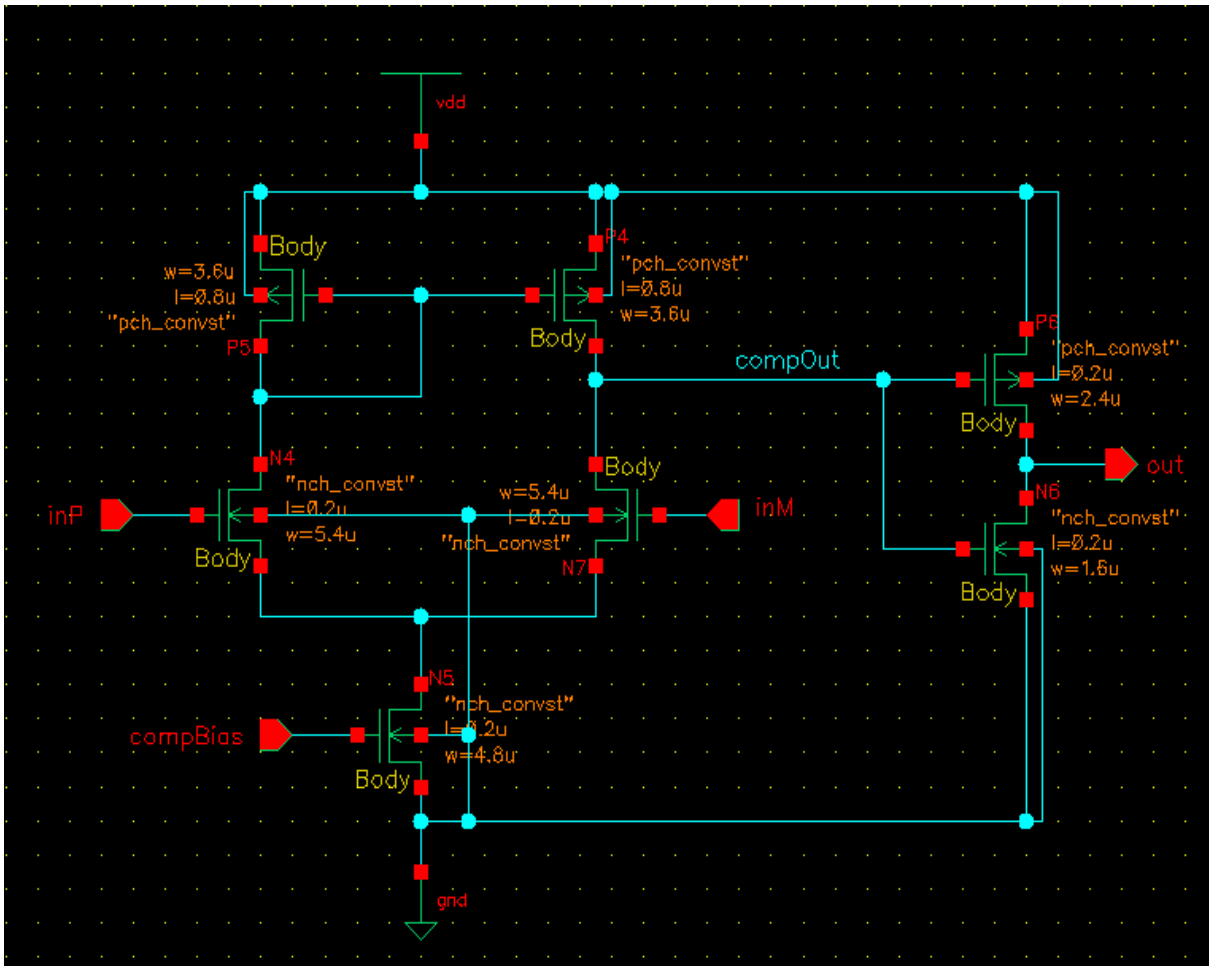


Image 13: New biasing circuitry, each column has individually adjustable DAC storage capacitor (blue box).

CAP12: Comparator

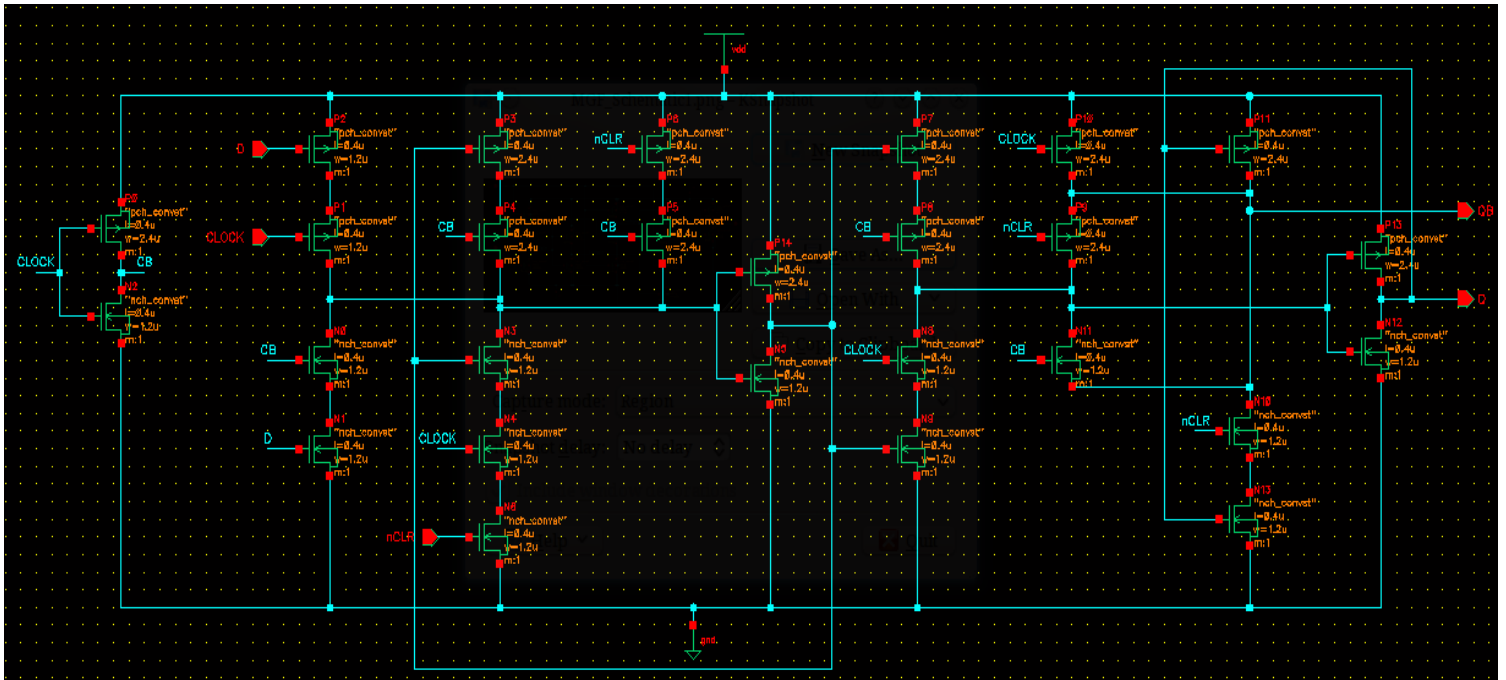
- Differential Pair
- Detect MIP
  - Minimum Ionizing Particle
- Transition time
  - ~10ns
- Less power use:
  - 13.796µW / cell



Differential pair comparator used in the CAP12.

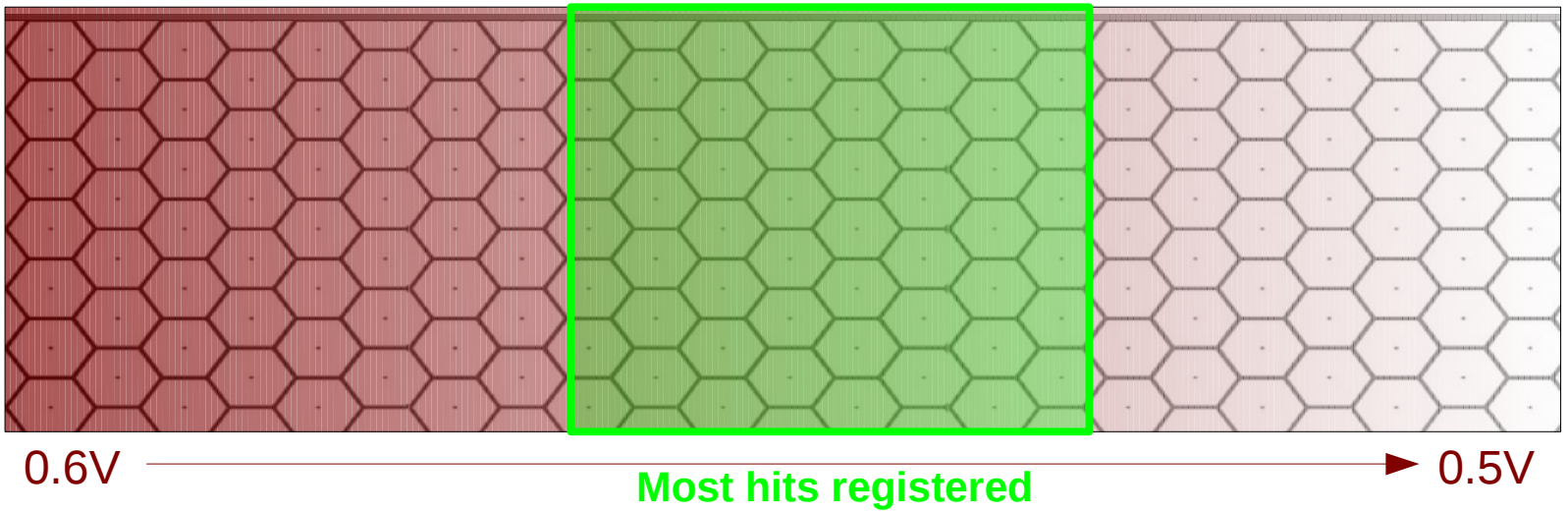
CAP12: DFF

- Smaller DFF
  - 26µm (W) x 14µm (H)
- Dominate periphery logic and power consumption
- Slightly faster, less power
  - >500MHz operation, 36.22µW



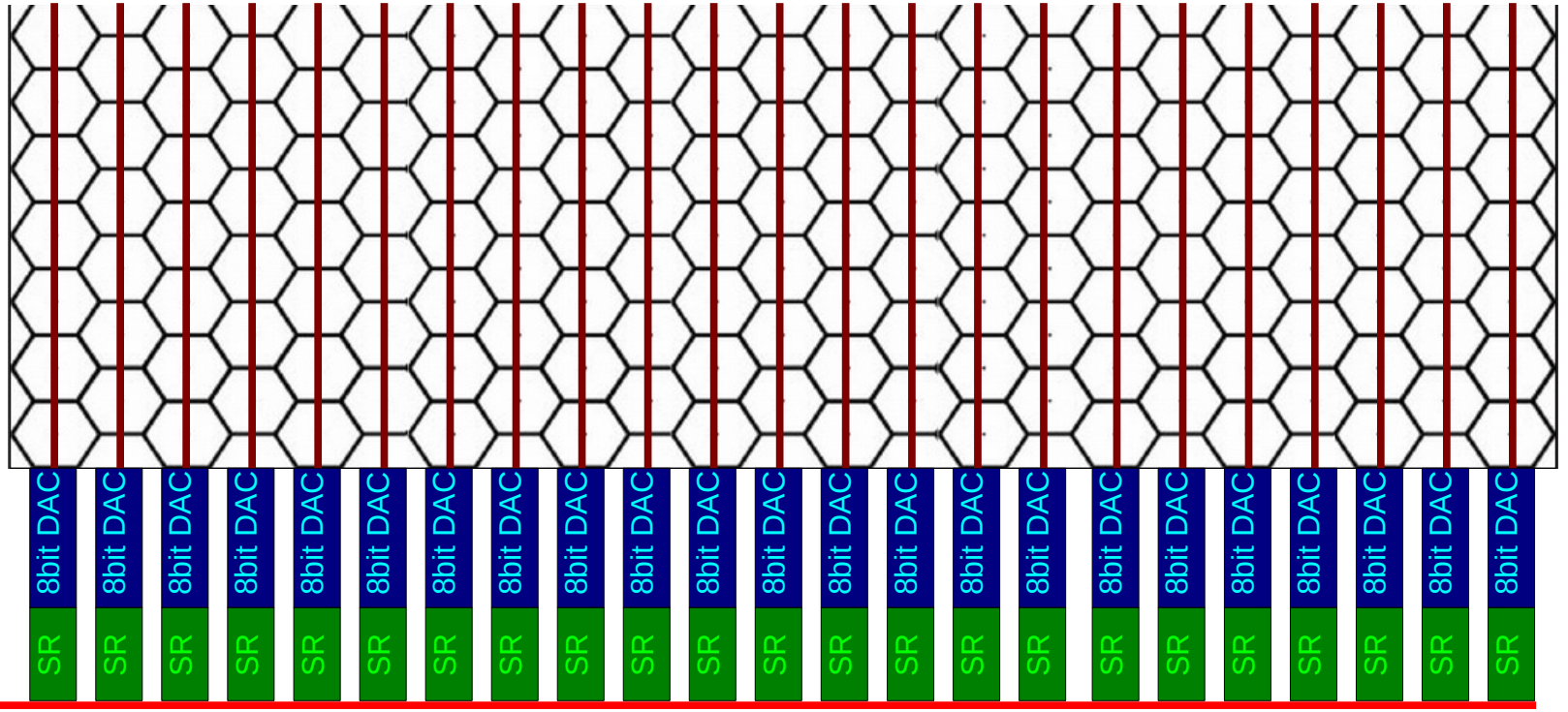
CAP12: Threshold Adjustments

- Previous designs showed threshold shifts across the array
  - Comparators transitioned at slightly different bias values. Require stability ~10mV.
  - Layout issues, manufacturing variability.



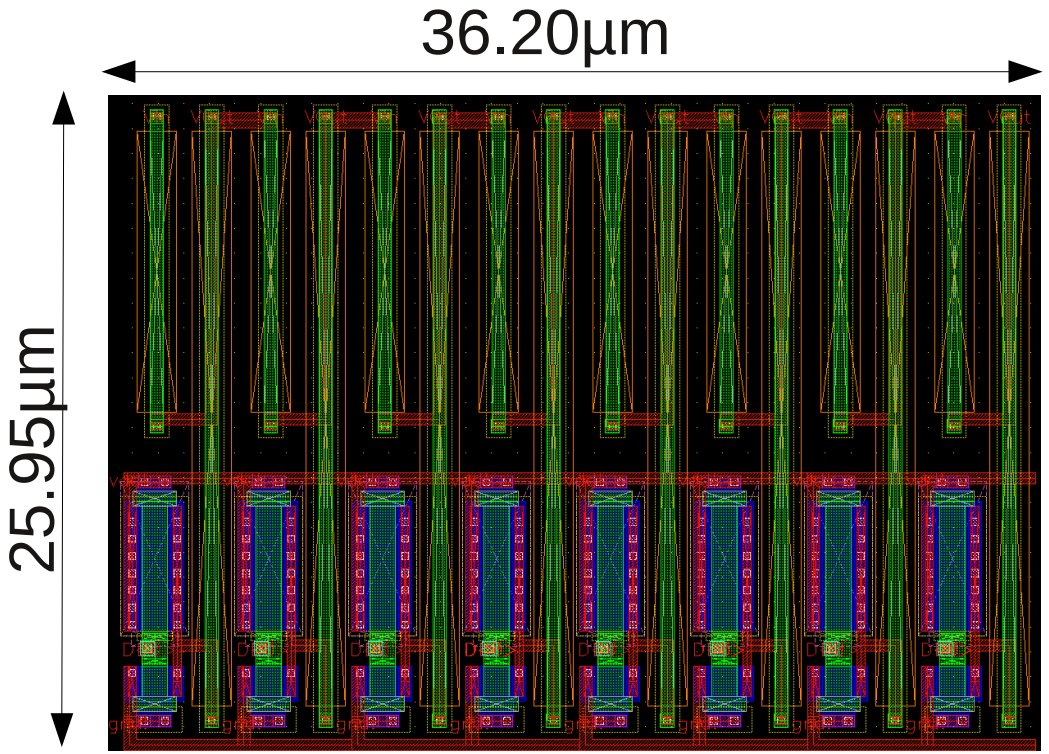
Individual DACs

- Each column has independent 8bit DAC
  - Only need to update ~1ms
  - Programmed via shift register



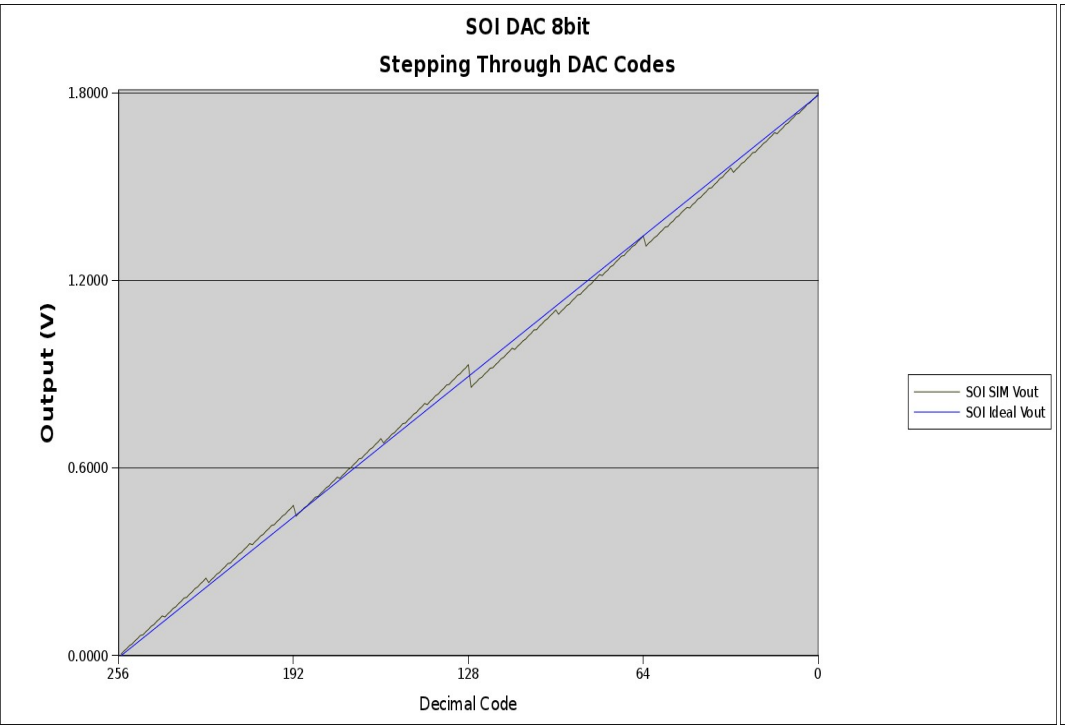
SOI DAC

- 8bit DAC used to control bias
- Simulated using process resistors
- Determines the width of each column
  - Must be compact

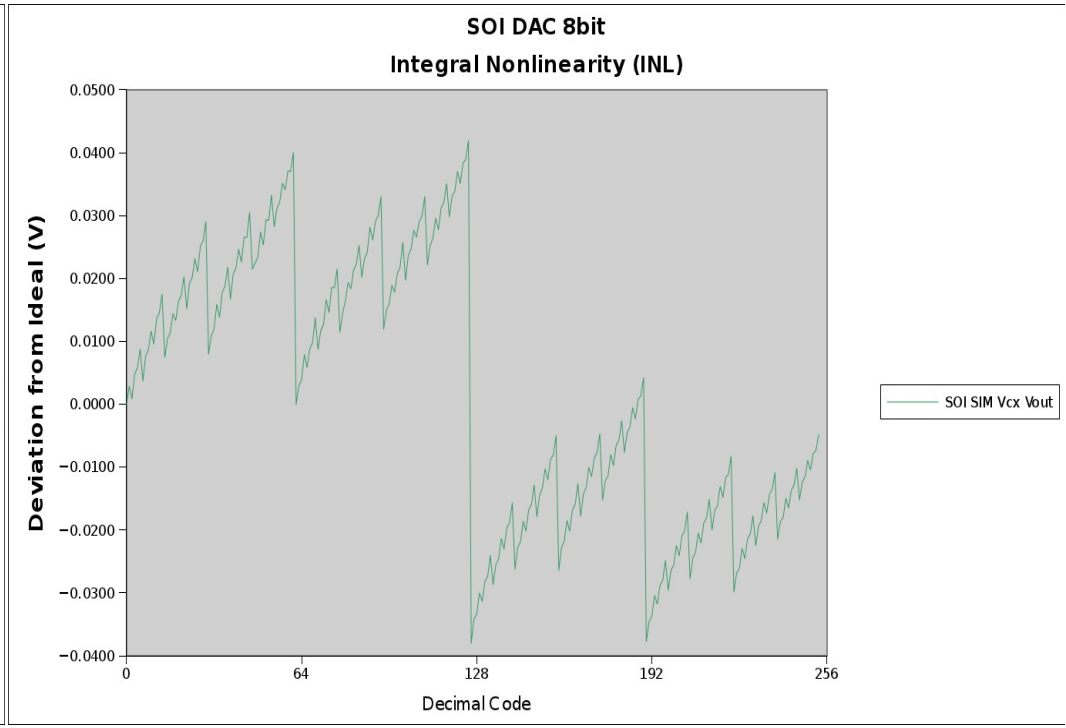


Layout view of a 8bit DAC in a 0.20µm SOI process.

SOI DAC: Performance



Stepping through DAC code to measure output voltage.



Integral nonlinearity of the 8bit DAC. LSB = 0.007V

- Not great linearity in simulation but will work over narrow range of values
- Other ASICs have shown better practical results compared to simulations

Conclusion

- Incremental improvements to the Hixel design
  - Better layout for improved backside biasing
  - Lower power consumption
  - Better isolation of periphery shift logic from main pixel array
  - Rewritten reconstruction software
  - Compatible with previous evaluation boards
- Expected back July 2011