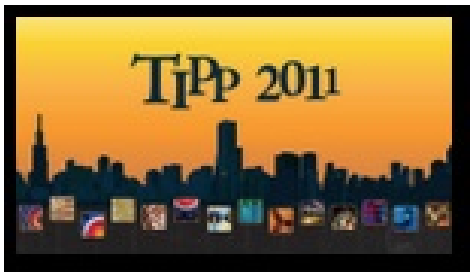

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Readout Electronics for the ATLAS LAr Calorimeter at HL-LHC

Friday, 10 June 2011 16:00 (30 minutes)

The ATLAS experiment is one of the two general-purpose detector designed to study proton-proton collisions (14 TeV in the center of mass) produced at the Large Hadron Collider (LHC) and to explore the full physics potential of the LHC machine at CERN. The ATLAS Liquid Argon (LAr) calorimeters are high precision, high sensitivity and high granularity detectors designed to provide precision measurements of electrons, photons, jets and missing transverse energy. ATLAS (and its LAr Calorimeters) has been operating and collecting p-p collisions at LHC since 2009.
The on-detector electronics (front-end) part of the current readout electronics of the calorimeters measures the ionization current signals by means of preamplifiers, shapers and digitizers and then transfers the data to the off-detector electronics (back-end) for further elaboration, via optical links. Only the data selected by the level-1 calorimeter trigger system are transferred, achieving a bandwidth reduction to 1.6 Gbps. The analog trigger sum signals are formed on the front-end electronics boards and sent, via copper cables, to the receiver part of the trigger system.
The number of channels in the LAr readout is ˜200K. The front-end electronics is composed by 58 electronics crates, housing 1524 signal processing boards (FEBs) plus 300 other electronics boards. Each crate is powered by a radiation tolerant power supply. There are ˜ 1600 optical links between the front- end and the back-end system. The back-end electronics consists of 16 crates, 192 Read Out Drivers (ROD). Each ROD receives data from up to 8 FEBs and calculates the energy deposited and the time of the deposition using an optimum filtering algorithm.

The current front-end electronics need to be upgraded to sustain the higher radiation levels and data rates expected at the upgraded LHC machine (HL-LHC), which will have 5 times more luminosity than the LHCin its ultimate configuration. The complexity of the present electronics and the obsolescence of some of components of which it is made, will not allow a partial replacement of the system. A completely new readout architecture scheme is under study and many components are being developed in various R&D programs of the LAr collaboration group.
The new front-end readout will send data continuously at each bunch crossing through high speed radiation resistant optical links. The data (˜100 Gbps for each board) will be processed real-time with the possibility of implementing trigger algorithms for clusters and electron/photon identification at a higher granularity than that which is currently implemented. The new architecture simplifies the system design while keeping many options open, such as pipeline design, shaping, gain setting, etc. Moreover it will eliminate the intrinsic limitation presently existing on Level-1 trigger acceptance.

This talk will cover architectural design aspects of the new electronics as well as some detailed progress on the development of several ASICs needed, e.g. new ADCs and/or new optical links. Preliminary studies with FPGA's to cover the backend functions including part of the Level-1 trigger requirements will also be presented.

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