Upgrade Design of TileCal Front-end Readout Electronics and Radiation Hardness Studies

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1. Overview of Tile Calorimeter Front-end Readout System at LHC

2. Upgrade Design of TileCal Front-end Readout Electronics

3. Radiation Hardness Studies and Test Results

4. Summary

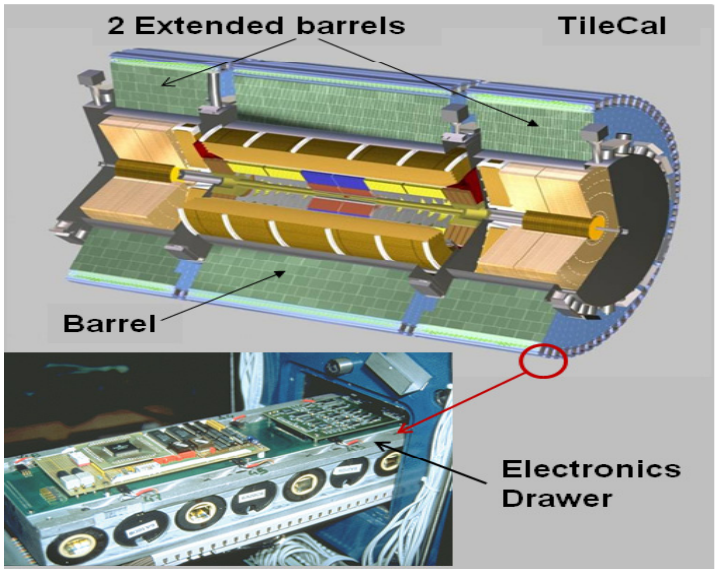
Overview of Tile Calorimeter Readout System at LHC

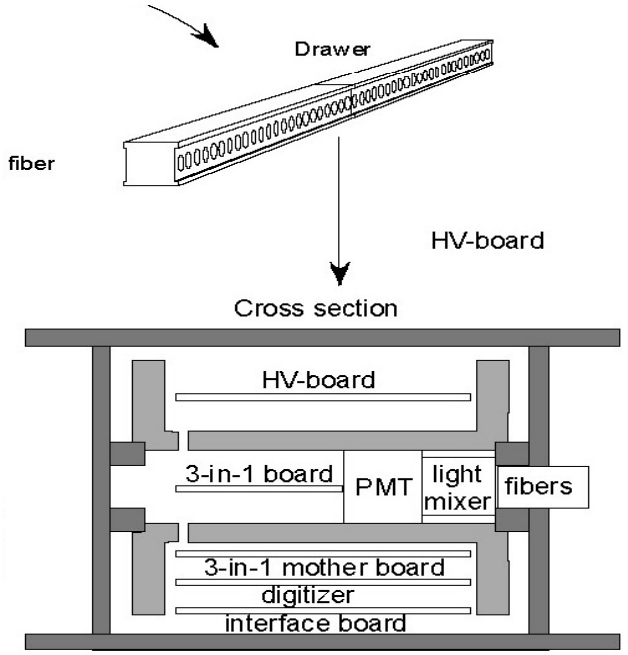
TileCal is to measure light produced by charged particles in plastic scintillators

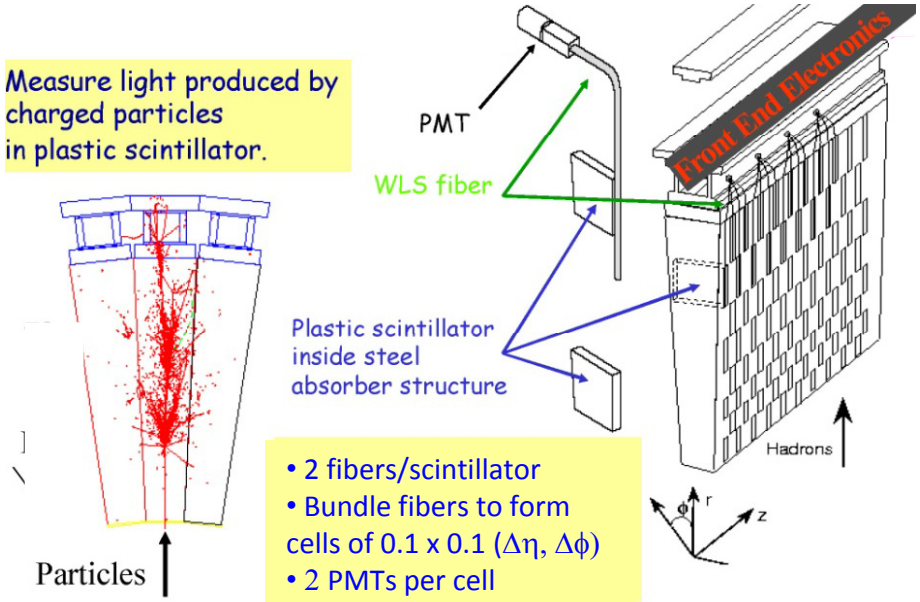
- Process ~10000 PMT signals
- 16-bit readout dynamic range (30MeV to 2Tev)
- Analog trigger
- Cesium calibration

Readout electronics housed in 256 drawers

- HV board
- Up to 45 PMT Blocks with 3-in-1 card
- 3-in-1 Motherboards
- Digitizer boards and interface board
- LVPS

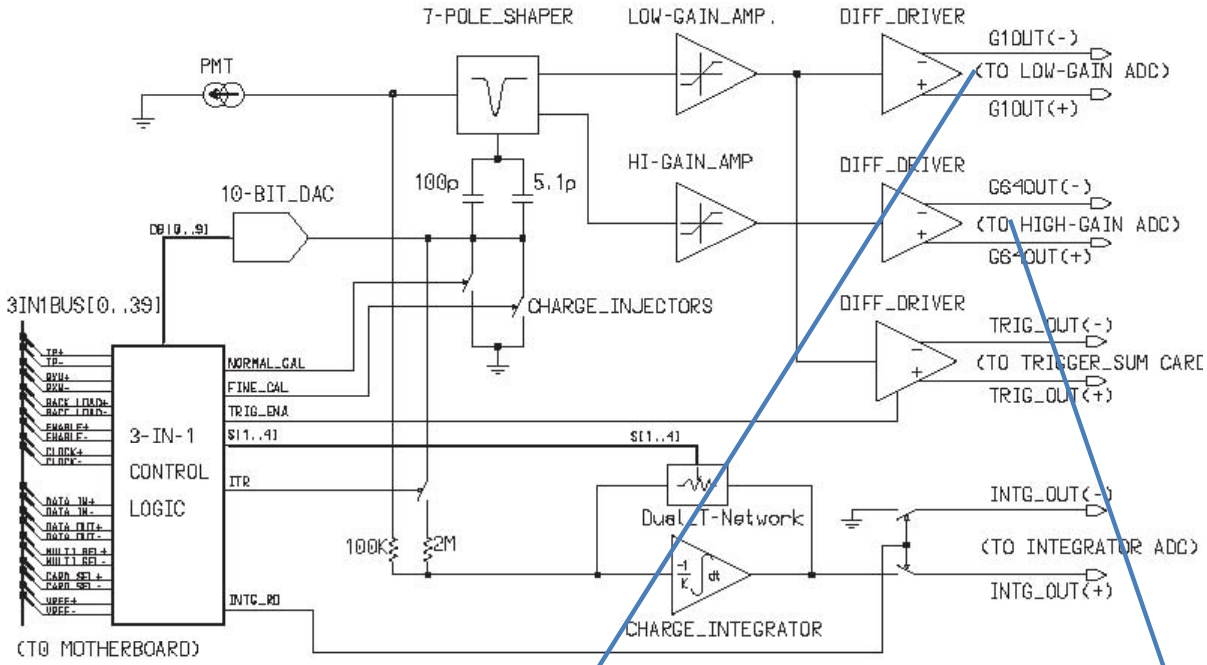


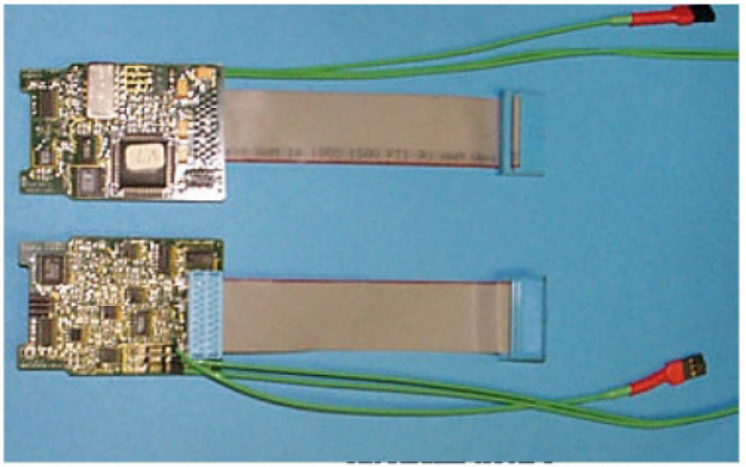


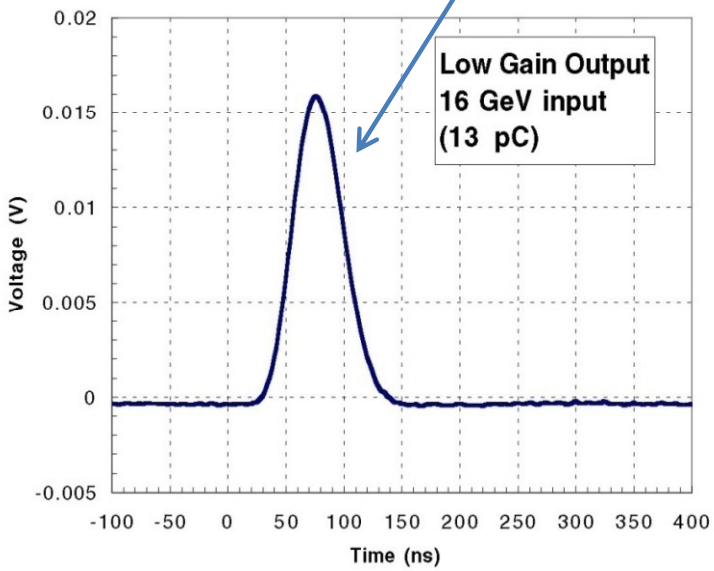


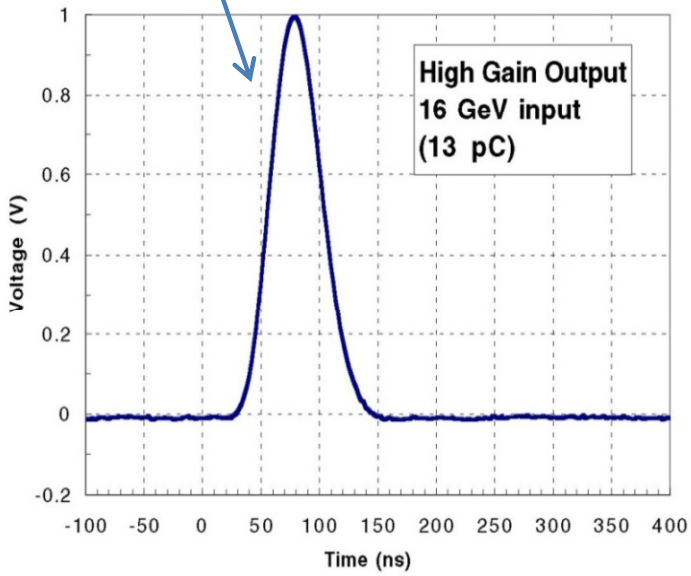
Current system has 3 layers of boards and many signals and power interconnects

TileCal Front-end Analog Electronics at LHC (3-IN-1 Card)



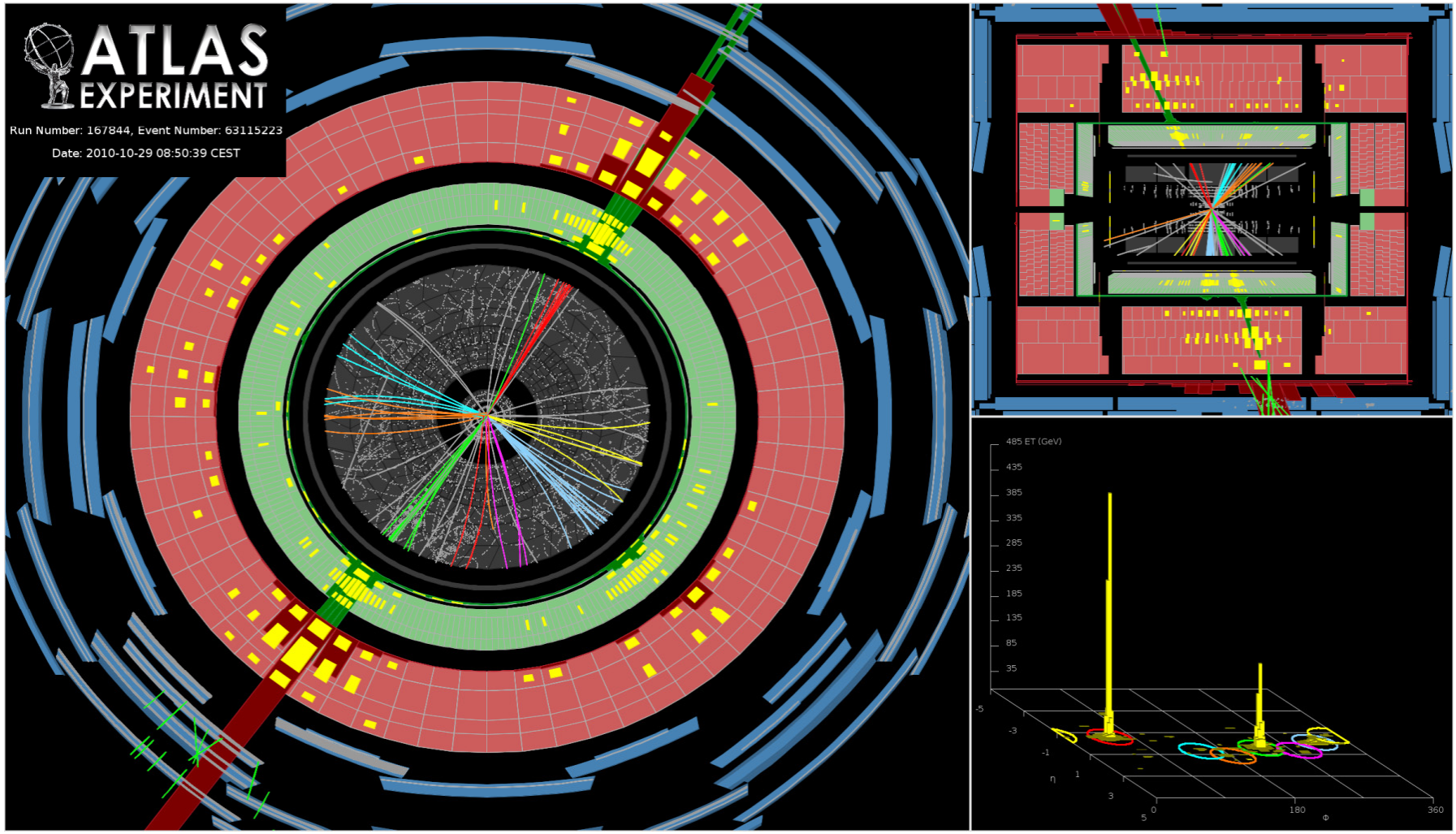






Performance of Current TileCal System at LHC

Event display of Run 167607, Event 63115223. This shows the highest-pT jet collected during 2010, which has pT of 1.5 TeV. The two leading jets are central high-pT jets with an invariant mass of 2.8 TeV. They have (pT, y) of (1.5 TeV, -0.58) and (1.0 TeV, 0.44), respectively. The missing ET in the event is 310 GeV. (ATLAS-CONF-2011-047, CERN, March 2011)



Motivation of Upgrade Design of Readout Electronics

- Lifetime of discontinued components is an issue
- Current system does not have adequate radiation tolerance for High Luminosity LHC
- Improve trigger
  - use full resolution of readout in digital trigger
- Improve reliability
  - single point failure immunity
- Improve resolution
  - 10bit to 12bit ADC
- Simplify powering issues
  - fewer voltages, local regulation
- Reduce control bus signals
- Reduce power consumption

Suggested TileCal Readout System Structure at HL-LHC

256 Electronics Drawers:

(1) 48 PMT Blocks with FE electronics and HV distribution electronics.

(2) 4 identical Main Boards and on-board electronics:

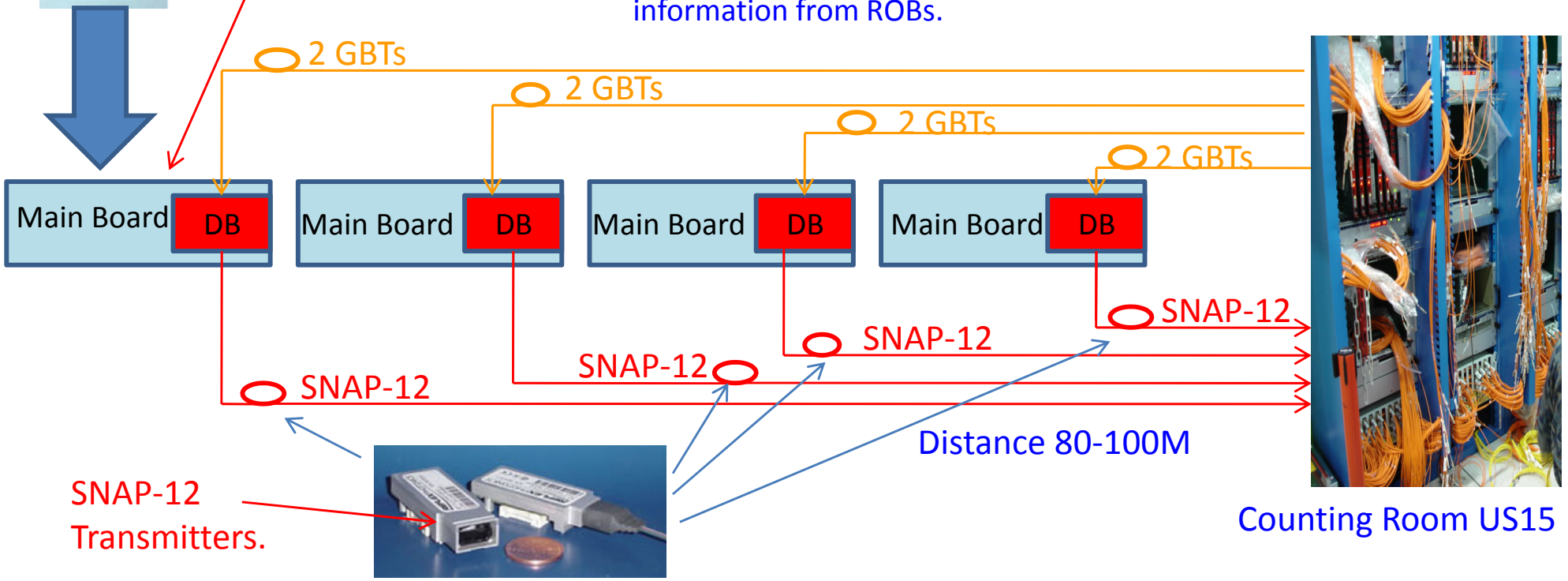
- 24-ch digitizers for low/high gain signals from 12 PMTs.
- Low-jitter 40MHz clock distributors for digitizers.
- Slow controls (calibration, Integrator gain settings, ADC input bias settings, status monitoring and house keeping etc.)
- LV regulators (DC/DC or linear regulators) Mother/Daughter Boards.

(3) 4 identical Daughter Cards and on-board electronics:

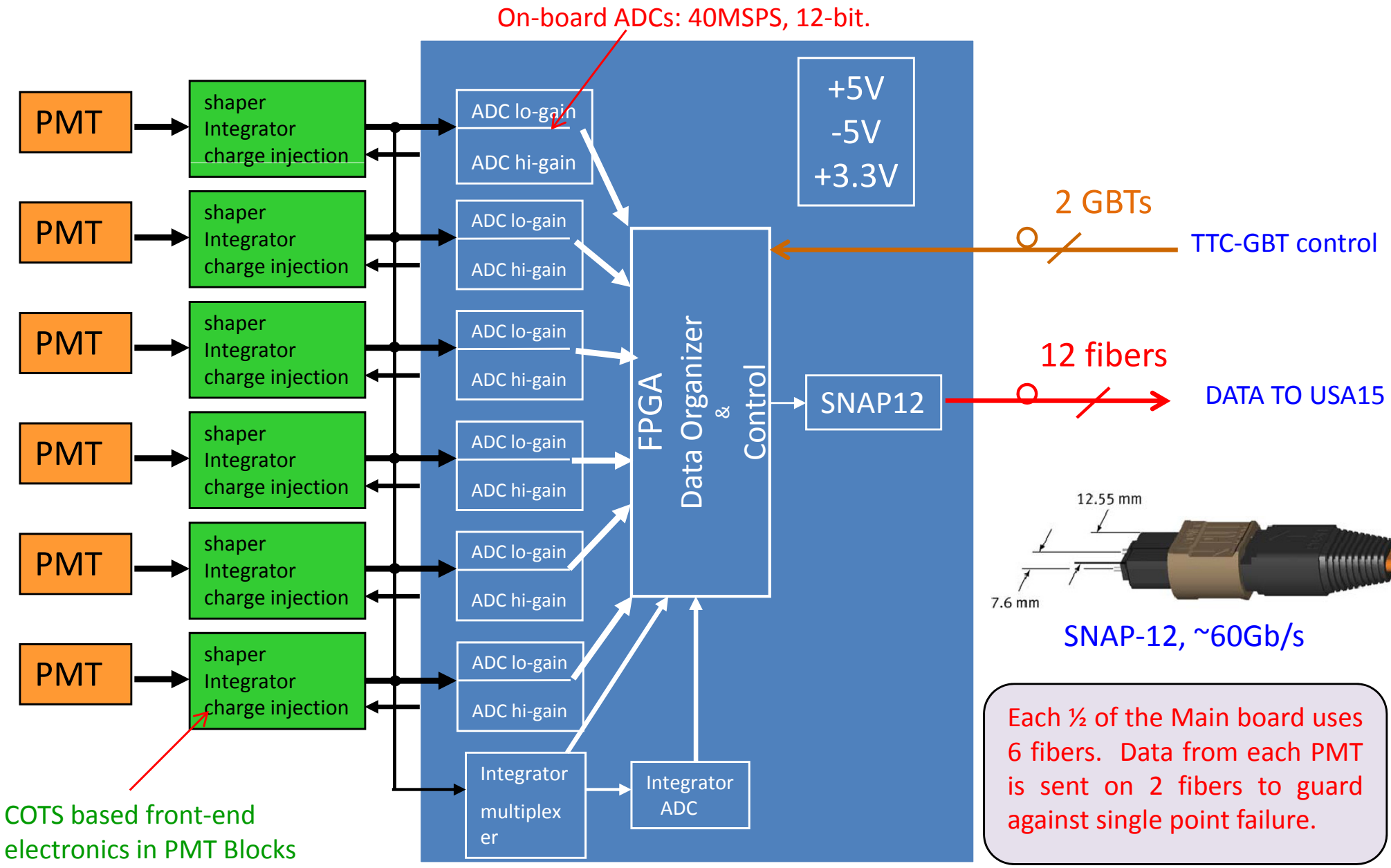
- 1 SNAP-12 module with 12 parallel optical fibers for transmitting data to ROBs
- 2 GBT links (in redundancy) for receiving timing, slow control information from ROBs.

Analog front-end card (3-in-1)

Each Main board handles 12 3-in-1 cards



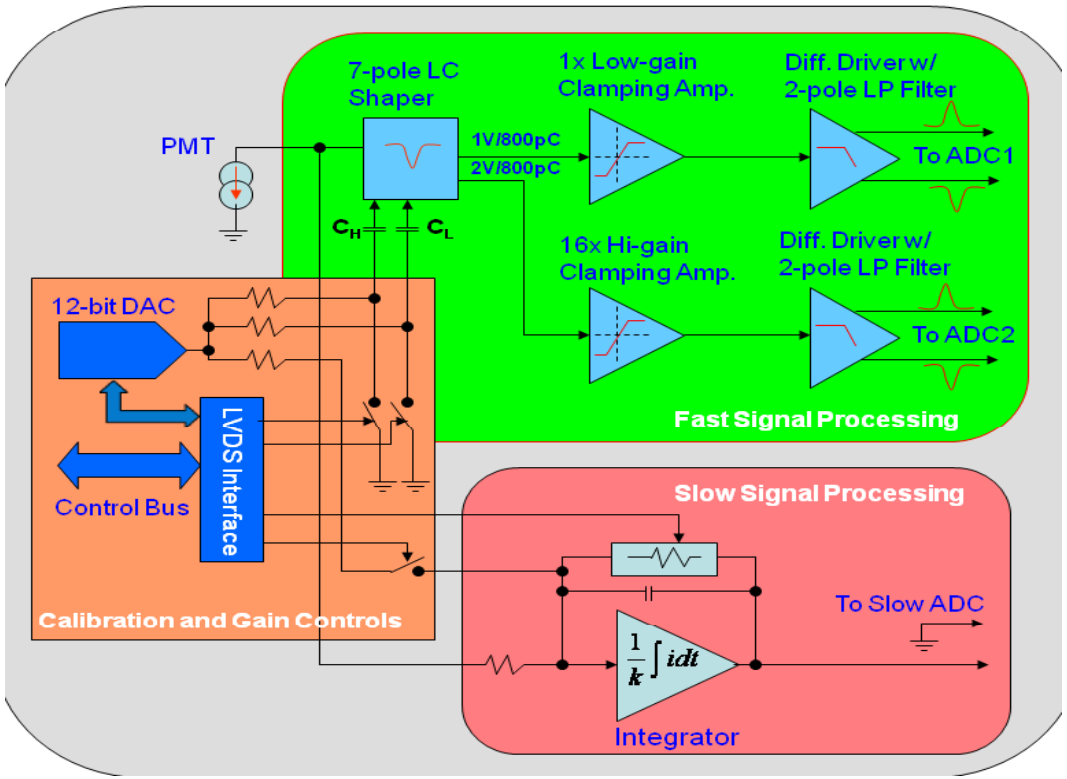
Main Board Readout Structure (1/2 Main Board)

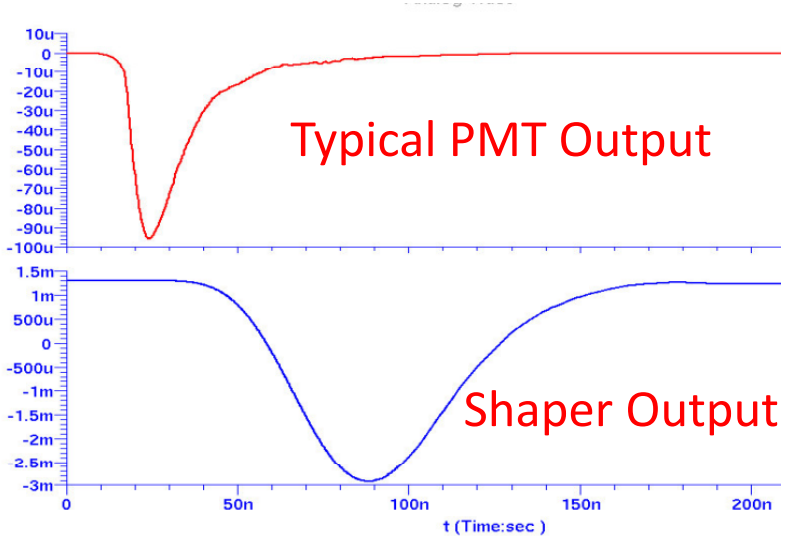


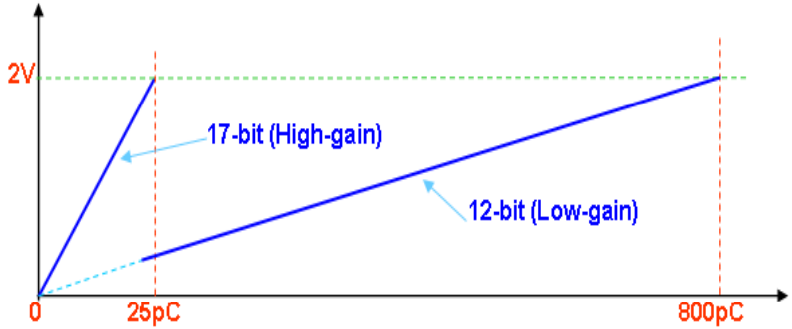
SNAP-12, ~60Gb/s

Each ½ of the Main board uses 6 fibers. Data from each PMT is sent on 2 fibers to guard against single point failure.

Newly Designed TileCal Analog Front-end Electronics at HL-LHC





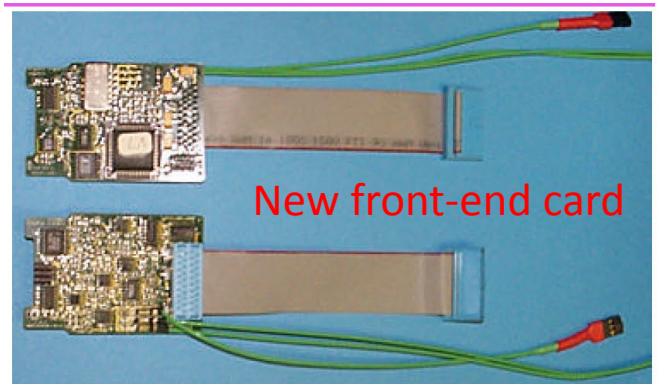


Bi-gain readout resolution

(1) Fast signal Processing
- 7-pole LC shaper and bi-gain readout
- Parallel digitization with 40MSPS 12-bit ADCs

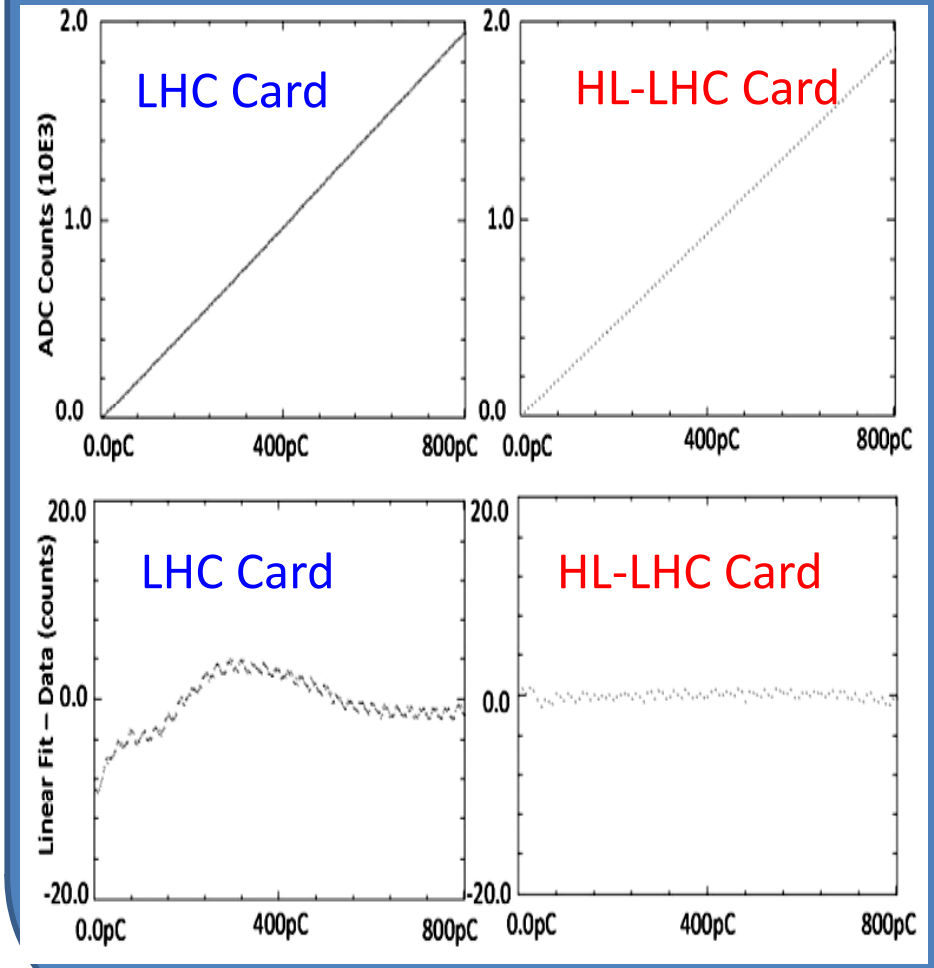
(2) Slow Signal processing
- 6 gain settings for Cs calibration and for monitoring of minimum bias current of proton-proton collisions

(3) Charge injection calibration and controls

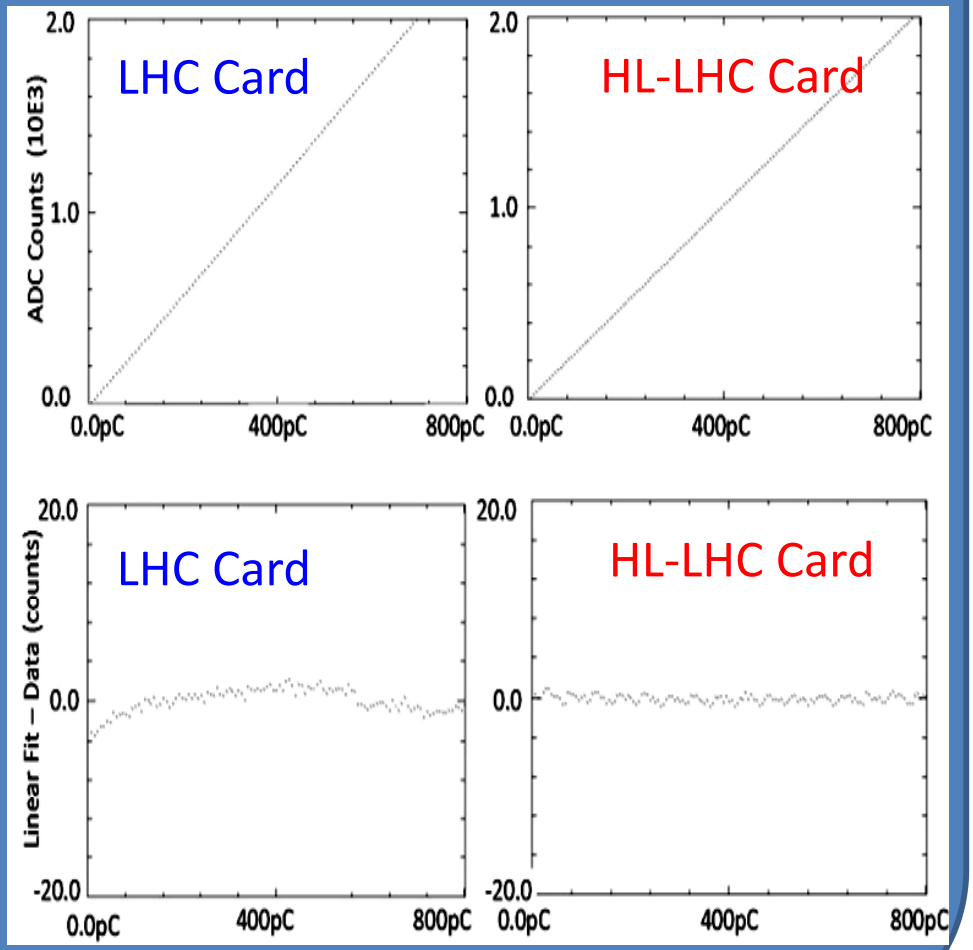


Readout Linearity Improvement

Low Gain Channel

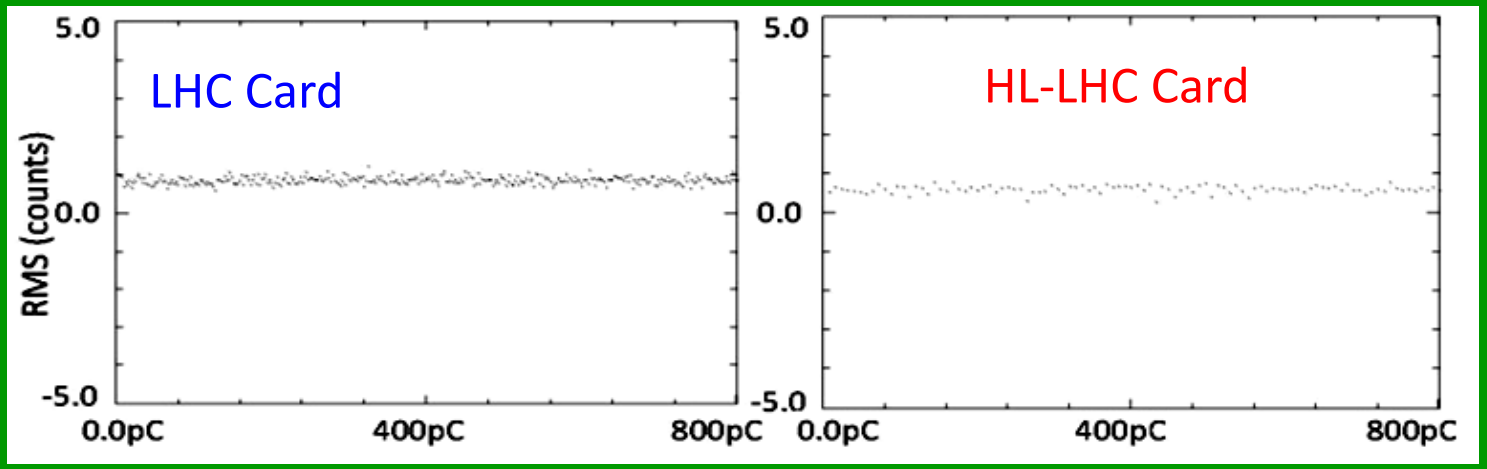


High Gain Channel

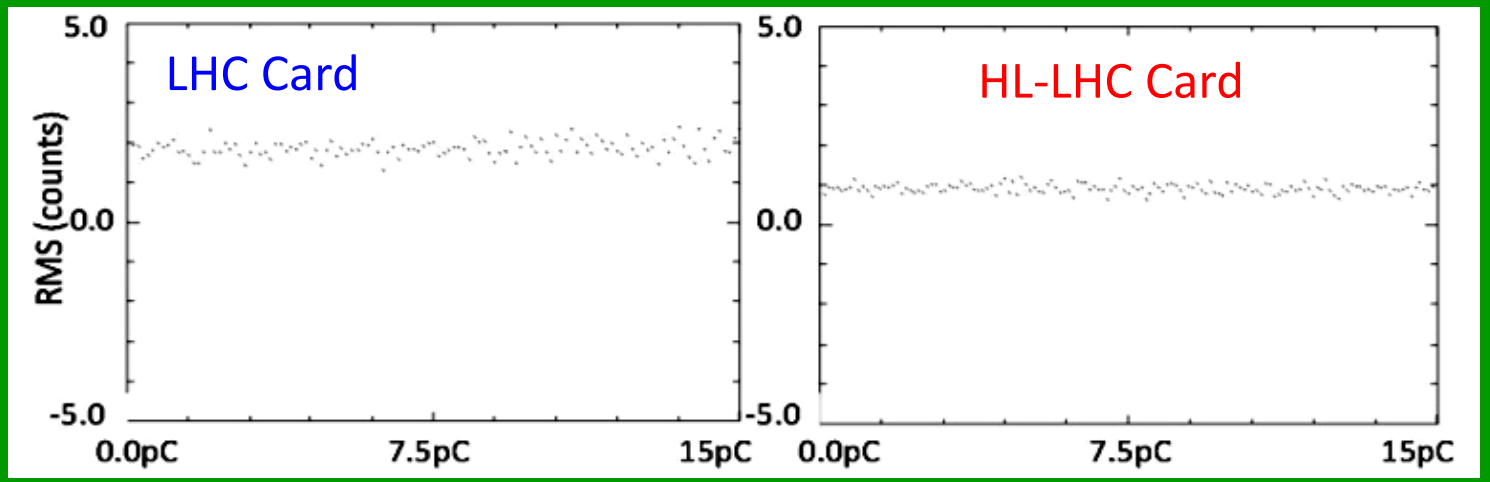


Readout Noise Improvement

Low Gain Channel RMS Noise



High Gain Channel RMS Noise



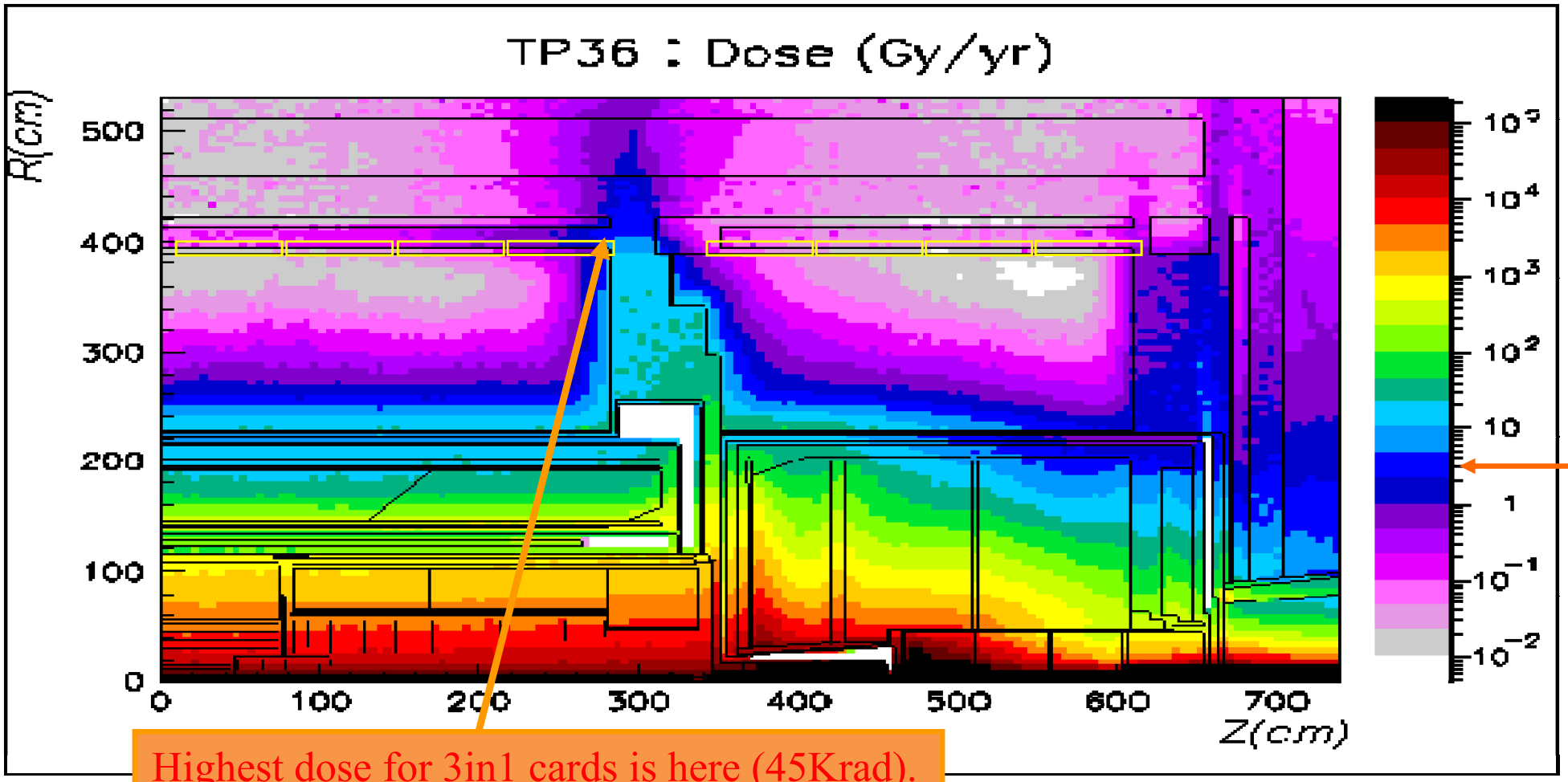
Radiation Hardness Studies

LHC/HL-LHC Ionizing Radiation Dose

Maximum rate 3in1 cards see is 3 Gy / year for LHC

15Gy/ years for HL-LHC x 10 year x 3 safety factor → 450Gy

45KRad (probably do not need x3 safety)



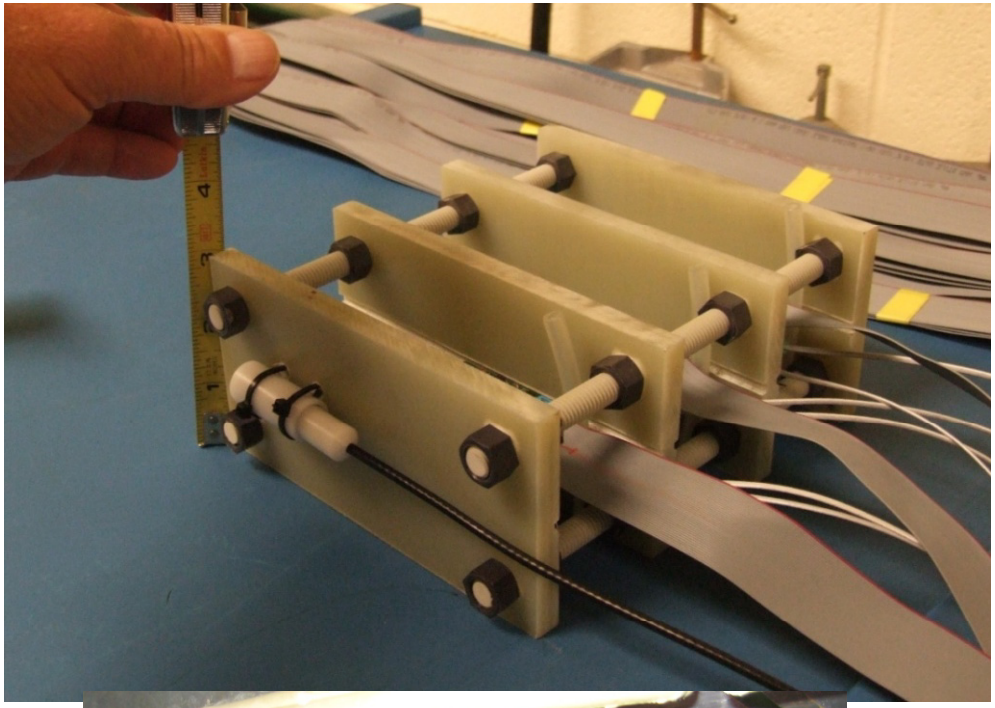
Radiation Test Site and Test Sources

Our original testing for LHC electronics was done at a Co-60 source at the Chemistry Department at Argonne National Laboratory. This source is no longer available.

We arranged testing for the upgrade electronics at the Advance Photon Source facility at Argonne .

Synchrotron radiation sources from 7 GeV Electrons at ANL APS

Setup of Radiation Test



Rack with 3 new analog front-end cards and an ION chamber set on top of the APS septum magnet.

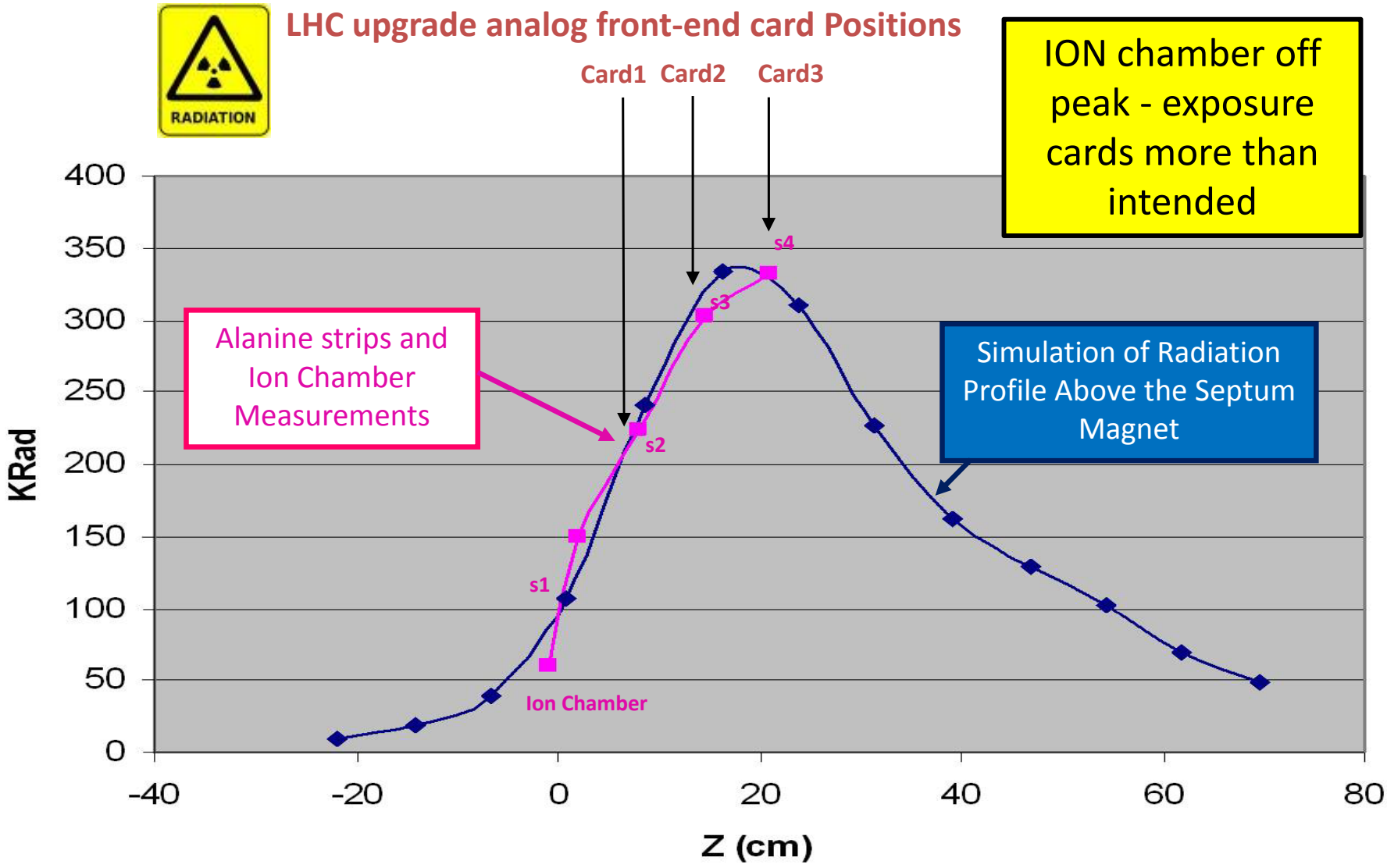
Radiation Test Sources and Intensity

Estimated dose 1KRad/17hrs
8.5KRad/week (6 day operation)

Radiation component	gamma	e- and e+	neutron	total
Peak DER (Sv/hr)	19.22	26.23	26.21	67.32
FWHM (cm)	34.97	40.21	34.57	37.38
zp (cm)	16.23	18.57	7.72	15.67

Radiation component	gamma	e-, e+	neutron
Peak E (MeV)	0.865	2.15	2.69

Radiation Test Result (1)



Radiation Exposure to Uprgade Analog Front-end Cards

Radiation Test Result (2)

Comparison of Charge Injection Switches Used on New LHC Upgrade Analog Front-end Card vs Current 3in1 Card

	TS5A2360	DG611DY
on resistance	0.9Ω	18 Ω
turn off time	2.5ns	12ns
turn off time	6ns	16ns
charge injection	1pC	4pC
leakage current	±20nA	20nA

A single component failed in radiation test of LHC Upgrade Analog Front-end Card, but met the requirement!

TS5A2360 failed at 71, 81 and 96 Krad (3 cards)
If radiation requirements are set higher that 70KRad we can revert to the DG611DY switch which survived to 333KRad.

Summary

- New COTS based design of TileCal Analog Front-end Card at HL-LHC looks very good
  - performance very good
  - survived radiation test
- Plan to test 60Gb/s 12 channel fiber optic transmission board in radiation environment (For error rate checking and correction)
- Our goal is to fully instrument TileCal wedges at CERN with new electronics for test beam and cosmic ray studies