
# An ATCA-based High Performance Compute Node for Trigger and Data Acquisition in Large Experiments

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# Agenda

- Motivation
- High Performance Compute Node
- Application in large experiments
- Lessons learned and challenges for the future

# Motivation

- Requirements from HEP experiments
- Future DAQ system
  - trigger-less DAQ?
- Concept introduction

# Requirements from HEP Experiments

- Design policy
  - High availability
  - High scalability
  - Universal I/O interface
- For the next generation HEP experiments
  - Huge number of channels
  - High data rate and event rate

  → High bandwidth and high performance computing needed

What the future trigger and DAQ will be?

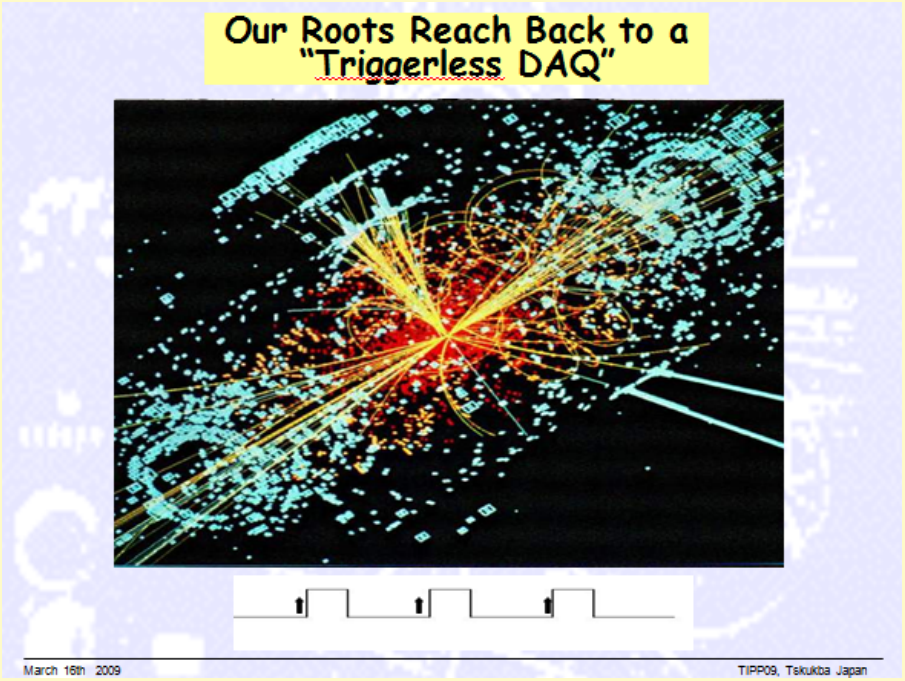
# Trigger-less DAQ

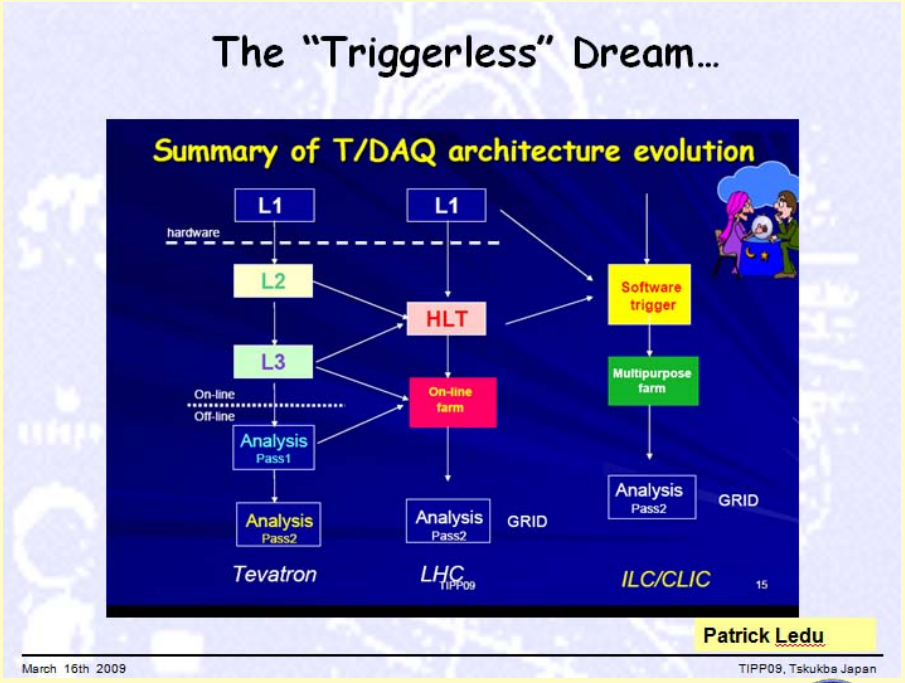
Our roots reach back to a "Triggerless DAQ"

—R. Tschirhart, TIPP09

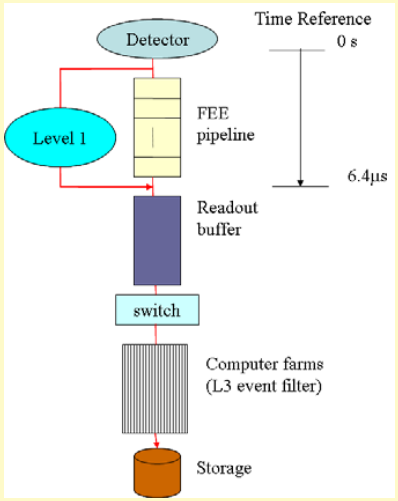
The "Triggerless" dream

—P. Ledu, TIPP09



# Future T/DAQ Architecture

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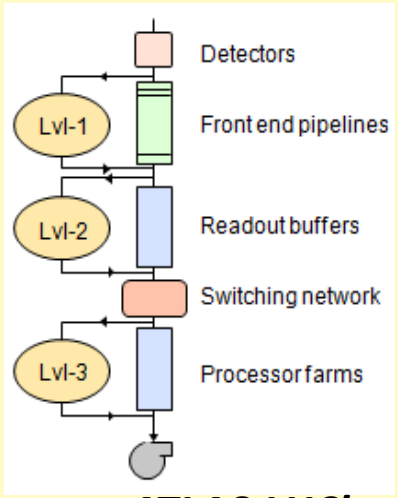
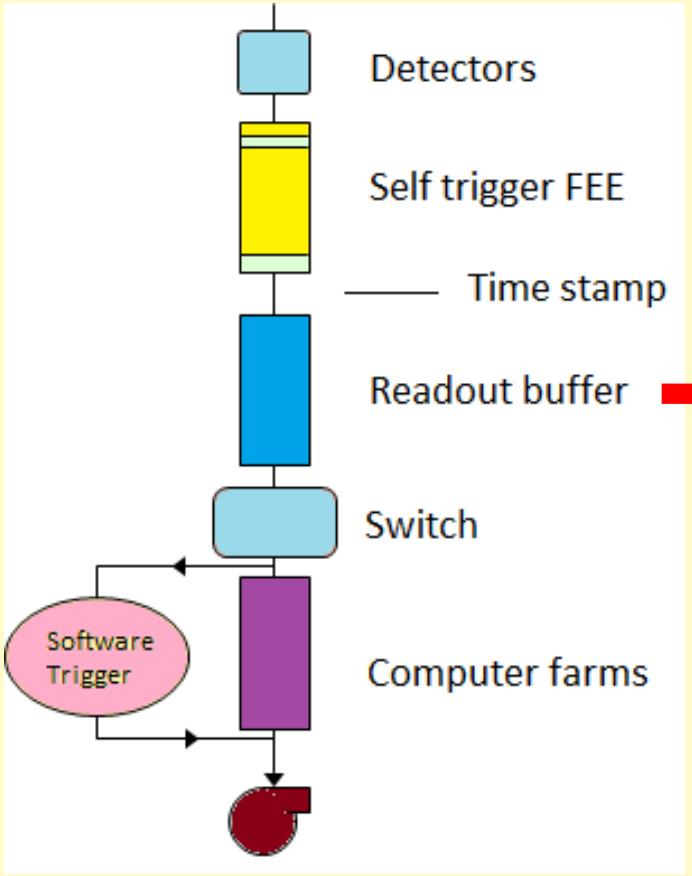



***ATLAS,LHCb***

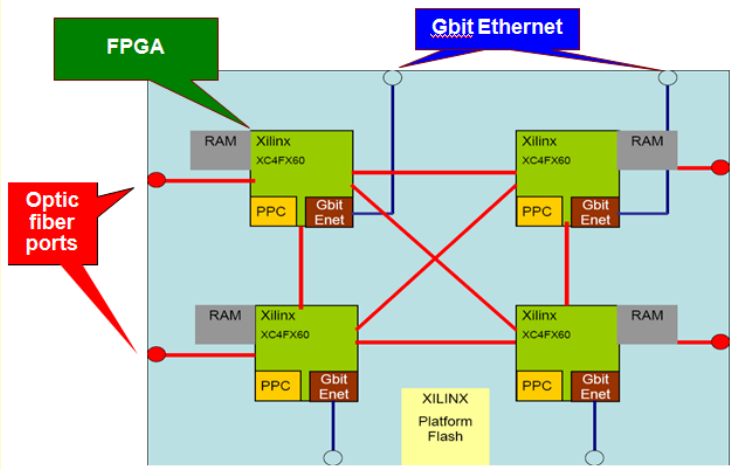


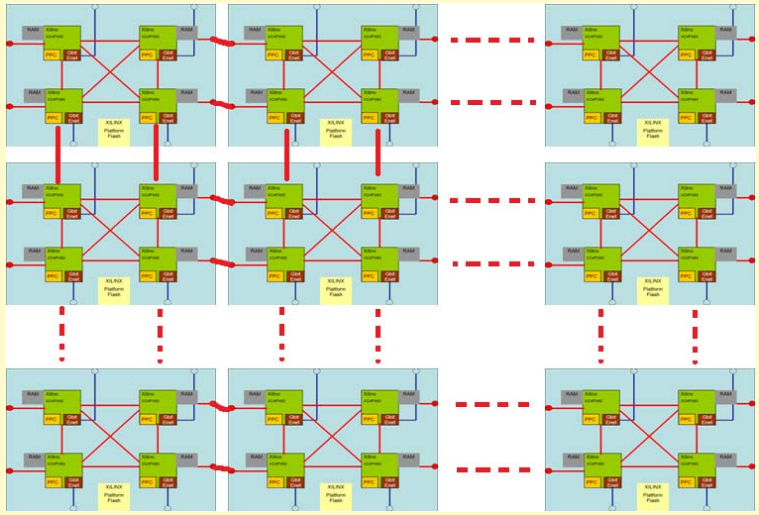

***PANDA***

Hao Xu talk: Introduction to PANDA DAQ System

# Concept Introduction

- High Performance Compute Node
- Goal:Universal high performance platform for multiple applications and experiments
- Configurable and Scalable Hardware Platform
  - Capable of High Performance Computing
  - Flexibility: Reusable
  - Scalability
    - Flexible network topology



# High Performance Compute Node

- Main feature
- Introduction to ATCA
- Current status

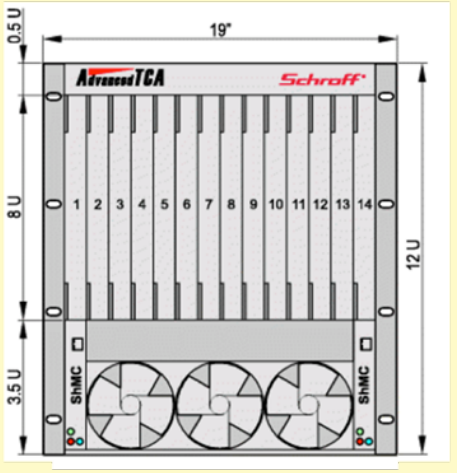
# Main Feature

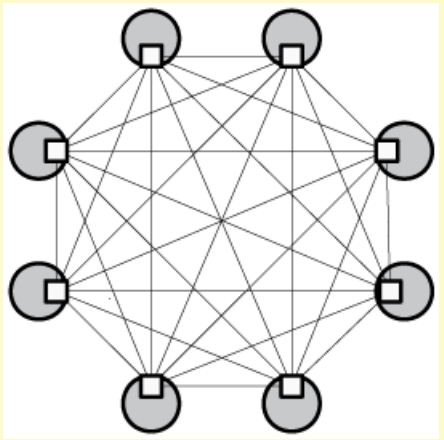
- High Performance Compute Power:
  - 5x Virtex-4 FX60-10/-11 FPGA
- High Bandwidth
  - 13x 2/3.125Gbps to backplane for interconnection
  - 5x Gigabit Ethernet
  - 8x 2/6.25Gbps Optical Links for data input
- Large buffer capacity
  - 2 GB 400MHz DDR2 SDRAM
- 2 Embedded PowerPC processors in each FPGA
  - Real time Linux/vxworks
- ATCA compliant
  - HA, Hot swap, Intelligent Platform Management Interface (IPMI)

# Introduction to ATCA

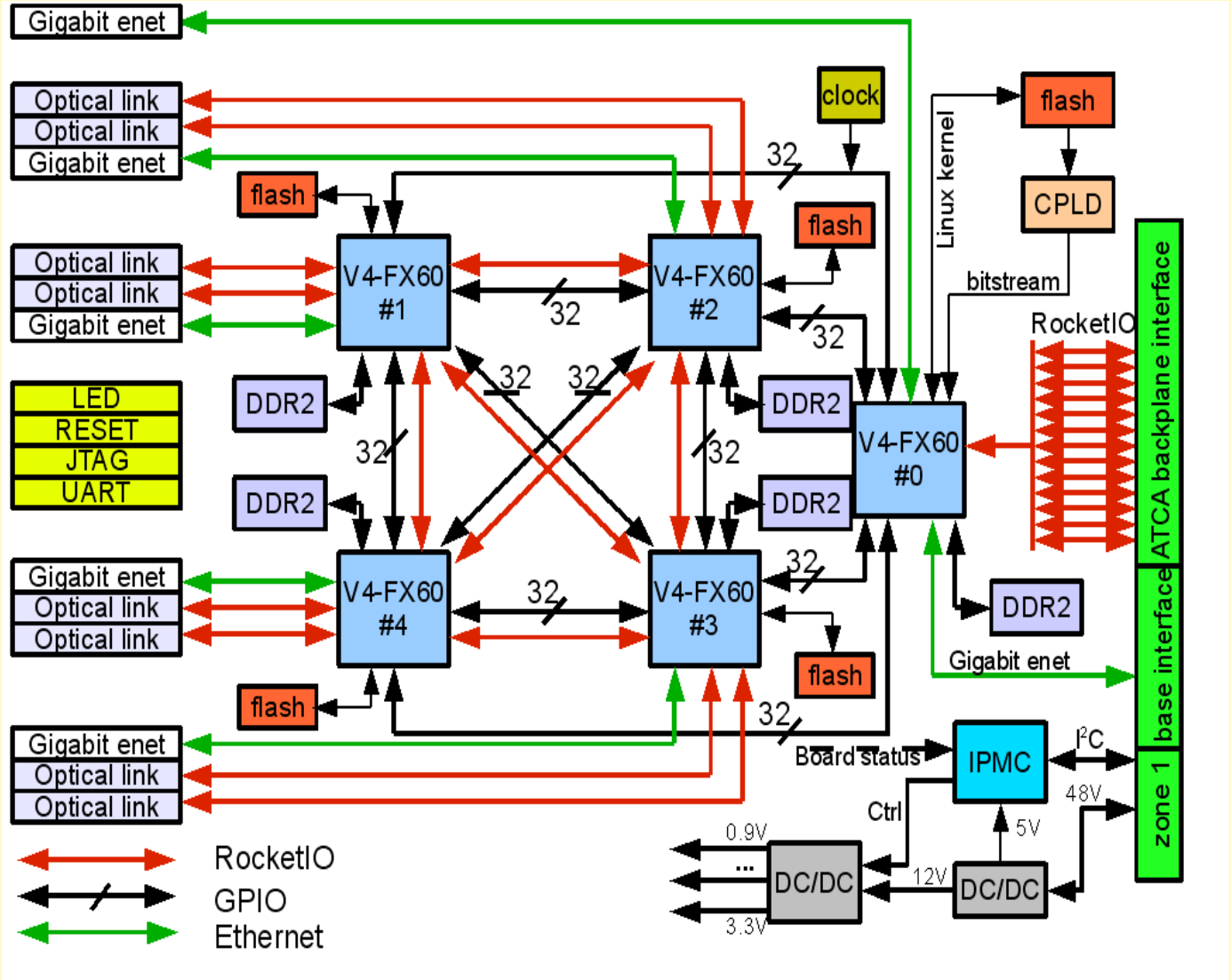
ATCA: Advance Telecommunication Computing Architecture

- PICMG standard
- 19” Rack: 14 slots – 8U
- Single Voltage supply: -48v
- Large Power and Cooling
  - 200W/slot
- High Availability
  - Shelf manager
  - IPMI controller
  - Hot swap capability
- High Speed Backplane
  - Point-to-point differential lines
  - Full mesh topology
- Rear Transition Module (RTM)

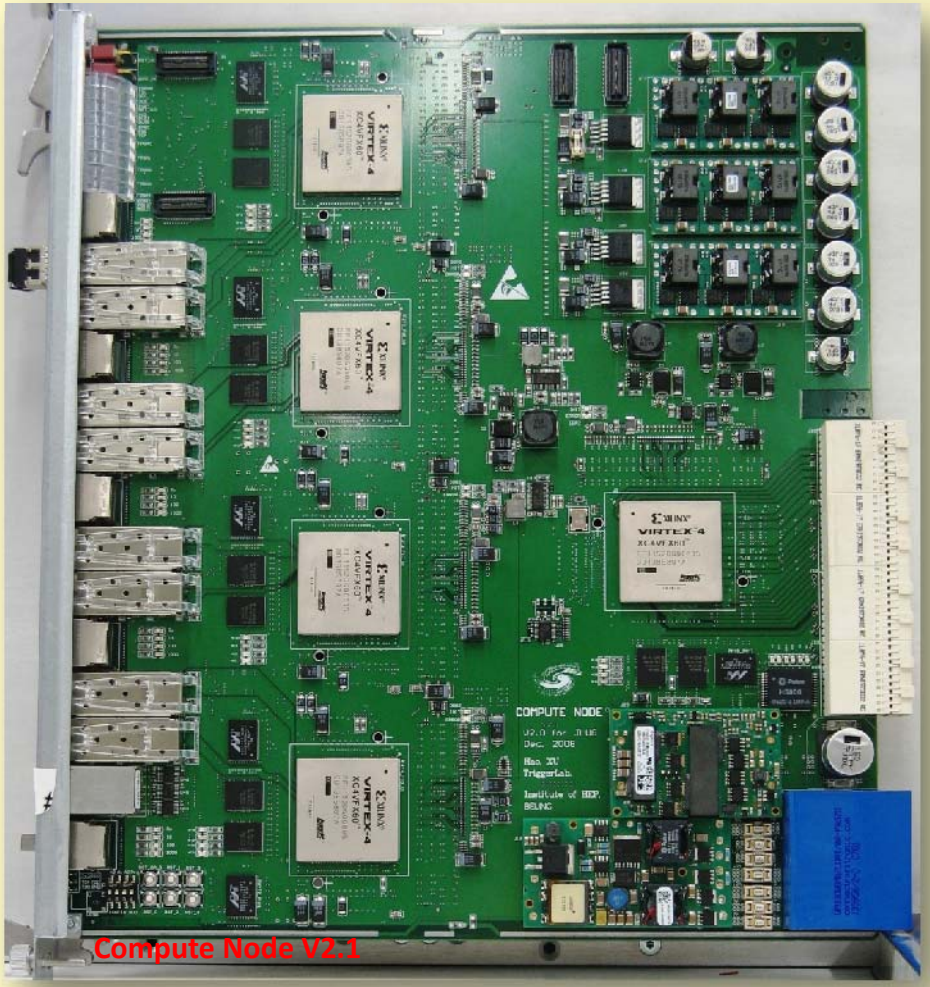


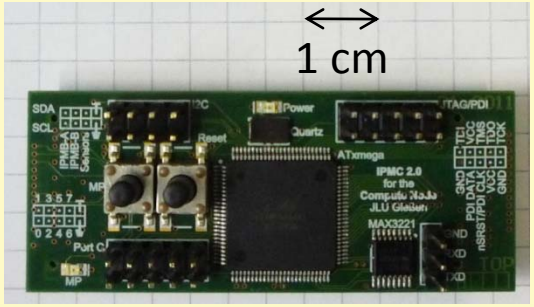



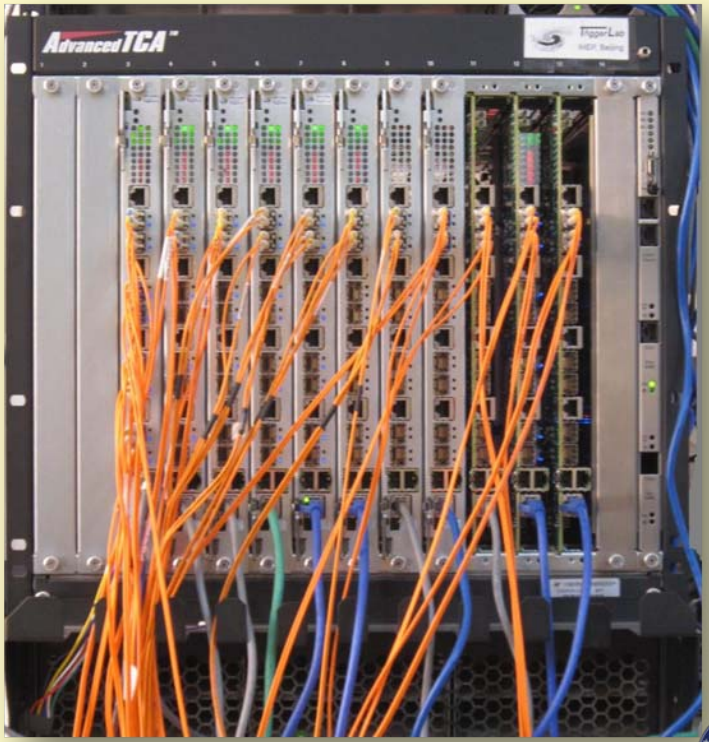
# Structure of HPCN



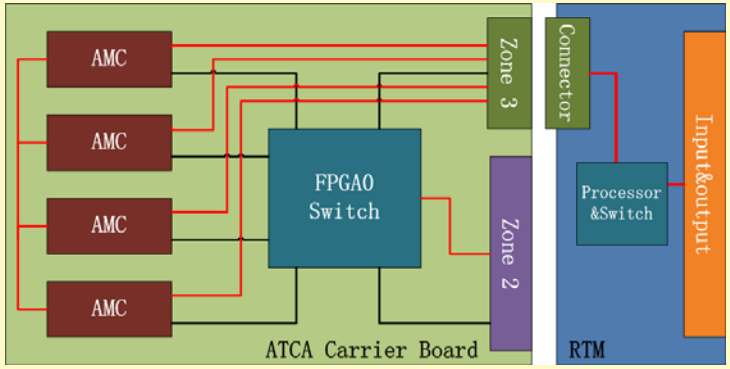
# Latest HPCN and IPMC PCB

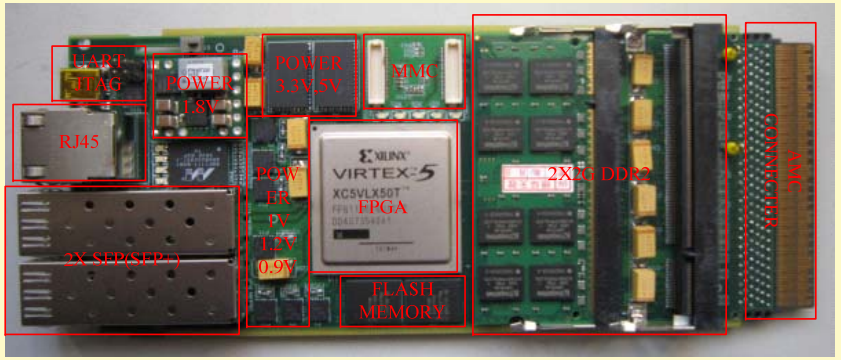


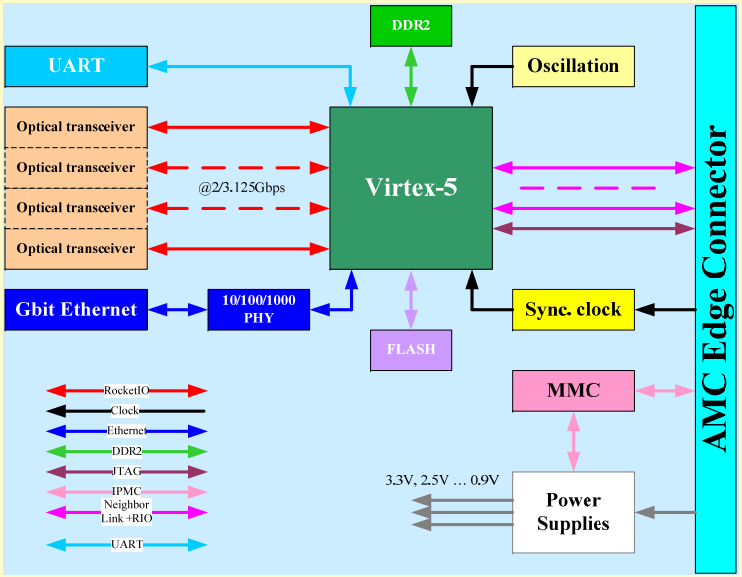



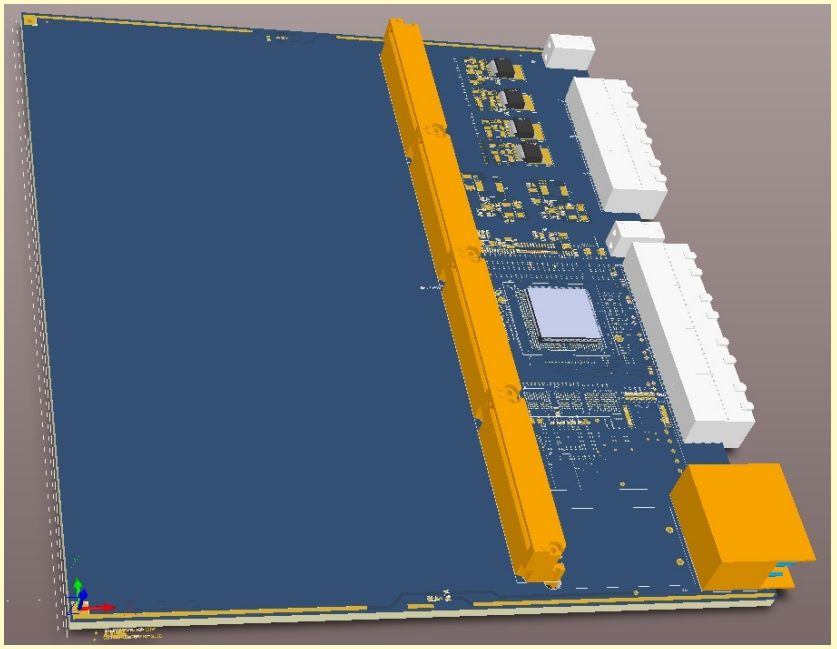



# AMC-based Upgrade

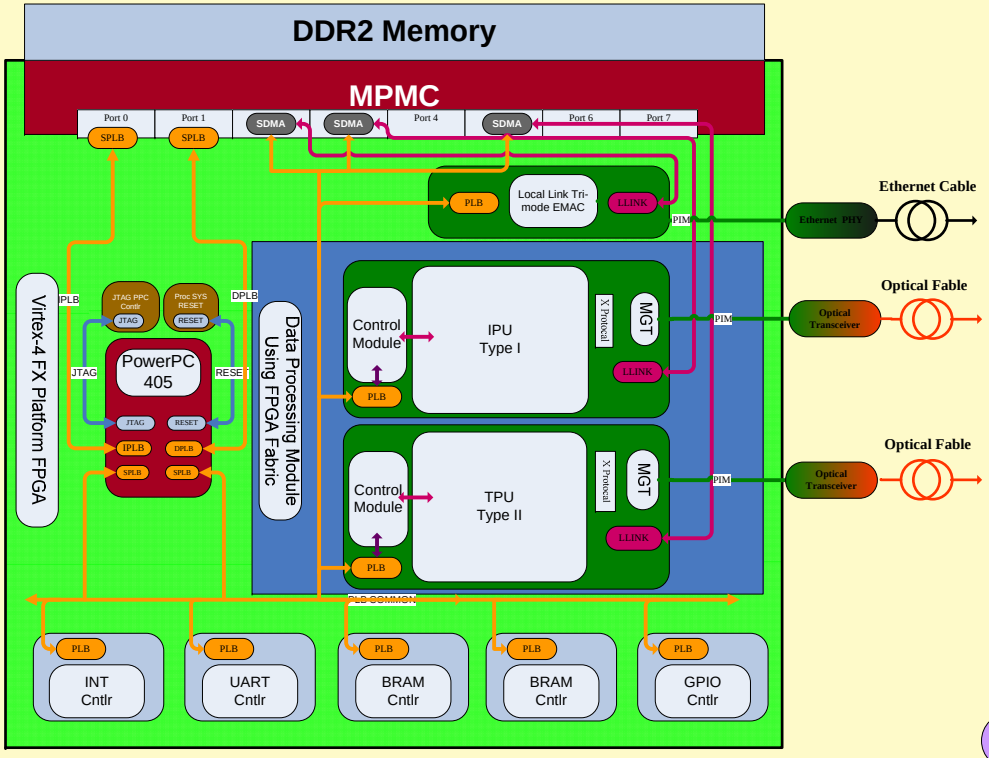


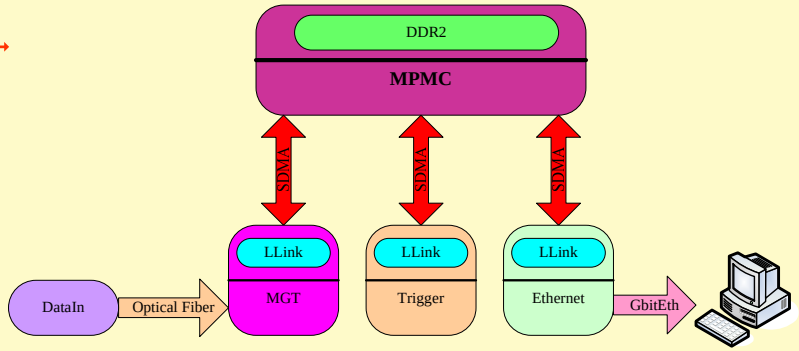



# System on FPGA and DATA Flow




XILINX

Linux


- Based on PowerPC hardcore inside Xilinx FPGA and other open source IP cores to build a general purpose system, Open source Linux is ported for system management and UDP/TCP stack processing
- Online trigger algorithms are designed as custom IP cores and a on-chip data switching module is build based on MPMC

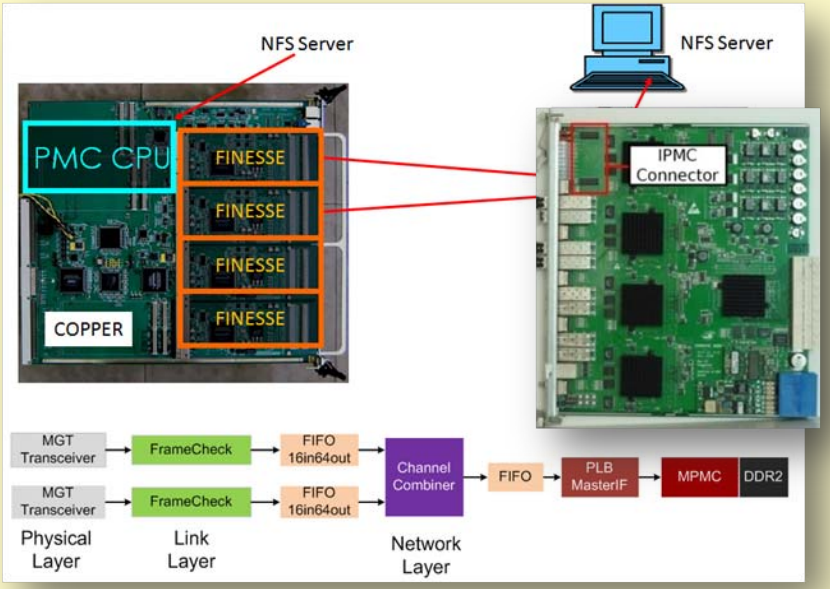
# Application in the Large Experiments

- PANDA DAQ system
- BELLE II PXD readout system
- BELLE II SVD data concentrator
- …

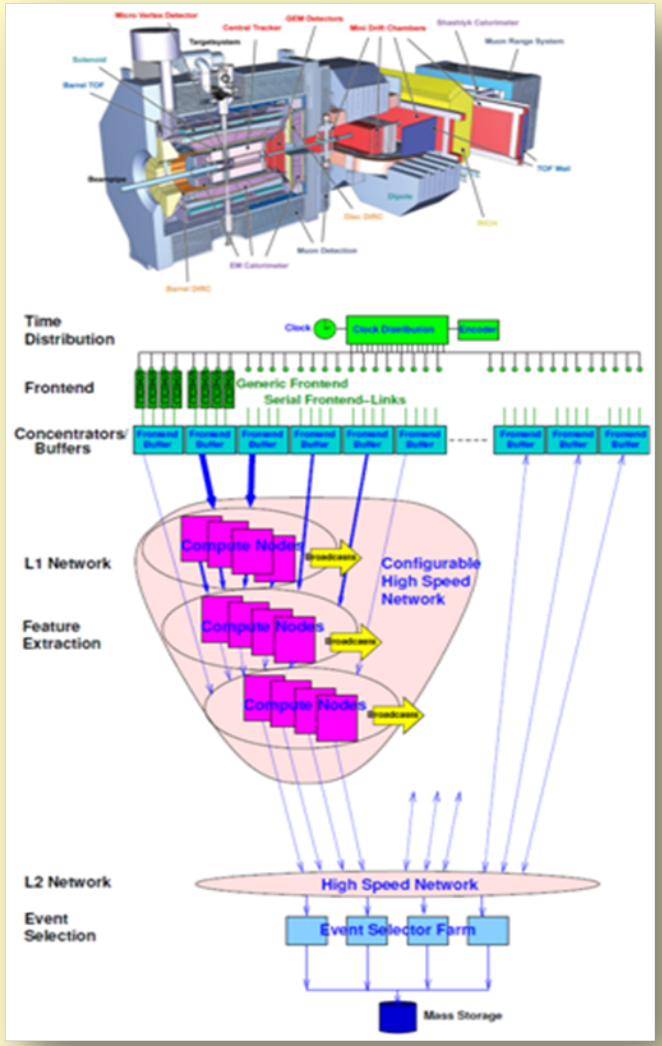
# PANDA DAQ System

Jerzy Smyrski talk: Overview of the PANDA experiment
Hao Xu talk: Introduction to PANDA DAQ System

- the 'heart' of the PANDA DAQ system
  - Tracking/cluster finding/…
  - Event building
  - Event filtering



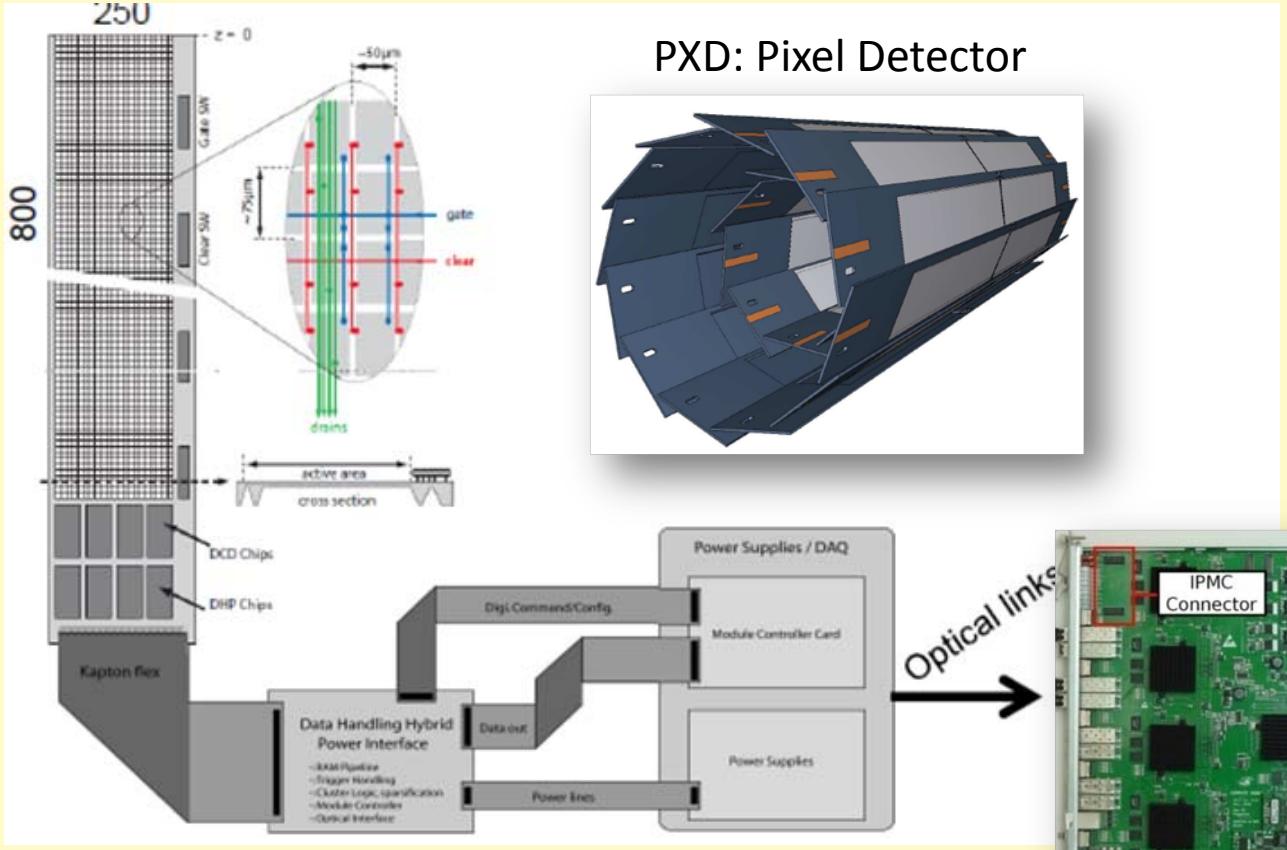

T/DAQ prototype test setup for EMC




PANDA detector & TDAQ structure

# BELLE II PXD Readout System

Gary S. Varner talk: The BELLE II detector
Ladislav Andricek talk: Ultra-thin fully depleted DEPFET active pixel sensors

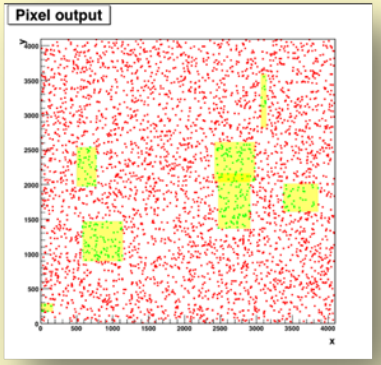



PXD: Pixel Detector






- Data size 20GB/sec (@20kHz, ~3% occupancy)
  - ~4.5Gbps/ch
- buffering for 5 seconds until HLT decision
  - 4GB DDR2 SDRAM
- New CN needed!!

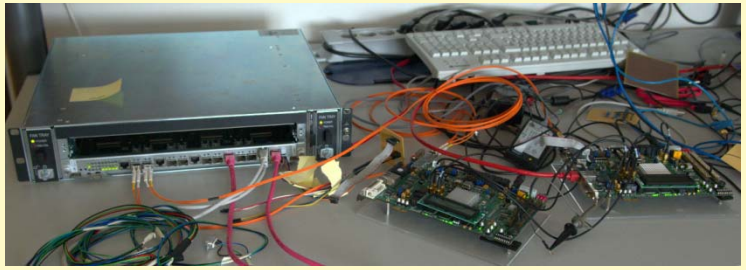



Regions of Interest(ROI) development on CN

# BELLE II SVD Data Concentrator

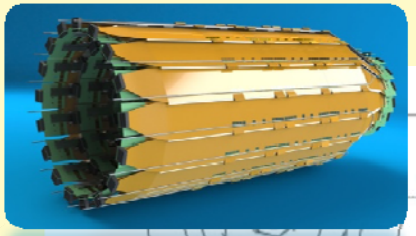
SVD: Silicon Vertex Detector

- Input
  - 42 links input
  - SFP Connectors
  - Dynamic bandwidth
- Output
  - 5~10 optical links
  - 6.25Gbps/ch
  - Dynamic bandwidth



test setup with Compute node

Gary S. Varner: The BELLE II detector
Christian Irmler: The BELLEII Silicon Vertex Detector



# Lessons Learned and Challenges for the Future

- ATCA is a good choice for DAQ system in the large HEP experiments
  - Intelligent architecture
  - High Availability
- Think widely before development, start from the current design.
- One design will not be suitable for every application. It should be easy to upgrade to meet various requirements.
  - Catching the commonality is the key
- Design should not be bonded onto any hardware resources. Otherwise it will be limited in the future.
  - Our embedded development is based on the PowerPC hard core.
  - Xilinx changes the embedded architecture from PowerPC to ARM in future productions
  - How to do next?
    - Change to ARM? Shall we change again if ARM is given up?
    - So, we will not use any embedded system relied on the hard core. We try to implement most of the function modules with Verilog/VHDL. It is really a great challenge!
- High bandwidth, large memory capacity and high performance computing are the challenges
  - The throughput from input to output should also be considered
    - PXD readout
      - Optical link input 6.25Gbps OK
      - Gbit Ethernet output OK
      - Bottleneck: throughput from optical link to DDR2 SDRAM

# Thank you for your attention