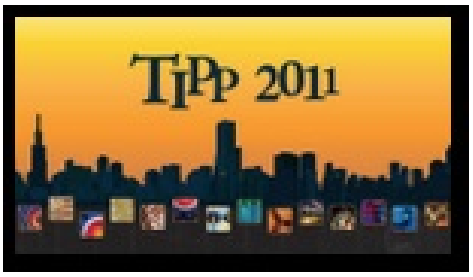


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# An ATCA-based High Performance Compute Node for Trigger and Data Acquisition in Large Experiment

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This paper describes the design of ATCA-based high performance compute Node for high level trigger and data acquisition in large physics experiment like PANDA, BESIII and Belle II. For an experiment like PANDA, the trigger and data acquisition system needs to handle interaction rates of the order of more than 10^7/s and data rates of 200 GB/s and more. The high level trigger and data processing with high performance is necessary. An ATCA compliant FPGA-based Compute Nodes system is designed for this purpose. Each CN features 5 Xilinx Virtex-4 FX60 FPGA chips and up to 10GB DDR2 memory. A total bandwidth of 52Gbps optical links (8ch x 6.5Gbps/ch) and 39Gbps electrical backplane links (13ch x 3Gbps/ch) are provided to receive data from front-end electronics and data transmission among different channels. The high data processing performance are accomplished by the fabric resources provided by 5 FPGA chips. 5 Gigabit Ethernet links are used to transmit processing results to mass storage. The finished version has been proved successful and is being used in trigger and DAQ development for PANDA system, and also under investigation for use in PXD in Belle II. The ATCA-based Trigger and Data Acquisition System is scalable and suitable for various applications for next-generation nuclear and particle experimental physics.

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