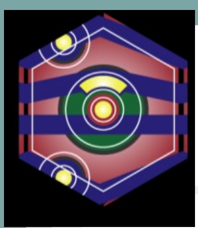
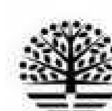
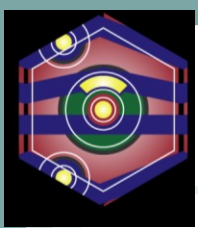


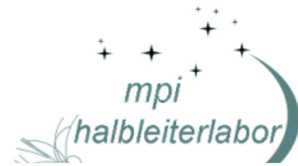
High Precision Vertexing at the Belle-II Experiment



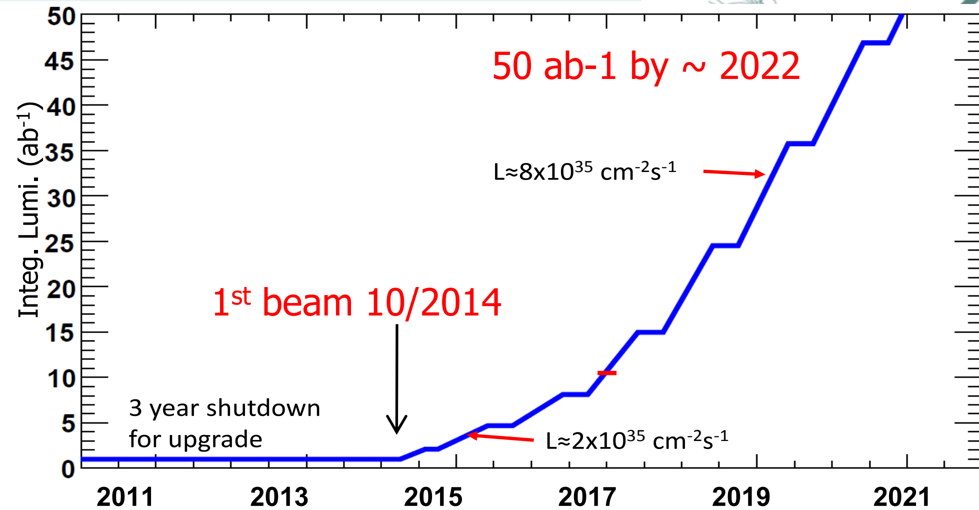
Jelena Ninkovic *for the DEPFET Collaboration (www.depfet.org)*

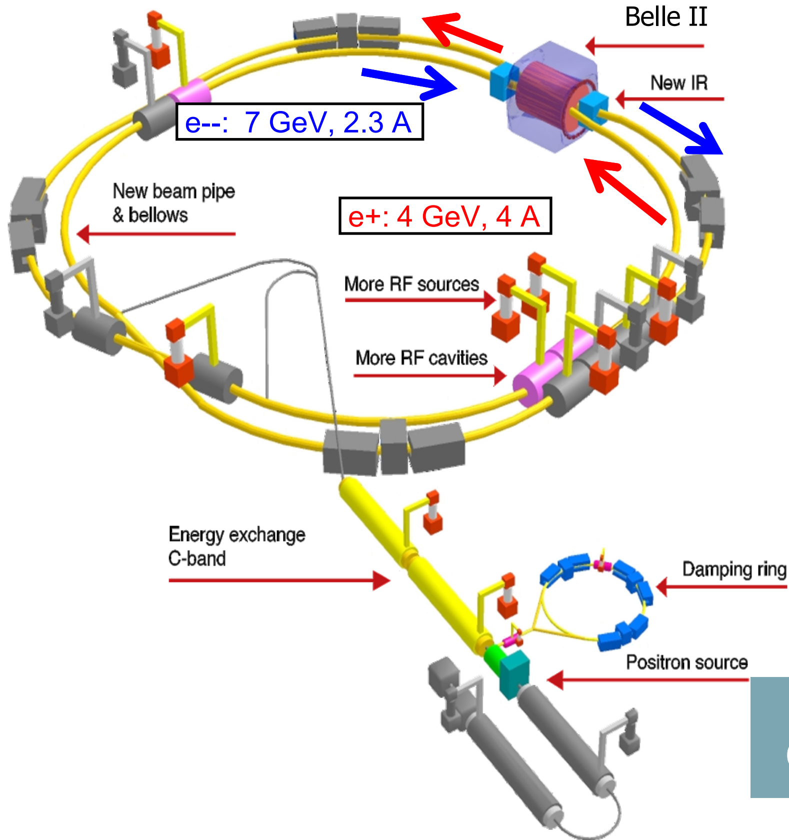


SuperKEKB



- e^-/e^+, 7 GeV & 4 GeV
- E_{cm} at Υ(4s) Resonance, (10.58 GeV)
- goal L = $8x10^{35}$ $cm^{-2}s^{-1}$

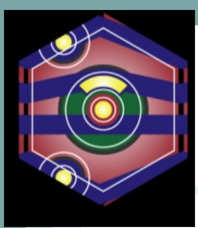




Machine parameter	HER (KEKB)	LER (KEKB)	HER (SuperKEKB)	LER (SuperKEKB)
Vertical beam size	0.94μm	0.94μm	59nm	59nm
Beam current(mA)	1188	1637	2600	3600
luminosity($cm^{-2}s^{-1}$)	$2.1x10^{34}$		$8x10^{35}$	

Smaller beam size & more current:
→ 40x higher luminosity

Higher Background: occupancy and rad. Damage
QED background, intra-beam scatter., beam-gas, synchrotron



Belle II Detector

mpi halbleiterlabor

KL and muon detector:
Resistive Plate Counter (barrel)
Scintillator + WLSF + MPPC (end-caps)

EM Calorimeter:
CsI(Tl), waveform sampling (barrel)
Pure CsI + waveform sampling (end-caps)

Particle Identification
Time-of-Propagation counter (barrel)
Prox. focusing Aerogel RICH (fwd)

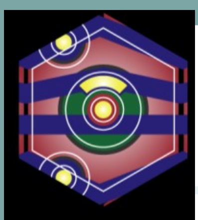
electron (7GeV)

Beryllium beam pipe
2cm diameter

Vertex Detector
2 layers DEPFET + 4 layers DSSD

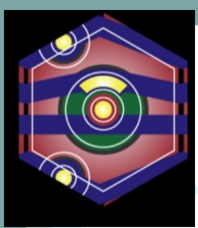
positron (4GeV)

Central Drift Chamber
He(50%):C_2H_6(50%), Small cells, long lever arm, fast electronics



Belle II Detector

Belle Silicon Vertex Detector (SVD): 4 layers DSSD
→ Belle II: 4 DSSD (SVD)+ **2 pixel layers (PXD)**



Belle II requirements

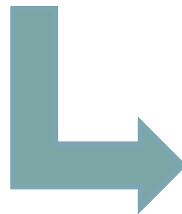
Higher beam induced background at superKEKB

-QED background, beam-gas interactions and synchrotron radiation

superKEKB is dominated by low momentum tracks (< 1GeV/c):

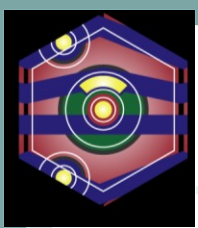
- Low material!!!
- IP resolution always dominated by MS error (beampipe & 0.14%X_0 Si) of ~ 9 µm at 1 GeV/c

→ **Modest intrinsic resolution of σ ~ 10 µm sufficient: pixels about 50µm**

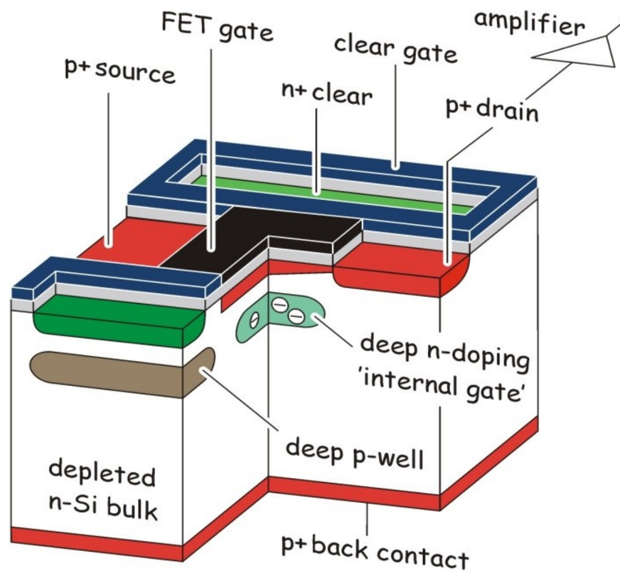


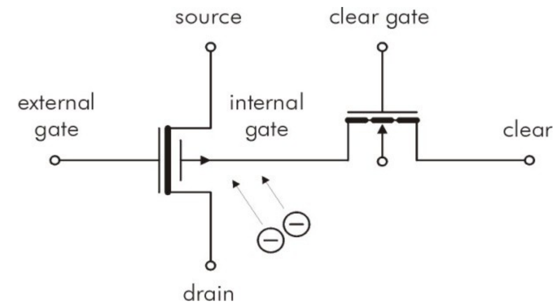
Tight schedule (2014) to develop a compete detector system

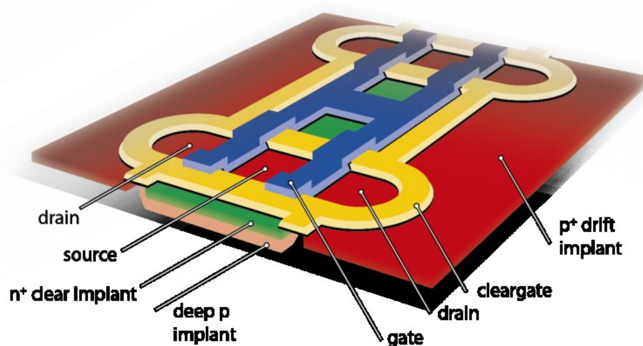
	Belle II
occupancy	0.4 hits/µm²/s
radiation	~1 Mrad/year
Duty cycle	1
Frame readout time	20 µs
Pixel size	50 x (50-75) µm²



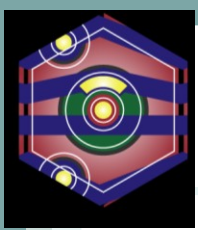
What is a DEPFET?





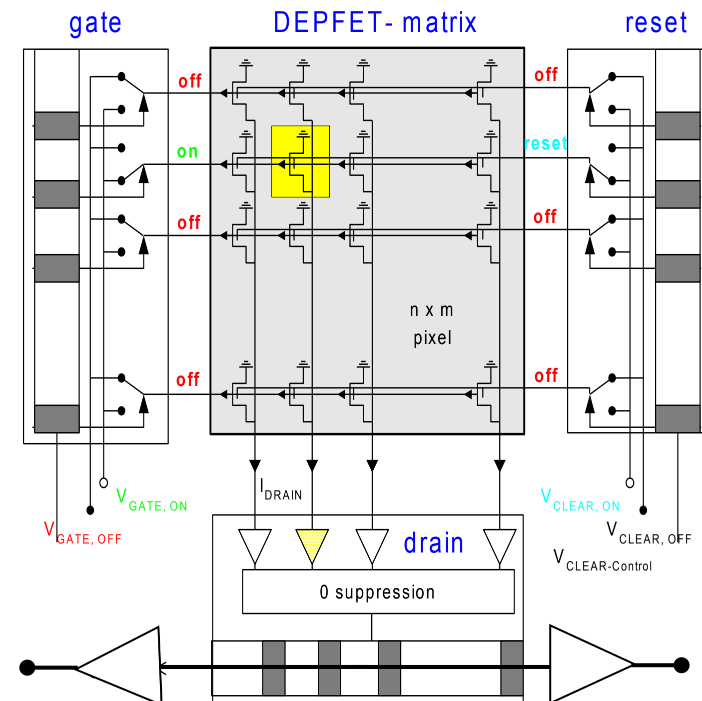


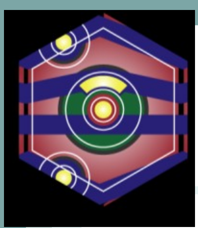
- **fully depleted sensitive volume**
  - fast signal rise time (~ns), small cluster size
- Fabrication at MPI HLL
  - Wafer scale devices possible
  - no stitching, 100% fill factor
- no charge transfer needed
  - faster read out
  - better radiation tolerance
- **Charge collection in "off" state, read out on demand**
  - potentially low power device
  - internal amplification
  - charge-to-current conversion
  - r/o cap. independent of sensor thickness
- **Good S/N > 20 for thin devices → ~40nA/µm for MIP**



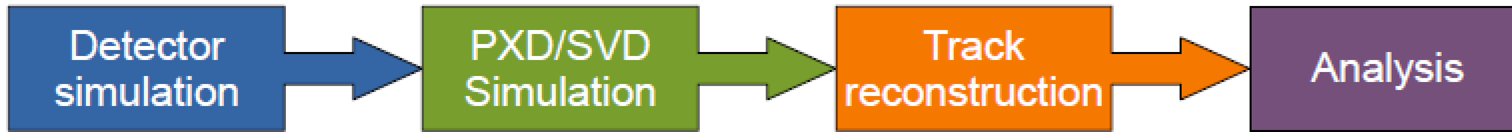
DEPFET matrix read-out

- Matrix read out in “Rolling shutter” mode
  - select row with external gate, read current, clear DEPFET
  - two different auxiliary ASICs needed, but no interconnect in sensitive area
  - only few rows active → low power consumption





Detector Design: Full simulation chain



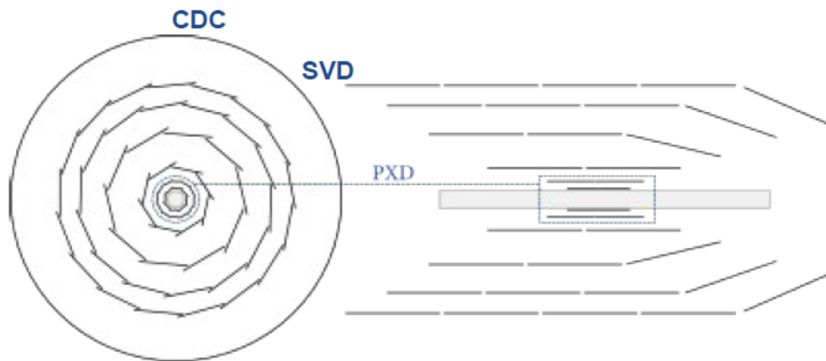
Particle gun (single event)
EvtGen (physics event)
Mokka geometry

Ionization points
Signal points
Electronic noise
Digitization and clustering

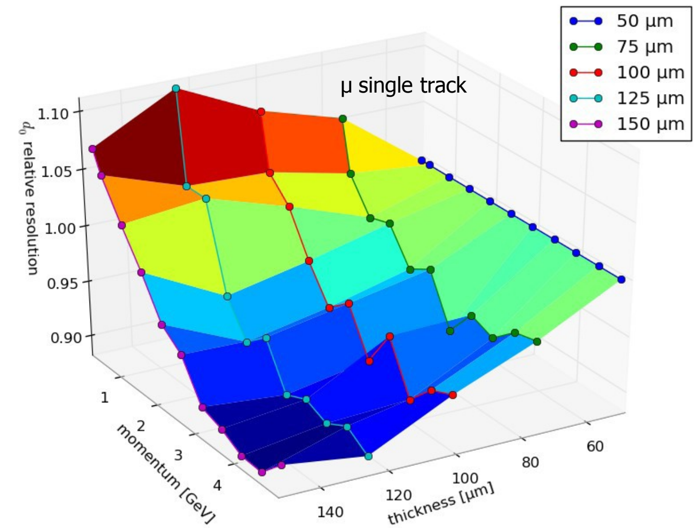
Marlin tracking
PXD+SVD+CDC

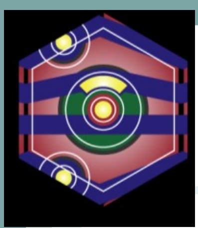
Physics channels

- Digitizer (Geant4) tuned with TBeam data:
- Electric noise
- Electric field in Si (charge collection time)
- Lorentz angle in magnetic fields

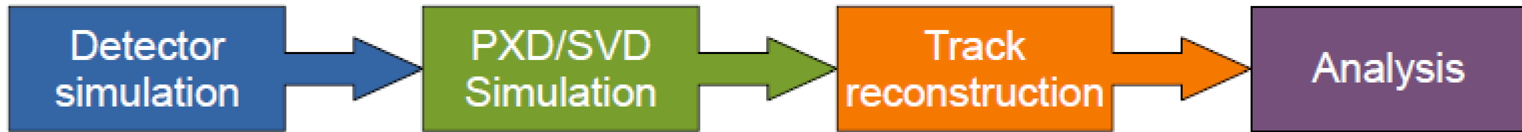


Optimization studies:
- Sensor thickness
- Pixel size
- Inner layer radius





Detector Design: Full simulation chain

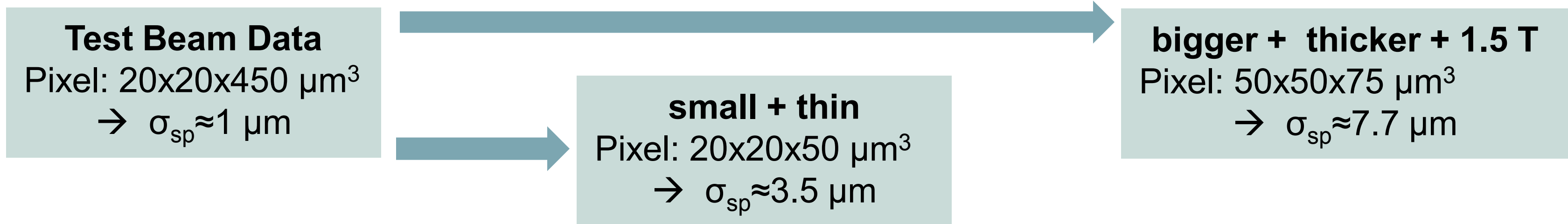


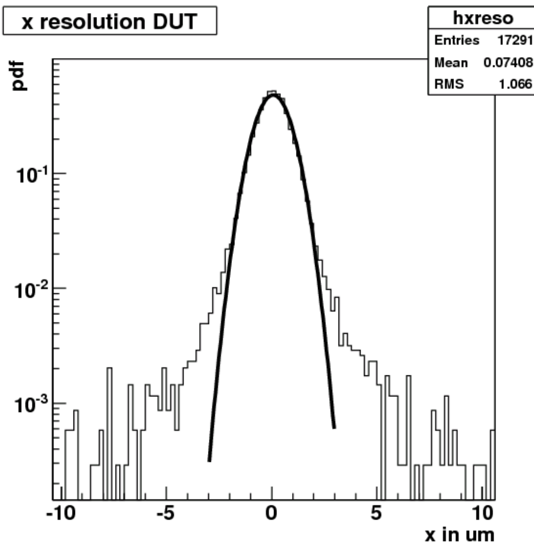
Particle gun (single event)
EvtGen (physics event)
Detector geometry
Material

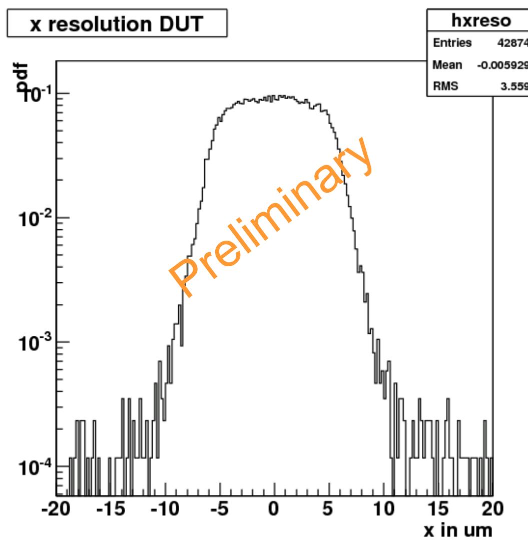
E-Field in Silicon
Lorentz angle in B-Field
A/D Conv. and clustering

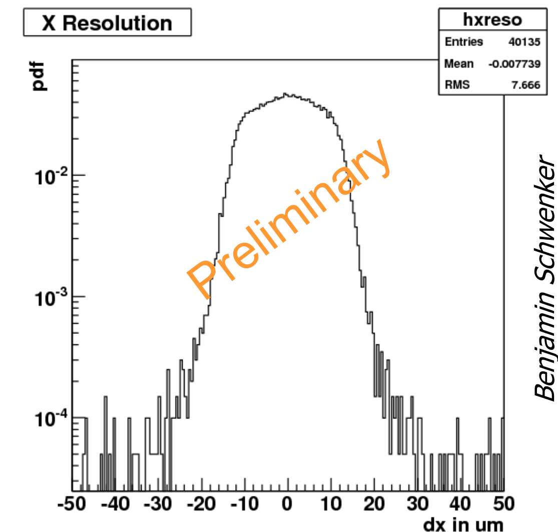
Marlin tracking
PXD+SVD+CDC

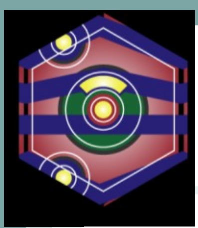
Physics channels



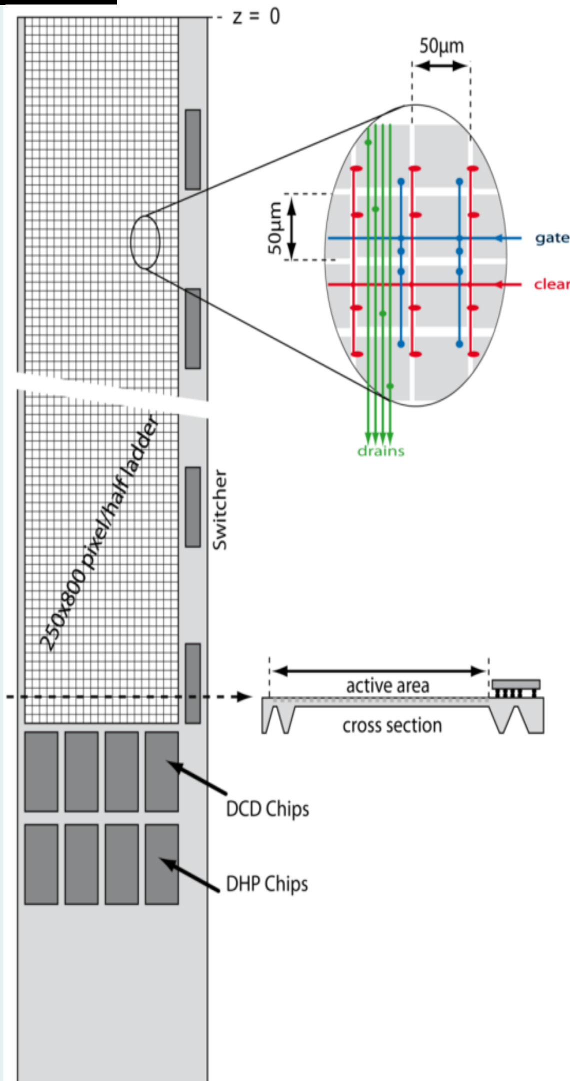








Belle II ladder

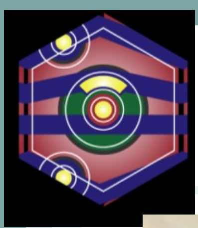


- All silicon module, sensitive area (DEPFETs) thinned
- Length: 90mm (inner), 123mm (outer), divided in half ladders
- 23 mm insensitive silicon on both sides (EOS)
- ASICs flip chipped to silicon substrate
- Insensitive part used as substrate for ASICs (MCM-D)

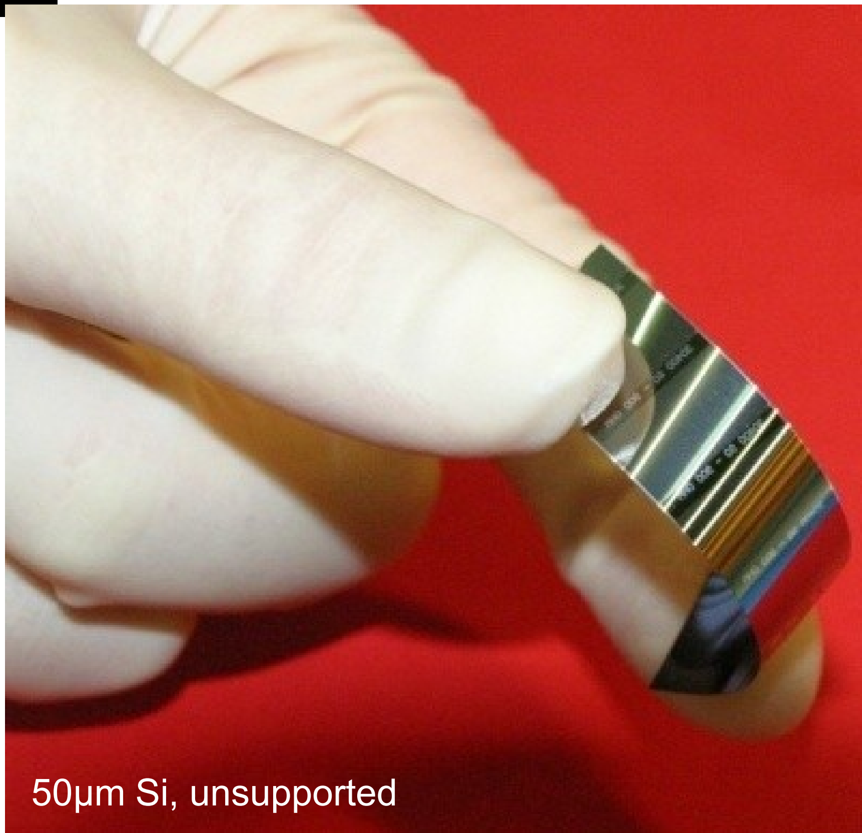
	Inner layer	Outer layer
# ladders	8	12
Radius	1.4 cm	2.2 cm
Pixel size	50x50 μm^2	50x75 μm^2
# pixels	1600(z)x250(R-ϕ)	1600(z)x250(R-ϕ)
Thickness	75 µm	75 µm
Frame/row rate	50 kHz/10 MHz	50 kHz/10 MHZ

Angular coverage 17°<θ < 155°

Belle II PXD
in total ~8Mpixels



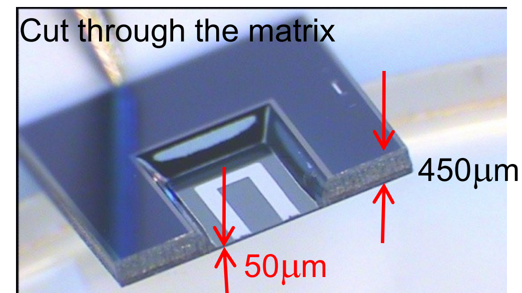
Self-supporting All-Silicon Module

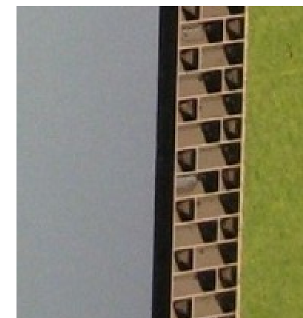


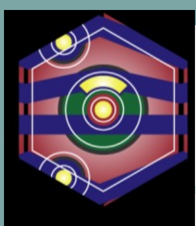
50μm Si, unsupported

50μm Si in Silicon frame

- Half-ladders (modules) are laser-cut
- Modules are supported by a monolithic silicon frame
- Two modules are assembled to one ladder
- overall length is 136 mm (inner) and 169 mm (outer)

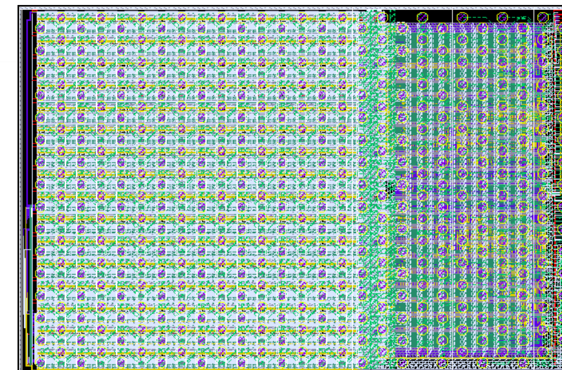




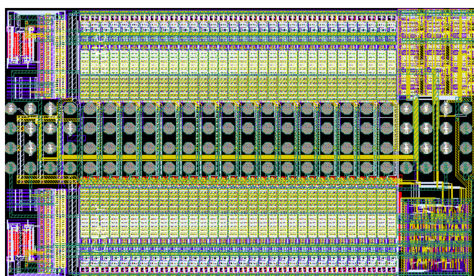


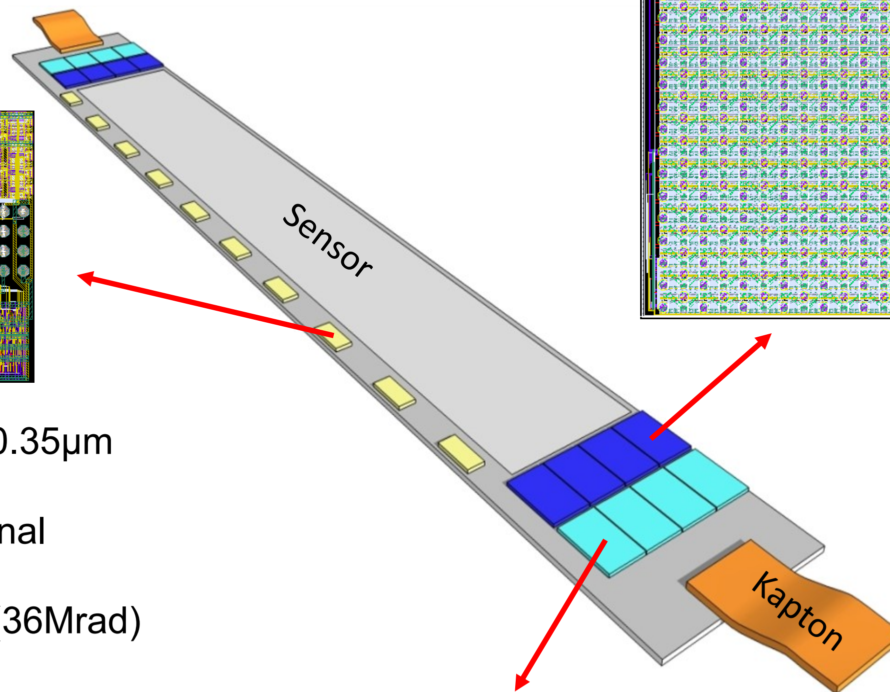
Auxiliary ASICs

DCDB (Drain Current Digitizer for BelleII)
Analog frontend and ADC



SwitcherB
Row control

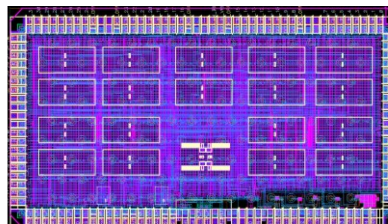




UMC 180nm
Size 3.3 × 5.0 mm²
Integrated ADC
Irradiation up to 7Mrad

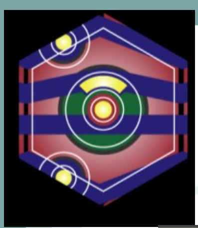
AMS high voltage 0.35µm
Size 3.6 × 2.1 mm²
Gate and Clear signal
Fast HV up to 30V
Rad. Hard proven (36Mrad)

DHP (Data Handling Processor)
Data reduction and Processing

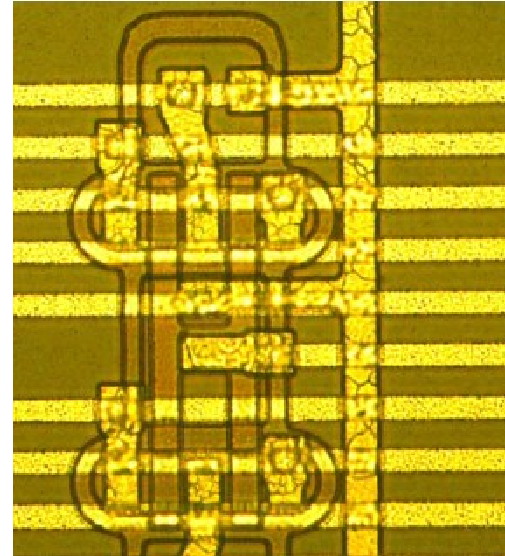


IBM CMOS 90nm → TSMC (65nm)?
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation

Switcher, DCD: Heidelberg U.
DHP: Bonn U., Barcelona U.



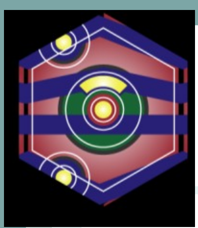
PXD6 Batch: Prototyping for Belle II



- 9 Implantations
- 19 Lithographies
- 2 Poly-layers
- 2 Alu-layers
- sums up to 89 steps with 1-5 WD each
- in between:
  - a lot of inspection steps!
  - process control, dummy wafer production..

→ **19 months processing time (16 after SOI pre-processing)**

First thin DEPFET production is finished!!!



mpi
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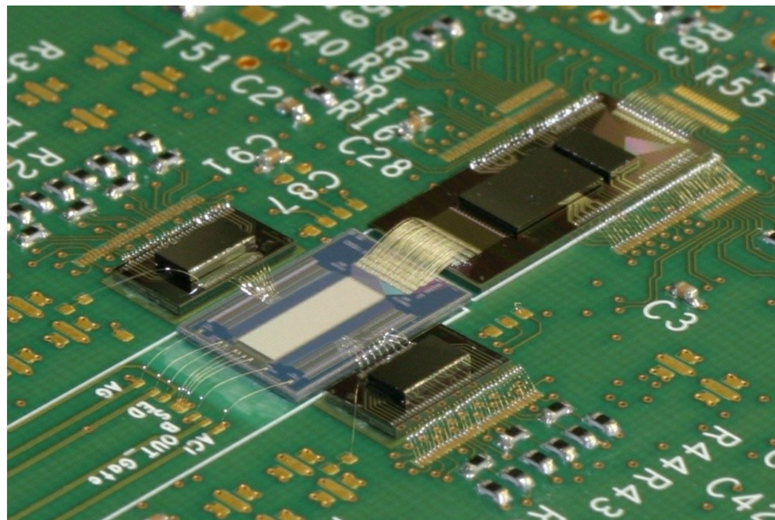
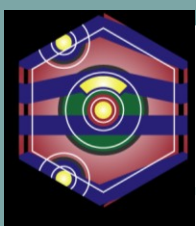
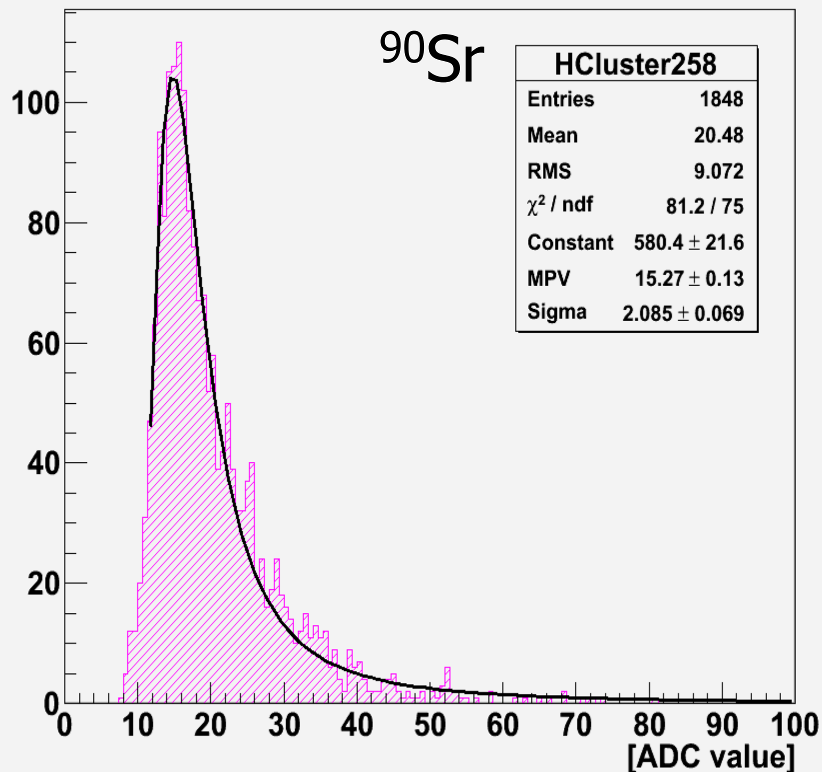
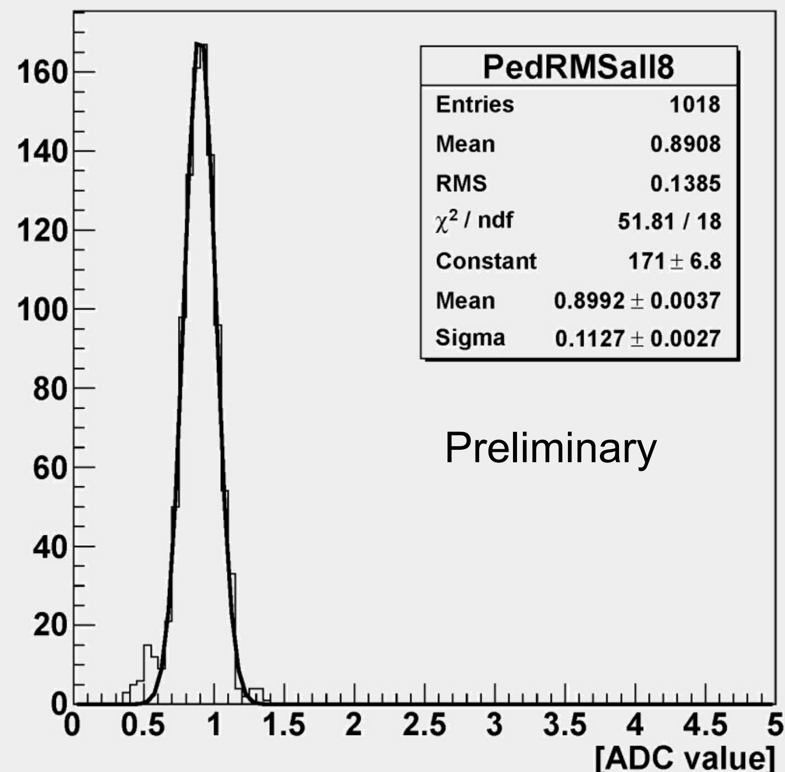




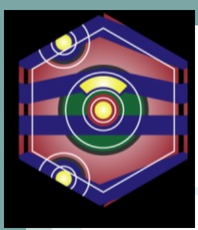
Thin DEPFET & DCDB@320MHz read out





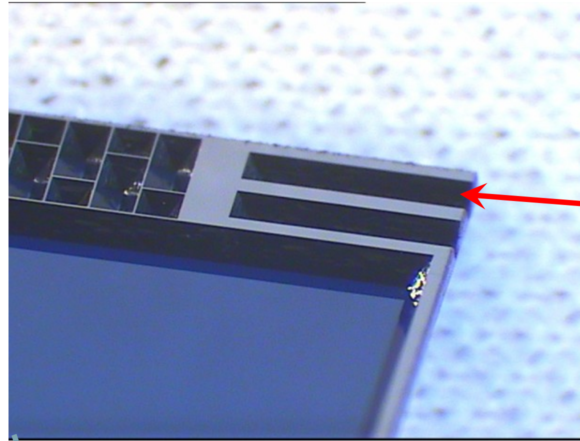
320MHz DCDB frequency = **100ns row read-out time**
S/N=17 – non yet optimal DEPFET voltages

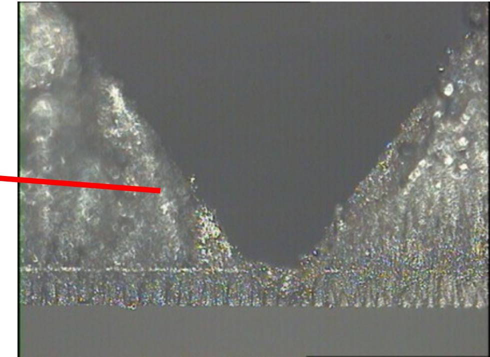
More results on thin DEPFET performance:
see **talk by L.Andricek on Monday at 14:40**

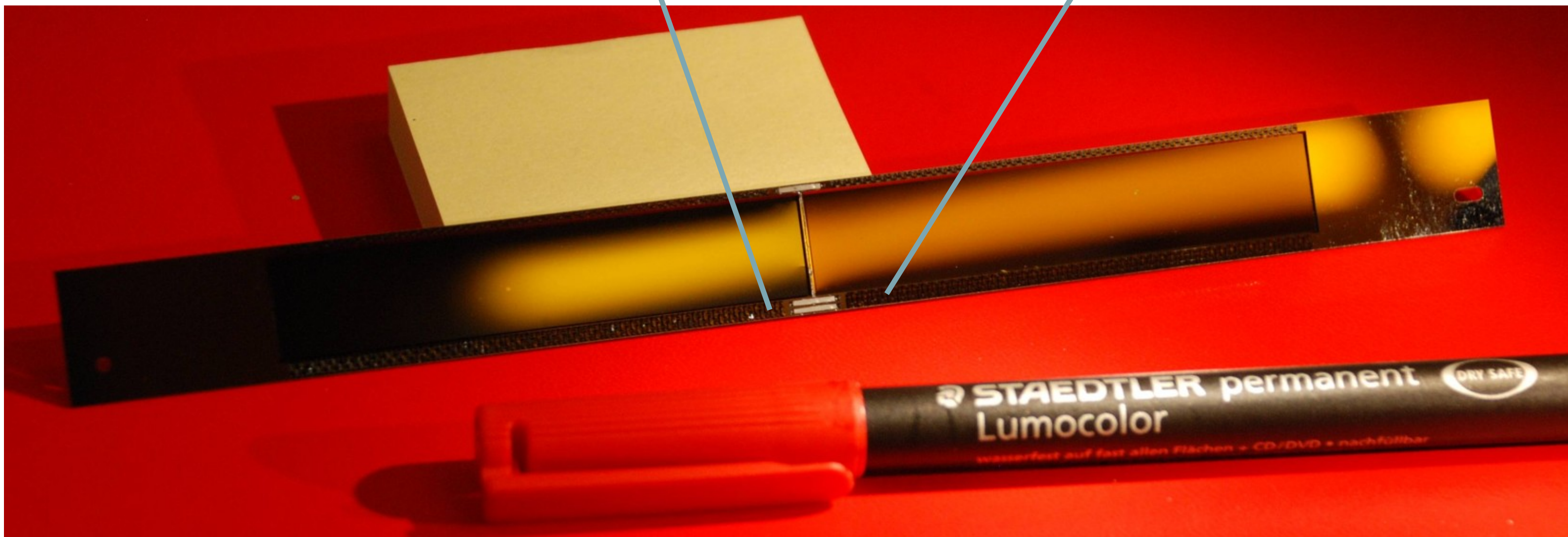


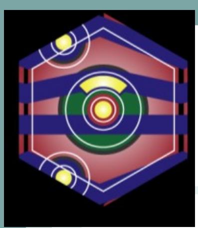
Micro joint between half-ladders

- -butt joint between two half-ladders
- -reinforced with 3 triangular ceramic inserts at the frame
- -about 2x300µm dead area per ladder



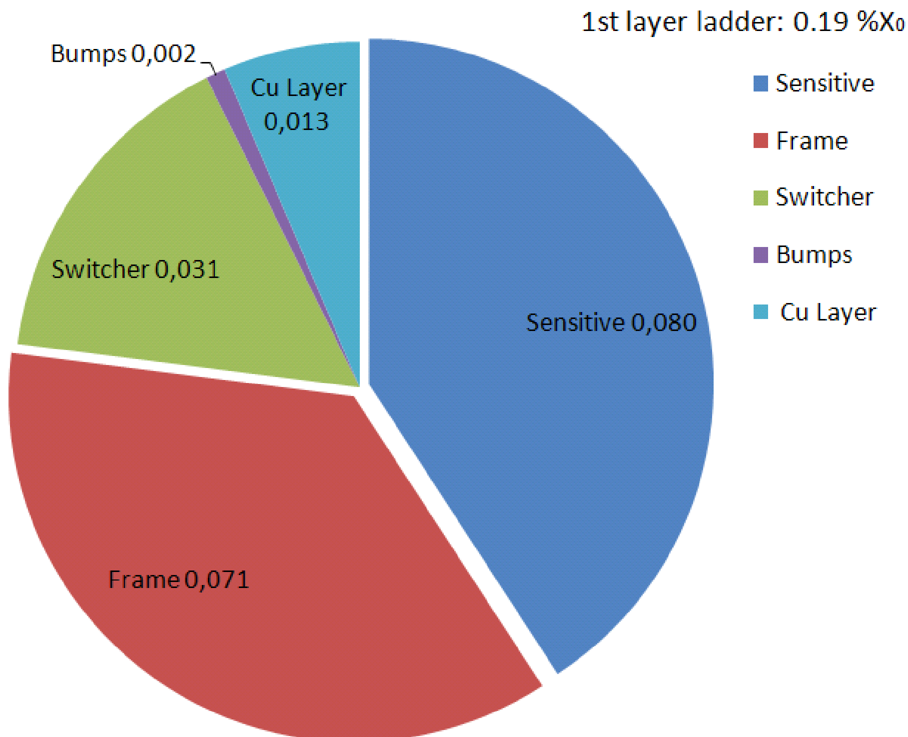






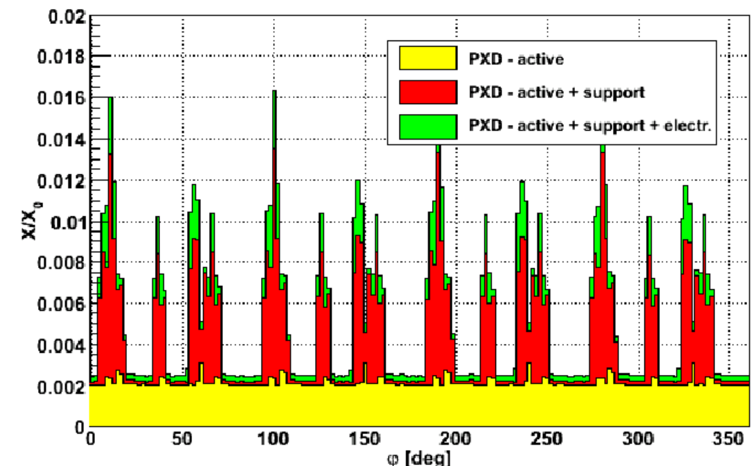
Total Material Budget within the Sensitive Volume

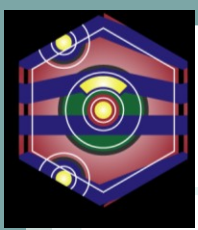
- sensitive area of the first layer ladder: 1.25x9.0 cm^2 (1.5x9.0 incl. frame), 75 µm thin
- support frame: 0.1+0.2 cm, 420 µm
- Switcher-Sensor Interconnect: Gold stud bumps, one bump/connection, Φ=48 µm
- Cu Layer t=3 µm, 50% coverage in acceptance
- Switcher dimensions: 0.15x0.36 cm^2
- Number of Switchers: 12 (32x2 channels per chip – gate and clear)
- Material reduction by frame perforation: 1/3



→ 0.19 $\%X_0$ in total

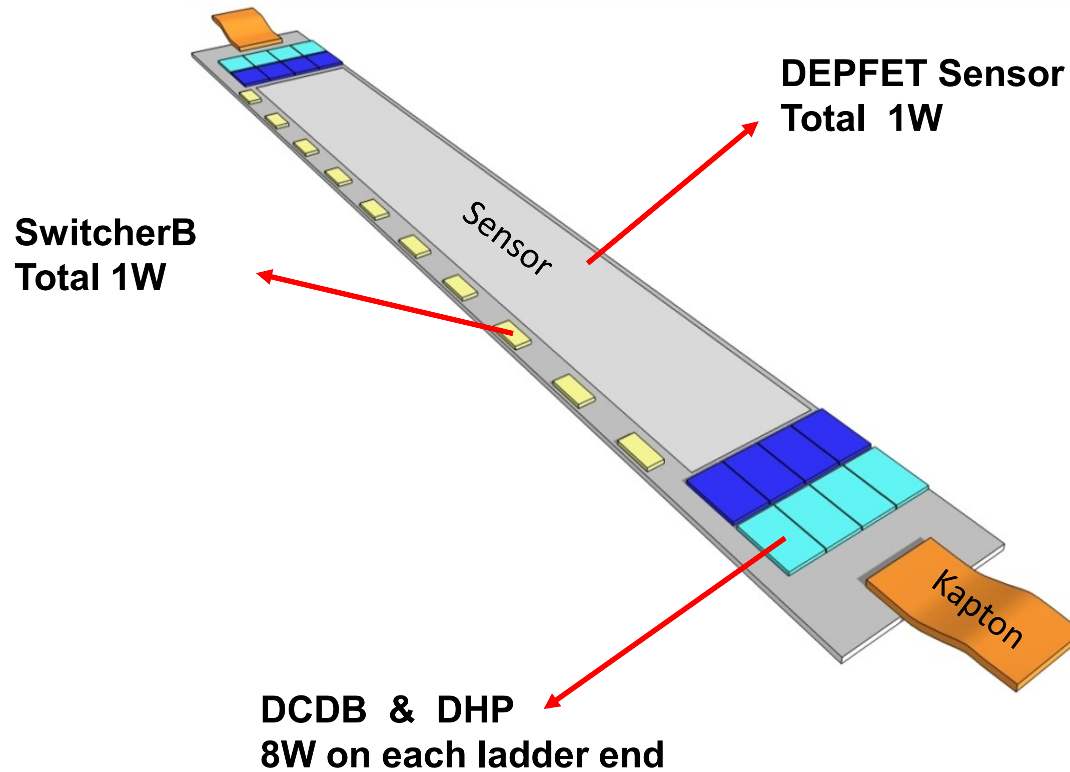
Silicon contribution (0.15%) experimentally confirmed

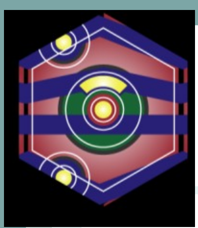




Temperature budget

mpi halbleiterlabor





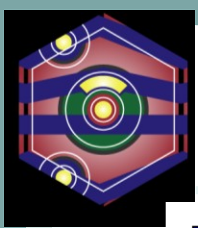
Support & cooling structure

PXD Cooling and support structure

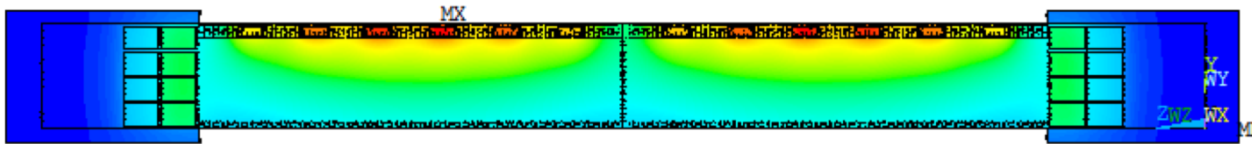
- Stainless steel
- Fast sintering
- Coolant: CO_2

Blue: CO_2 capillaries
Yellow: Air channels

Down to -40ºC in the end of the stave



Support & cooling structure



Temperature distribution along the ladder

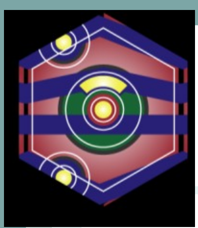
T_{env}=-5ºC
T_{cb}=8ºC

$T_{SENSORmax}$=14ºC
DeltaT=4.7ºC

Carbon fiber capillaries
(Under study!)

Kapton cables

Inner layer ladder

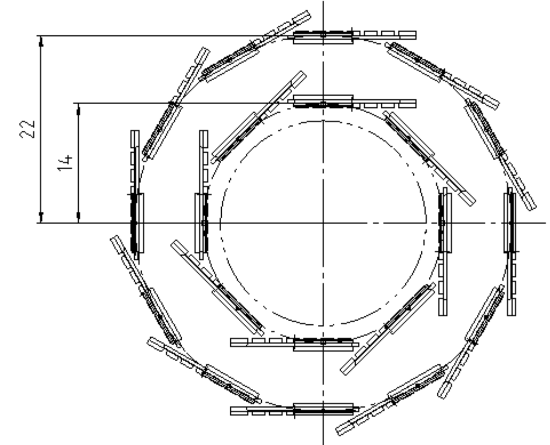


Support & cooling structure

Full PXD

Outer layer

Stress relieves



- The high-precision, low mass DEPFET Pixel Detector (PXD) for Belle II is in the construction phase
  - the first thinned sensor prototypes are currently being tested
  - target read out time of 100ns/row is achieved
  - work packages within the DEPFET collaboration are covering all aspects of PXD (ASICs, mechanical, thermal, DAQ …)

- This project gives a strong push for the DEPFET@future e^+e^- colliders, many techniques developed for Belle II are also applicable at future e^+e^- colliders

I did not talk about:

Radiation tolerance
Auxiliary ASICs
Data acquisition and slow control
…