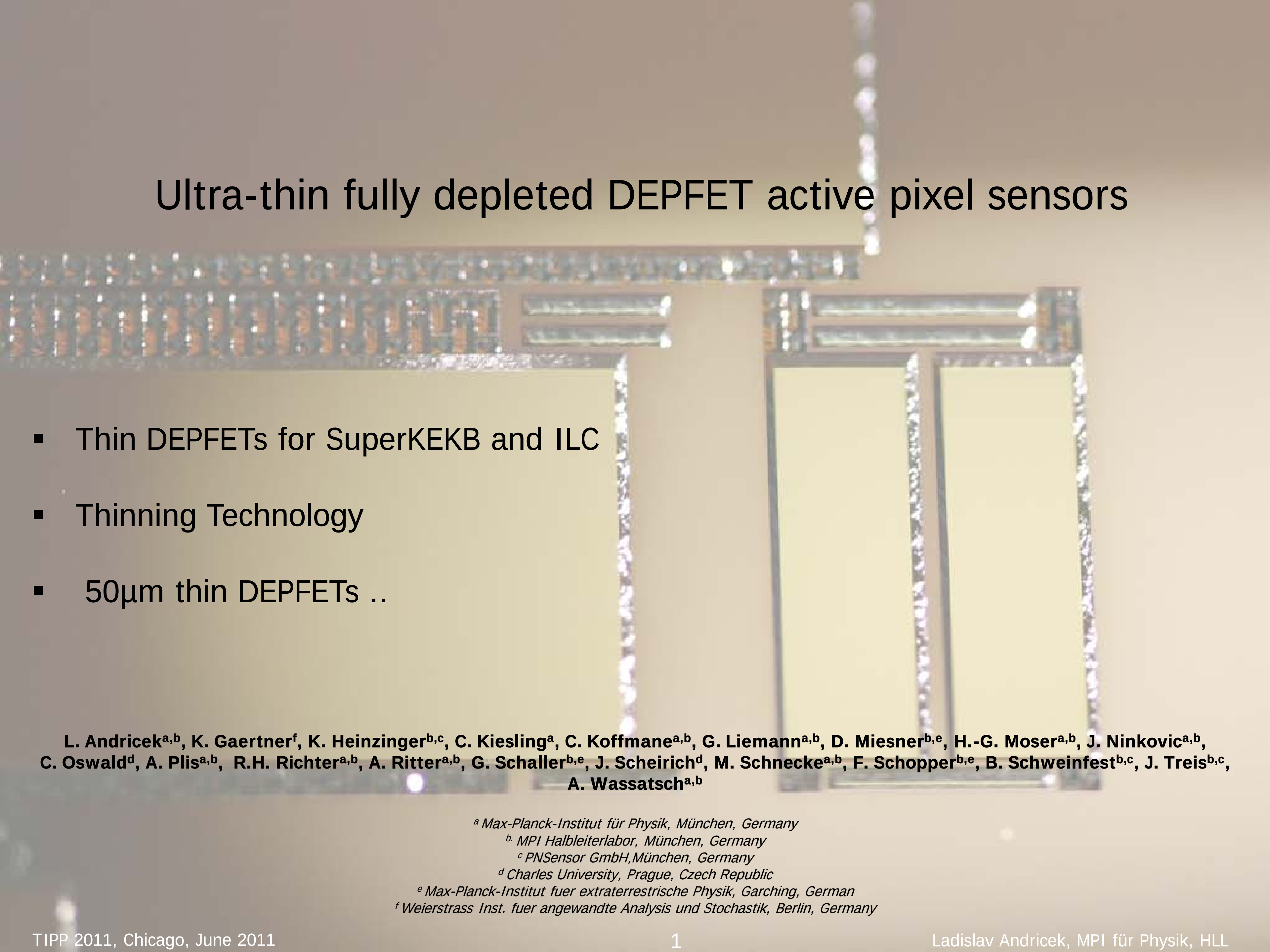


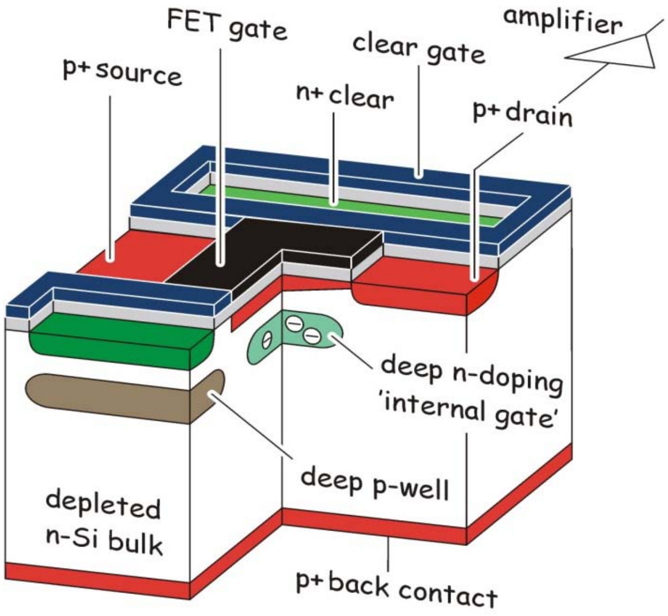
Ultra-thin fully depleted DEPFET active pixel sensors

- Thin DEPFETs for SuperKEKB and ILC
- Thinning Technology
- 50µm thin DEPFETs ..

L. Andricek[a,b], K. Gaertner[f], K. Heinzinger[b,c], C. Kiesling[a], C. Koffmane[a,b], G. Liemann[a,b], D. Miesner[b,e], H.-G. Moser[a,b], J. Ninkovic[a,b], C. Oswald[d], A. Plis[a,b], R.H. Richter[a,b], A. Ritter[a,b], G. Schaller[b,e], J. Scheirich[d], M. Schnecke[a,b], F. Schopper[b,e], B. Schweinfest[b,c], J. Treis[b,c], A. Wassatsch[a,b]

[a] Max-Planck-Institut für Physik, München, Germany
[b.] MPI Halbleiterlabor, München, Germany
[c] PNSensor GmbH,München, Germany
[d] Charles University, Prague, Czech Republic
[e] Max-Planck-Institut fuer extraterrestrische Physik, Garching, German
[f] Weierstrass Inst. fuer angewandte Analysis und Stochastik, Berlin, Germany

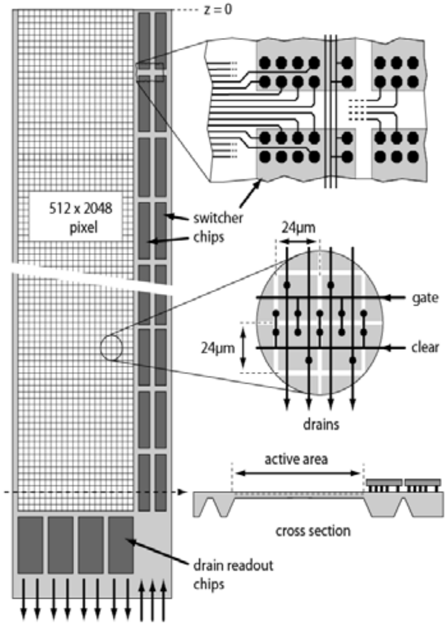
DEPFET in a nutshell

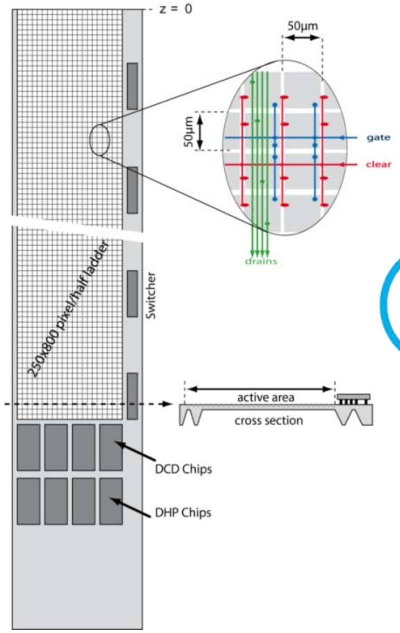


- **fully depleted sensitive volume**
  - fast signal rise time (~ns), small cluster size
  - **double sided processing**
- Fabrication at MPI HLL
  - Wafer scale devices possible
  - no stitching, 100% fill factor
- no charge transfer needed
  - faster read out
  - better radiation tolerance
- Charge collection in "off" state, read out on demand
  - potentially low power device
- **internal amplification**
  - charge-to-current conversion
  - **r/o cap. independent of sensor thickness**
  - **Good S/N for thin devices → ~40nA/µm for mip**

→ Thin active pixel sensors for Belle II and future e+e- colliders

ILC VXD vs. SuperKEKB PXD (from a DEPFET point of view)





-: radii: 15, 26, 37, 48, 60 mm .... 14, 22 mm

-: ladder length: 125mm(L0) and 250mm(L1-4) .... 136 mm(L0) and 169mm(L1)

-: sensitive width: 11mm (L0), 15mm(L1), 22mm(L2-4) 12.5mm (L0, L1)

-: number of ladders: 10/11/12/16/20 → 130 sensors .... 8/12 → 40 sensors

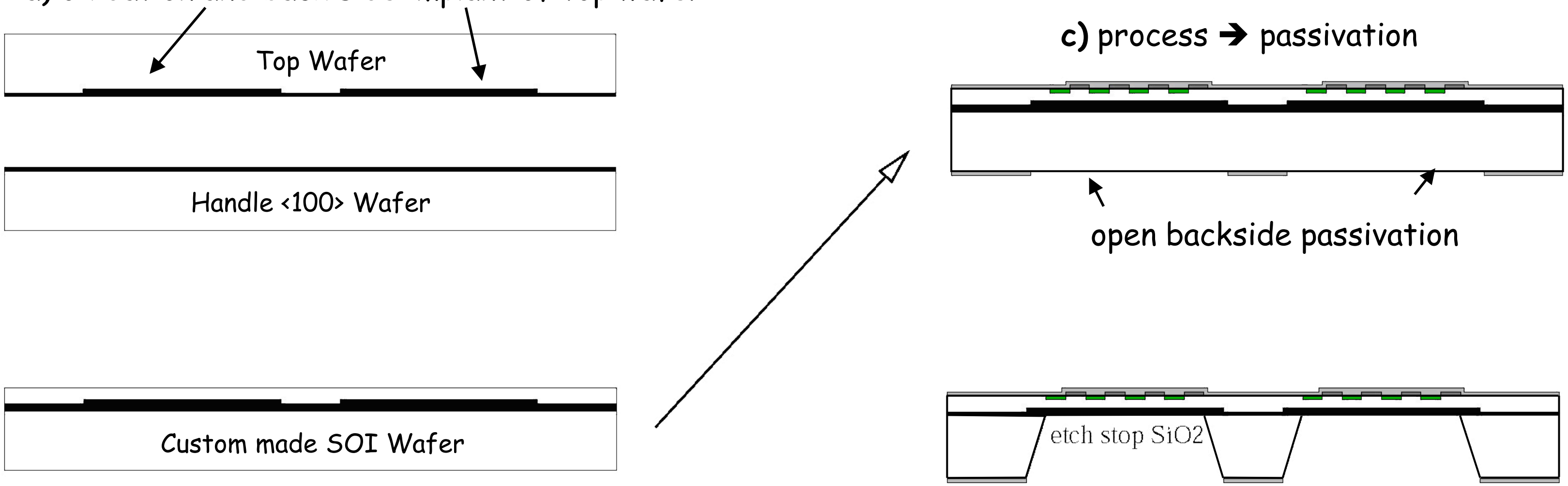
-: pixel size: ≈20 µm .... 50x50 µm^2 (L0) 50x75 µm^2 (L1)

-: Row rate: ≈40 MHz .... ≈10 MHz

-: number of pixels: ≈800 Mpix .... ≈8 Mpix

minimal material for both!!! for sensor and support!!!

Processing thin detectors - the SOI approach


a) oxidation and back side implant of top wafer

b) wafer bonding and grinding/polishing of top wafer

c) process ➔ passivation

open backside passivation

d) anisotropic deep etching opens "windows" in handle wafer

The DEPFET thickness becomes a free parameter, adjustable to the needs of the experiment!

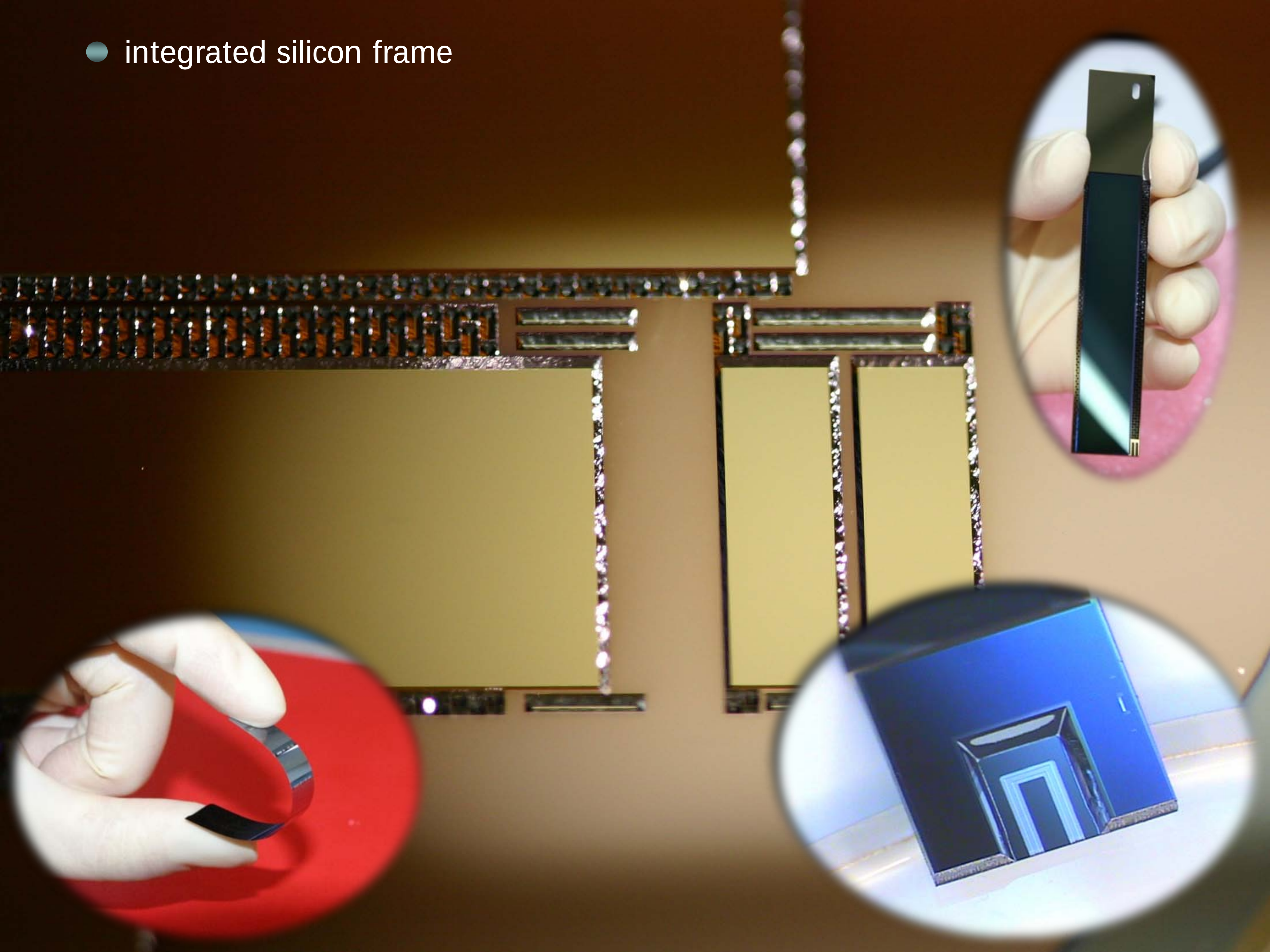
Key Process Modules:

-: Wafer Bonding and thinning of top layer (external)
-: Sensor fabrication on SOI
-: Etching of the Handle Wafer
-: Litho on extreme topographies

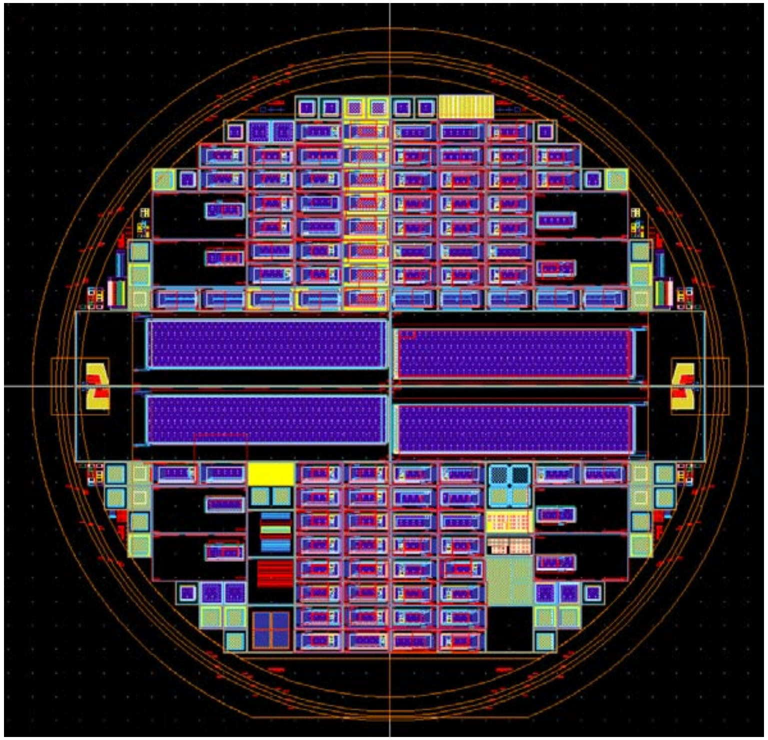
Developed for ILC VXD, the technology found its way into other projects:

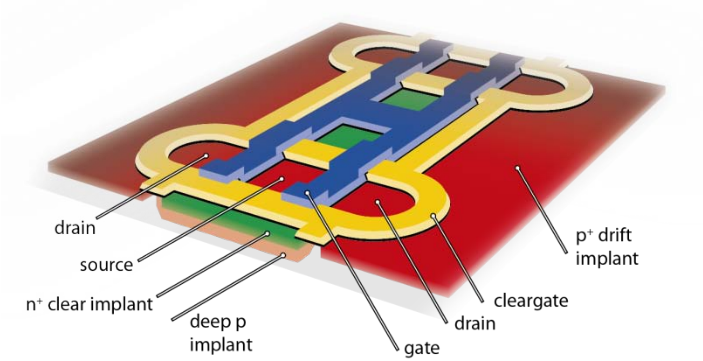
-: 50 µm thin **DEPFETs** for Belle II PXD (will be 75 µm finally)
-: production of thin (75 and 150 µm) **pixel sensors** ATLAS upgrade
-: production of **Geiger-mode APDs (Simpl)** on 70 µm top layer

- integrated silicon frame



PXD6: prototyping for Belle II and ILC

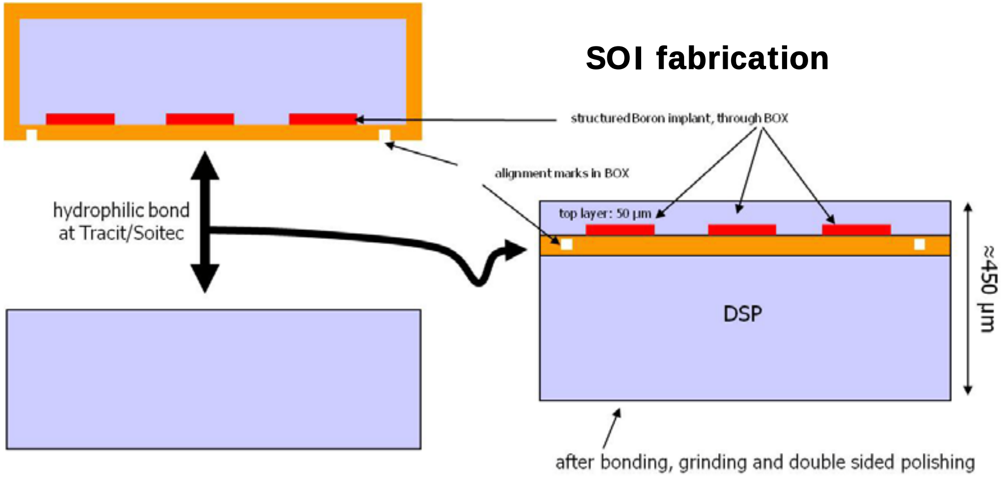




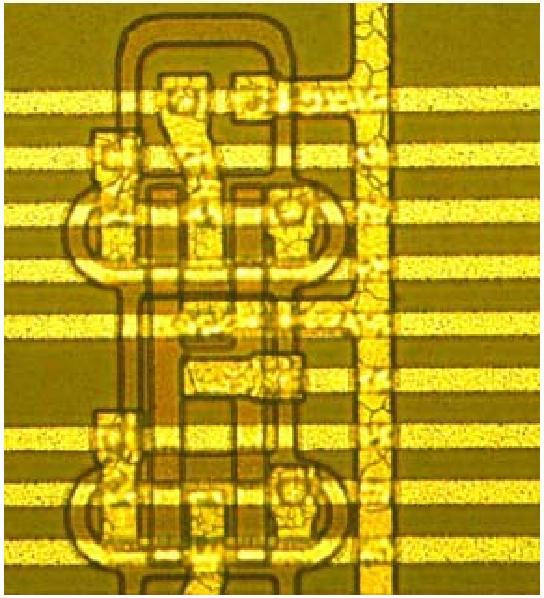
- 8 SOI wafers (50 top layer, 400 µm handle wafer)
  + 2 reference wafers on std. 450µm material
- Pixel design and material (“low res” FZ) adapted to 50 µm top layer thickness (Vfd≈15V), extensive device simulations to find the right geometry for the optimal electric field shape
- About 100 test matrices in different variations
  - pixel sizes from 20 µm to 200 µm
  - shorter gate length,
  - improved clear structures,
  - various field shapes..
- Technology variations on the wafer level
  (new dry etch techniques..)
- 4 half-ladders for Belle II with the most
  promising design options

PXD6: prototyping for Belle II and ILC

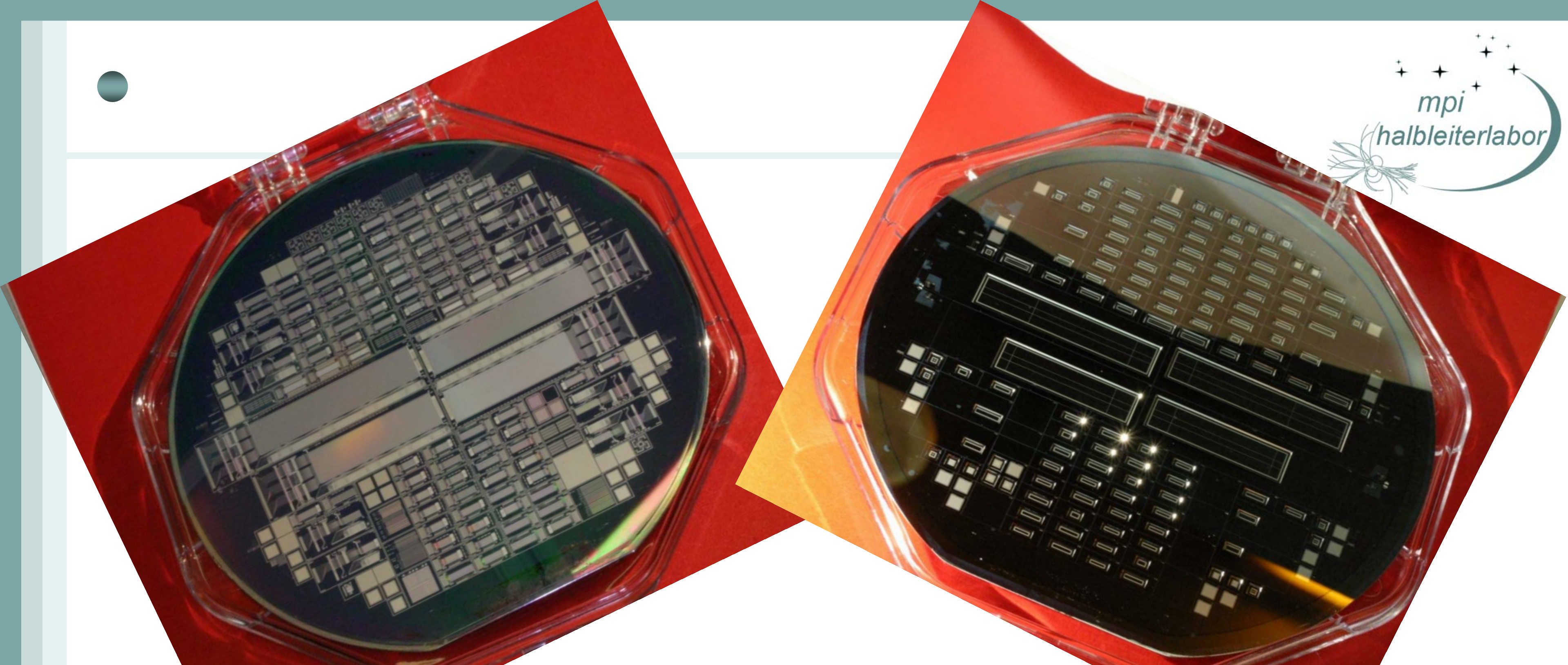
SOI fabrication

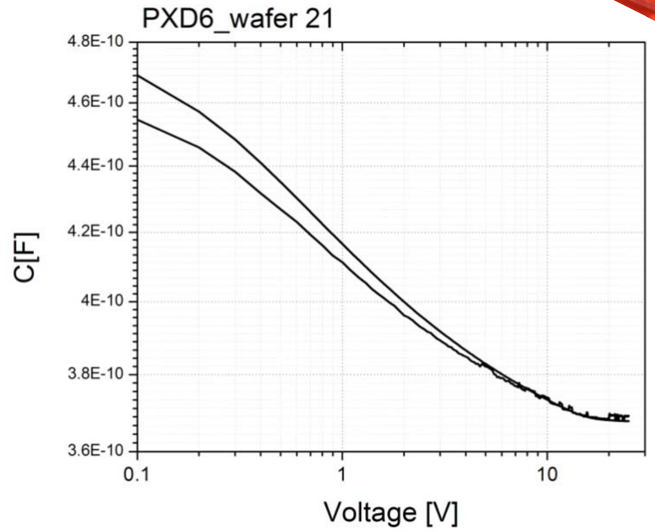


front side processing



- SOI fabrication
- 9 Implantations
- 19 Lithographies
- 2 Poly-layers
- 2 Alu-layers
- back side processing (etching and lithography steps)
- sums up to 89 steps with 1-5 WD each
- in between:
    - a lot of inspection steps!
    - process control, dummy wafer production..





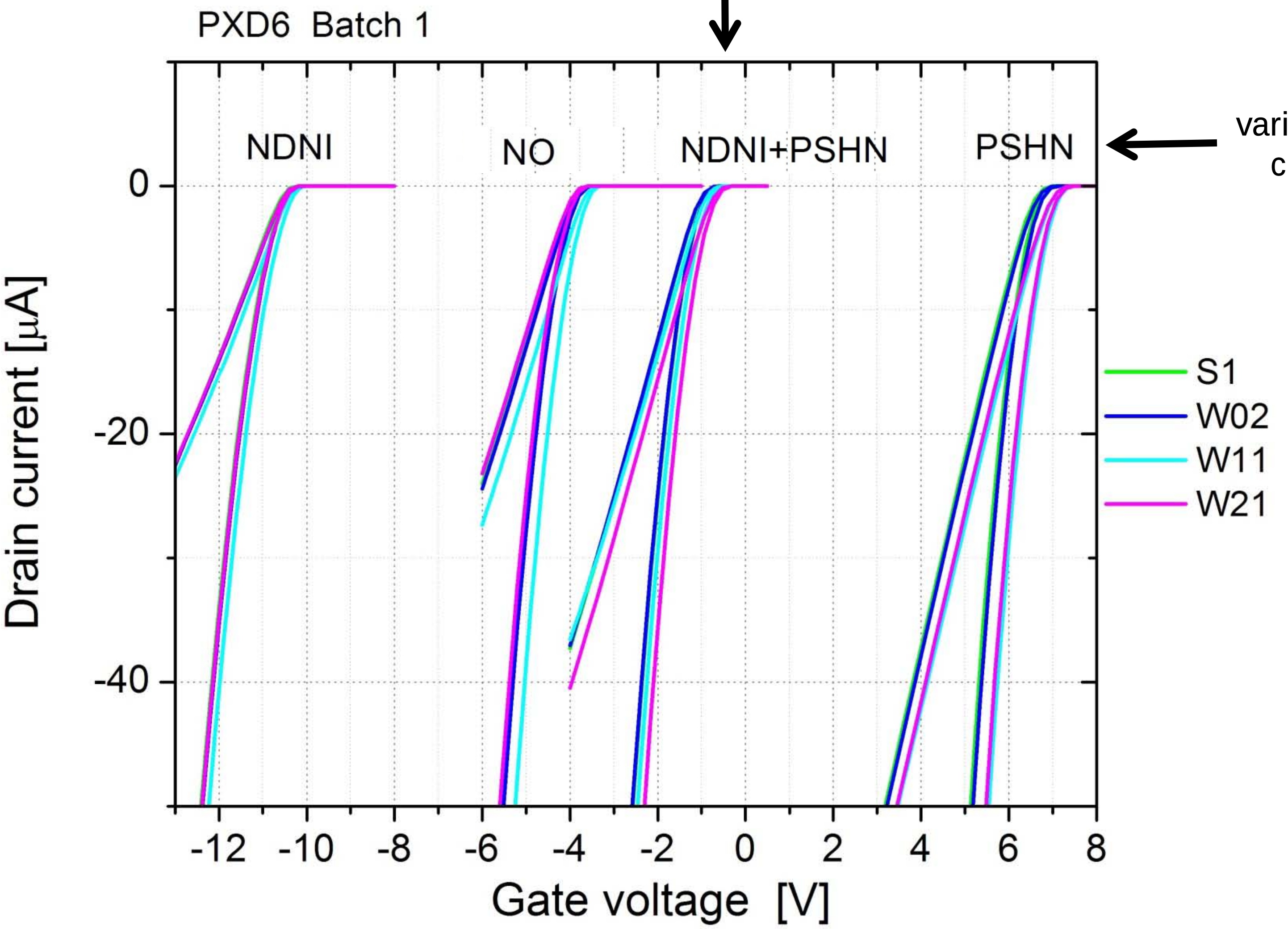
CV measurements:

- ✓ Full depletion as expected 10..15 V
- ✓ from C_{min}: thickness **is** 50 µm ☺

IV measurements: $I_{rev} \approx$ 200 pA/cm^2

DEPFET (and MOSFET) input characteristics → V_{th}

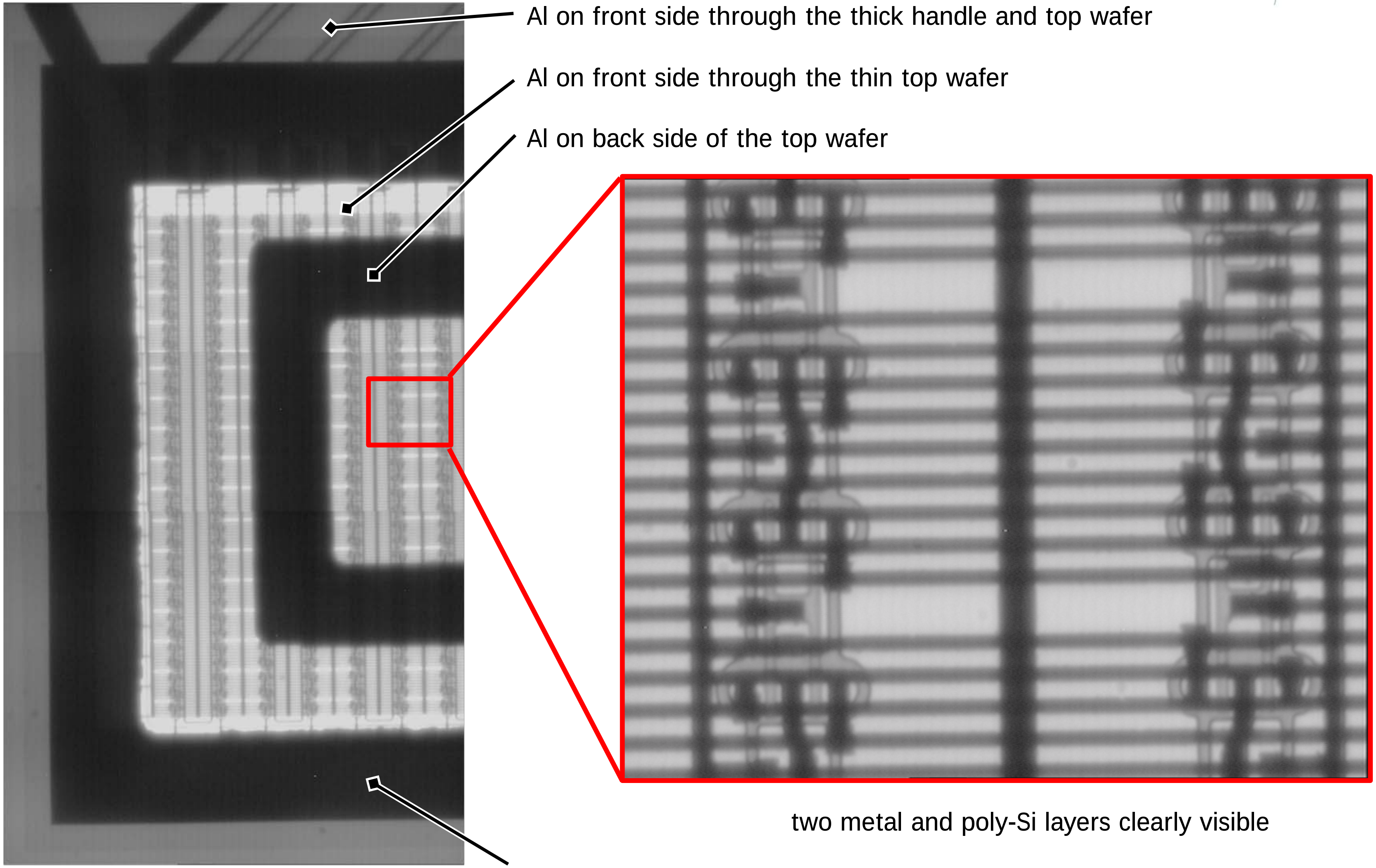
MOSFET with all implants (→ DEPFETs) have as expected a V_{th} ~ 0V



various implants in channel region

thick ref. wafer

IR micrographs



Al on front side through the thick handle and top wafer

Al on front side through the thin top wafer

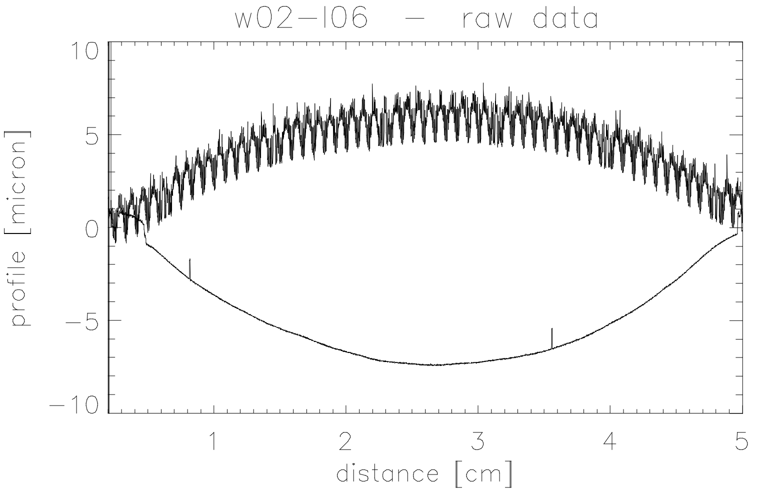
Al on back side of the top wafer

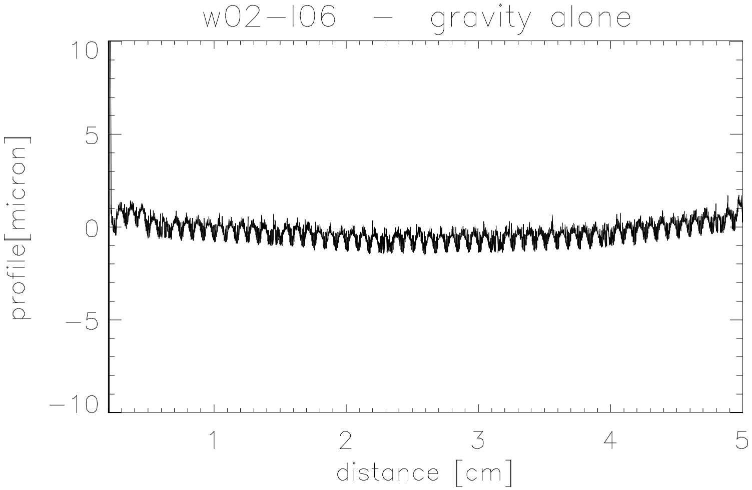
two metal and poly-Si layers clearly visible

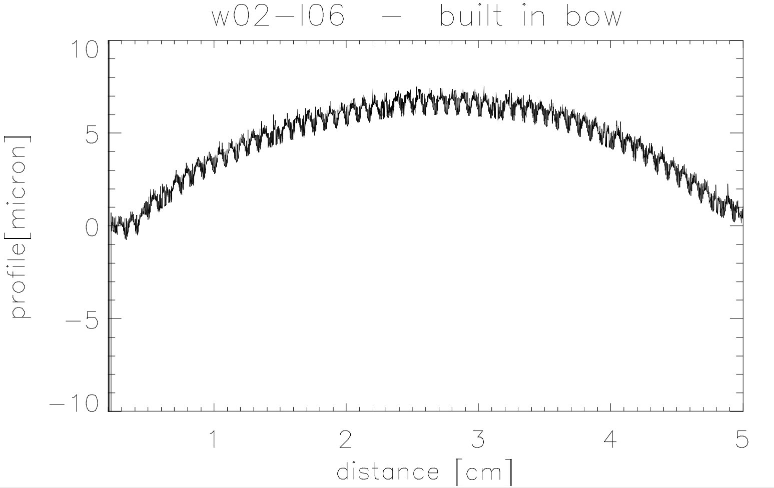
slope of the handle wafer

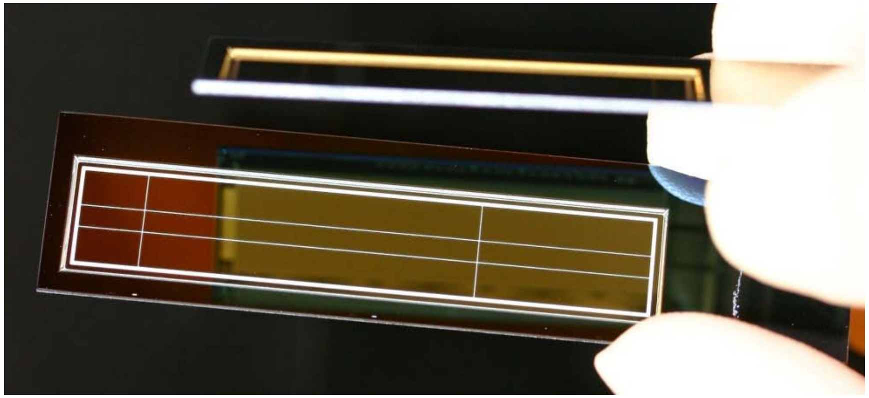
distortions – bow and warp

gravity effect = Δy/2

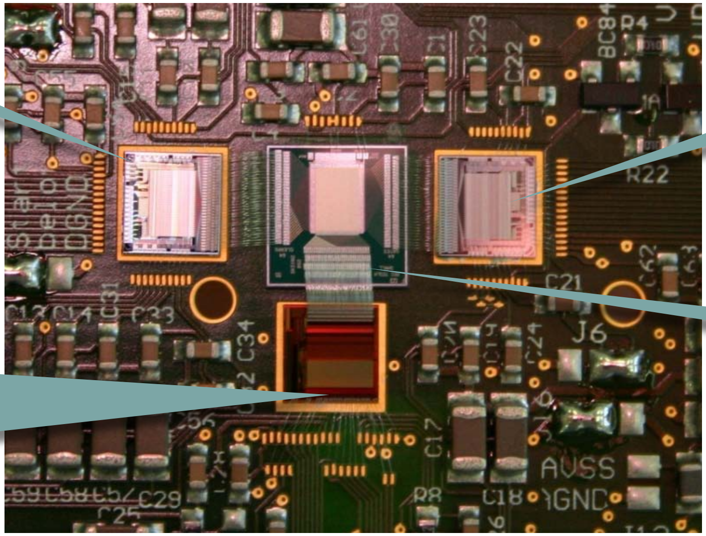








first tests with the well known ILC prototype system

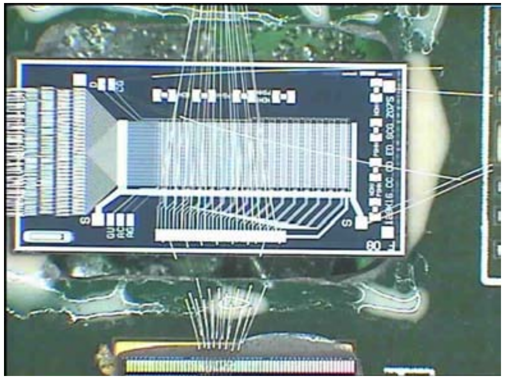


r/o ASIC CURO

- current based readout chip
- 50 MHz band width in the f/e

- our well known work horse since years!
- but with known features resulting in a higher noise

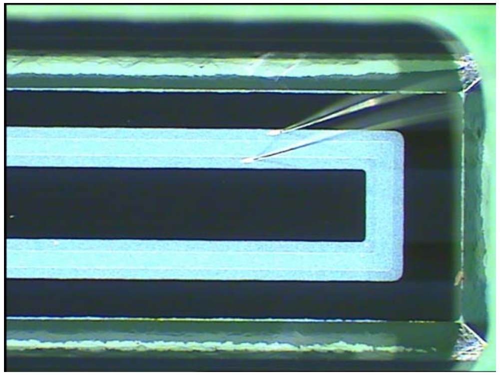
→ layout of the sensor has changed and so did the connections to the read-out system!!



creative bonding on the front

Many thanks to Danilo,
our wire bond expert!!!

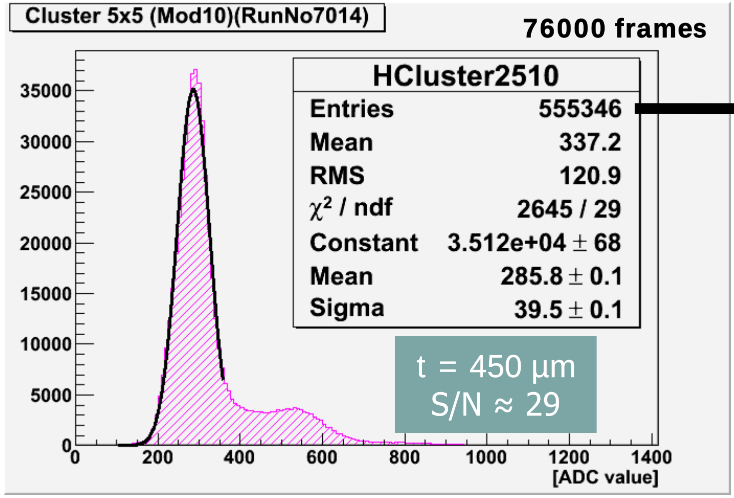
wire bonds on 50 µm Si on the back



latest results with the Belle II read-out system shown on Friday by Jelena Ninkovic

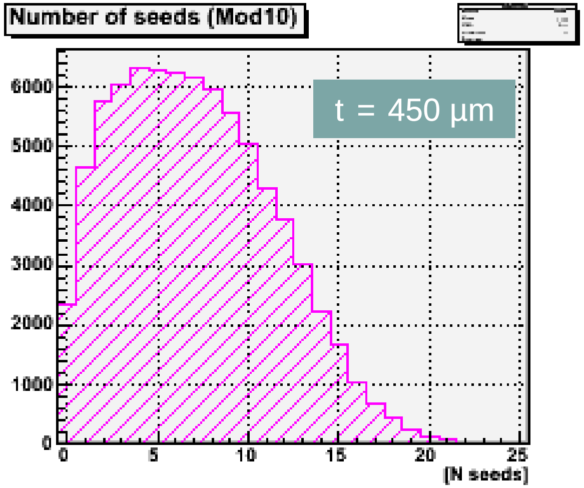
signal measurements I – Cd109

- 2 DUTs: 32x64 pixels Belle II PXD design, L=6 µm, pixel size 50x75 µm^2, same design on front
  - ▷ I : 450 µm standard FZ material
  - ▷ II: 50 µm SOI



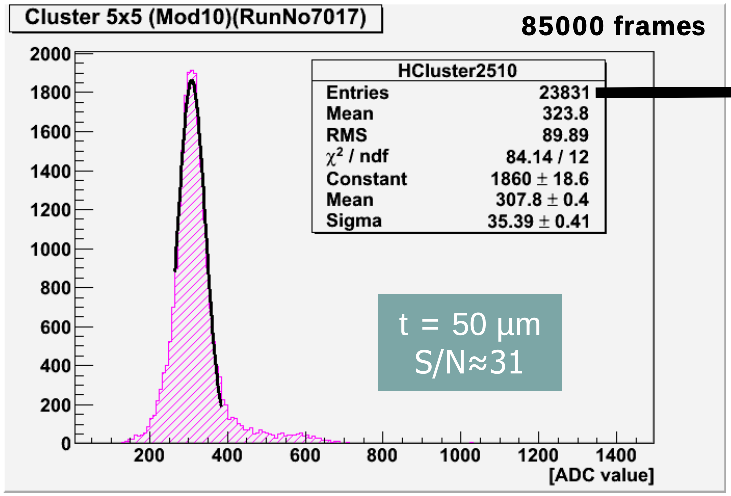
HCluster2510	
Entries	555346
Mean	337.2
RMS	120.9
χ^2 / ndf	2645 / 29
Constant	3.512e+04 ± 68
Mean	285.8 ± 0.1
Sigma	39.5 ± 0.1

Thick: 7 clusters/frame



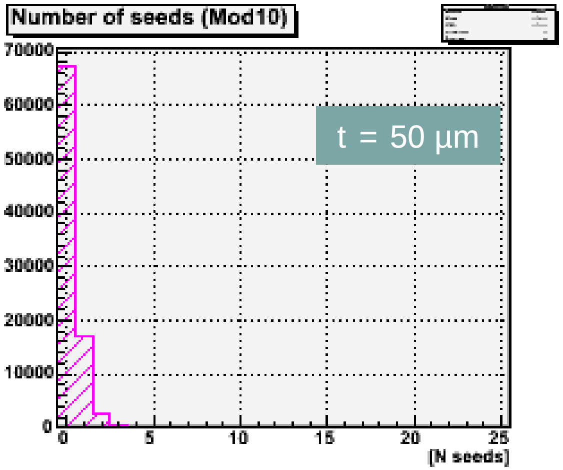
- ▷ 22keV photons
- ▷ ~6000 e/h pairs
- ▷ does not depend on t!

- ▷ but count rate is reduced
- ▷ photons just pass w/o conversion



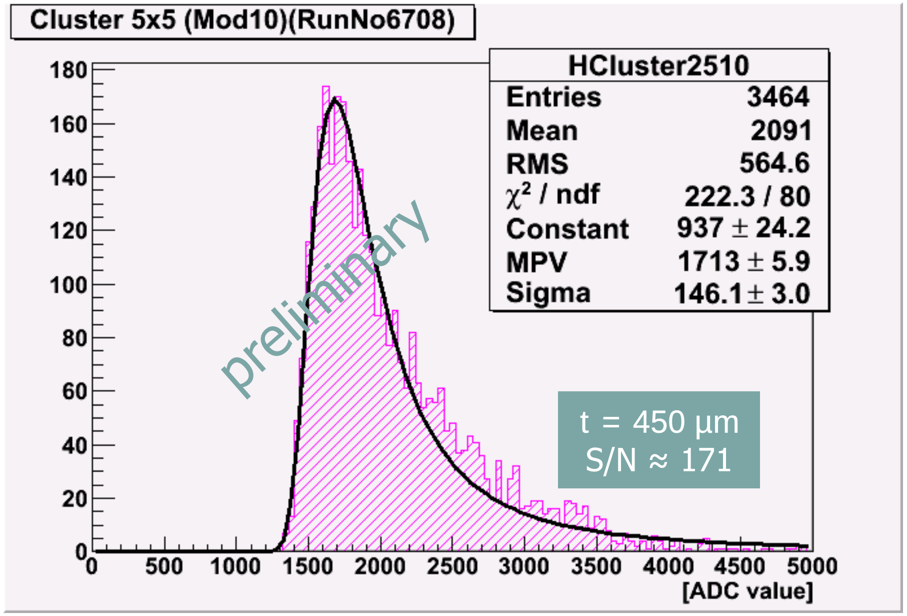
HCluster2510	
Entries	23831
Mean	323.8
RMS	89.89
χ^2 / ndf	84.14 / 12
Constant	1860 ± 18.6
Mean	307.8 ± 0.4
Sigma	35.39 ± 0.41

Thin: 0.28 clusters/frame



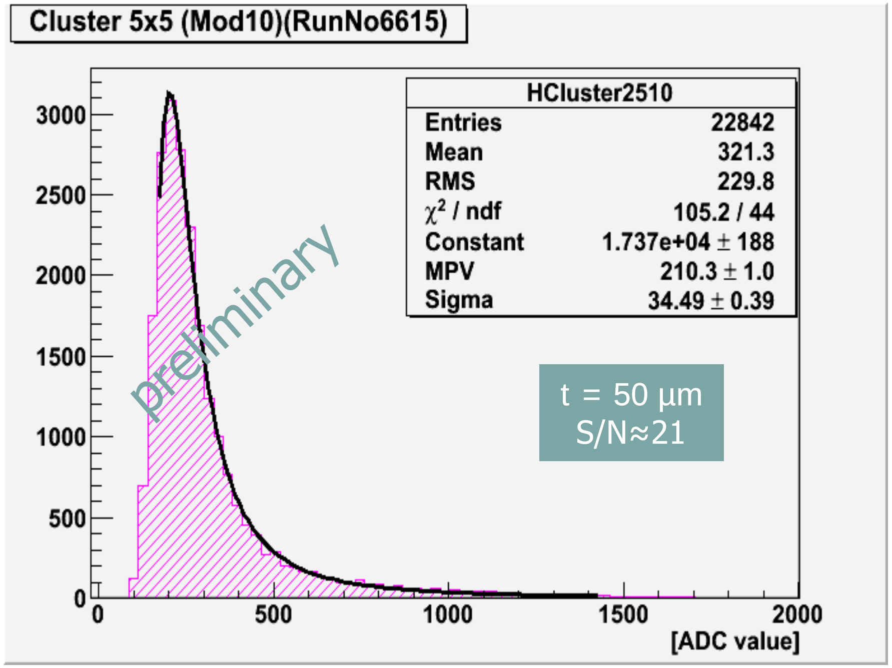
signal measurements II – Sr90

- 2 DUTs: 32x64 pixels Belle II PXD design, L=6 µm, pixel size 50x75 µm^2, same design on front
  - ▷ I : 450 µm standard FZ material
  - ▷ II: 50 µm SOI



t = 450 µm
S/N ≈ 171

- ▷ β source, ~2MeV end energy, close to mip
- ▷ photons and LE e$^-$ blocked by 4.3 mm plastic
- ▷ external scintillator trigger below the sensor



t = 50 µm
S/N≈21

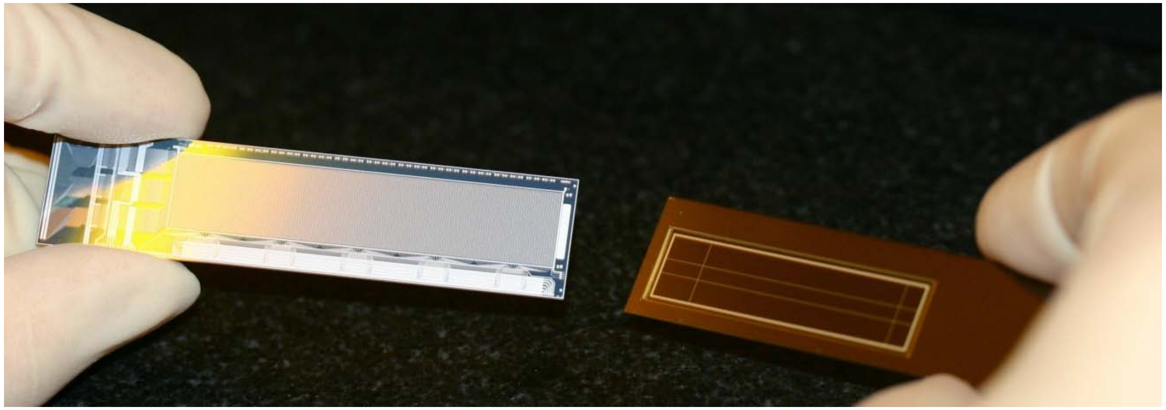
- ▷ from Cd90 we know: 1 ADU → 19.8 e$^-$
- ▷ Sr90 signal with 50µm: 210 ADU → 4164 e$^-$

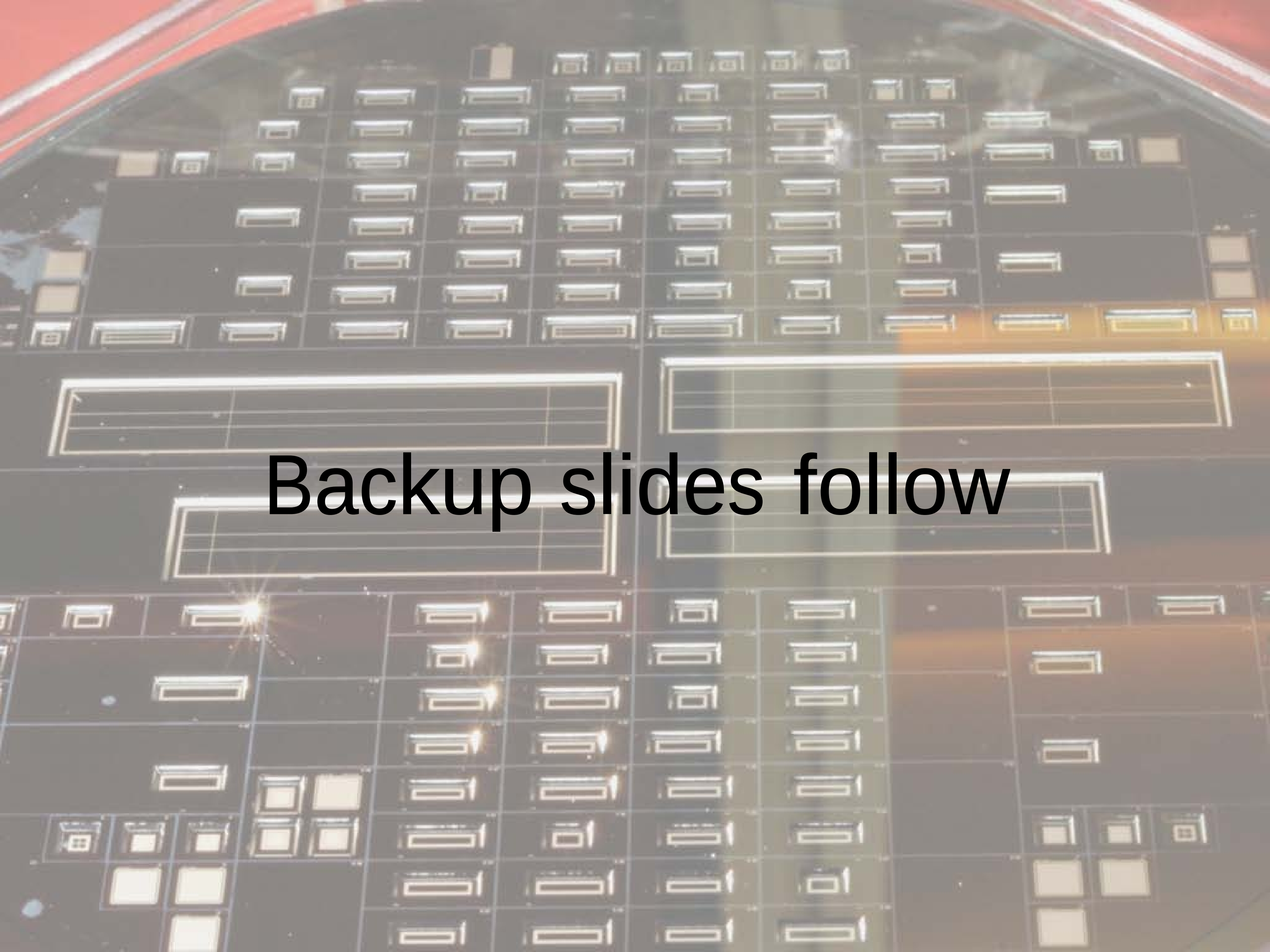
- ▷ expect ~80e-/µm for a mip: ~4000 e$^-$ for 50µm

- ▷ signal(450µm) : signal(50µm): 8.2

Summary

- The thinning technology, developed on mechanical and electrical test vehicles was successfully integrated in the latest DEPFET production run.
- The thickness of the final active area is pre-defined by the thickness of the device layer of SOI the wafers. In this way the final thickness becomes a free parameter adjustable to the requirements of the experiments.
- Although developed for and qualified with DEPFETs, the technology is applicable to all kinds of double side processed fully depleted sensors
- The production of the first thin DEPFETs was a major milestone in the Belle II PXD project.
- First test show that thin DEPFETs have the expected performance. More tests, in particular beam tests to measure the single point resolution of thin active pixel sensors will follow.

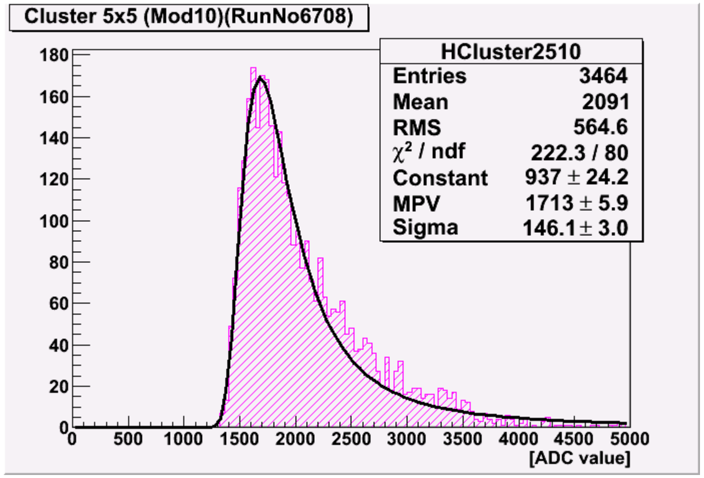




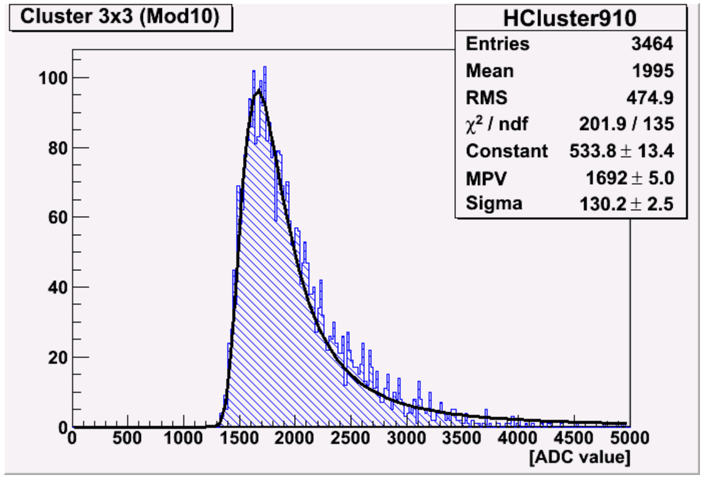
Backup slides follow

H 3.0.21 450μm thick DEPFET matrix & ^{90}Sr

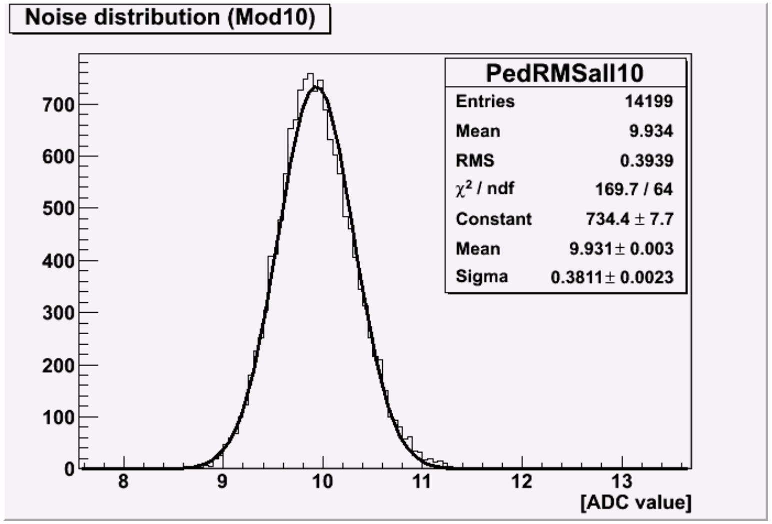
β Source 43mm plastic +extr trigger   cuts seed 800ADU thr 600ADU


Cluster 5x5 (Mod10)(RunNo6708)

HCluster2510	
Entries	3464
Mean	2091
RMS	564.6
χ^2 / ndf	222.3 / 80
Constant	937 ± 24.2
MPV	1713 ± 5.9
Sigma	146.1 ± 3.0


Cluster 3x3 (Mod10)

HCluster910	
Entries	3464
Mean	1995
RMS	474.9
χ^2 / ndf	201.9 / 135
Constant	533.8 ± 13.4
MPV	1692 ± 5.0
Sigma	130.2 ± 2.5


Noise distribution (Mod10)

PedRMSall10	
Entries	14199
Mean	9.934
RMS	0.3939
χ^2 / ndf	169.7 / 64
Constant	734.4 ± 7.7
Mean	9.931 ± 0.003
Sigma	0.3811 ± 0.0023

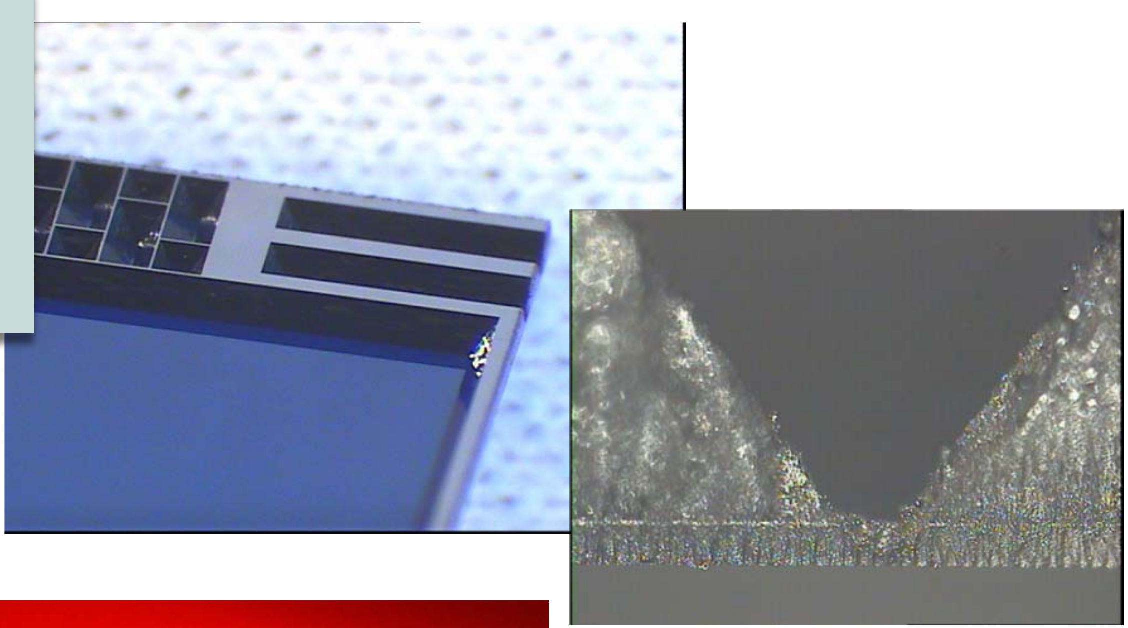
micro joint between half-ladders

- butt-joint between two half-ladders
- reinforced with 3 ceramic inserts
- 2x300µm dead area per ladder

Mechanical tests → remarkably robust!!

Bowing: up to 1mm sagitta (over 10 cm)

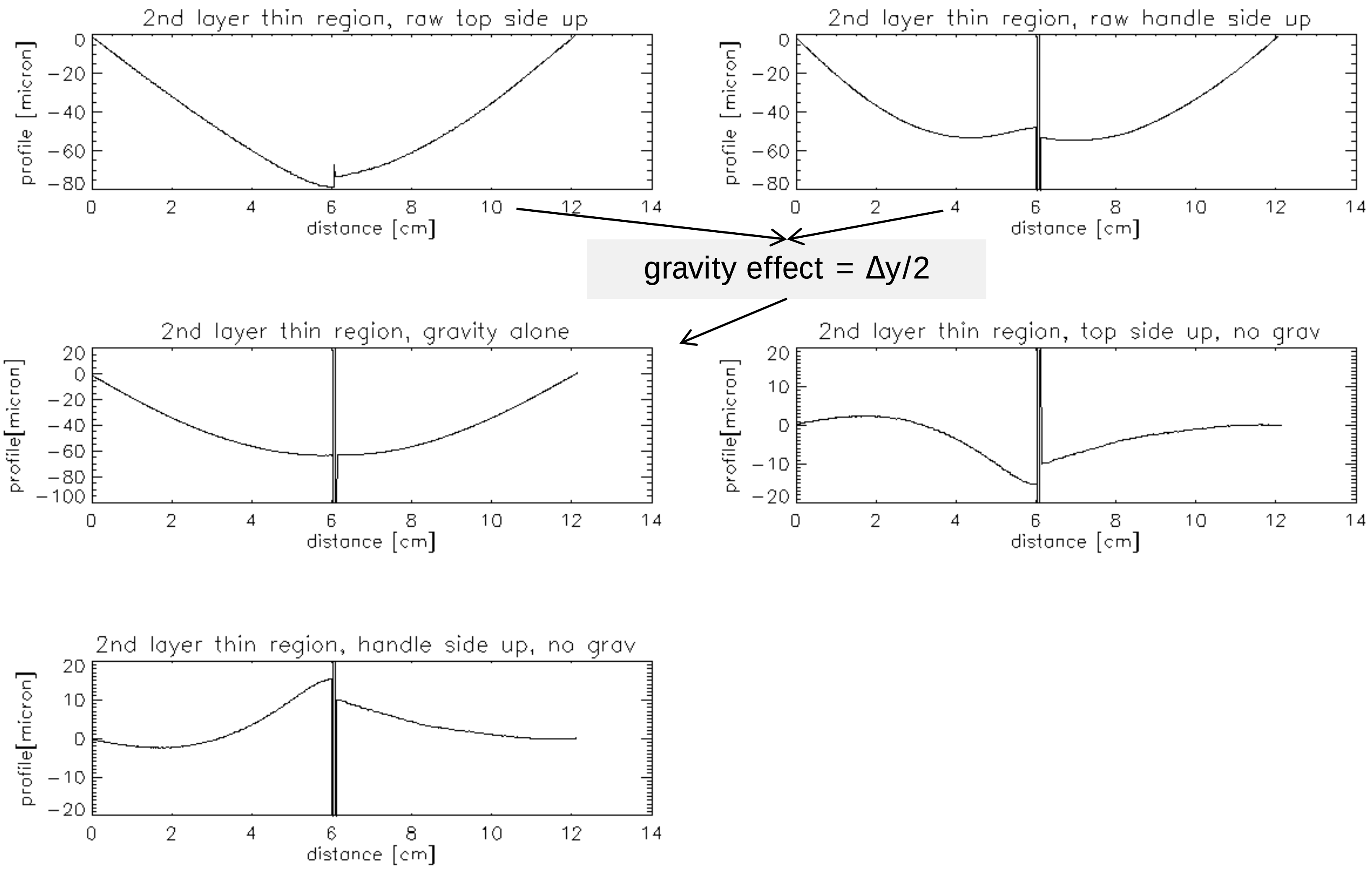
Tension: 40 to 60 N, then the Silicon broke



Thinning procedure and the entire technology qualified in R&D on many mechanical, thermal, and electrical samples (diodes, MOS).

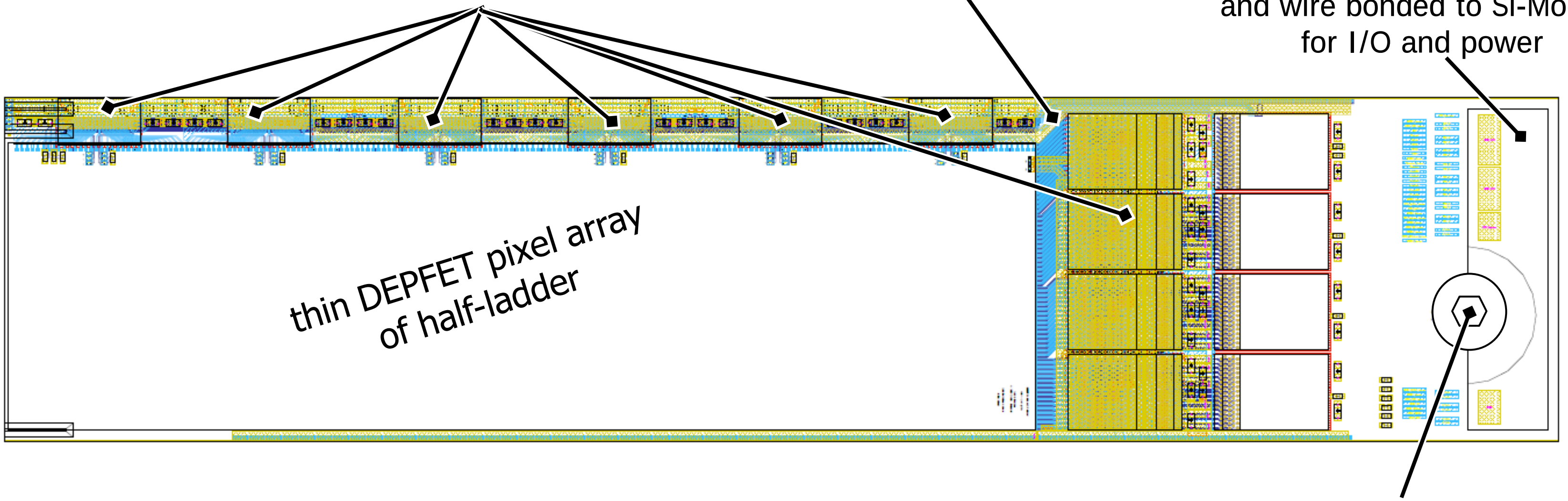
→ ready for a real run!

Micro joint between half-ladders



gravity effect = Δy/2

self supporting all-silicon module

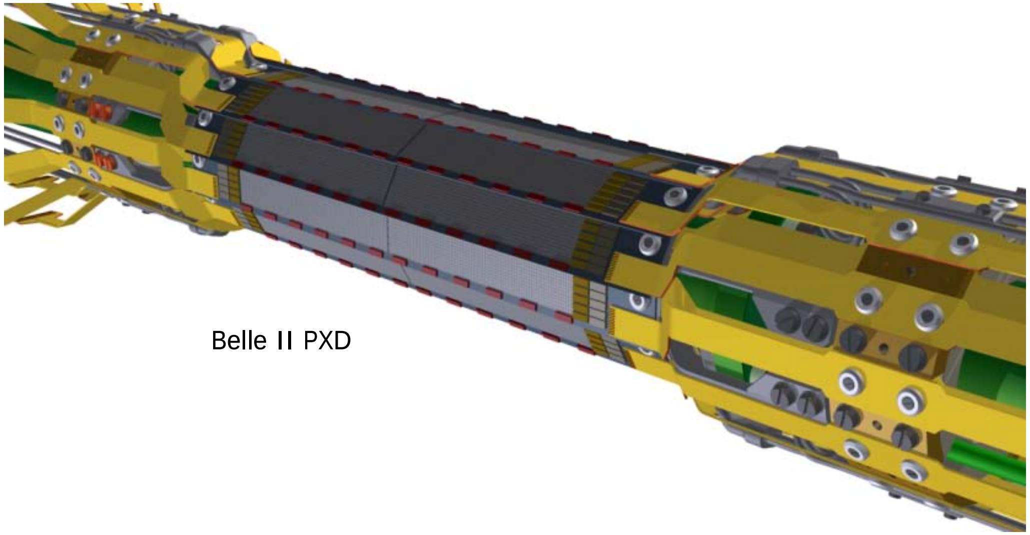


bump bonded steering and r/o ASICs

3 metal layers on periphery

3 layer kapton cable attached
and wire bonded to Si-Module
for I/O and power

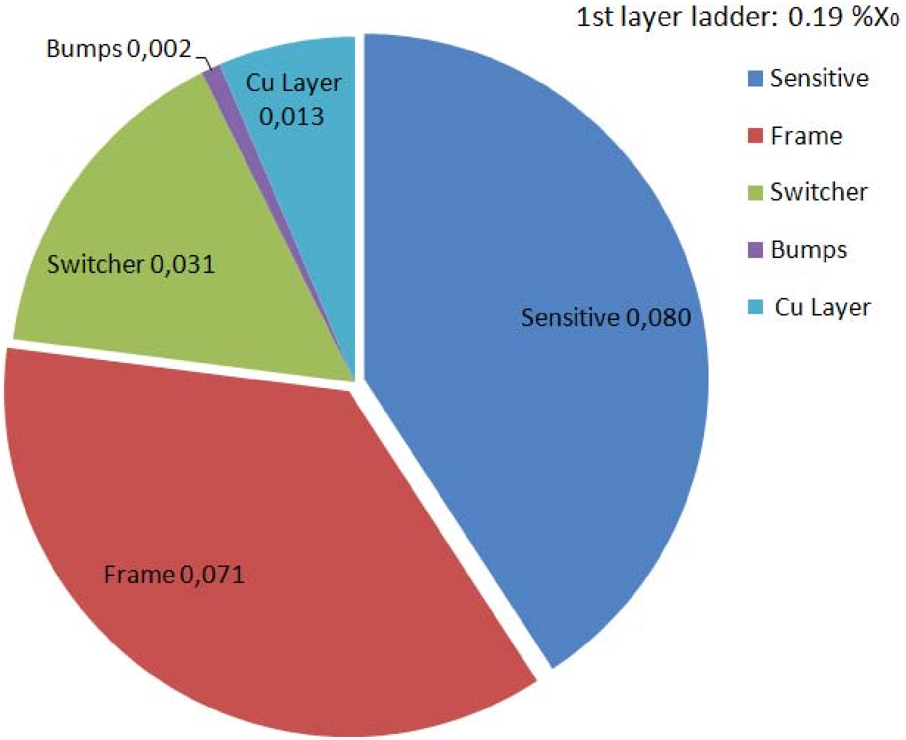
screw through Si
mounting to cooling structure



Belle II PXD

Total Material Budget within the Sensitive Volume (Belle II)

- sensitive area of the first layer ladder: 1.25x9.0 cm^2 (1.5x9.0 incl. frame), 75 µm thin
- support frame: 0.1+0.2 cm, 420 µm
- Switcher-Sensor Interconnect: Gold stud bumps, one bump/connection, Φ=48 µm
- Cu Layer t=3 µm, 50% coverage in acceptance
- Switcher dimensions: 0.15x0.36 cm^2
- Number of Switchers: 12 (32x2 channels per chip – gate and clear)
- Material reduction by frame perforation: 1/3



→ 0.19 %X_0 in total

Silicon contribution (0.15%) experimentally confirmed