SiPMs with bulk integrated resistors – Future perspectives –

- Concept of SiPMs with Bulk Integrated Quench Resistors – SiPMI concept
- First results from the prototype production
- Future perspectives

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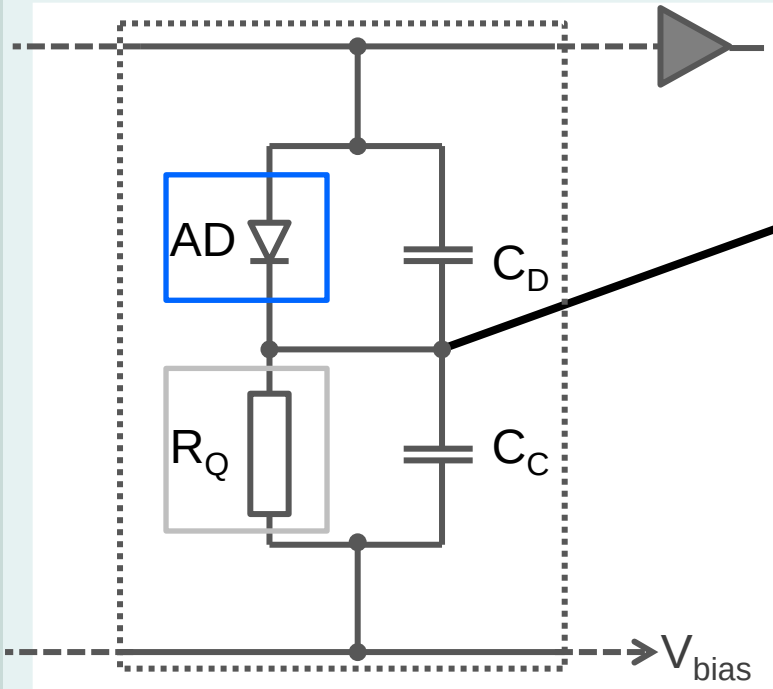
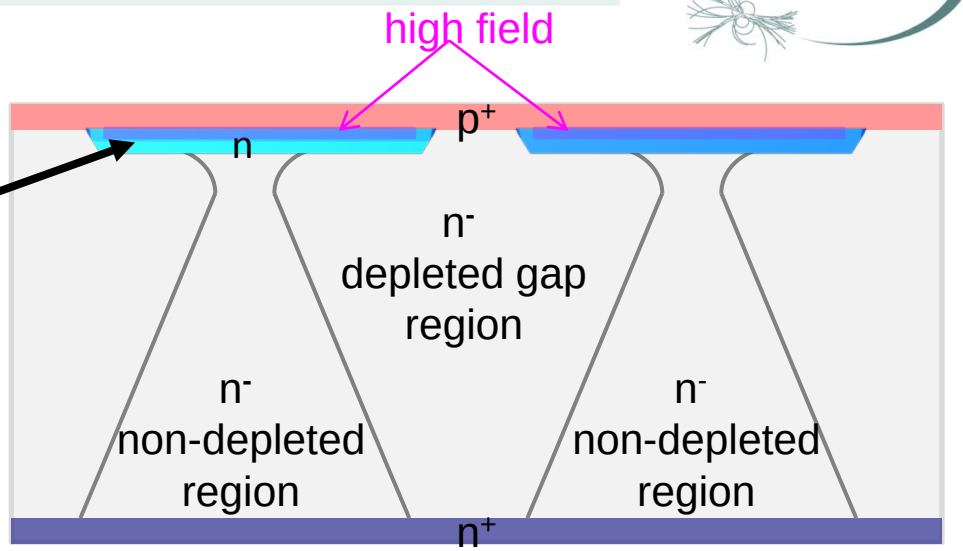
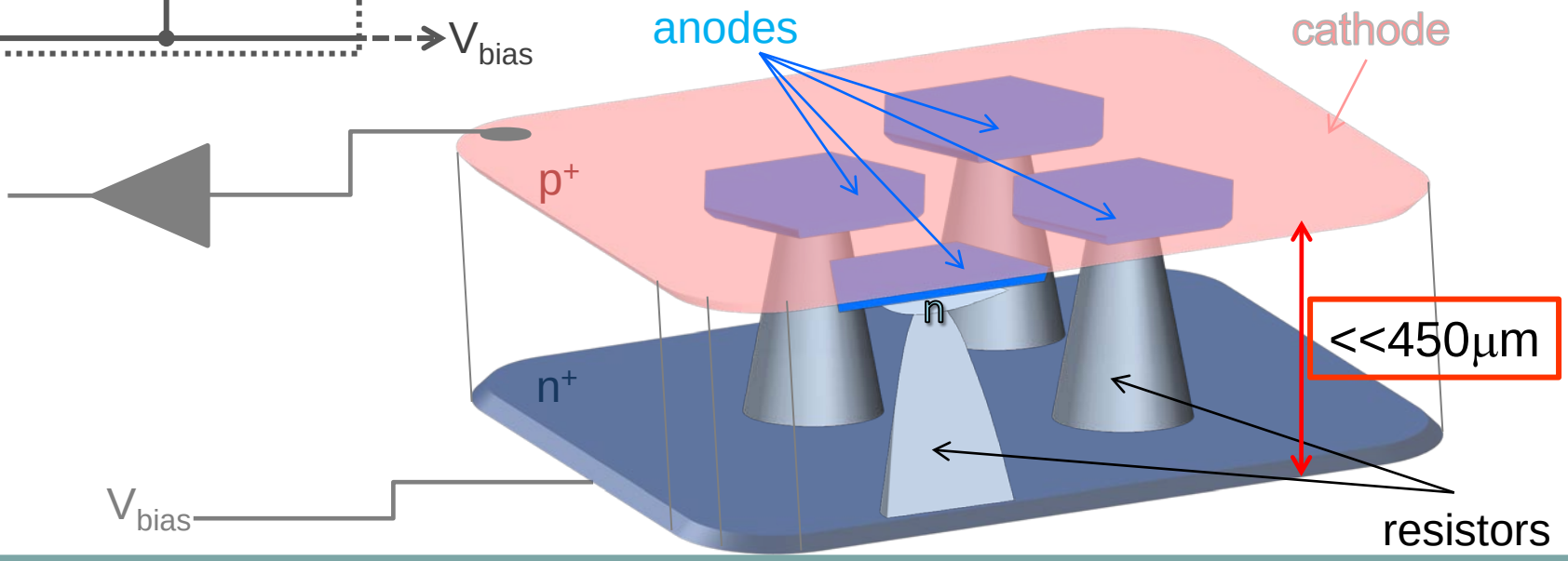
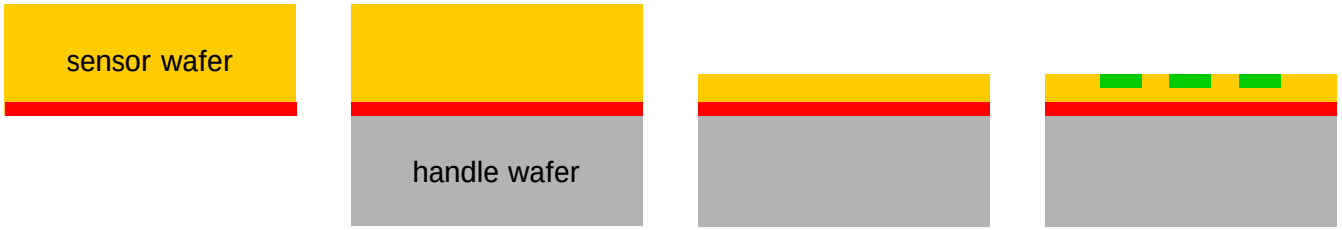
SiPM cell components → SiMPl approach





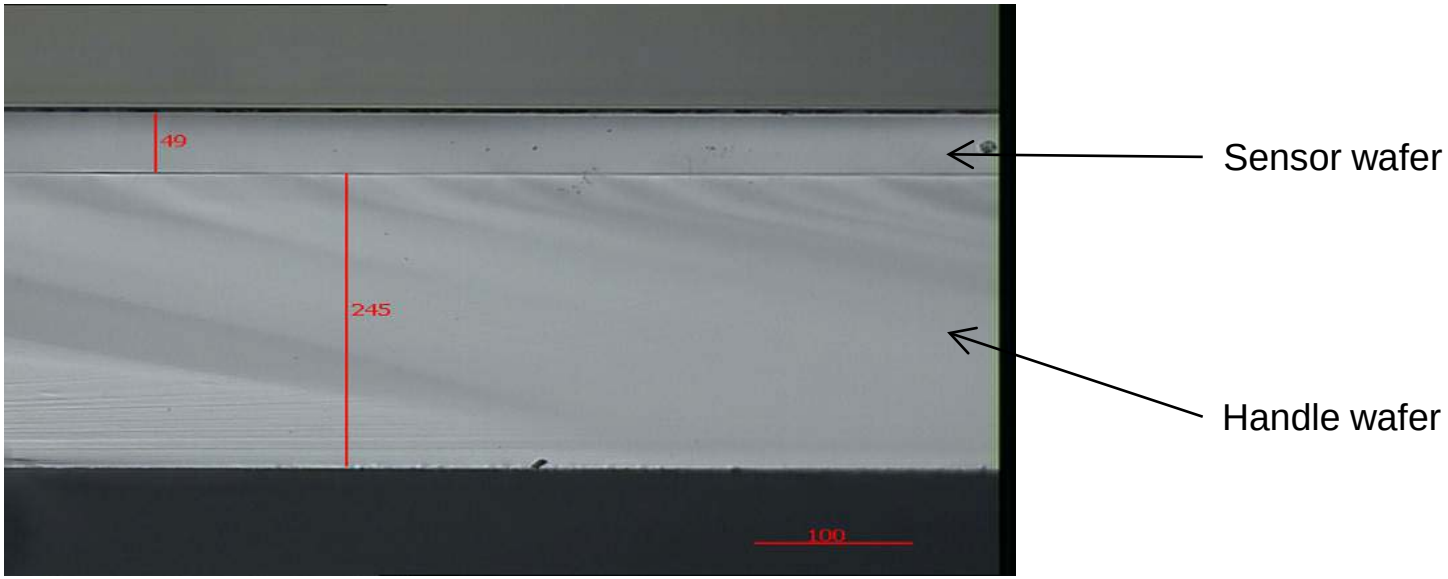


SOI wafers



1. implant backside on sensor wafer
2. bond sensor wafer to handle wafer
3. thin sensor side to desired thickness
4. process SiMPl arrays on top side

Industrial partner → HLL



Advantages and Disadvantages

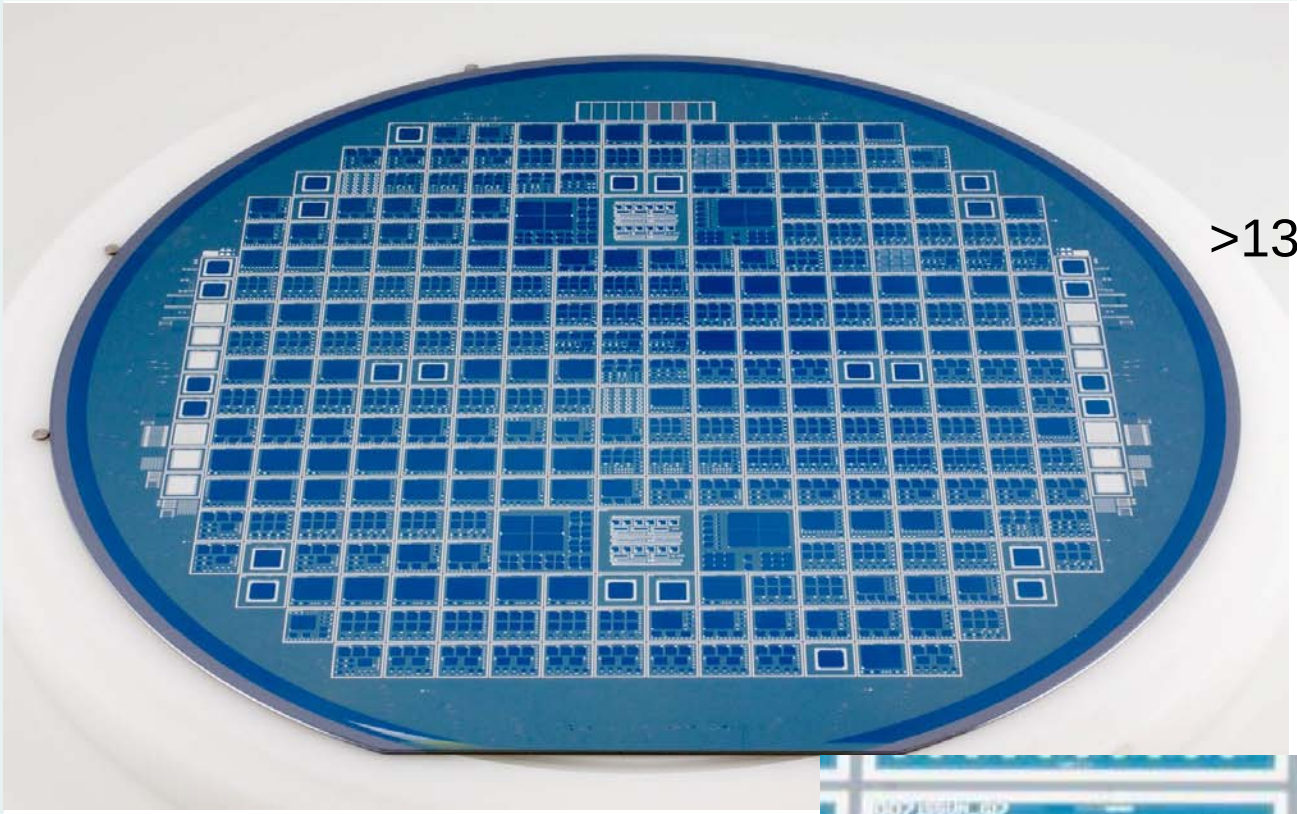
Advantages:

- no need of polysilicon
- free entrance window for light, no metal necessary within the array
- coarse lithographic level
- simple technology
- inherent diffusion barrier against minorities in the bulk -> less optical cross talk

Drawbacks:

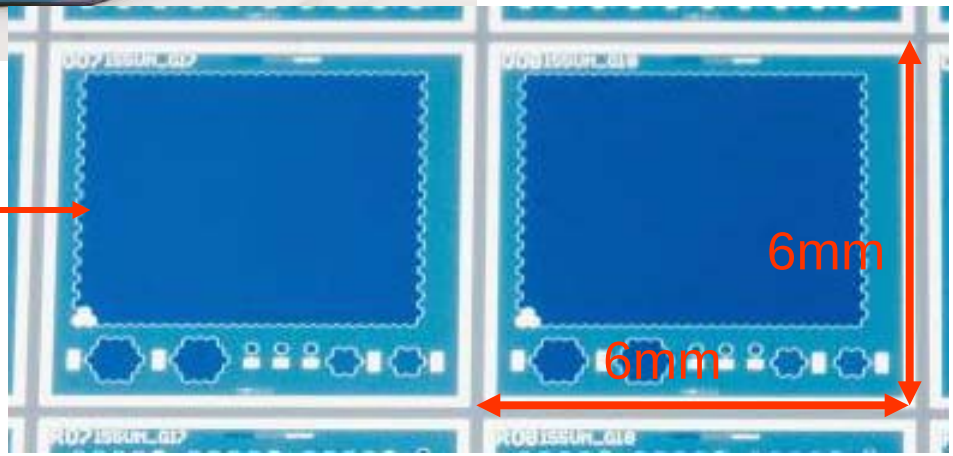
- required depth for vertical resistors does not match wafer thickness
- wafer bonding is necessary for big pixel sizes
- significant changes of cell size requires change of the material
- vertical ‘resistor‘ is a JFET -> parabolic IV -> longer recovery times

Prototype production



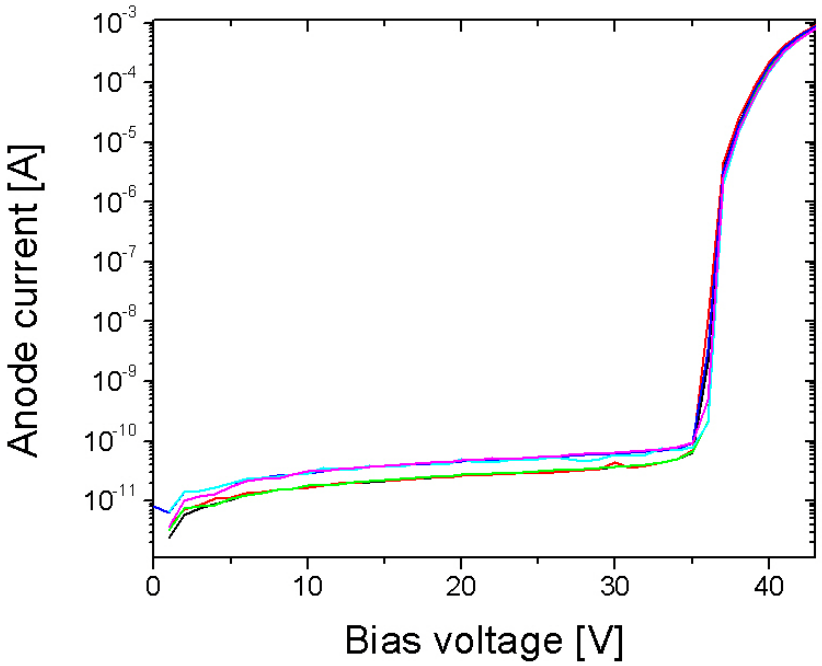
>130 different chips

30x30 array
sensitive area free

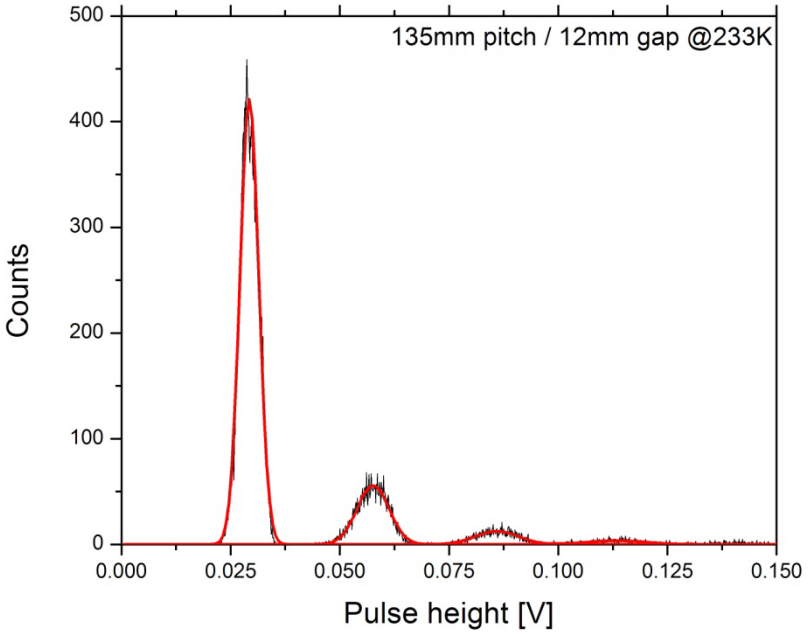


Results

Static measurements



Dynamic measurements

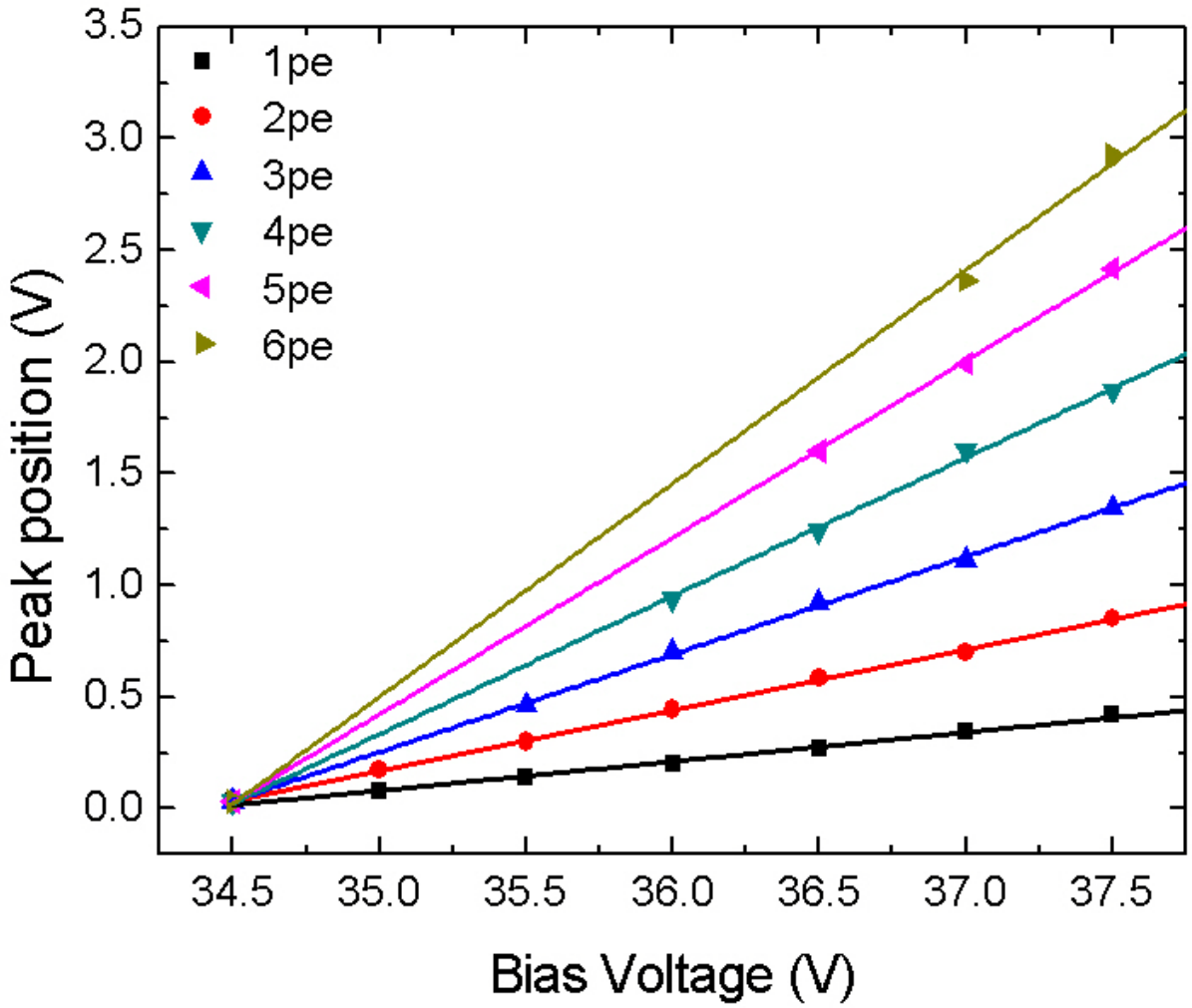


High homogeneity over big distances!
6 (10x10) arrays placed over
6mm distance

High homogeneity within the array!

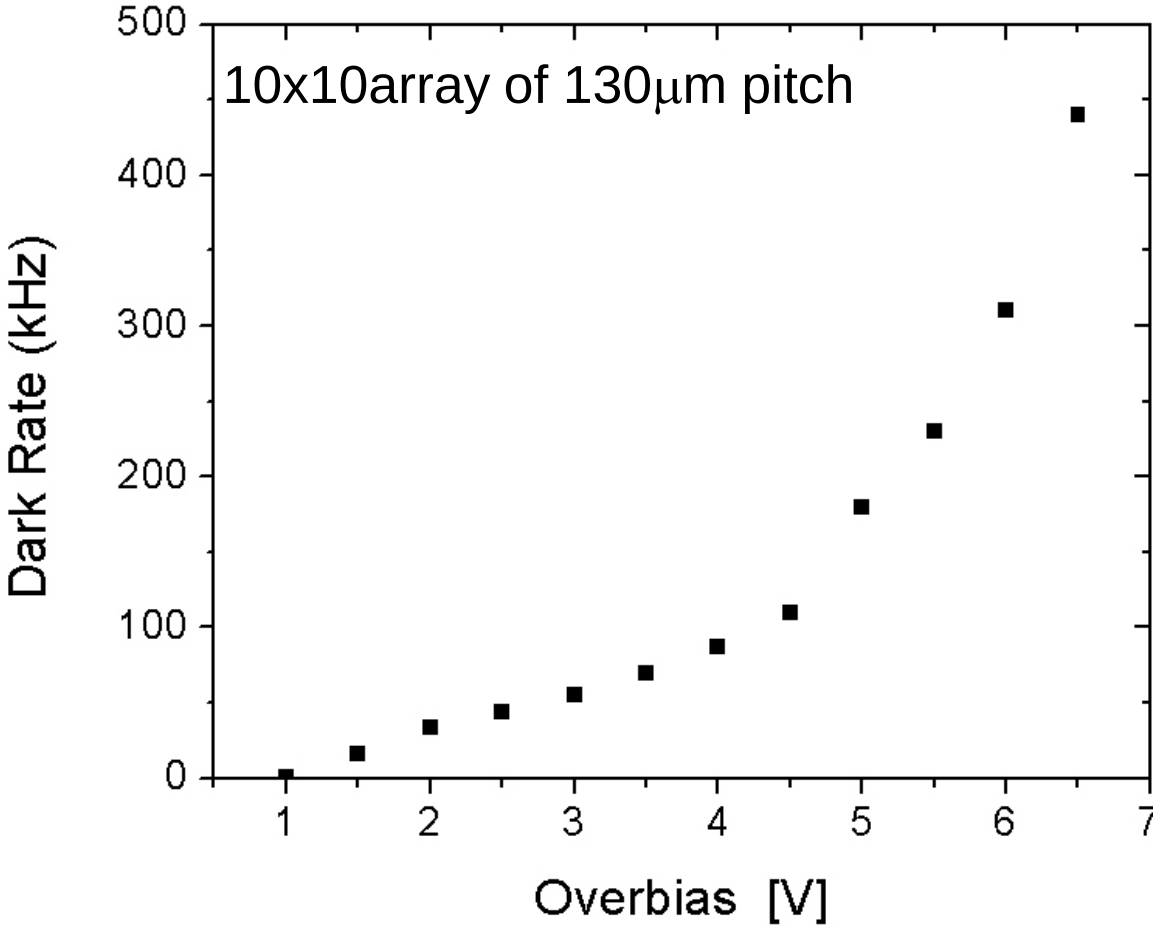
Gain linearity

10x10 array of 130μm pitch @ -30°C



Dark rate

Due to the non optimal process sequence of the high field processing ~10MHz @300K for 4V overbias



Normal operation up to 4.5V overbias @227K

Fill factor & Cross Talk & Photon Detection Efficiency

Produced SiMPl devices have the world record in the fill factors!

Pitch / Gap	Fill factor	Cross talk meas. (ΔV=2V)	PDE calc. (ΔV=2V)	PDE calc. (ΔV=5V)
130μm / 10μm	85.2%	29%	39%	61%
130μm / 11μm	83.8%	27%	38%	60%
130μm / 12μm	82.4%	25%	37%	59%
130μm / 20μm	71.6%	15%	32%	52%

PDE estimate:

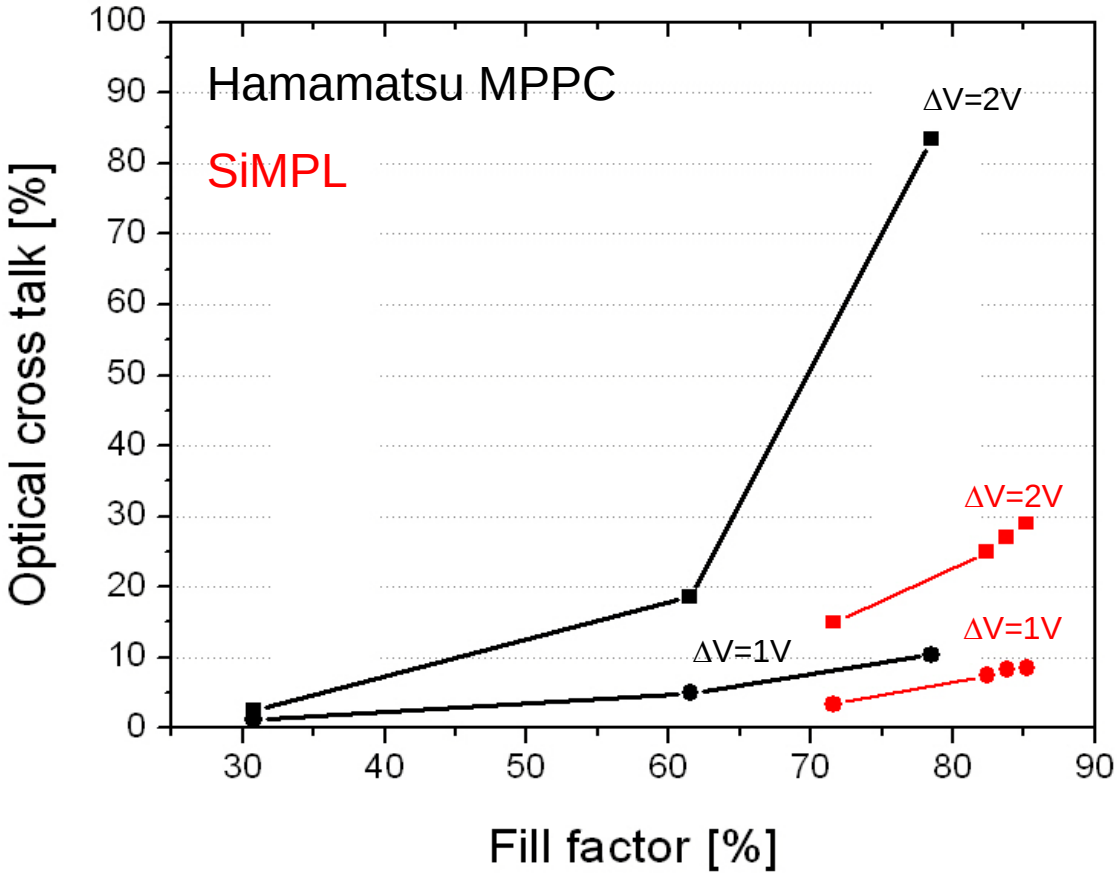
- Optical entrance window: 90% @400nm
- Geiger efficiency : 50% @ 2V overbias

80% @5V overbias

Fill factor & Cross Talk

Produced SiMPl devices have the world record in the fill factors and still lower cross talk!

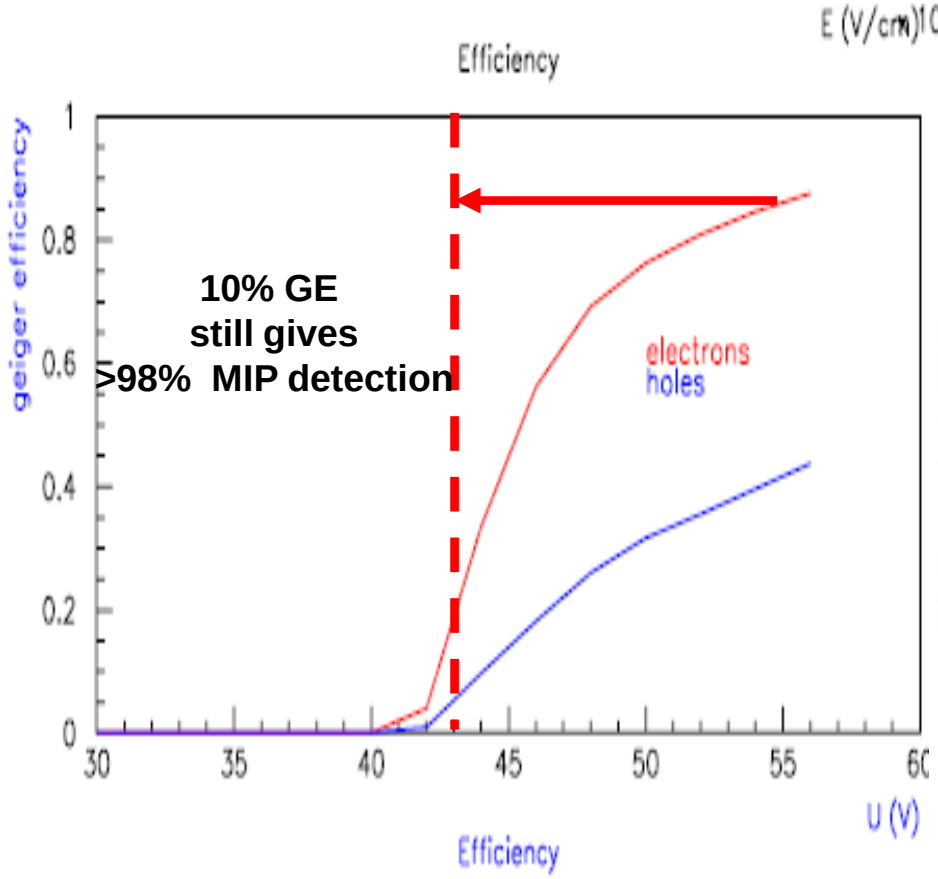
No special cross talk suppression technology applied
just intrinsic property of SiMPl devices

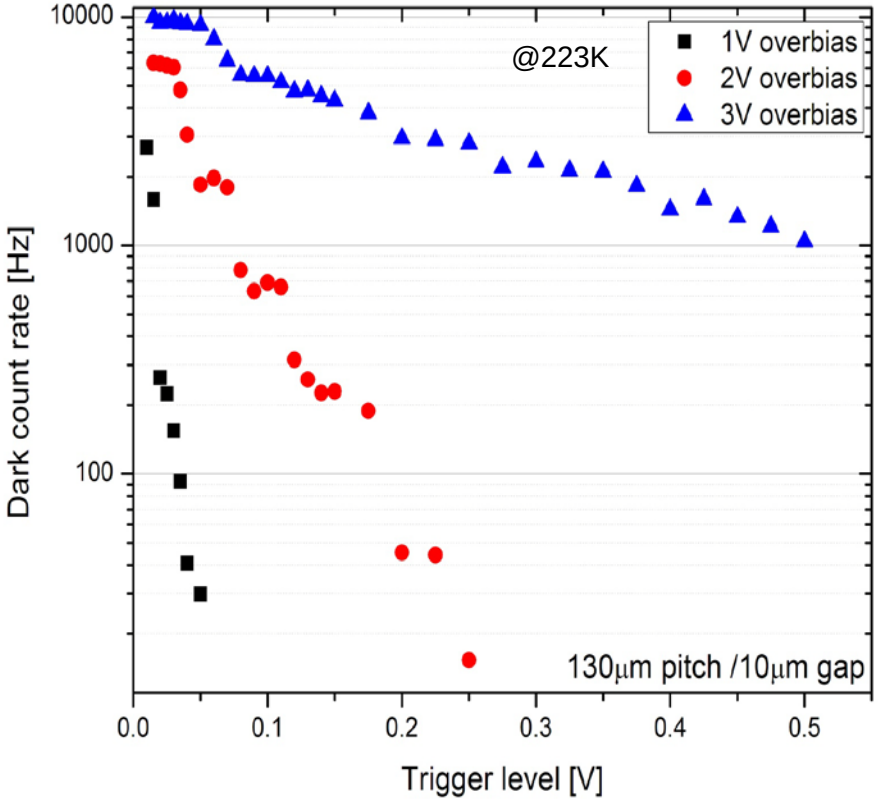


Detection of particles

Excellent time stamping due to the fast avalanche process (<1ns)

MIP gives about 80pairs/μm → huge signal in SiPM→ allows operation at small ΔV





Reduction of dark rate and cross talk by order of magnitude

Detection of particles

Dark rate: 1 MHz/mm² = 1 hit/µm²/s = O(Belle II)

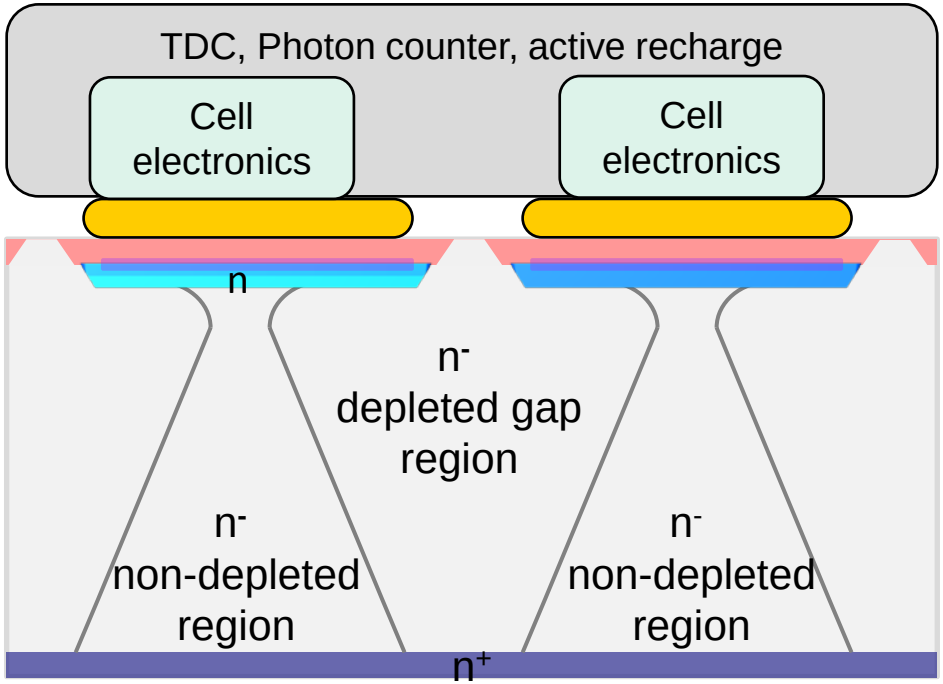
With 20 µm pitch and 12 ns time stamp: occupancy: 2.5 $x10^{-6}$

Power (analogue): ~ 5 µW/cm²
Dominated by dark rate

Possible problems:

- Radiation hardness (dark rate increases due to bulk damage)
- Cross talk
- Efficiency (fill factor)
- Digital power

Next generation SiMPl devices



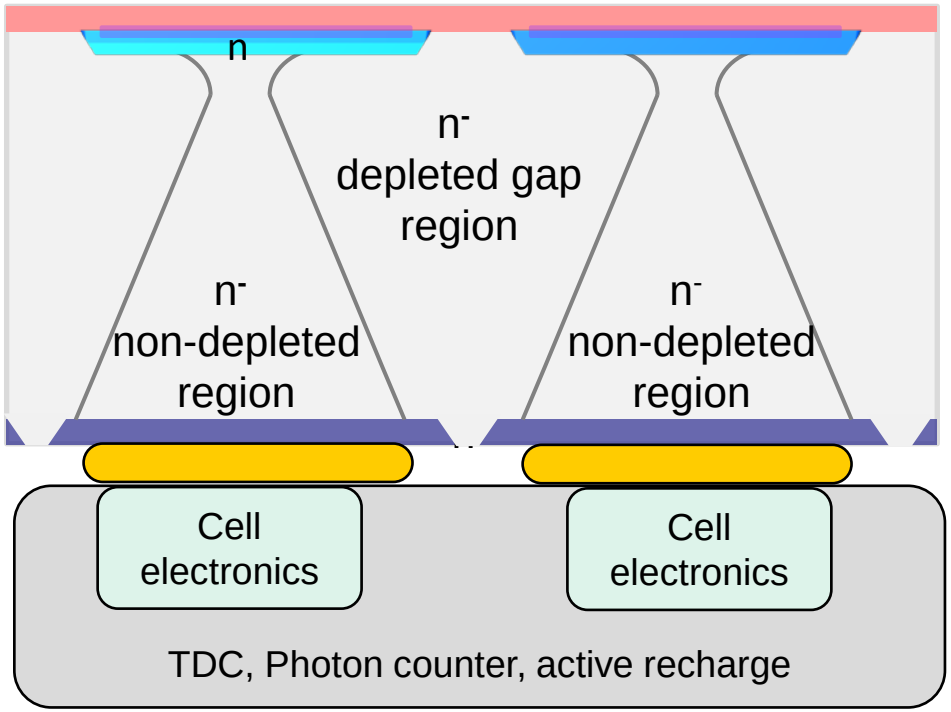
Topologically flat surface

High fill factor

Adjustable resistor value

Pitch limited by the bump bonding

Next generation SiMPl devices



Topologically flat and free surface

High fill factor

Sensitive to light

1. Structured implant on backside on sensor wafer

2. bond sensor wafer to handle wafer

3. thin sensor side to desired thickness

4. process SiMPl arrays on top side

Summary

Silicon photomultiplier array with individual quench resistors, integrated into the silicon bulk - SiMPl detector

- Required flexibility for quench resistor adjustment comes with wafer bonding technique (for small pixels an epitaxial layer is also suitable)
- No polysilicon resistors, contacts and metal necessary at the entrance window
- Geometrical fill factor is given by the need of cross talk suppression only
- Very simple process, relaxed lithography requirements

Prototype production finished – quenching works , first measurements very promising, functional devices with very high fill factor and low cross talk

Next generation SiMPl devices with electronics interconnected

- on front side can be used for trackers at future colliders
- on back side → high sensitivity, high fill factor digital SiPM

Thank you for your attention!