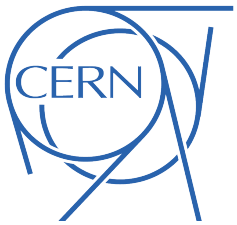
The TDCpix readout ASIC: a 75 ps resolution timing front-end for the Gigatracker of the NA62 experiment

Gianluca Aglieri Rinella,
M. Fiorini, P. Jarron, J. Kaplon, A. Kluge,
E. Martin, M. Morel, M. Noy, L. Perktold

CERN European Organization for Nuclear Research
NA62 Collaboration



Outline

Introduction

- NA62 Gigatracker
- TDCpix readout ASIC

Design of TDCpix

- Architecture
- Front-End
- TDC

Prototype ASIC

- Measured performances

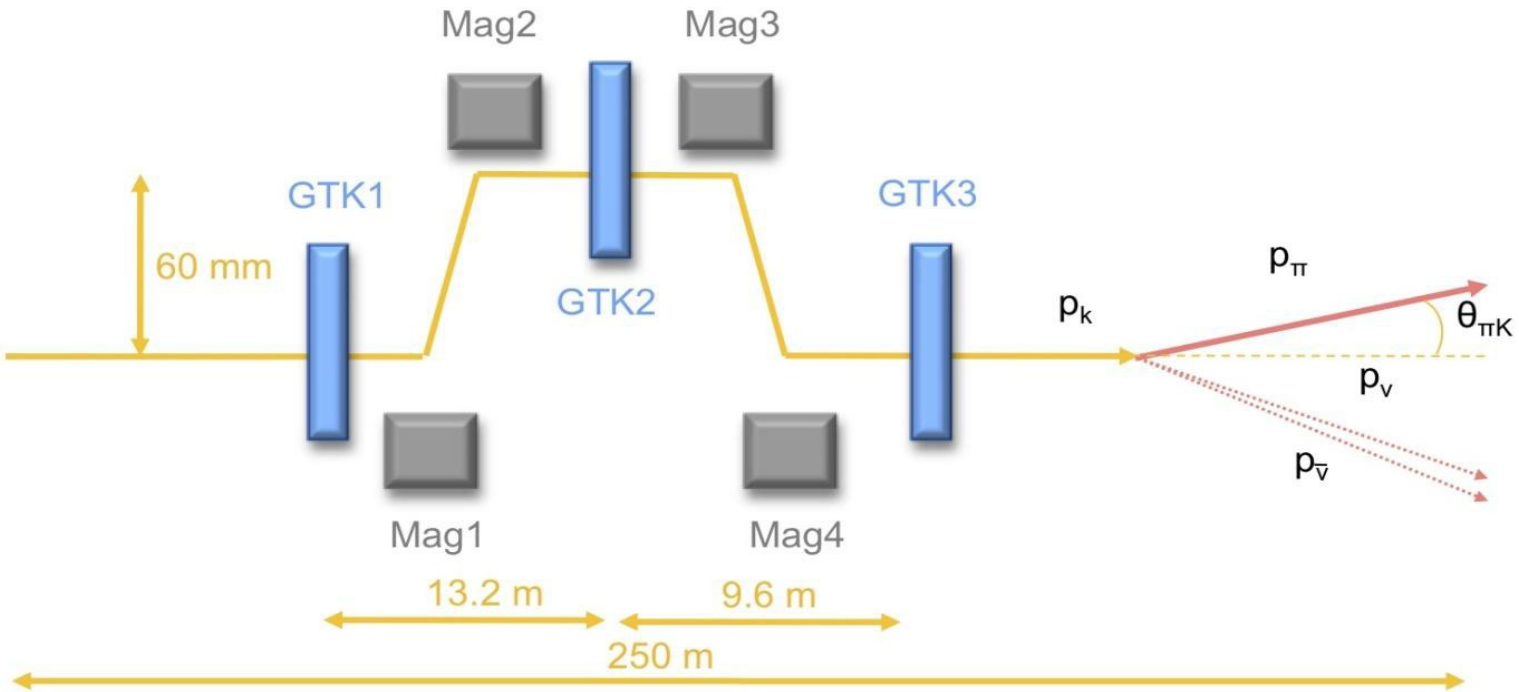
NA62 experiment and Gigatracker

NA62 experiment at CERN SPS

- Direct measurement of rare decay $K^+ \rightarrow \pi^+ \nu \bar{\nu}$
- In flight decay of Kaons from a high rate (~1 GHz) hadron beam

Gigatracker: Kaon spectrometer

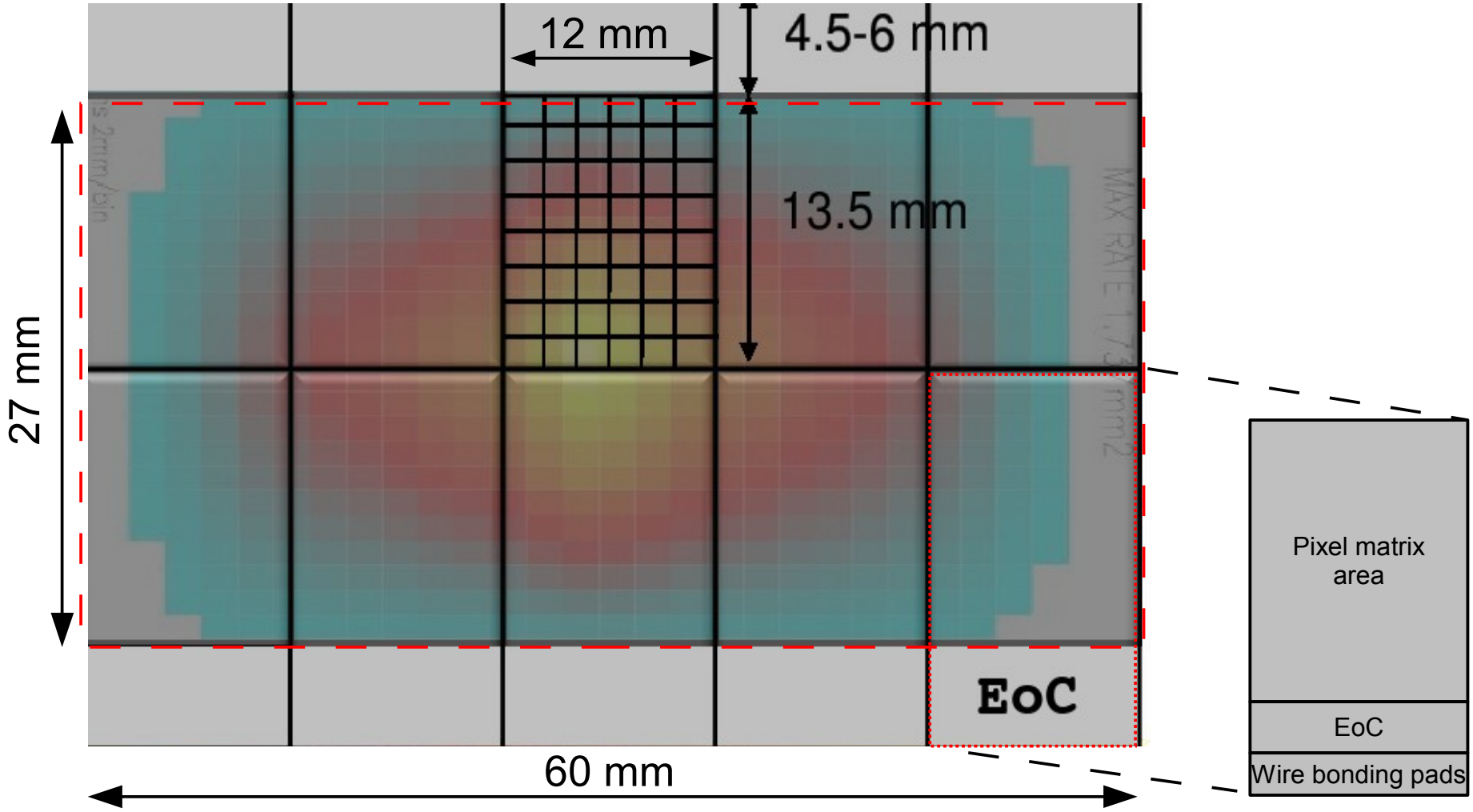
- 150 ps resolution time stamping, 200 ps for each station
- Follow talk by M. Fiorini, 10-Jun-2011, 14:20, Semiconductor Detectors



Detector geometry and beam profile

Total particle rate 1 GHz

Peak beam intensity 1.73 MHz/mm^2



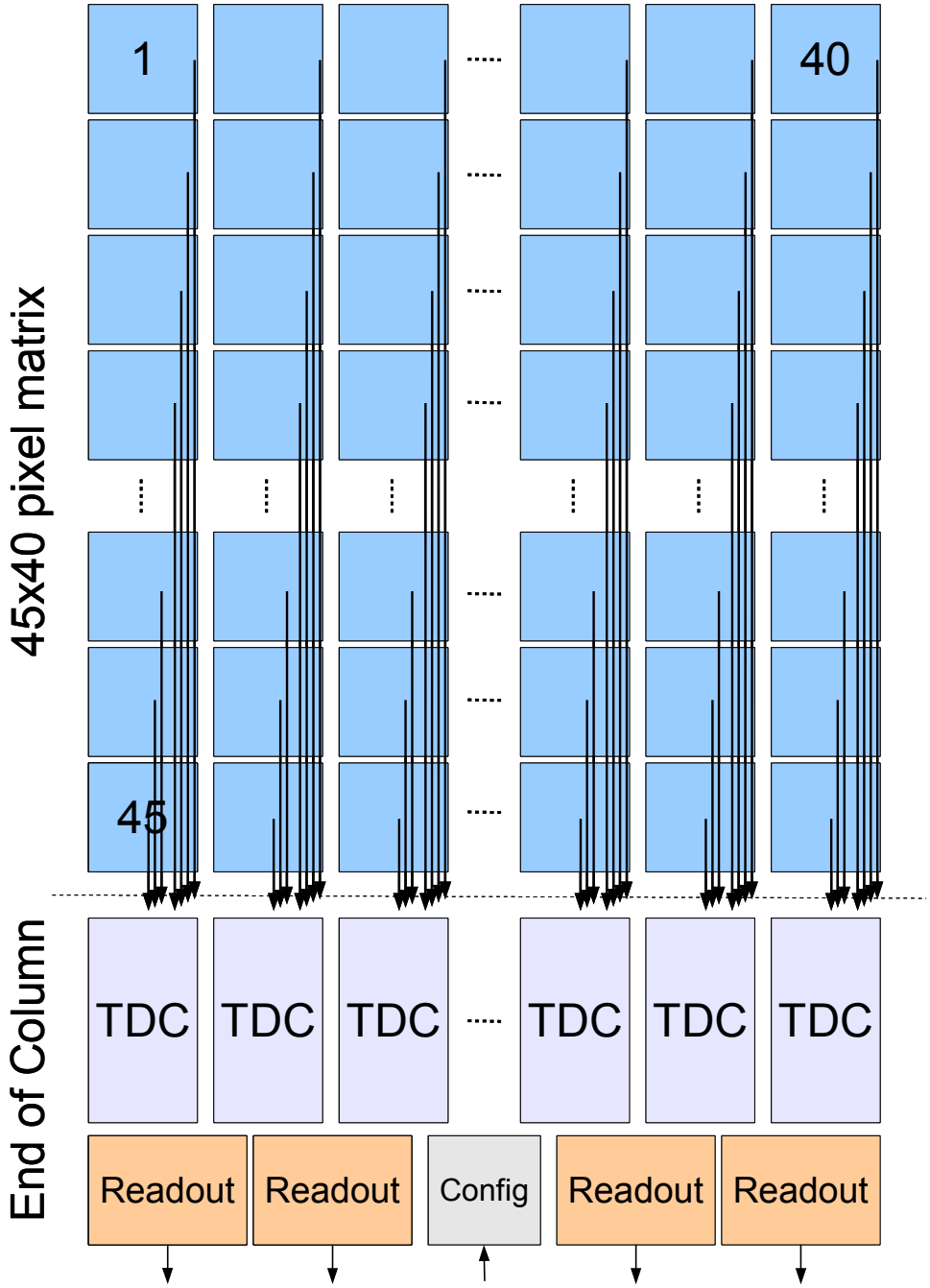
TDCpix block diagram

Requirements

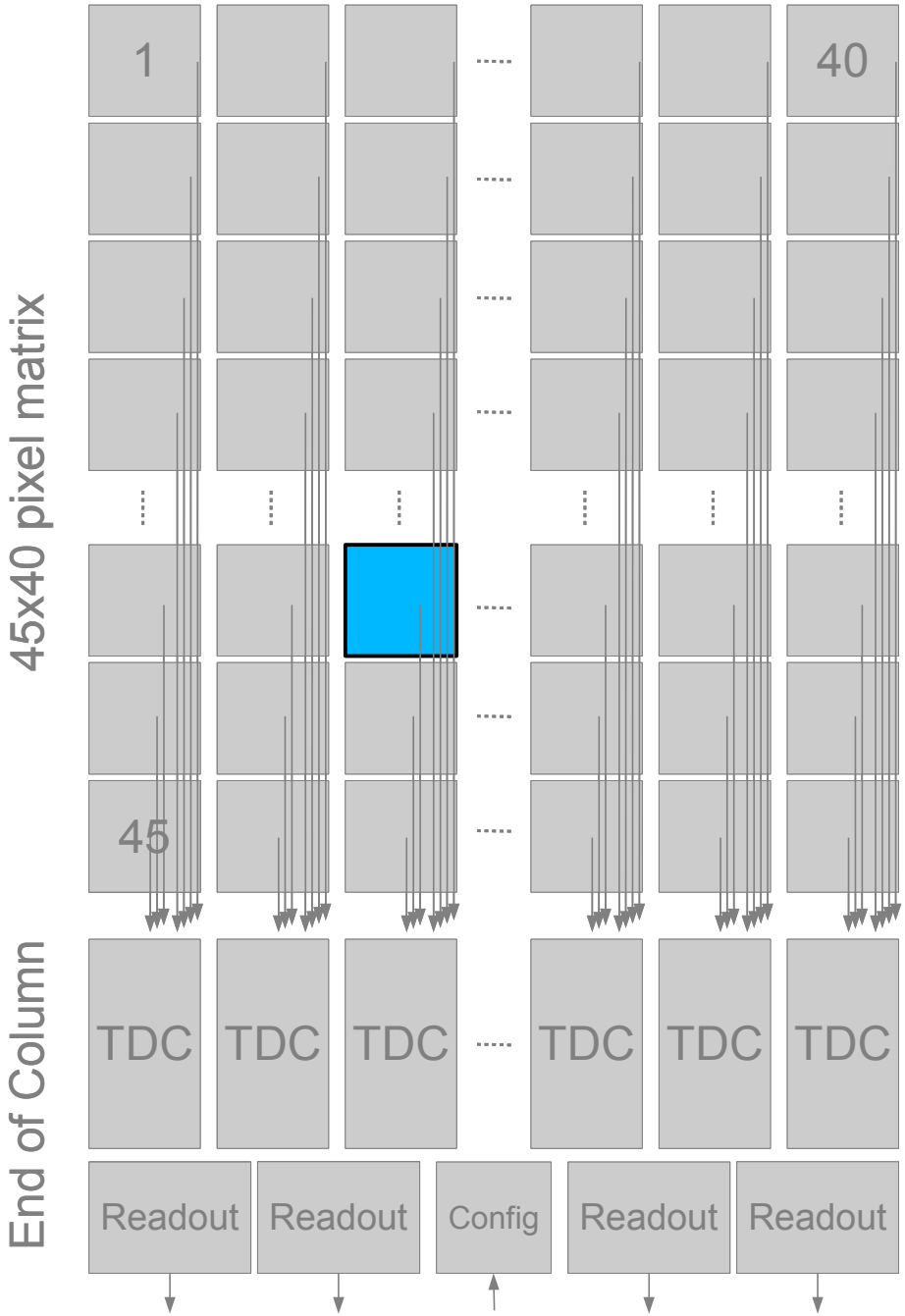
- 45 x 40 pixel channels
  300 x 300 μm²
- Chip hit rate ~130 MHz
- Timing resolution 200 ps RMS
- Readout efficiency 98 %
- Power budget 2 W/cm²

Architecture

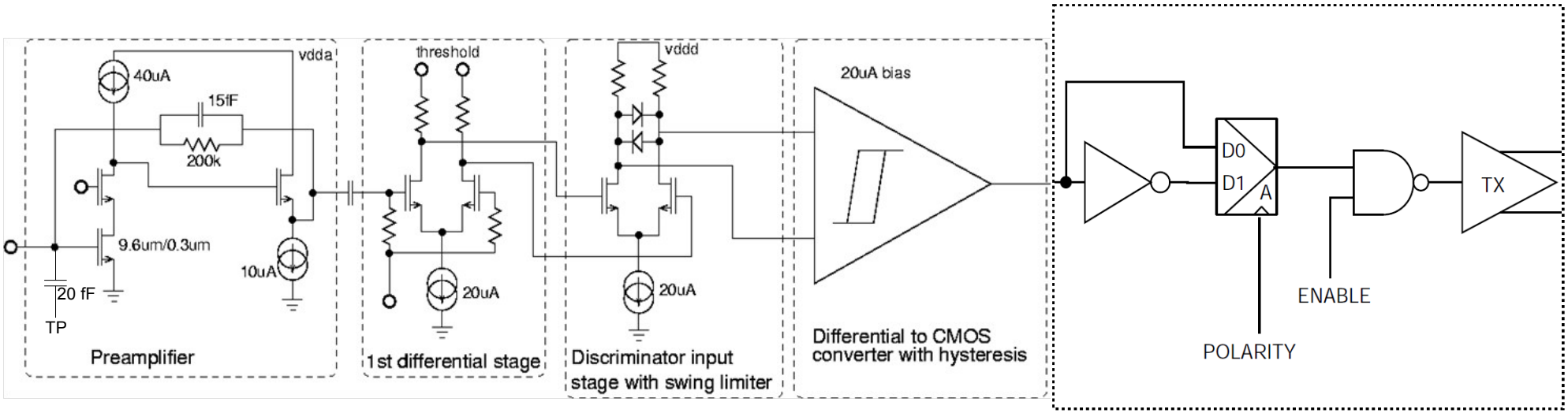
- Analog pixel matrix, digital EoC
- Transmission lines send discriminated hits to EoC
- Data driven, trigger-less
- Data output: 4x 2.4 Gb/s
- IBM CMOS 130 nm, 1.2V, 8 Metal layers



Pixel cell


1
40
45x40 pixel matrix
45
End of Column
TDC
TDC
TDC
TDC
TDC
TDC
Readout
Readout
Config
Readout
Readout

Pixel cell



Dynamic Range	0.6-10 fC / 3600-60000 e-
Gain	75 mV/fC
Peaking time	5 ns
ENC (no sensor)	130 e-
FE power	130 µA (56%)
TX line driver	100 µA (44%)
Full matrix power	500 mW

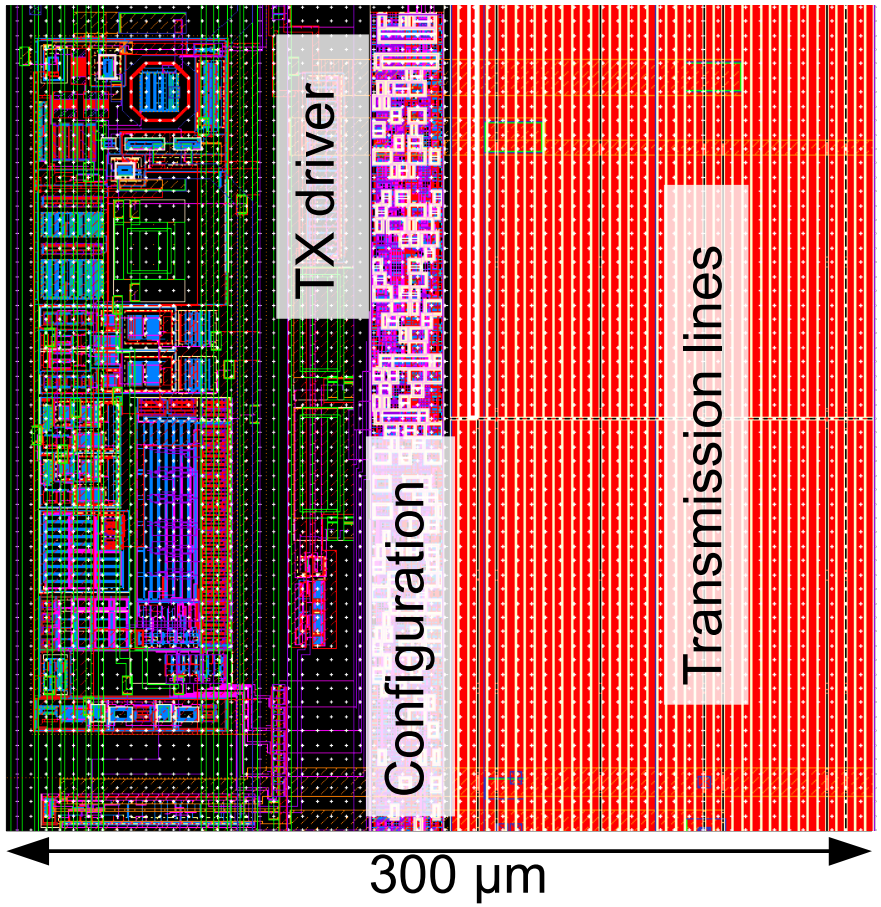
Pixel cell

Circuits occupy half of pixel area

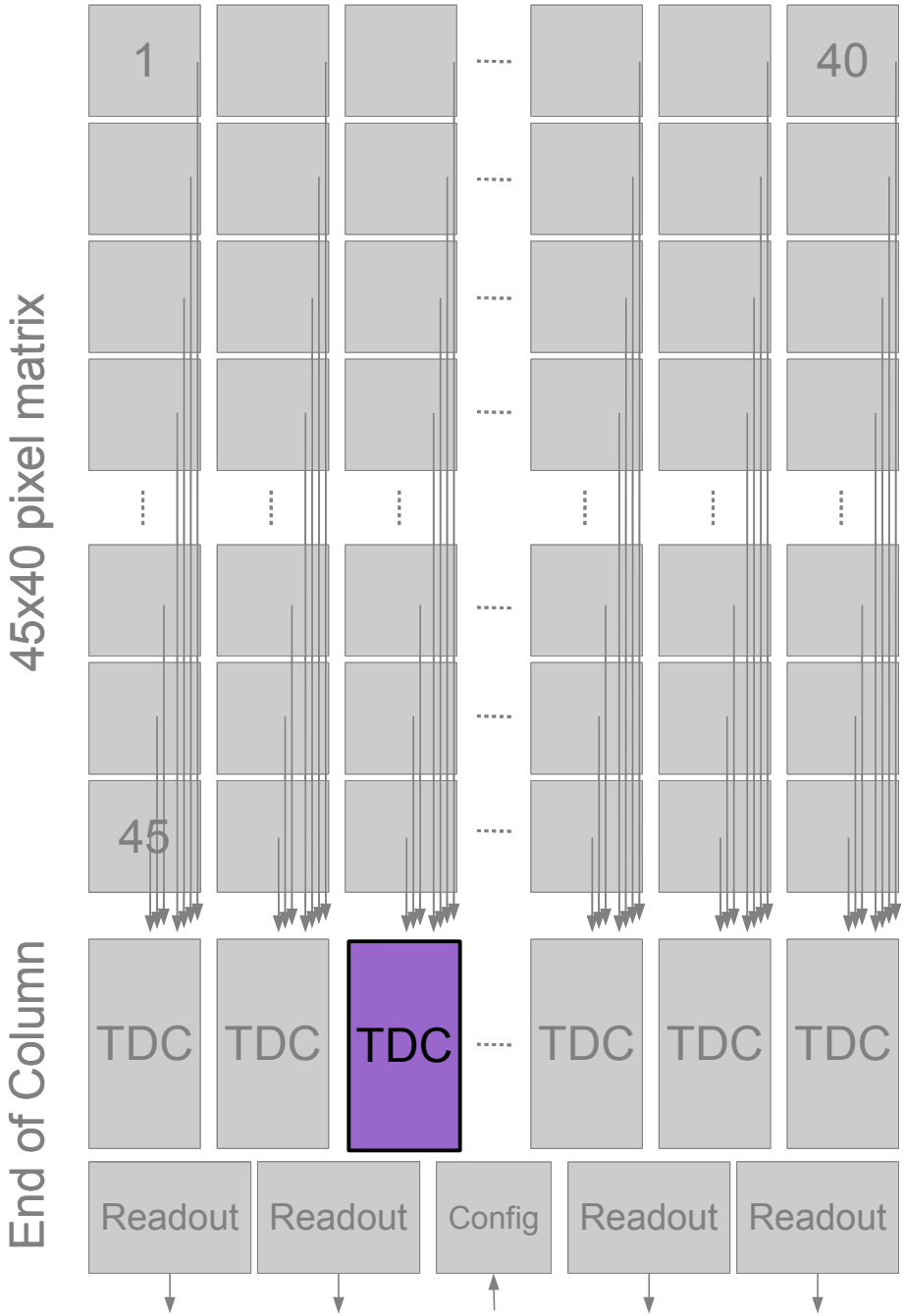
- Half column for transmission lines

Layout focus on immunity to noise

- Full separation of pixel matrix from EoC circuitry
- Analog section inside isolated implant well
- Front-end transistors in triple wells



TDC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40
45x40 pixel matrix
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End of Column
TDC
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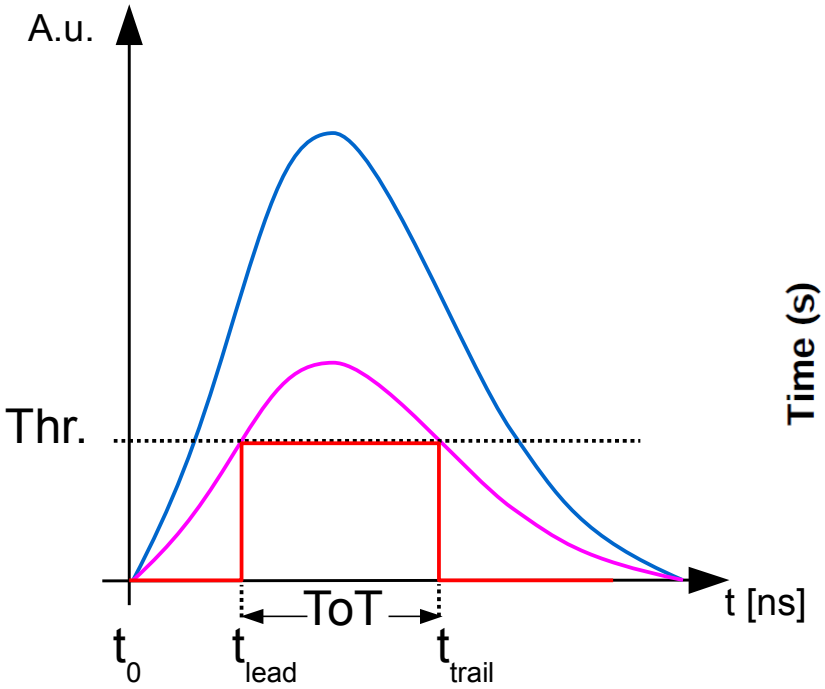
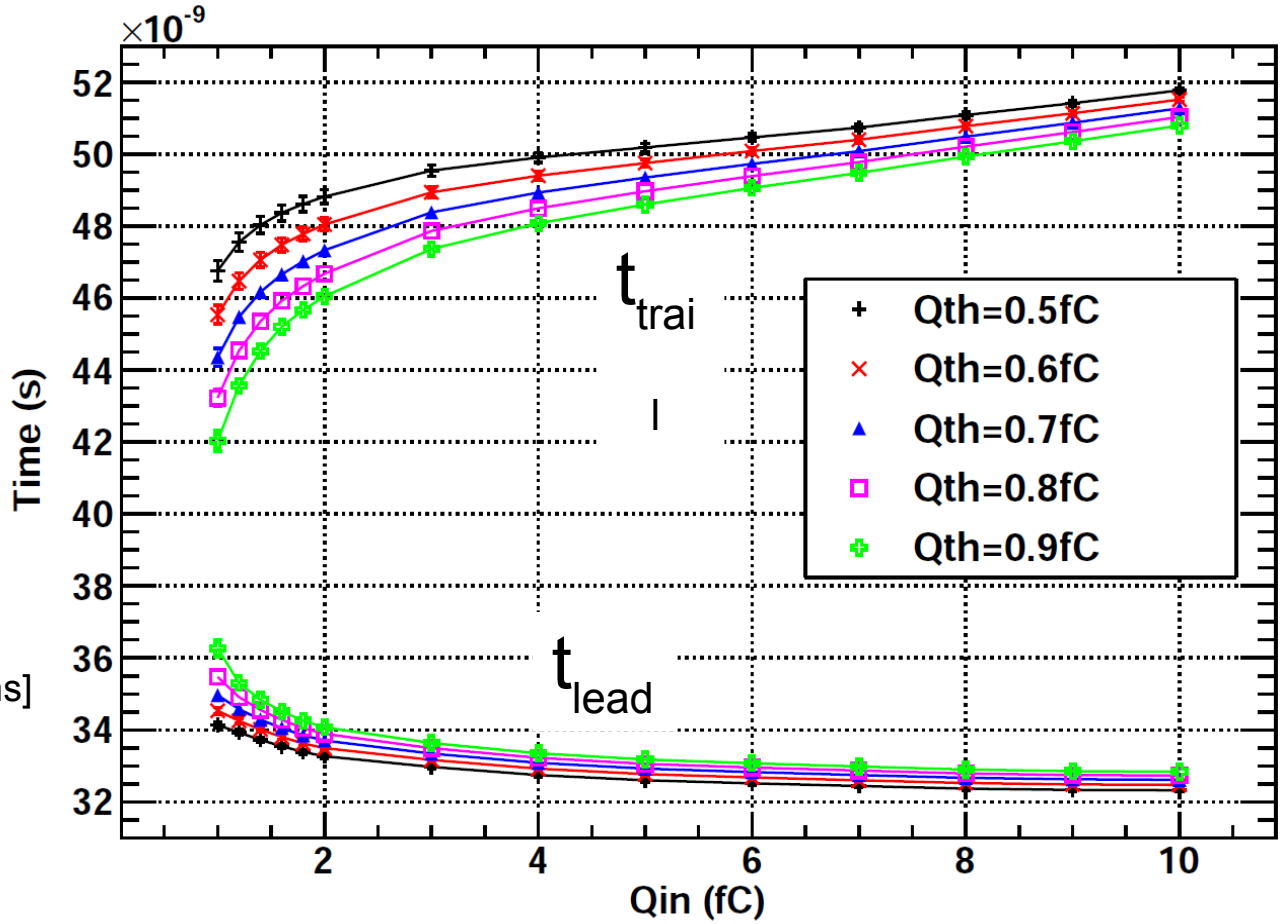
TDC
TDC
Readout
Readout
Config
Readout
Readout

Time walk and Time Over Threshold





TDC

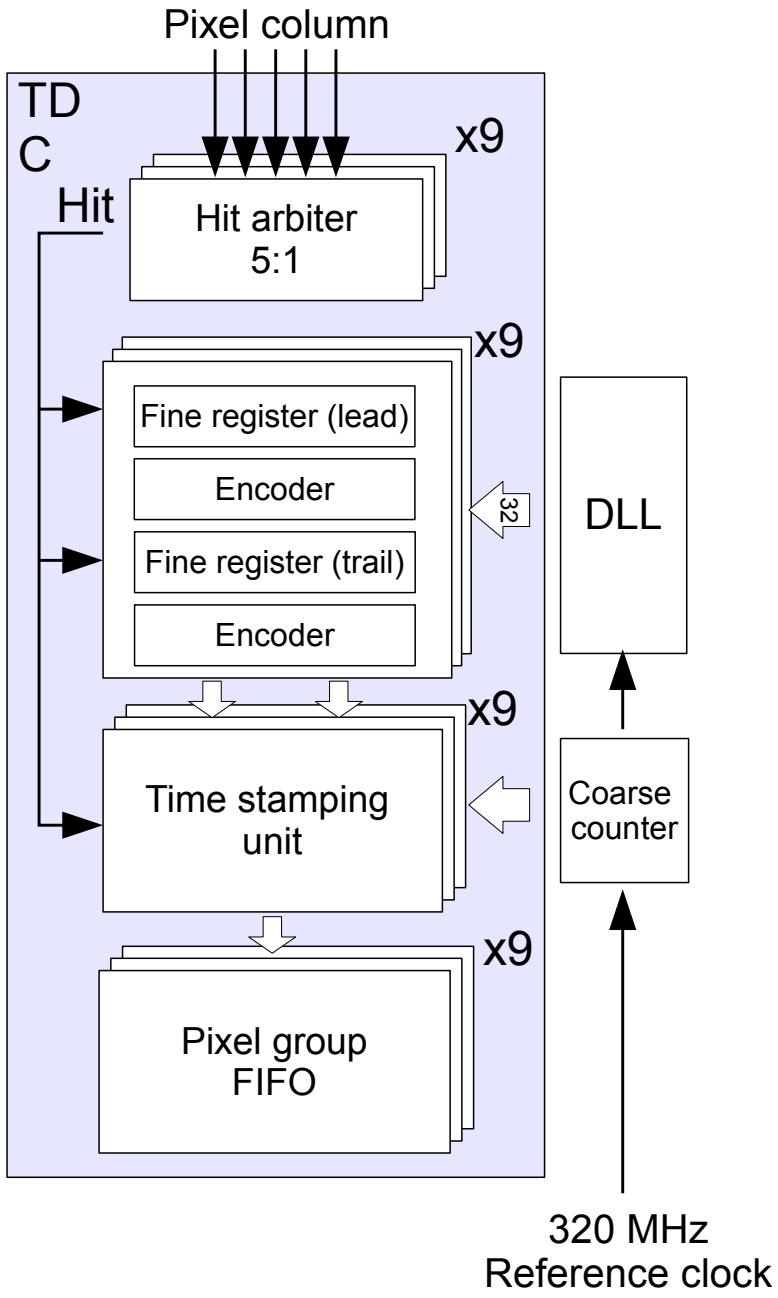
Delay Locked Loop based TDC

- 32 bins, 97 ps width

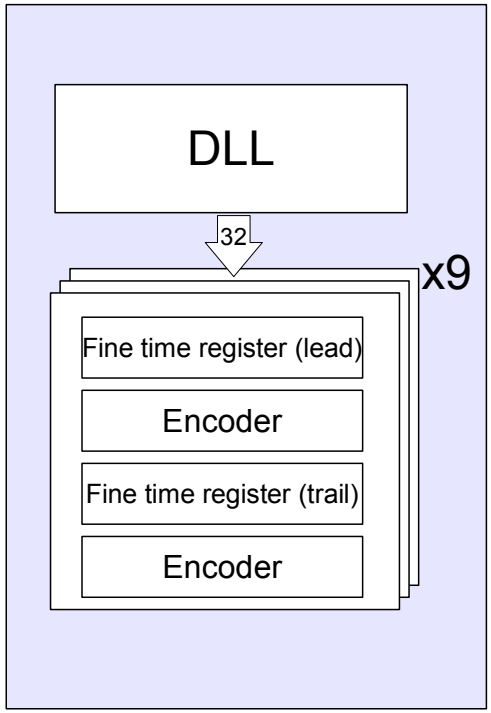
Hit multiplexing

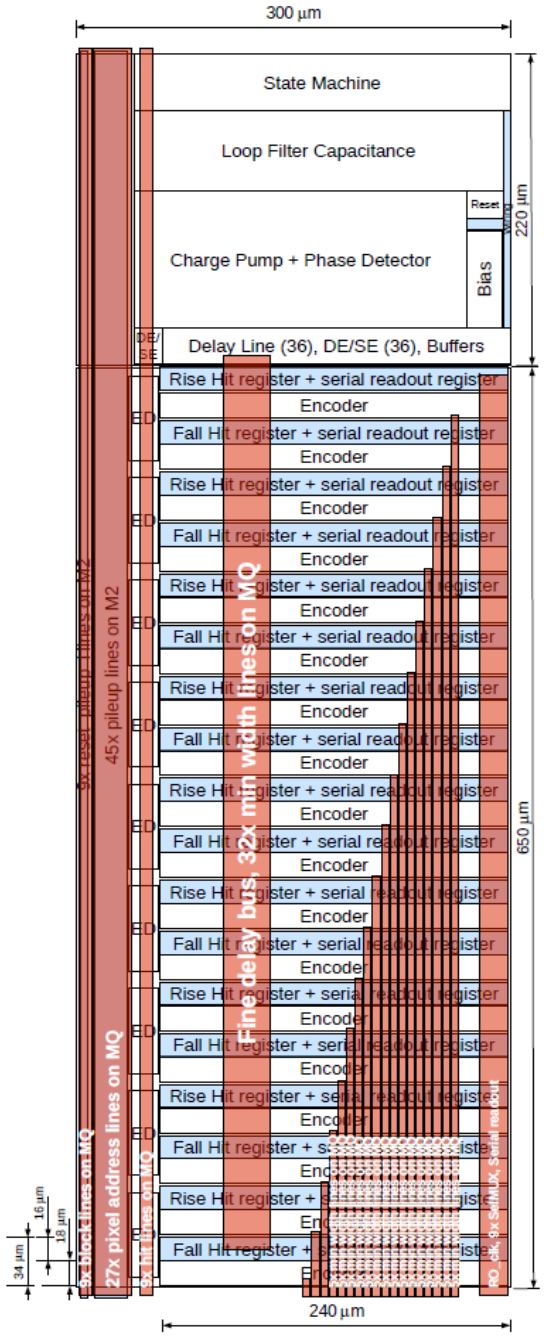
- Extensive simulation with realistic stimulus
  - 99.4% hits recorded, 0.6% hits collide, pile-up recorded

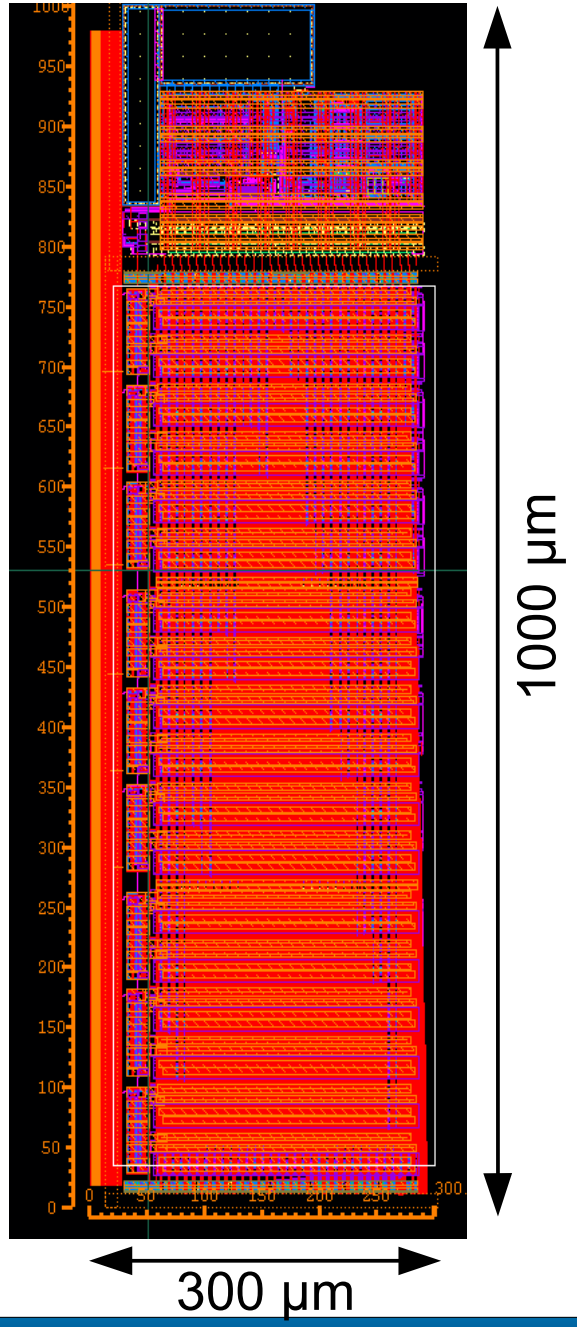
	Power [mW]
DLL	20
Register bank	5
20x DLL + 40x banks	600 (14% of chip budget)



TDC floor planning and layout







Introduction

- NA62 Gigatracker
- TDCpix readout ASIC

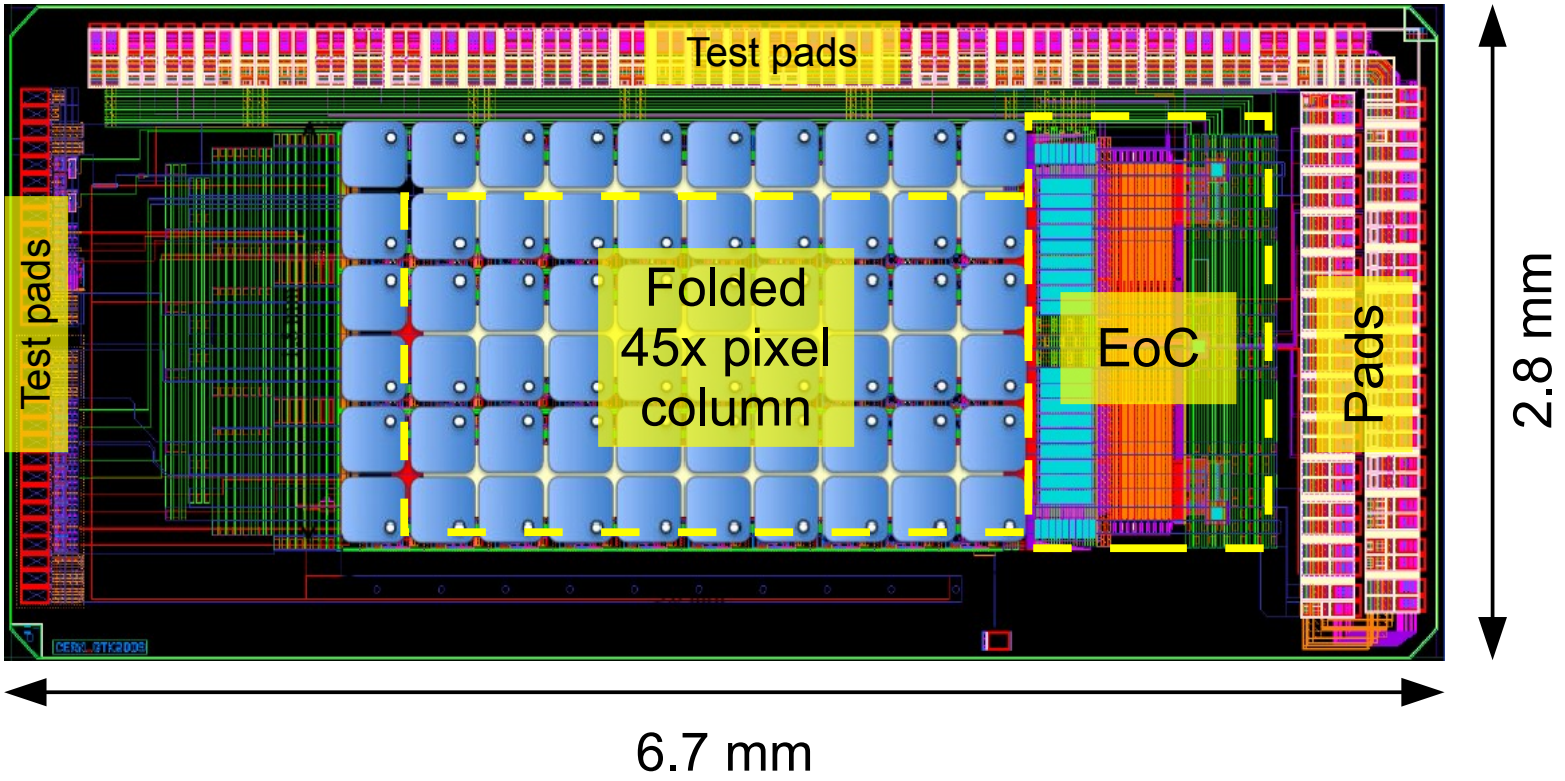
Design of TDCpix

- Architecture
- Front-End
- TDC

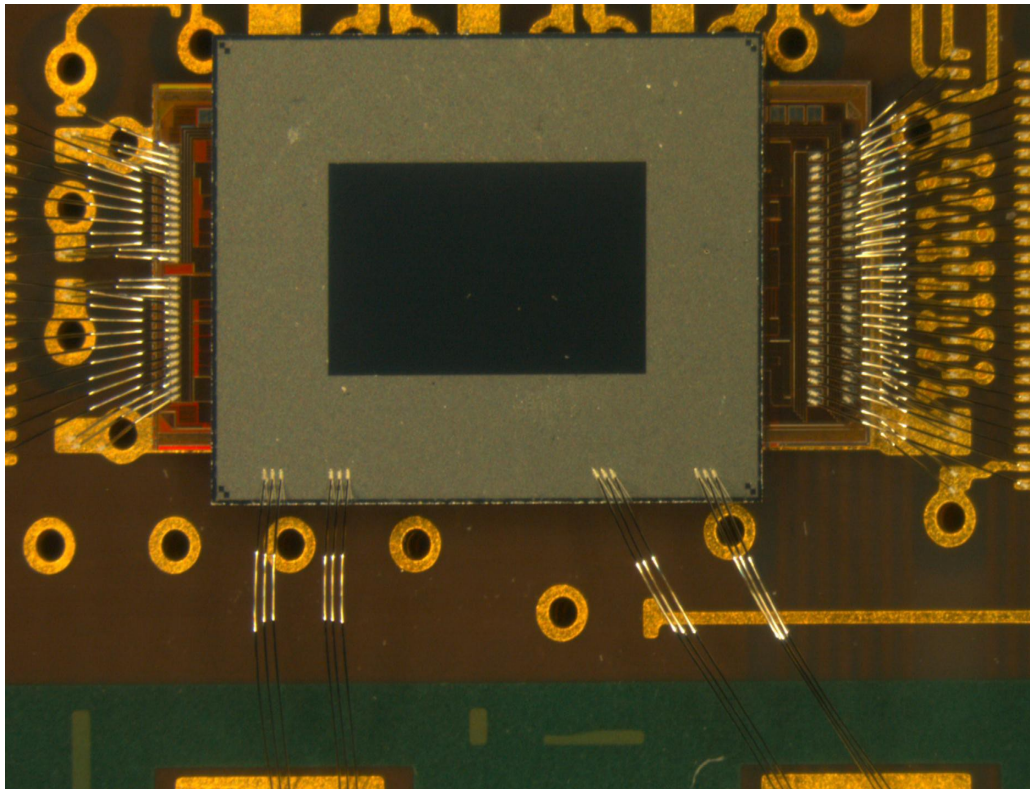
Prototype ASIC

- Measured performances

Prototype ASIC



Prototype hybrid pixel assemby



Charge injection methods

- Electrical test pulse
- Focused IR laser
- Radioactive source
- Particle beam

Pixel performance

Uniform gain

- 72 ± 1.5$_{RMS}$ mV/fC

Pixel baseline distribution

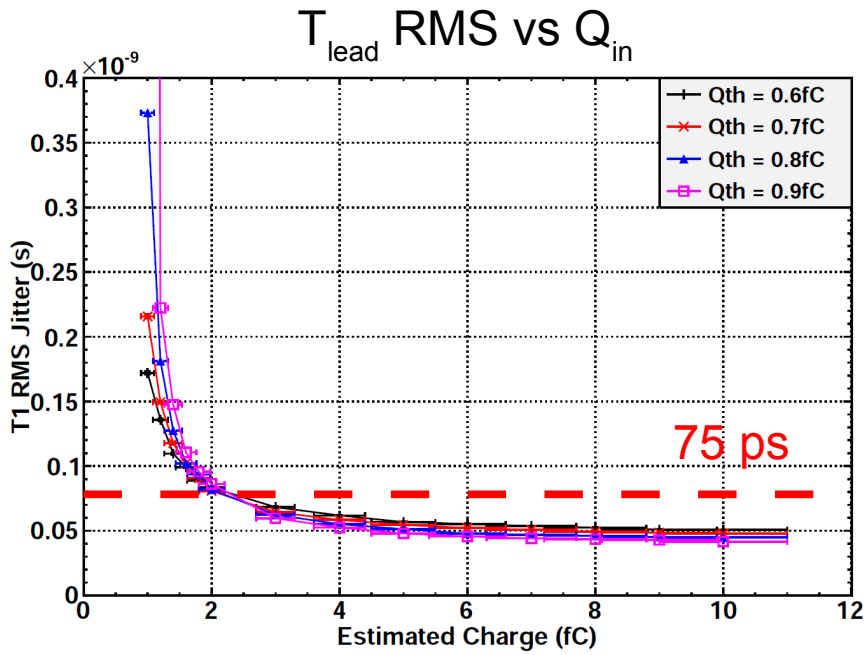
- 50 mV peak to peak
- Trim circuit in the final TDCpix ASIC

Noise 180 e$^-$ (ENC)

- C$_{det}$ = 250 pF

Discriminator jitter

- < 75 ps RMS (Q > 2 fC)



Charge injection with laser
300 V detector bias

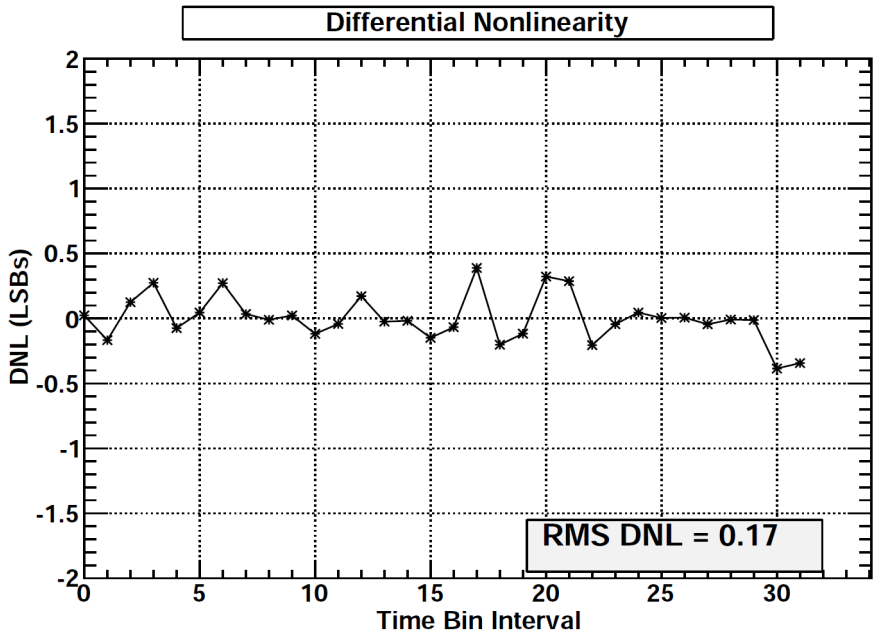
TDC performance

TDC jitter

- < 10 ps RMS

Single hit timing resolution

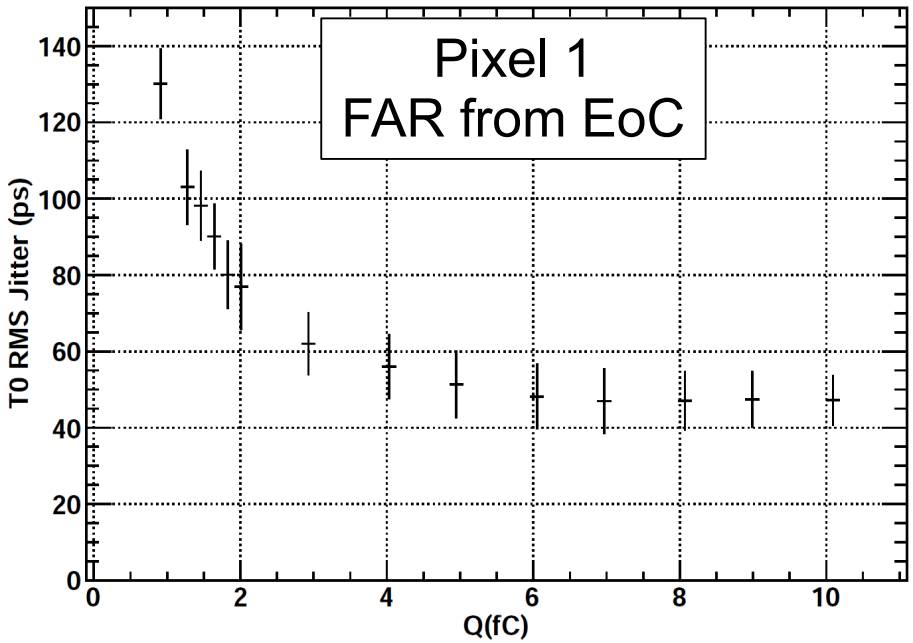
- ~ 40 ps RMS
  - f_{clk} = 320 MHz, T_{bin} = 97.7 ps

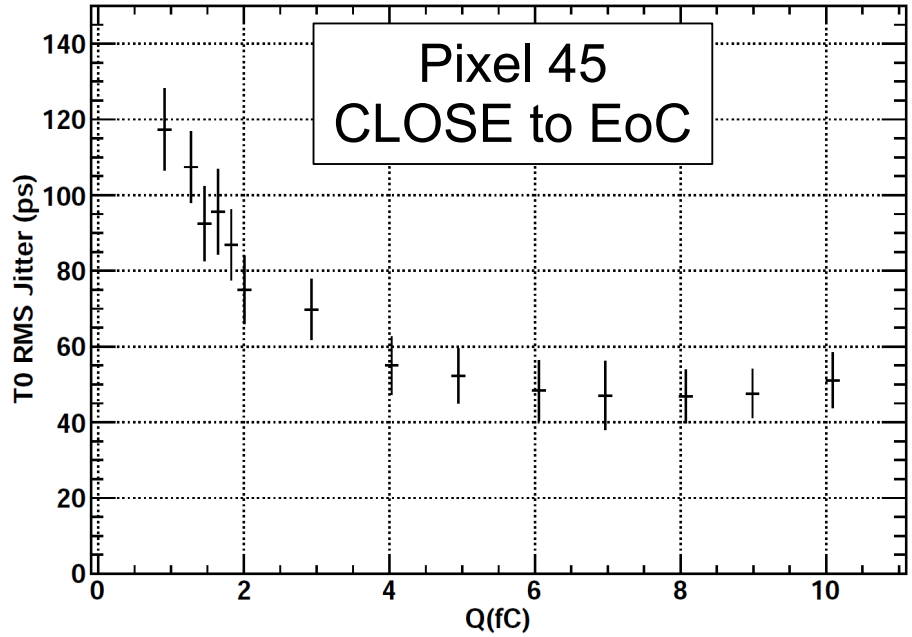


Full chain timing performance

T_0 RMS < 75 ps

- Q > 2 fC
  - Time walk correction included
- Charge injection with laser
  - Detector bias 300 V
  - Fixed position, pixel center

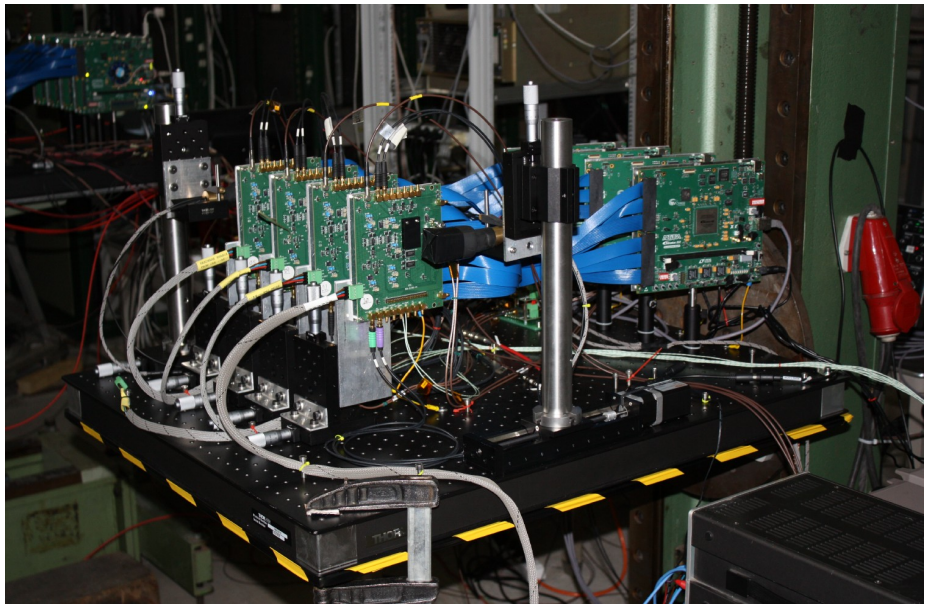


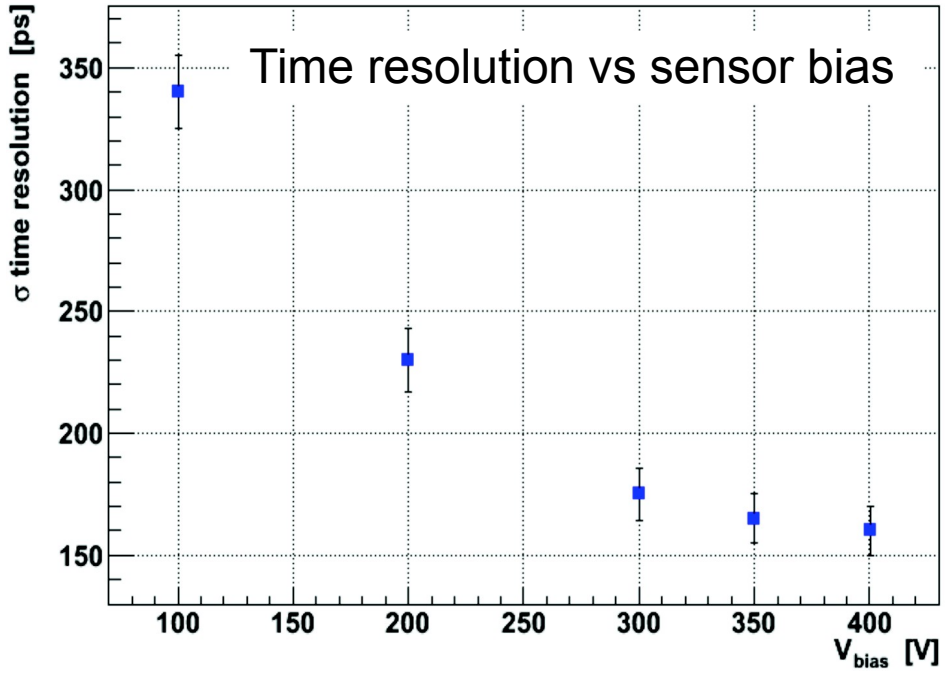


Timing particles in beam test

Four prototype assemblies

- Detection efficiency > 95 %
  - Without threshold trimming
- Timing resolution < 175 ps RMS
  - 200 μm Si, 2.4 fC MPC





Timing resolution limit of sensor

Timing resolution

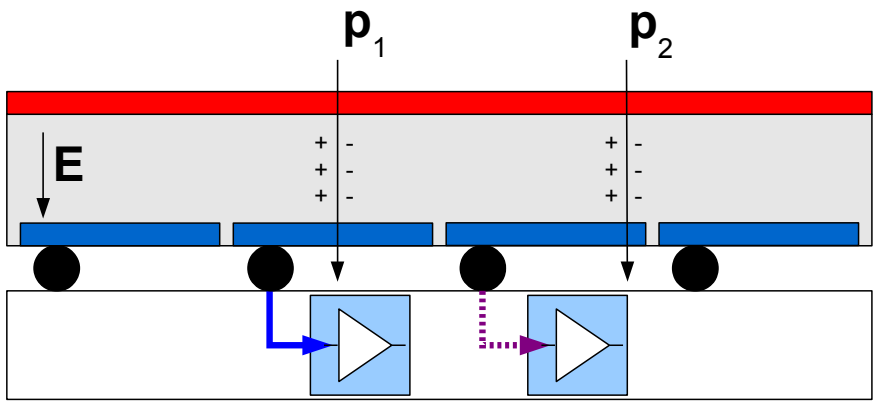
- Laser: 75 ps RMS
- Test beam: 175 ps RMS

Random fluctuations of input current signal shape

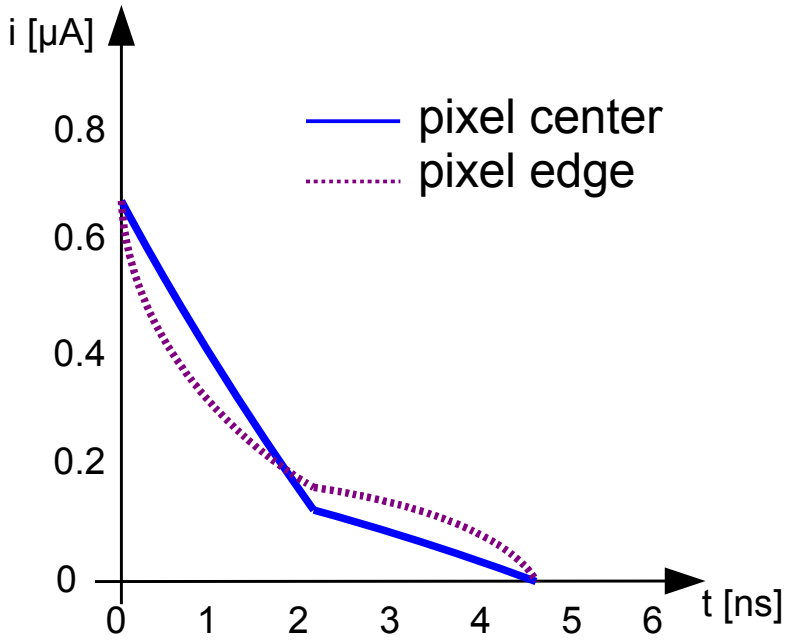
- Position of track hit in pixel
- Charge straggling

Ongoing studies

- Track hit position
  - Position scan with laser: 85 ps RMS
- Charge straggling
  - > 60 ps RMS



Sensor current pulses



Summary

Design of TDCpix for the NA62 Gigatracker

- 45x40, 300x300 μm^2 pixels readout
- Time tagging of 130 Mevents/s

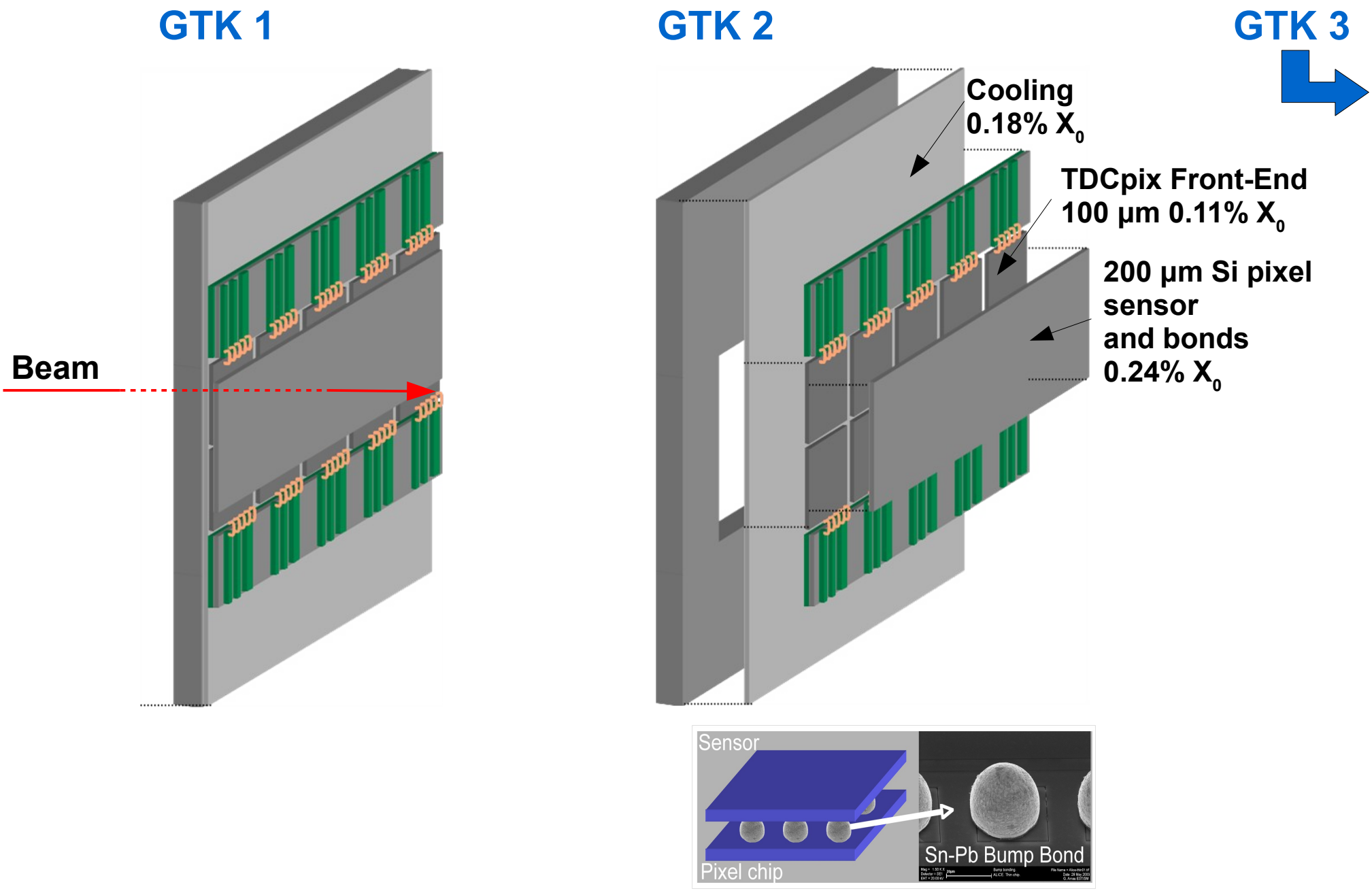
Measured performances of prototype ASIC

- 180 e^- ENC front end
- 75 ps discriminator jitter (Q > 2 fC)
- Low jitter and linear TDC, 40 ps timing resolution
- 75 ps RMS timing resolution for constant input pulse shape (Q > 2 fC)
- 175 ps RMS timing resolution with particles in beam test

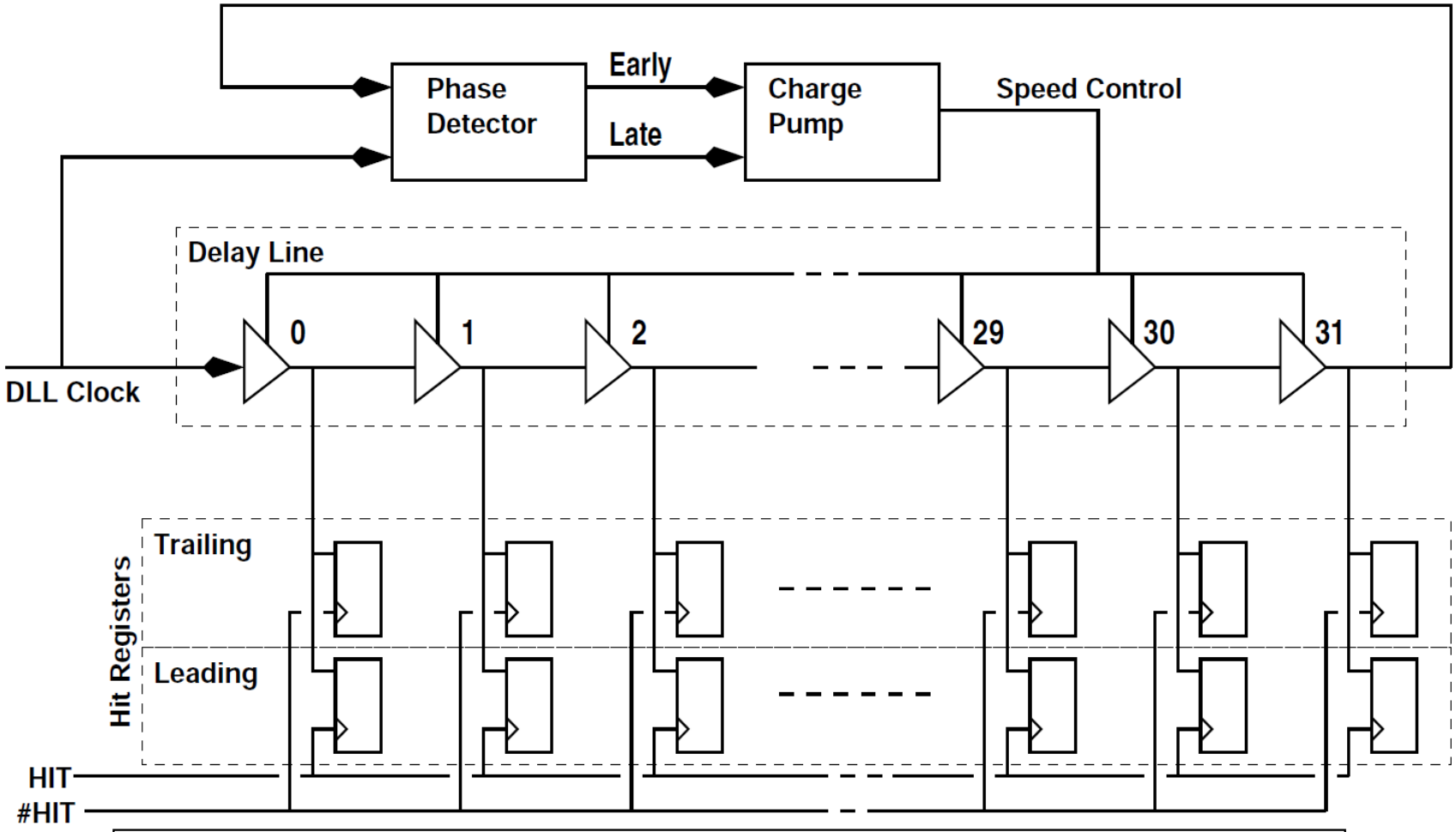
Timing resolution dominated by random fluctuations of sensor current

Spare slides

Gigatracker stations



Delay locked loop based TDC



320 MHz clock, 32 starved delay cells $\rightarrow$ 97 ps time bin.

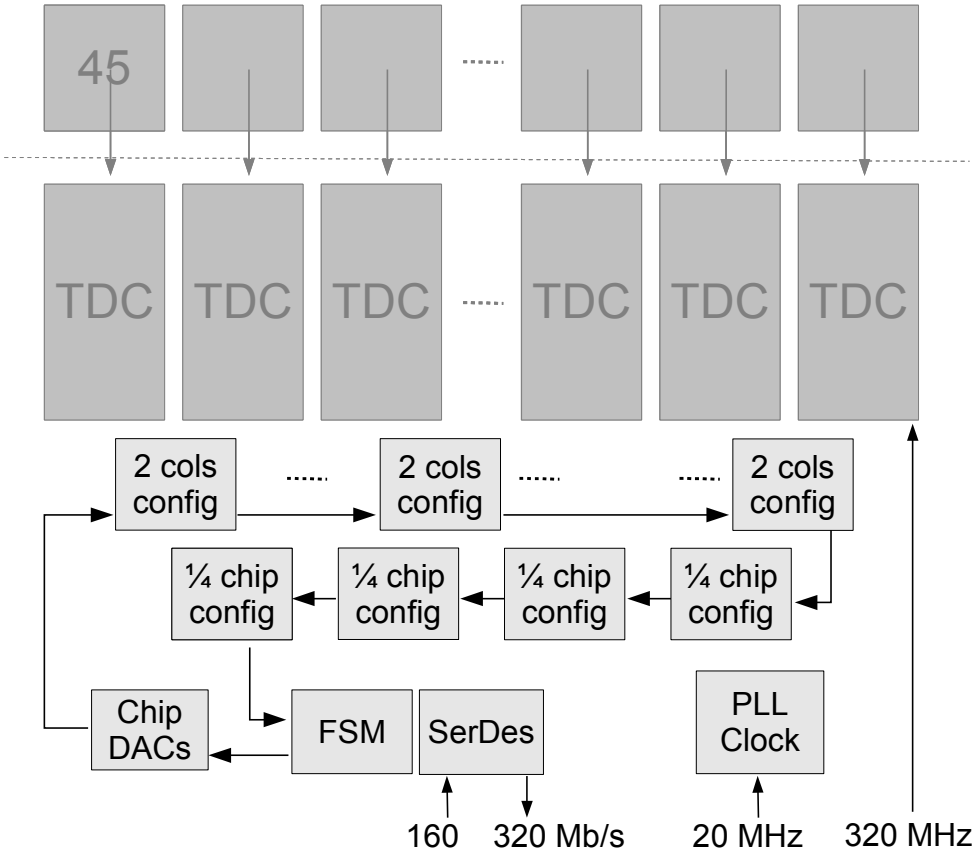
Configuration and SEU

Serial configuration interface

- ~17000 configuration bits
- Double column daisy chains in pixel matrix

SEU

- Cross section $2 \cdot 10^{-14}$ cm^2/FF
- Flow 66 MHz/cm^2
- SEU rate: $2.24 \cdot 10^{-2}$ Hz



Triple Module Redundancy

- All configuration FFs, state machines, FIFOs and counters

- No TMR on data path registers
  - Data remain shortly on chip

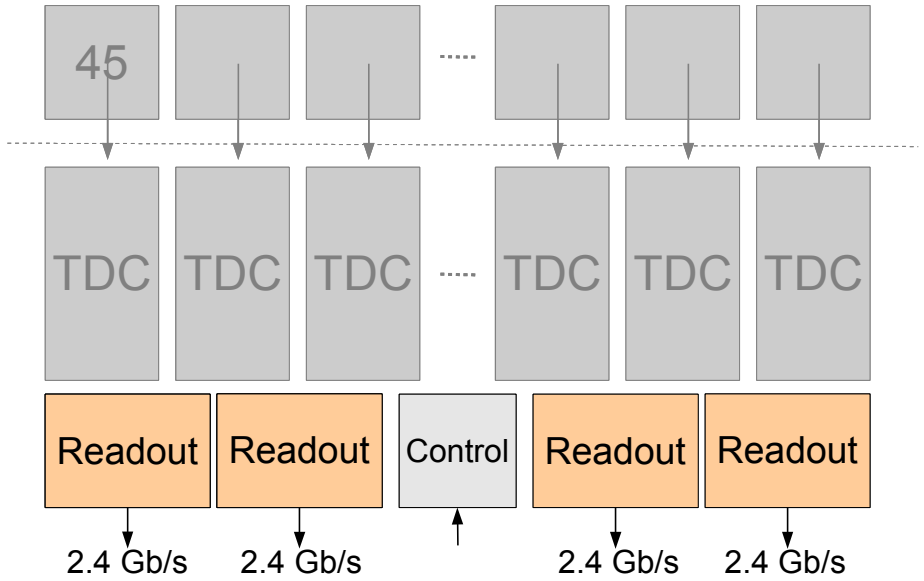
Data serialization

Multiplexing of 4 groups of 10 columns

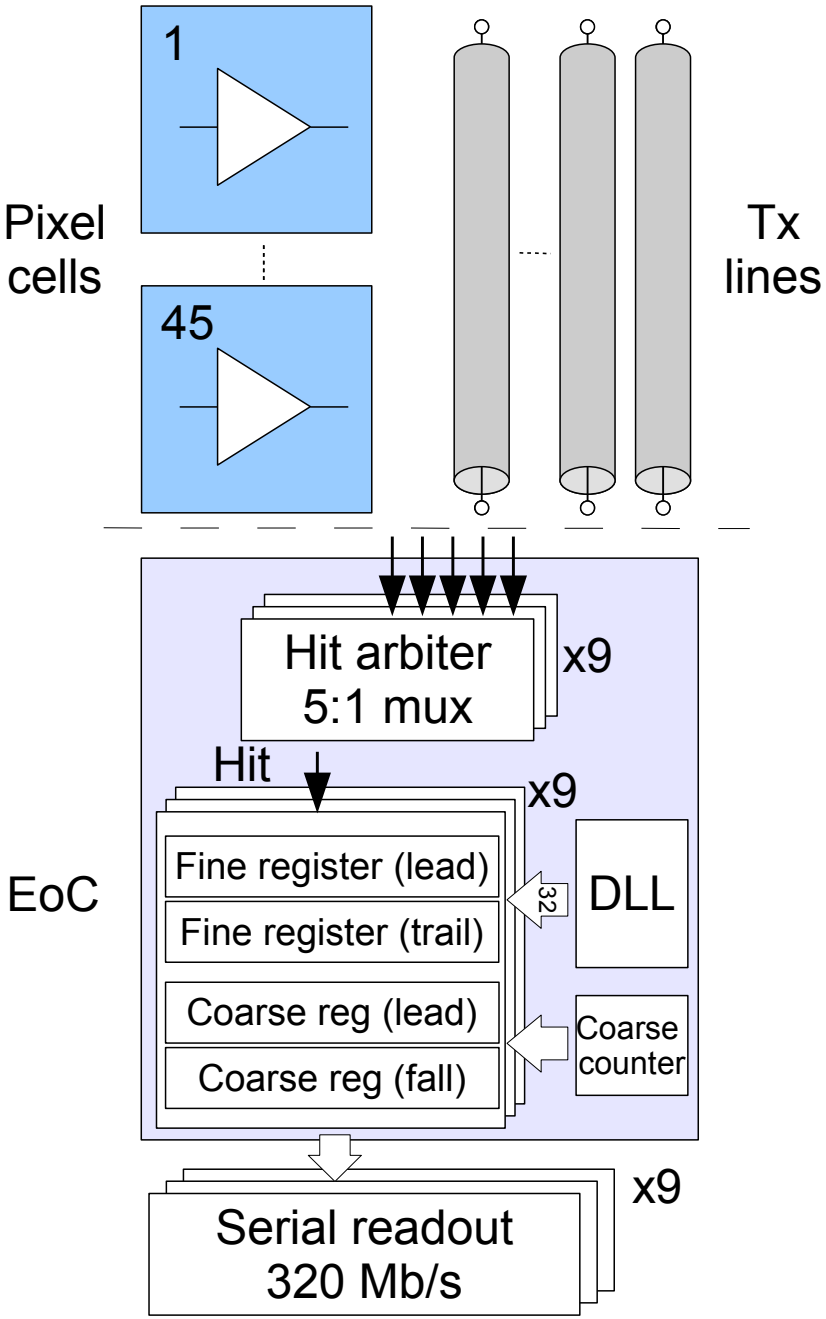
- 10 columns 27 Mhits/s
- Hit data word 48 bits
- 8b/10b encoding 60 bits

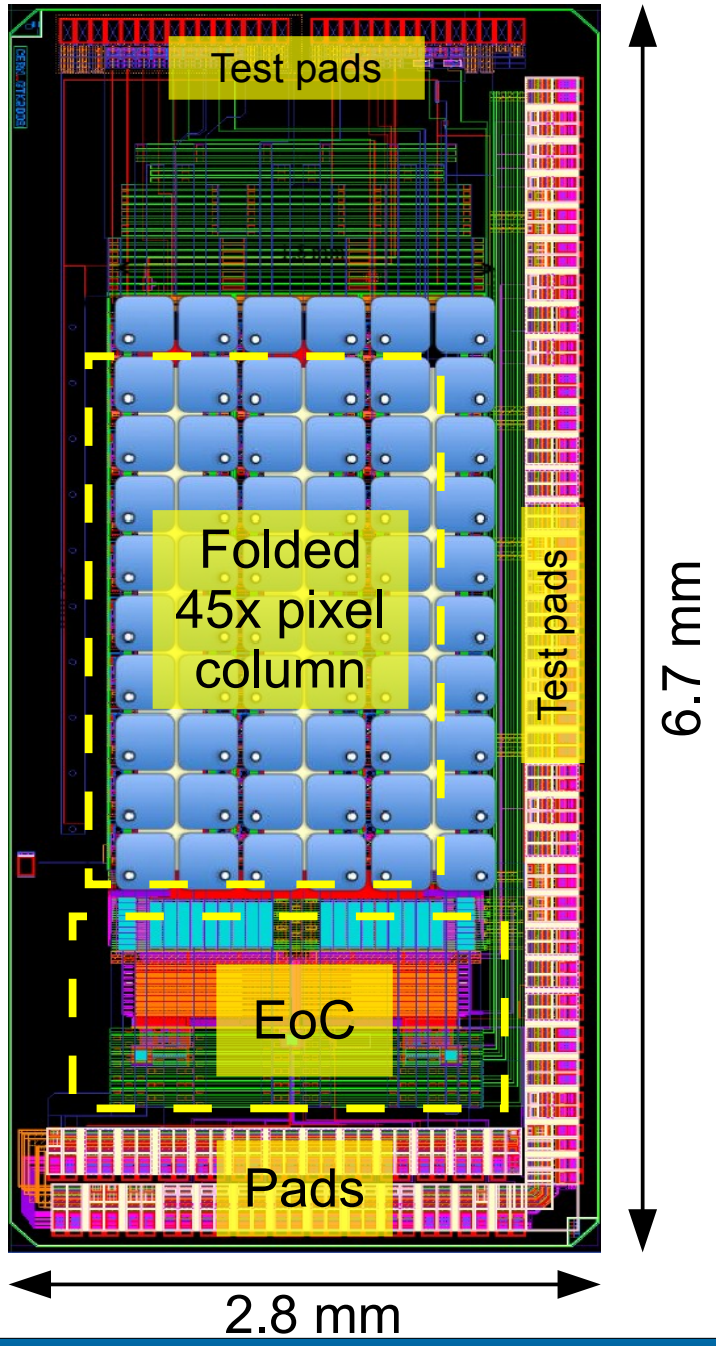
2.4 Gb/s serial transmitters

- Expected to use significant fraction of remaining power budget



Prototype EoC demonstrator ASIC





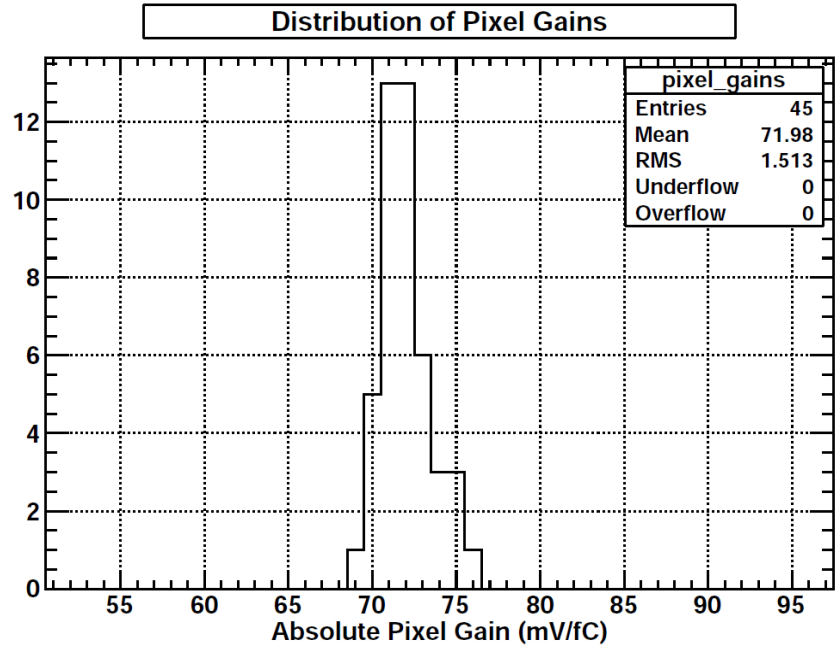
Pixel performance

Uniform gain

- 72 ± 1.5$_{RMS}$ mV/fC

Pixel baseline distribution

- 1117 ± 10.8$_{RMS}$ mV
- Peak to peak: 50 mV
- Offset trim in the final TDCpix ASIC

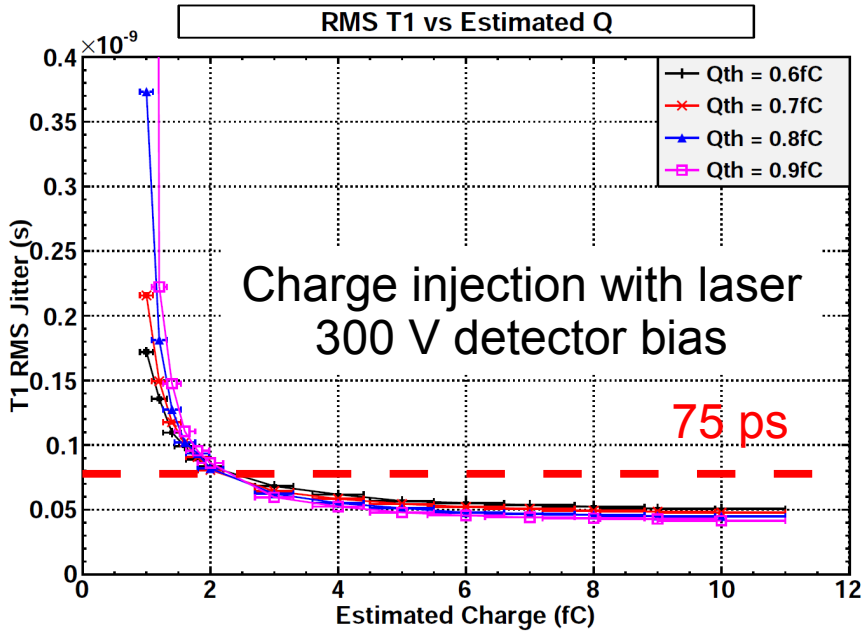


Noise 180 e$^-$ (ENC)

- Bonded to detector C_{det} = 250 pF

Discriminator jitter

- < 75 ps RMS (Q > 2 fC)



TDC performance

TDC jitter

- < 10 ps RMS

Single hit timing resolution

- ~ 40 ps RMS
  - f_{clk}= 320 MHz, T_{bin}= 97.7 ps
  - Correcting for non-linearity 30 ps