Contribution ID: **369** Type: **Oral Presentation**

The TDCpix readout ASIC: a 75 ps resolution timing front-end for the Gigatracker of the NA62 experiment

Thursday 9 June 2011 17:20 (20 minutes)

NA62 is a new experiment at CERN Super Proton Synchrotron aiming at measuring ultra rare kaon decays.
The Gigatracker (GTK) detector shall combine performing on-beam tracking of individual particles with an excellent time resolution of 150 ps rms.
The peak flow of particles crossing the detector modules reaches 40 MHz/cmˆ2 for a total rate of about 1 GHz.
A hybrid silicon pixel detector is being developed to meet these requirements.

Our team is designing the final pixel chip for the NA62 GTK.
The TDCpix chip will feature 1800 square pixels of 300x300 umˆ2 arranged in a matrix of 45 rows x 40 columns.
Bump-bonded to the pixel sensor it shall perform time stamping of particle hits with a timing accuracy better than 200 ps rms and with a dead time below 1%.

The chosen architecture provides full separation of the sensitive analog amplifiers of the pixel matrix from the noisy digital circuits of the Time to Digital Converters (TDCs) and of the readout blocks.
Discriminated hit signals from each pixel are transmitted to the end of column region.
An array of TDCs is implemented at the bottom of the pixel array.
The TDCs operate by latching the fine time codes generated by Delay Locked Loops (DLL) and have a nominal time bin of ˜100 ps.
Time stamp and time-over-threshold are recorded for each discriminated hit and the correction of the discriminator's time-walk is performed off-detector.
Data are continuously transmitted on four 2.4 Gb/s serial output links.

A prototype ASIC including the key components of this architecture has been manufactured.
The achievement of specification figures such as a time resolution of the processing chain of 75 ps rms as well as charged particle time stamping with a resolution below 200 ps rms were demonstrated experimentally.

This contribution will focus on the development and the design of the final TDCpix chip.
A description of the on-going design will be given, presenting and discussing the lessons we learned and the challenges that we are still facing.
The ongoing R&D effort provided an understanding of some of the constraints limiting the charged particle timing resolution that can be achieved with hybrid planar silicon pixels.
Considerations and results on these aspects will be presented lastly.

Author: Dr AGLIERI RINELLA, Gianluca (CERN, European Organization for Nuclear Research)

Co-authors: KLUGE, Alexander (CERN, European Organization for Nuclear Research); MARTIN, Elena (Universitè Catholique de Louvain); KAPLON, Jan (CERN, European Organization for Nuclear Research); PERKTOLD, Lukas (CERN, European Organization for Nuclear Research); FIORINI, Massimiliano (CERN, European Organization for Nuclear Research); NOY, Matthew (CERN, European Organization for Nuclear Research); MOREL, Michel

(CERN, European Organization for Nuclear Research); JARRON, Pierre (CERN, European Organization for Nuclear Research)

Presenter: Dr AGLIERI RINELLA, Gianluca (CERN, European Organization for Nuclear Research)

Session Classification: Front-end Electronics

Track Classification: Front-end Electronics