A concept for power cycling the electronics of CALICE-AHCAL with the train structure of ILC

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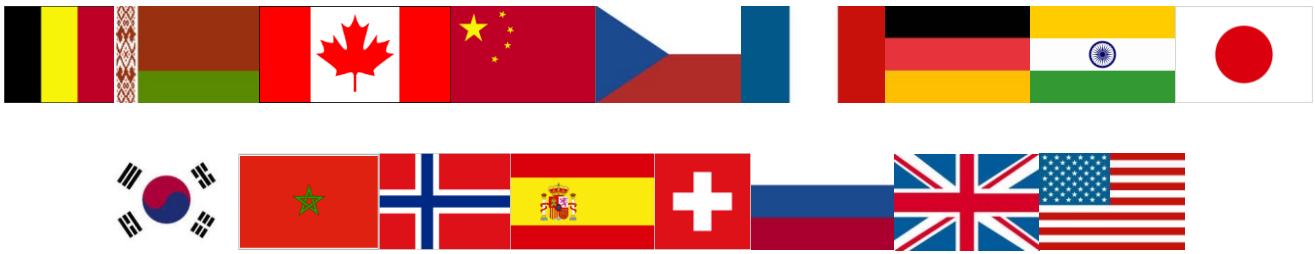
For CALICE collaboration

Chicago , June 11th, 2011



HELMHOLTZ ASSOCIATION

DESY

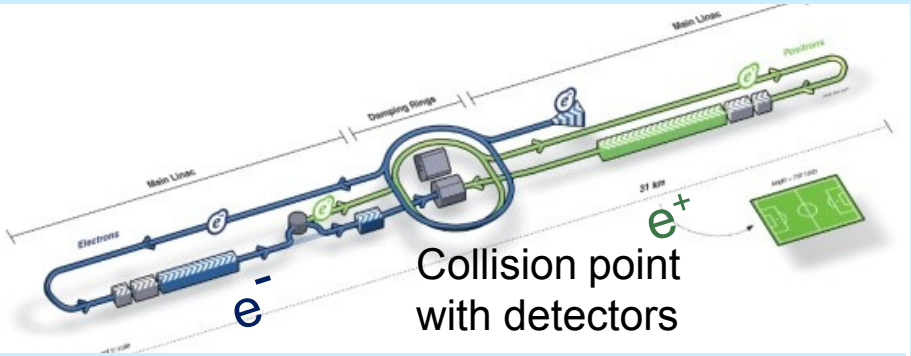
Outline

- Introduction: ILC, ILD, AHCAL for CALICE
- Motivation for power cycling
- Building blocks for power cycling
- Summary

Accelerator and Detector for e^+e^-

ILC: International Linear Collider

e^+e^- collider with 0.5 -1 TeV

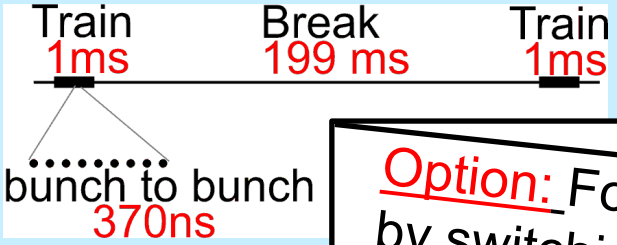


Technology:

- Superdonducting cavitities 1.3 GHz
- Bunch structure within trains

  1ms long trains, 199ms break, ….

  bunch to bunch 337ns



Option: For factor 100 by switching off the fast analogue electronics for 99.5% of the time

ILD: International Large Detector

e^+e^- needs precise detectors

$$\Delta E/E\ (jet) = 30\%/\sqrt{E(jet)}$$

Concept:

Particle flow algorithm

$$E = \sum_{charged} P_i + \sum_{neutrals} E_i$$

Measure showers of individual particles

Technology:

- High granularity calorimeters
- e.g. CALICE-AHCAL-barrel

  4 million readout channels

  60 thousand channels per m^3

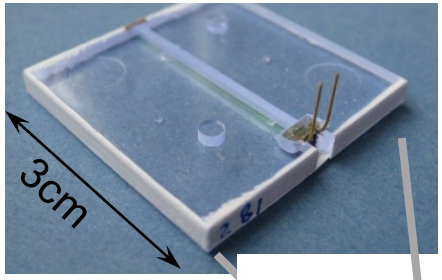
Need

Low power per channel: 40µW/channel can be reached by power cycling

AHCAL: Analog-Hadron- CALorimeter for ILD

Scintillator tiles

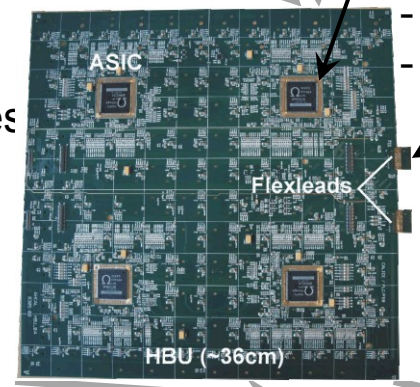
with SiPM readout



Plugged to
the back of a

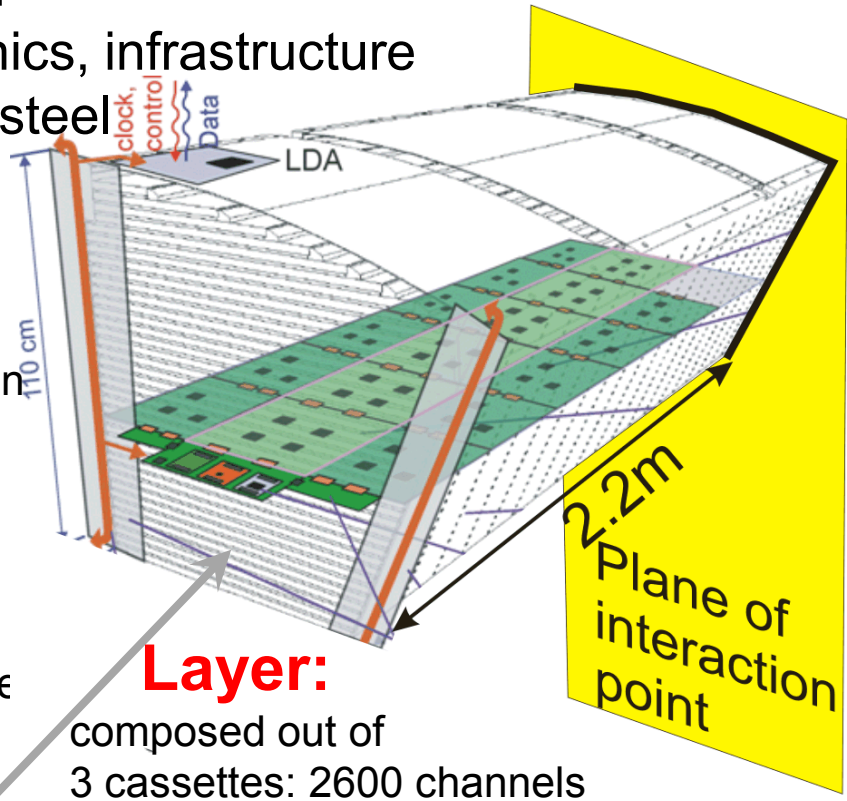
Readout board

12 x 12 tiles
36x36 cm^2



Sampling sandwich with

48 layers each
- 3 mm scintillator
- \+ 2.5 mm electronics, infrastructure
- +12 mm stainless steel



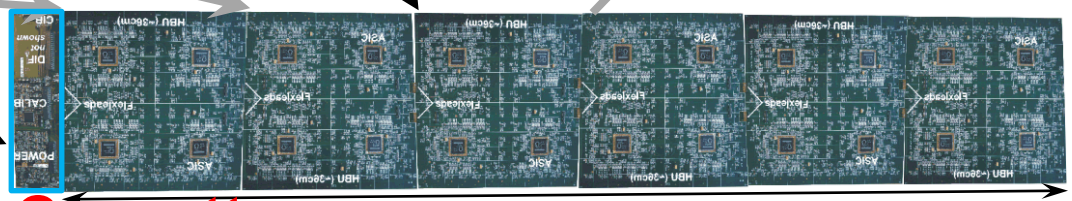
ASIC's for
- analogue signals,
- local storage while train
- ADC's
- data transfer

Interconnects with
flex foils
for signals,
GND and powe

Layer:

composed out of
3 cassettes: 2600 channels

Control electronics
and power
connections



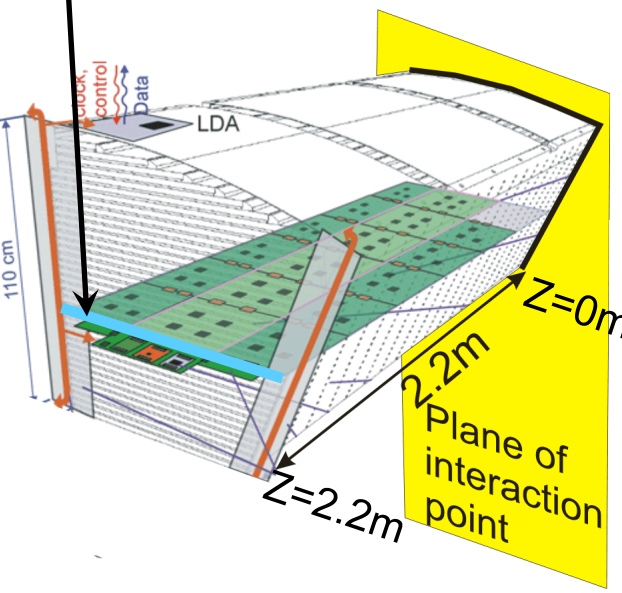
Cassette: 2.2m long structures: 864 channels

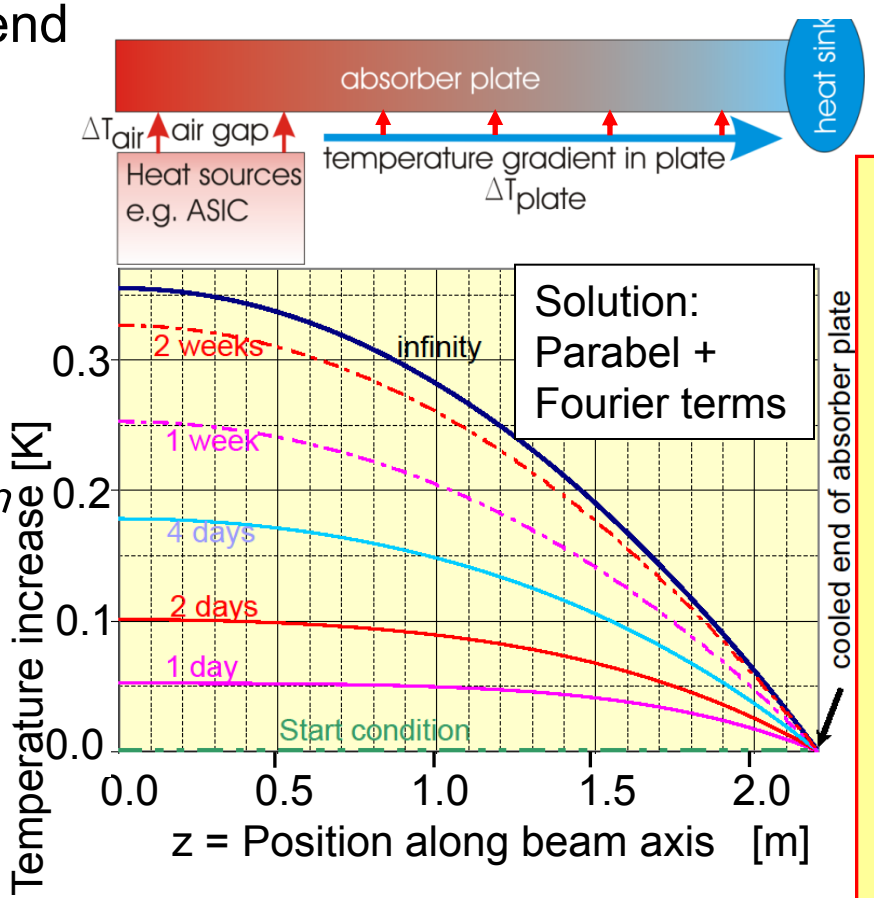
Motivation: Power Cycling to avoid active Cooling

Mechanical design constraint:

- No cooling within calorimeter
  to keep homogeneity and simplicity
- Cooling only at service end

$$\frac{\partial T}{\partial t} = \frac{1}{heat\ cap./area}\left.\frac{power}{area}\right|_{electronics} + heat\ conductivity\ \frac{\partial^2 T}{\partial z^2}$$





With
- Stainless steel
- Long structure

Heat

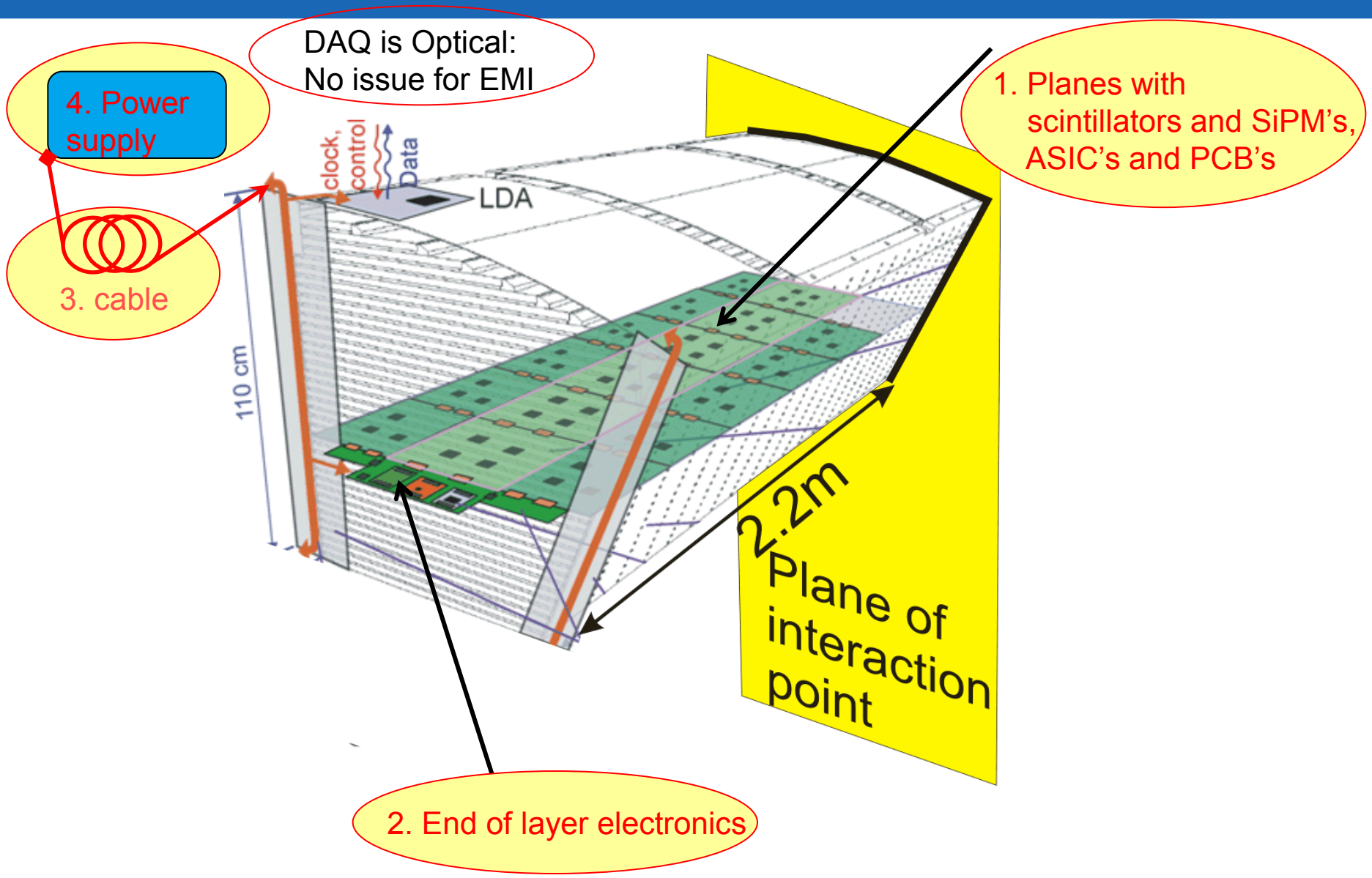
Electronics with
1% power cycle
25µW/channel
SiPM I_{dark}
+15µW/channel

⇒ **Need**

Power cycling
To keep heat up
below 0.5⁰C

- No heat transfer radial
  "bad due to sandwich"
- Cylindrical symmetry
- Symmetry at IP-plane

Building Blocks for the Power System

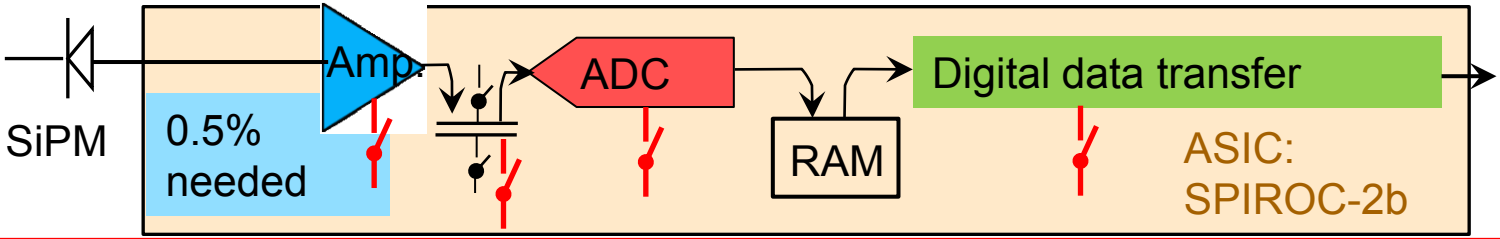


ASIC for fast SiPM Signals consuming Low Power

L. Raux et al., SPIROC Measurement: Silicon Photomultiplier Integrated Readout Chips for ILC, Proc. 2008 IEEE Nuclear Science Symposium (NSS08)

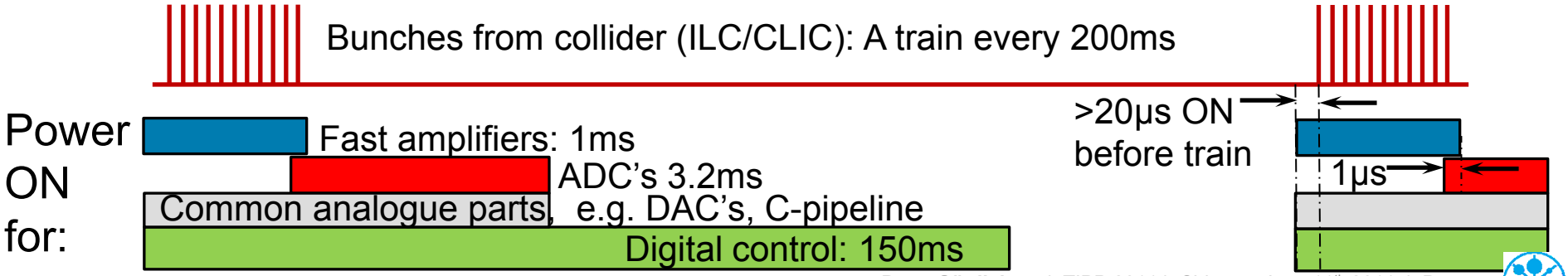
Functional tasks of the ASIC:

- Amplify the SiPM signal and generate self trigger
- Store an identified signal: 16 per train: capacitor pipeline
- Digitize
- Multiplexed data transfer even with more ASIC's



Algorithm for power cycling:

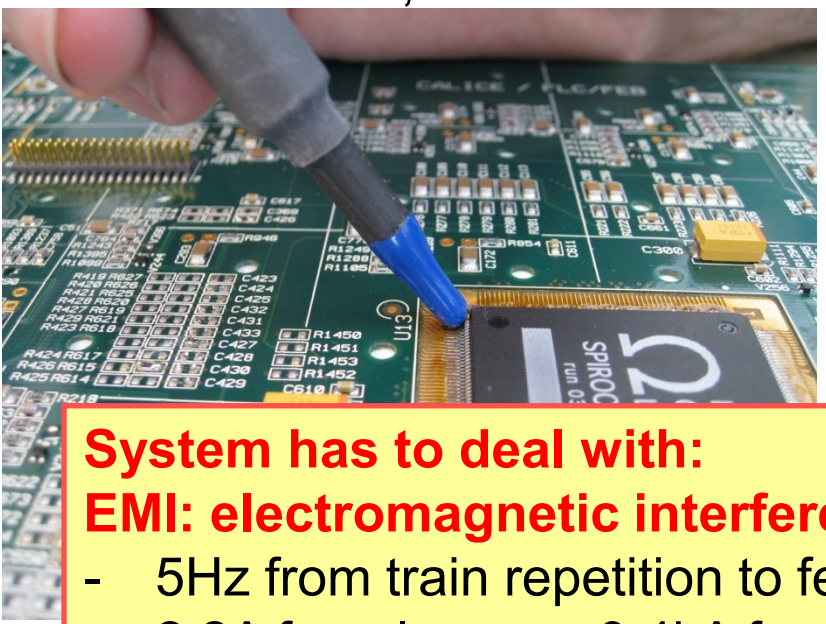
The ASIC **switches the current** of the functional blocks OFF.
ASIC gets supplied **all the time with voltage**.
PCB electronics and instruments **stabilize the voltage**



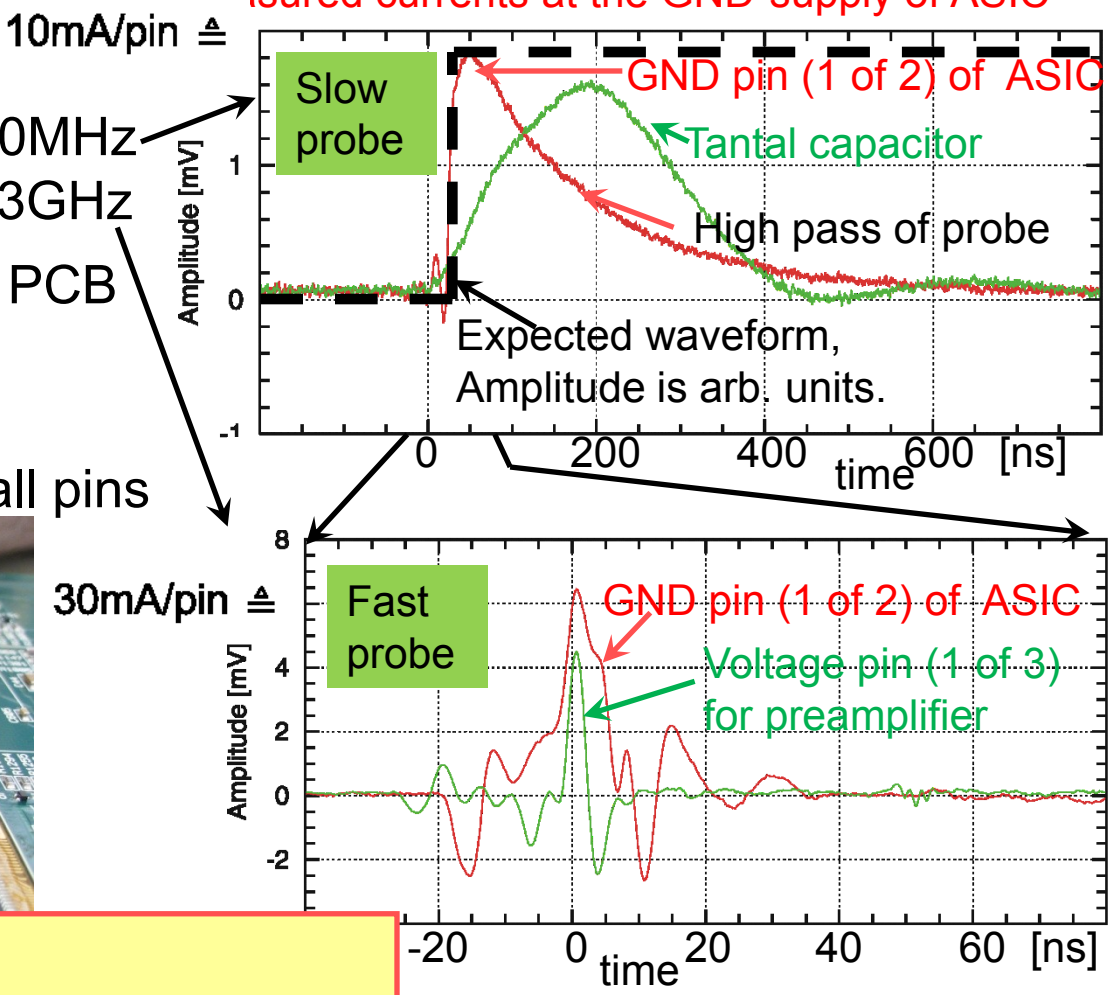
ASIC as current switch

Measurements:

- Inductive current probes
  - Slow: 0.25 – 50MHz
  - Fast: 30MHz-3GHz
- Setup: ASIC+ capacitors on a PCB
- Expectation is
  - ~ 1mA/channel
  - ~40mA/ASIC, summed over all pins



Measured currents at the GND-supply of ASIC



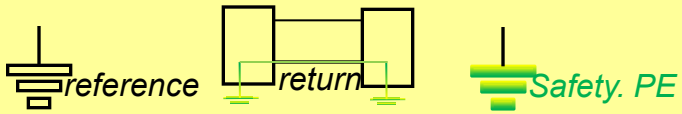
System has to deal with:

EMI: electromagnetic interference

- 5Hz from train repetition to few 100MHz
- 2.2A for a layer, 3.4kA for AHCAL-barrel

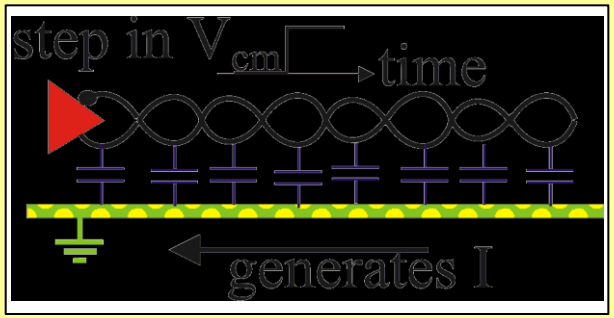
Electro Magnetic Interference in a Power Cycled System

Reference ground:



- Need good definition
- Any induced/applied current produces voltage drops
- Separation between reference / power return / safety
  or controlling currents
  and keeping currents within "own" volume and instrumentation

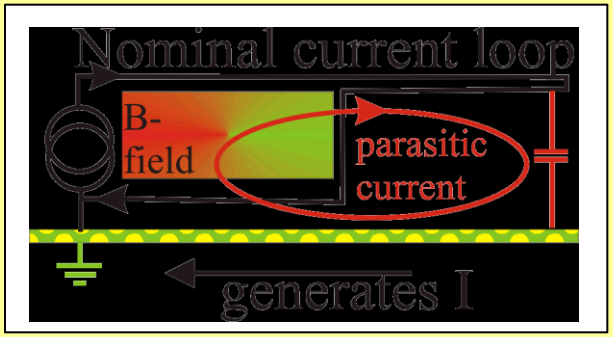
Capacitive coupling



To do:

- Keep common mode voltage stable
- Guide induces currents to source
- Keep GND-reference closer
  than foreigns

Current loops



To do:

- Controlling return currents
- Keeping loops small
- Avoid overlapping with
  foreign components.

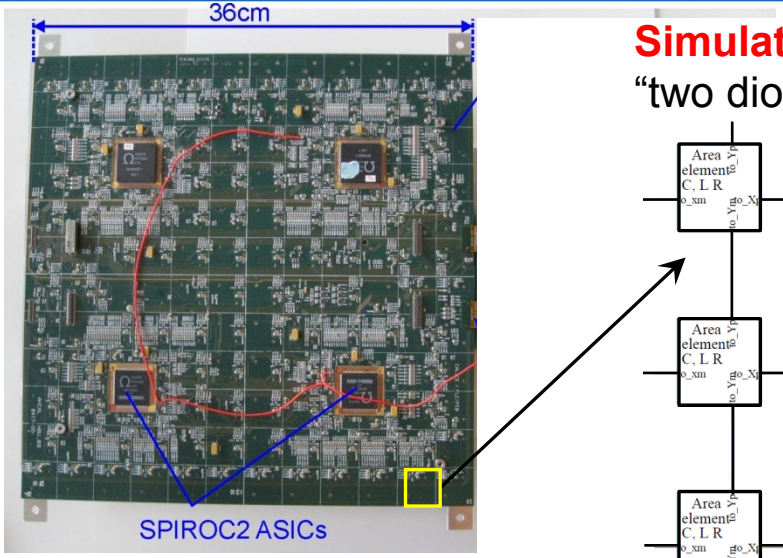
Guideline: Avoiding emission avoids in most cases picking up of noise

Keeping the high Frequencies local

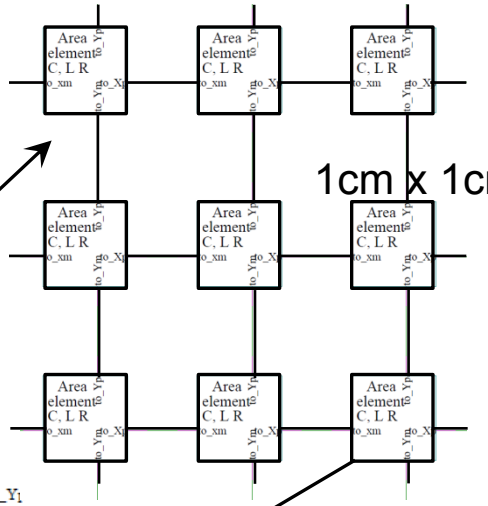
36 x 36 cm PCB
with scintillators, SiPM's LED

144mA switched current

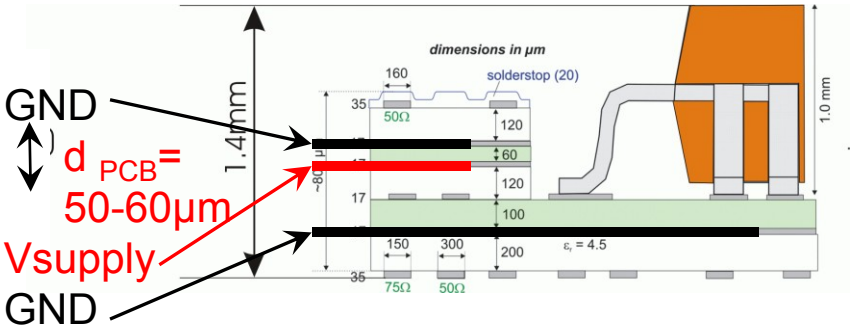
Part of a thin cassette between absorber layer of HCAL

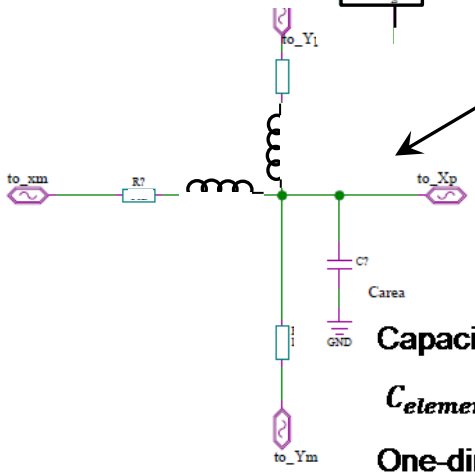


Simulation model:
"two diomensional delay line"



Layer structure of PCB:





By that one get
- a thin PCB and also
- **A good high frequency capacitor 60pF/cm²**
- Layout with short distance to via maintain the performance.

Capacitor well known:

$$C_{element} = \varepsilon_0 \varepsilon_r \frac{Area_{element}}{Thickness_{PCB-layer}}$$

One-dimensional delay well known

$$time_{element} = c\sqrt{\varepsilon_r}\, length_{element}$$

Inductivity:

$$L_{element} = time_{element}^{\ 2} / C_{element}$$

Voltage for ASIC stabilized by local discrete Capacitors

Capacitors mounted to the 36x36cm² PCB

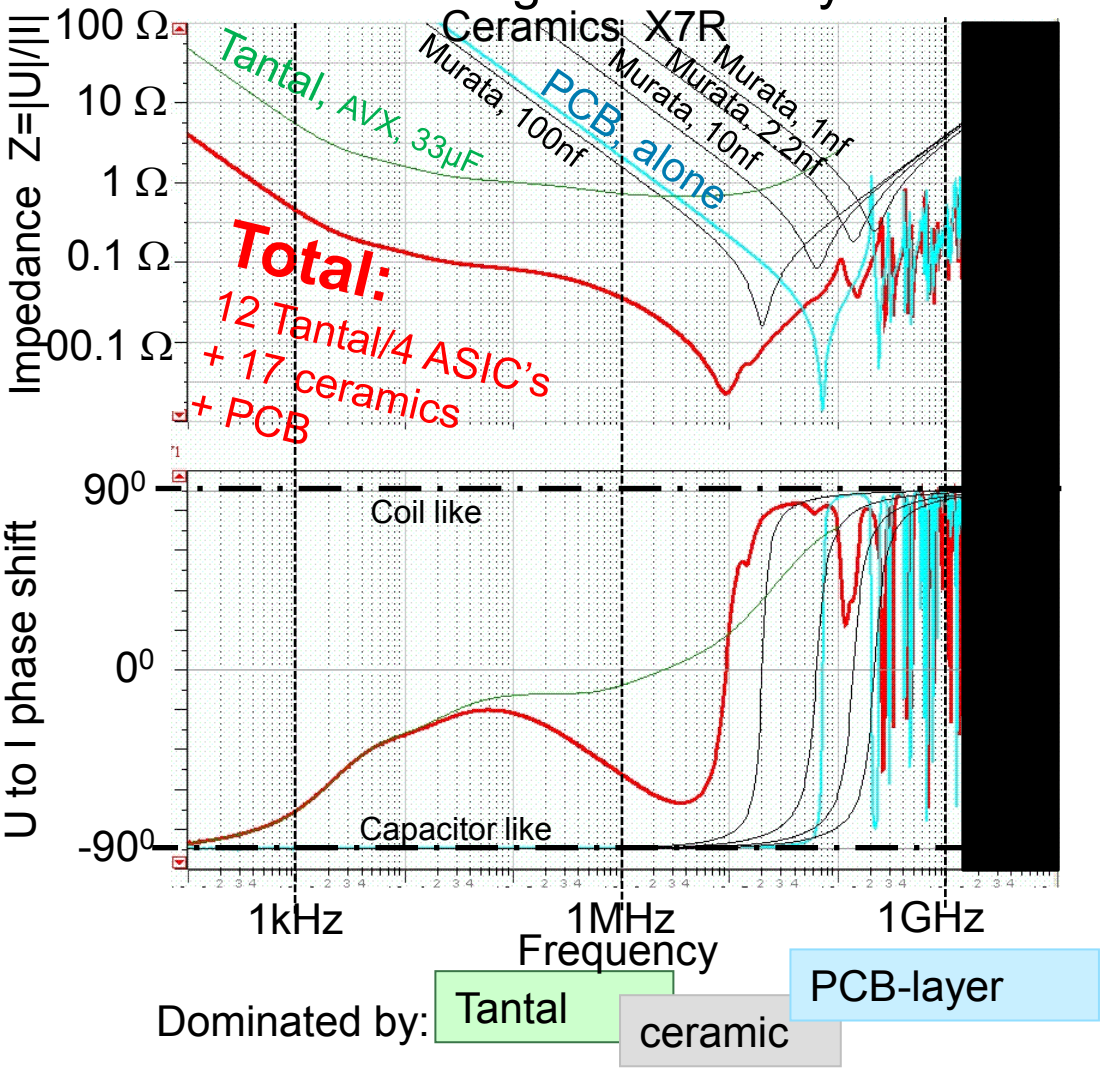
ASIC is supported over wide frequency range with Z< 0.1Ω
144mA generates <20mV

Oscillations are dumped for wide frequency range with phase ≠ ±90⁰

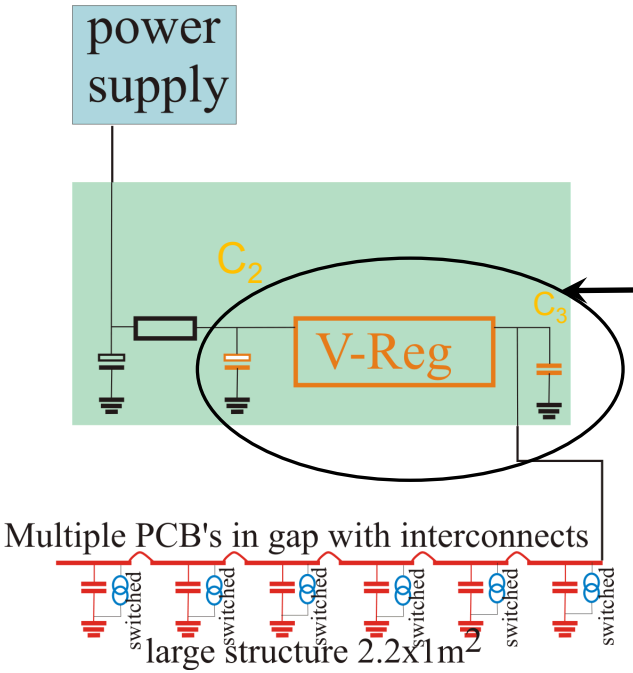
Trust in simulation:
- <1.5GHz=(1/10) granularity
- No resistive behavior of ASIC is included. That over estimates the resonances at high frequencies

Result:
- Locally good for > 10kHz
- Additional effort < 10kHz

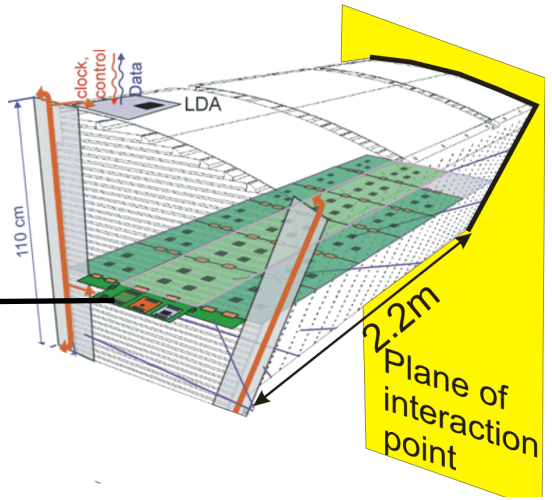
Simulation of voltage induced by current



Low frequency charge storage for < 10kHz



At end of layer,
there is a bit of
- space
- cooling



Concept:

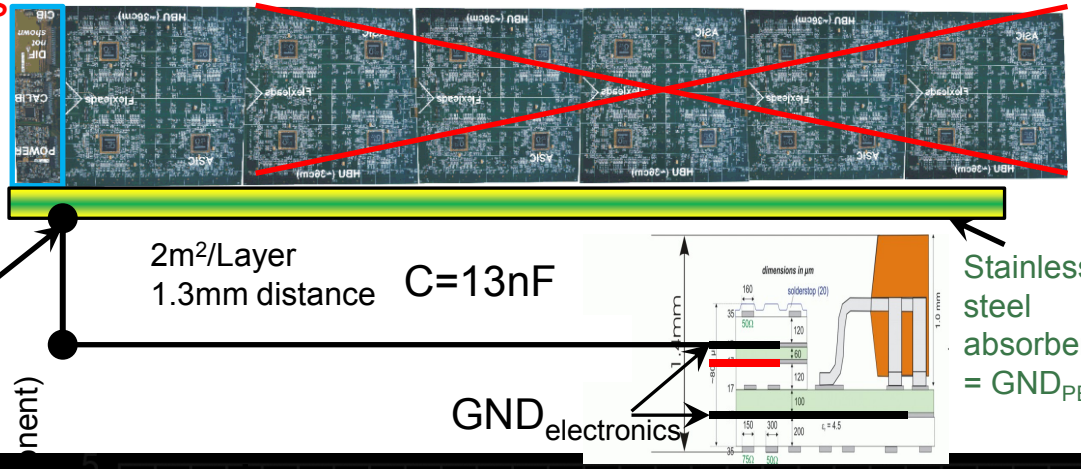
- Charge for the train stored in a capacitor C_2
- Voltage drop allowed ~ 0.6V
- Fast voltage regulator $\gg 10kHz, \ll 10\mu s$
- Charge for faster reaction is within the distributed capacitors + C_3

C_2 = 3.4mF bank of few Tantal
a voltage regulator with external FET > 2A
C_3+distributed = 2mF

Voltage at ASIC: Measurement

Reduced test setup: Control board, 1 interconnect, 1 board

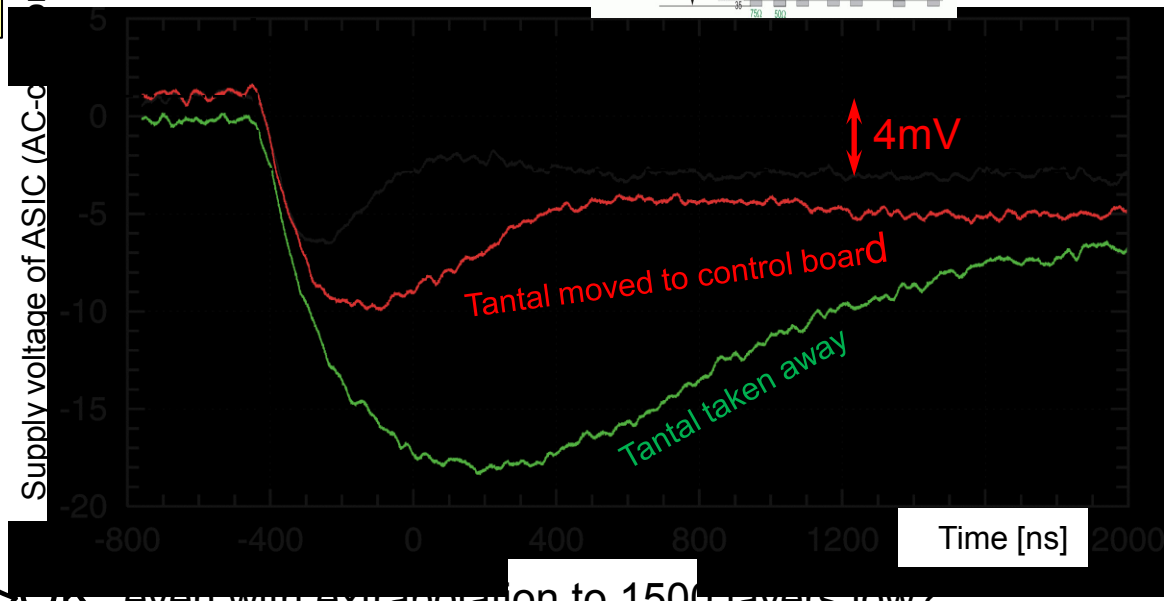
Control electronics for layer



Definition of GND-point:
- good for keeping sensitive SiPM's stable
- single connection to reduce currents in GND_{PE} system

Voltage step:
- Measured 4mV, 400ns
- Extrapolate to full system
  < 80mV at far end

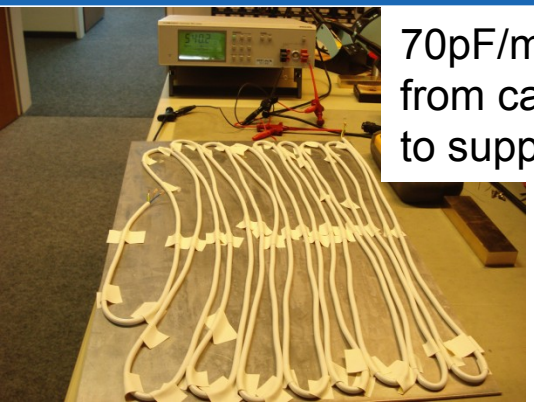
OK for operation,
over-,undervoltage, time, …



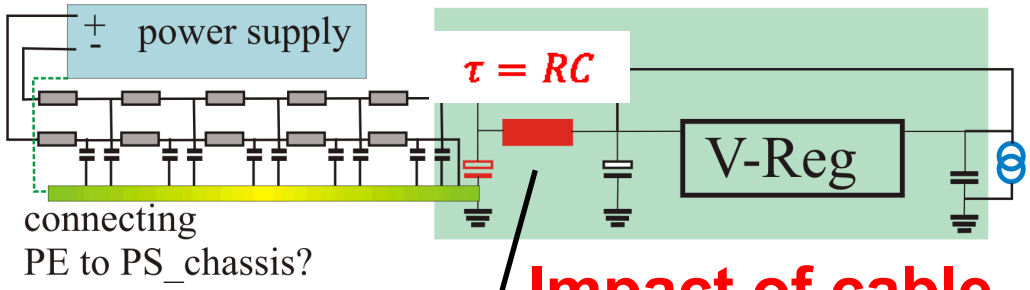
Induces current into GND_{PE},
if step is on $GND_{electronics}$
  < 2 mA per layer

⇒ OK, even with extrapolation to 1500 layers low?
Investigations of reason and improvements possible, to be watched

Integrating to Infrastructure



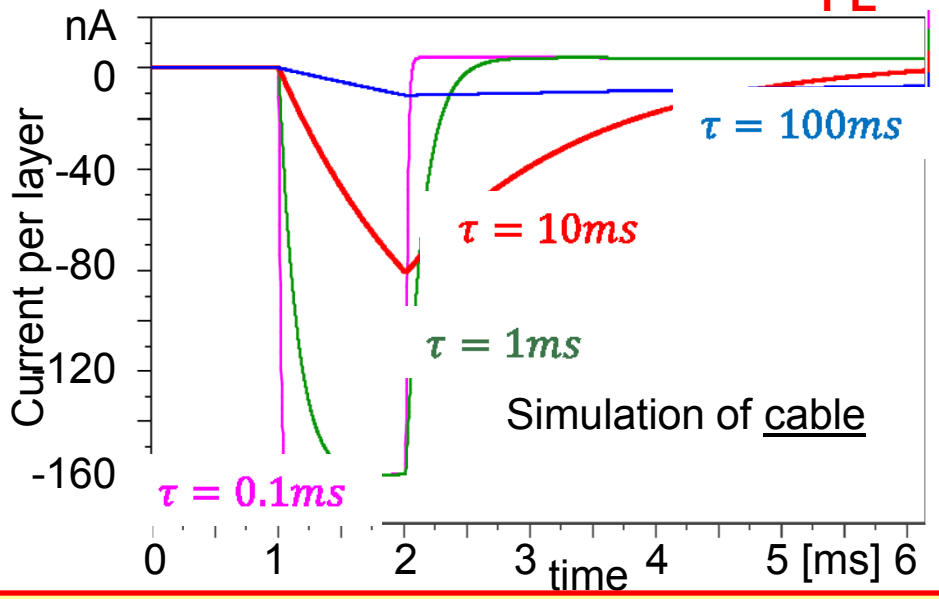
70pF/m
from cable
to support



50m cable, 1mm², on a cable support

ASIC
as
switched
current
sink

Current induced into GND_{PE}



With 1500 layers of AHCAL: I_{PE}=120μA
Really small, but not including all parasitics!
Don't be too reluctant in EMI-rules

Impact of cable

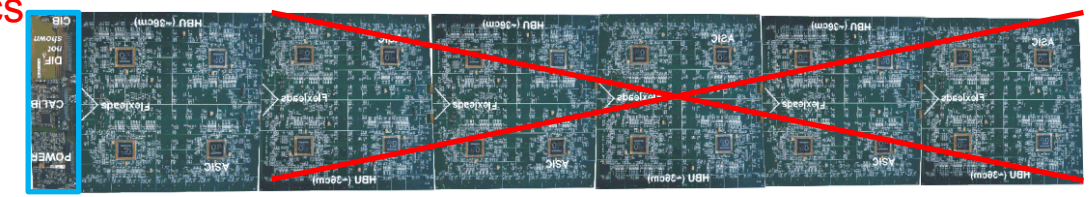
is a combination of choises:

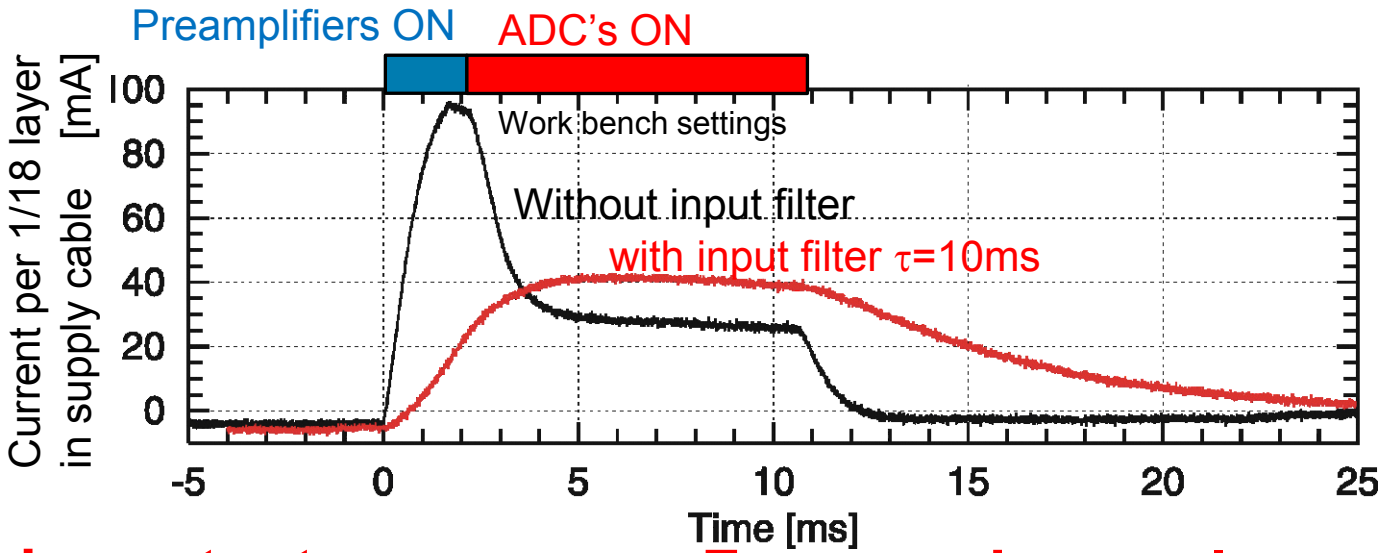
- Input filter: R=10Ω, C=1mF
  reasonable mechanical size
  EMI better τ=100ms
- Power supply behavior
  here neglected capacitance to PE, might be 2 order of magnitude larger than cable!
  Here: ideal V-source
- Mechanical integration and galvanic isolation
  per (group or) layer
  and pair of wires for it

Current in Supply Cable

Reduced test setup: Control board, 1 interconnect, 1 board,
Short cable to laboratory supply

Control electronics
for layer





Input filter important to
lower amplitude fluctuations
and remaining frequencies within cable
Inportant: EMI-crosstalk to others

Frequencies are low
Electronics like to have larger τ
to smoothen further ⇔
Mechanics easier in service-hall

Summary

- Detectors for Linear Colliders requires many channels with low power
- Train structure allows 99% time to be OFF: Factor 100 in critical regions
- Coherent fast switching ON/OFF of high current:
  CALICE-AHCAL: 2.2A*layers : 3.4kA for the barrel
  5Hz to few 100MHz
- System aspects at local design
  - Local defined return-pathes for current
  - Local charge storage for wide frequency range

  that keeps
  - the impedance small
  - the currents leaving a defined volume small with slow rise times
- System aspects within the infrastructure
  Lower frequency part handled by cables and power supply
  Good integration of power supplies and cables.
- Simulation leaves many parasitic effects out
  Underestimates the high frequency EMI-disturbance
  …. Experiments, concepts to be better than simulation promises
- Experimental setups and integration into ILD to be continued