Design of the ATLAS IBL Readout System

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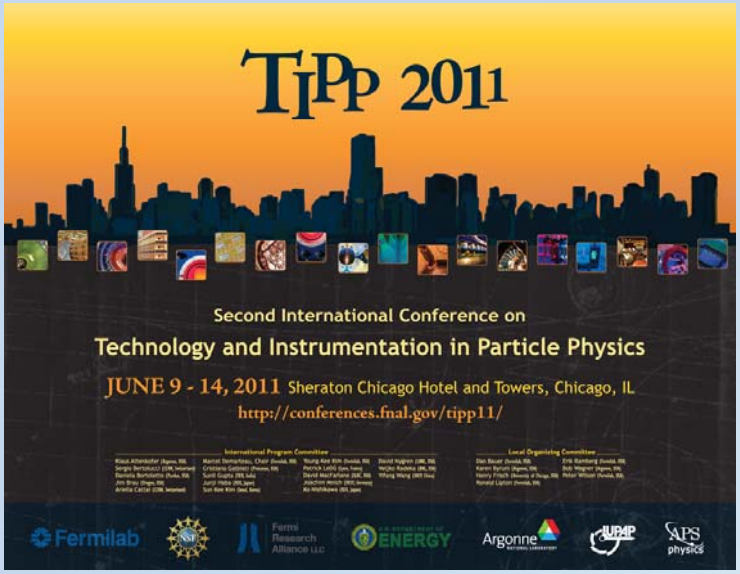
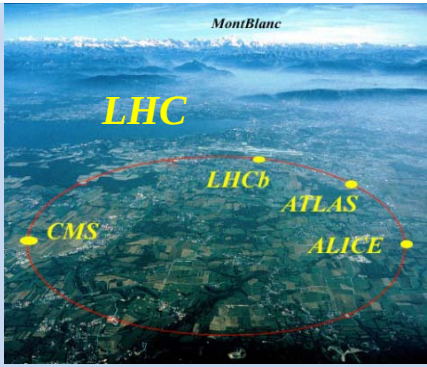
Outline:

- Detector Introduction
- Architecture Description
- Comparison to the Present Pixel System
- Test, Readout and Calibration Procedures
- Roadmap, Status and Outlook



1) INFN Bologna
2) CERN
3) Fachbereich C Physik, Bergische Universitaet Wuppertal
4) University of Bologna
5) II. Physikalisches Institut, Universitaet Goettingen
6) LNBL, Berkeley, U.S.A
7) ZITI, LS Informatik V, Heidelberg University, Mannheim
8) INFN Genova

The ATLAS Detector



Barrel region

25 meters diameter

Endcap region

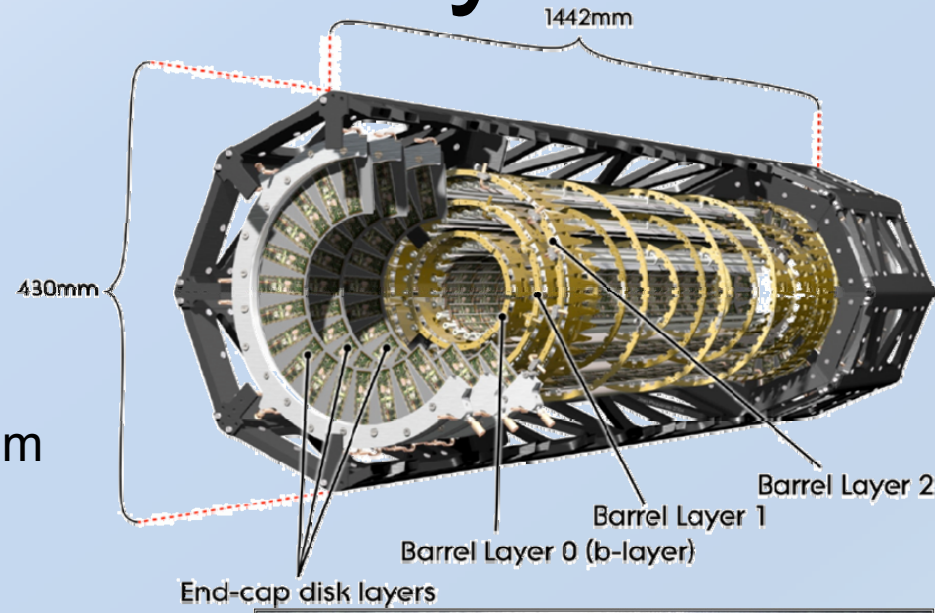
Endcap region

44 meters length

ATLAS Insertable B-Layer

Atlas Pixel Detector

- The innermost detector with
- 3 tracking points up to $|\eta|<2.5$ layers barrel and 3+3 disks
- 1744 modules with 46080 pixel 50x400 μm^2
- 80 millions channels total.
- 16.9 KW cooled via an evaporative C_3F_8 system

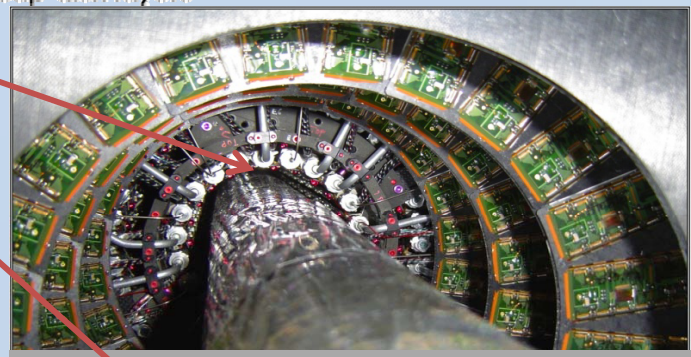


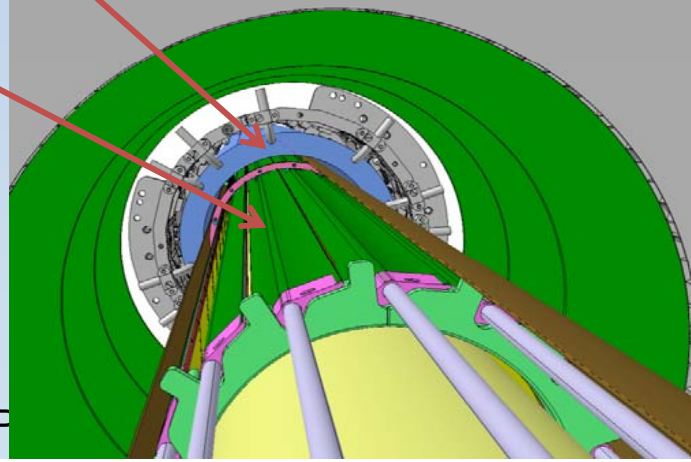
IBL:

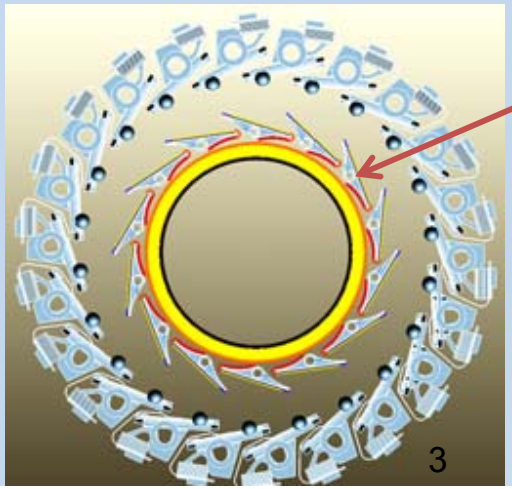
- Add a fourth innermost layer
  - New smaller Beryllium Beampipe
  - Old Pixel detector kept in till Phase 2

Time schedule

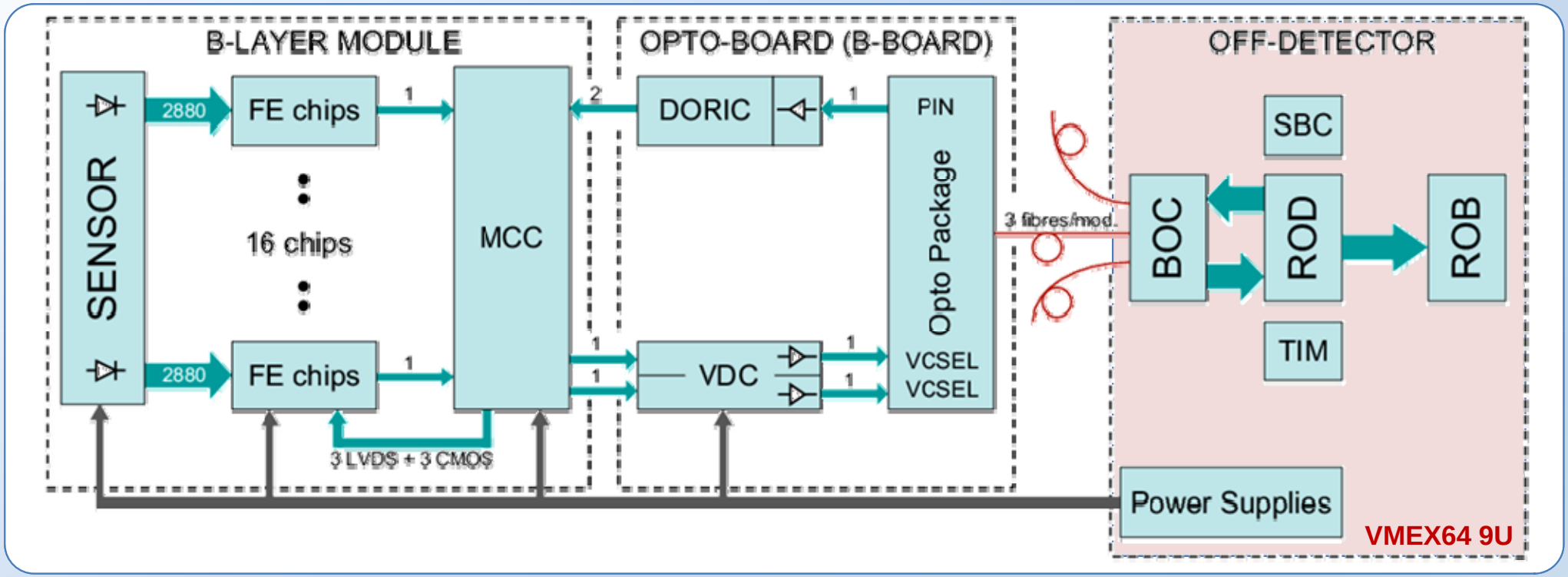
- 2015-17 ➔ moved to the shutdown in 2013-14 !!!







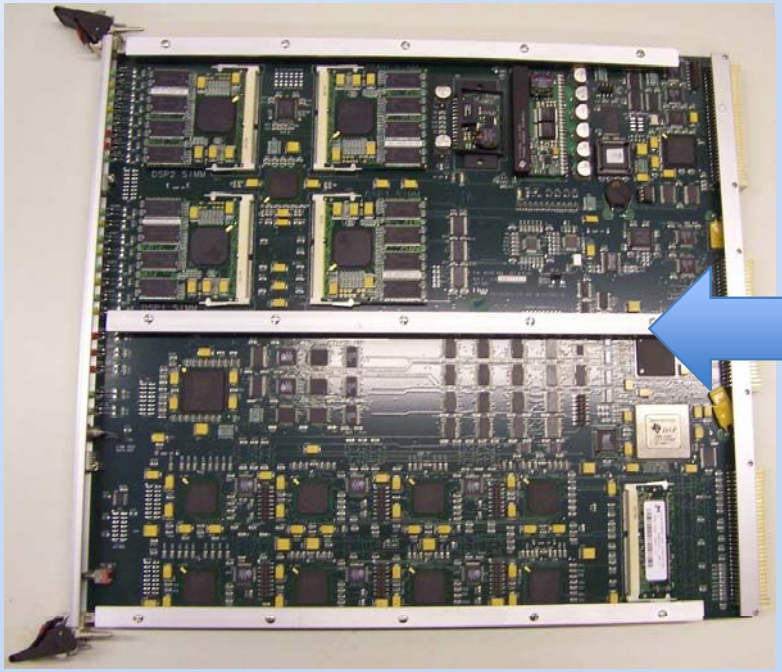
Pixel Readout Scheme



- Each module has 16 FE-chips and 1 module controller chip
- Data transferred to and from modules via 80m optical link
  - 1 downlink per module, 1 uplink for L1, L2, Discs, 2 uplinks for B-Layer
- Each VCSEL array services 6 or 7 modules (both on-detector and off-detector)
- Readout System VMEx64:
  - Back of Crate (BOC) + Readout Driver (ROD)

Present Pixel ReadOut

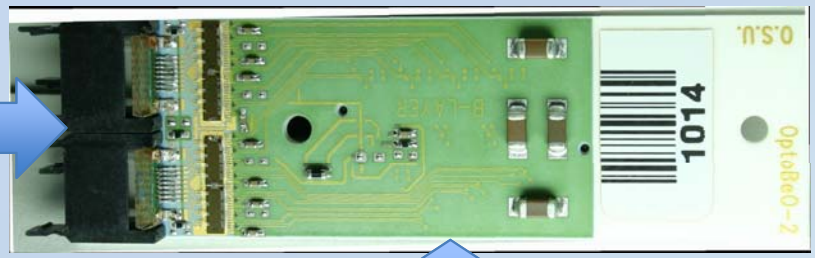
- FE Modules can send data with 40(L2), 80(L1, Disk) or 2x80 Mbit/s(B)
- 4 LVDS connections to Module: Clock, Data In, 2 x Data Out
- OptoBoard services 6/7 modules, converts electrical to optical
- BackOfCrate card encodes clock/data, decodes in 40Mbit/s streams
- ROD with 4 + 1 Digital Signal Processors (4GFlops) and 1GB RAM



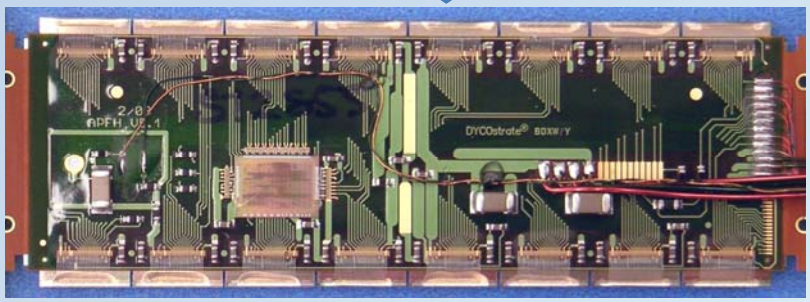
ROD

BOC

Optoboard



Module



New Frontend Chip (FE-I3 → FE-I4)

The smaller radius of the IBL and potential luminosity increase results in higher hit rate

FE-I3 (present pixel detector)

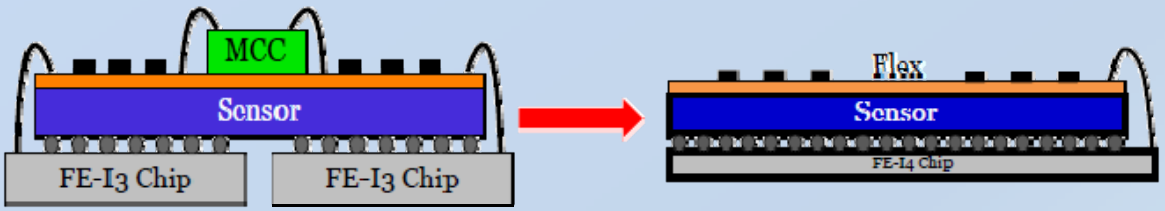
- Column drain architecture saturated
- Total inefficiency would be very high for IBL (>90%) assuming Phase I upgrade of the LHC

FE-I4 (IBL)

- New digital architecture with local column buffer
- Smaller pixel size
- Thinner chip with reduced inactive surface
- 160 Mbit/s + 10b/8b data encoding

IBL

- 14 staves; each with 16 x 2 chips.



	FE-I3	FE-I4
Pixel Size [μm²]	50x400	50x250
Pixel Array	18x160	80x336
Chip Size [mm²]	7.6 x10.8	20.2 x 19.0
Active Fraction	74%	89%
Analog Current [μA/pix]	26	10
Digital Current [μA/pix]	17	10
Analog Voltage [V]	1.6	1.5
Digital Voltage [V]	2	1.2
Pseudo-LVDS [Mb/s]	40	160

New (IBL) Readout

Motivation:

- New front-end chip: Higher data bandwidth + 10bit/8bit encoding
- Limited Spares + components obsolescence
- VME bandwidth limit for monitoring and calibration procedures
- Newer components/technologies available

Goal:

- Keep concept (architecture + integration in ATLAS, TTC) etc:

  → IBL will run as part of Pixel Detector within ATLAS

➔ **Develop new BOC + ROD**

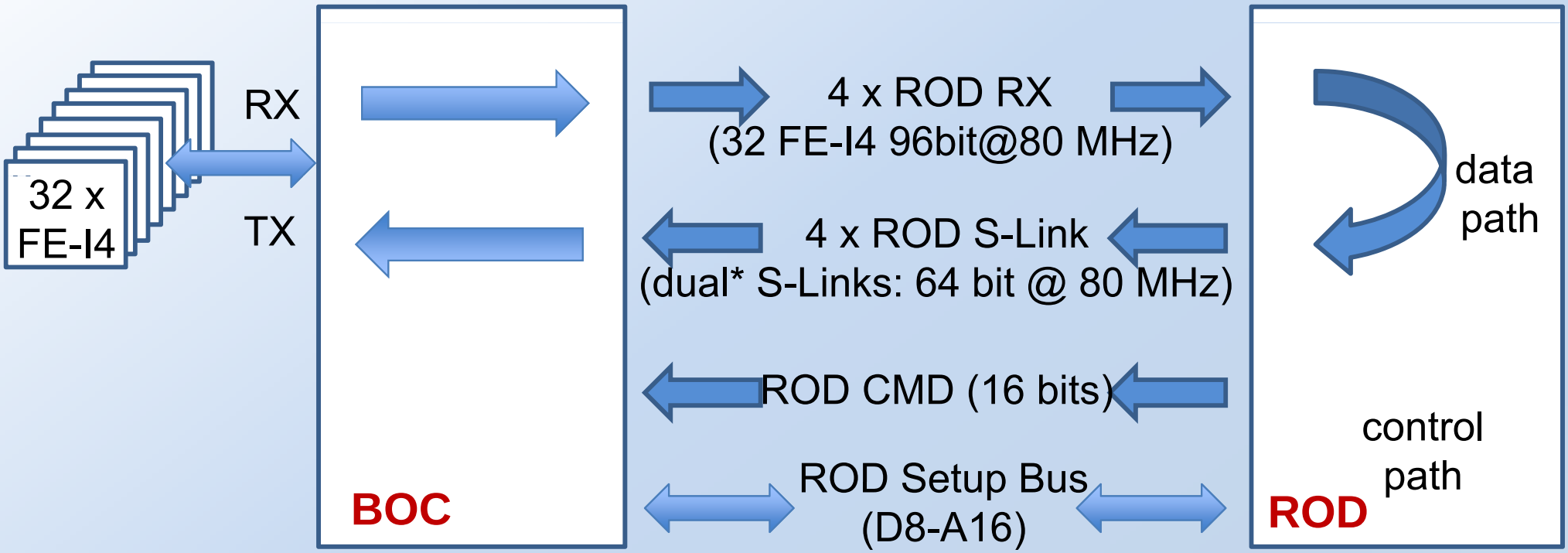
- Use up-to-date technologies and components improving integration and bandwidth
- 1 Master DSP + 4 Slave DSP (old ROD)→ FPGA Virtex + PPC core

✓ Only one simulation environment needed

✓ Move most of the time consuming processing outside on external PC farm exploiting commodity hardware (PCs) and/or GPU

✓ Advantage in software maintainability (same environment as for offline software)

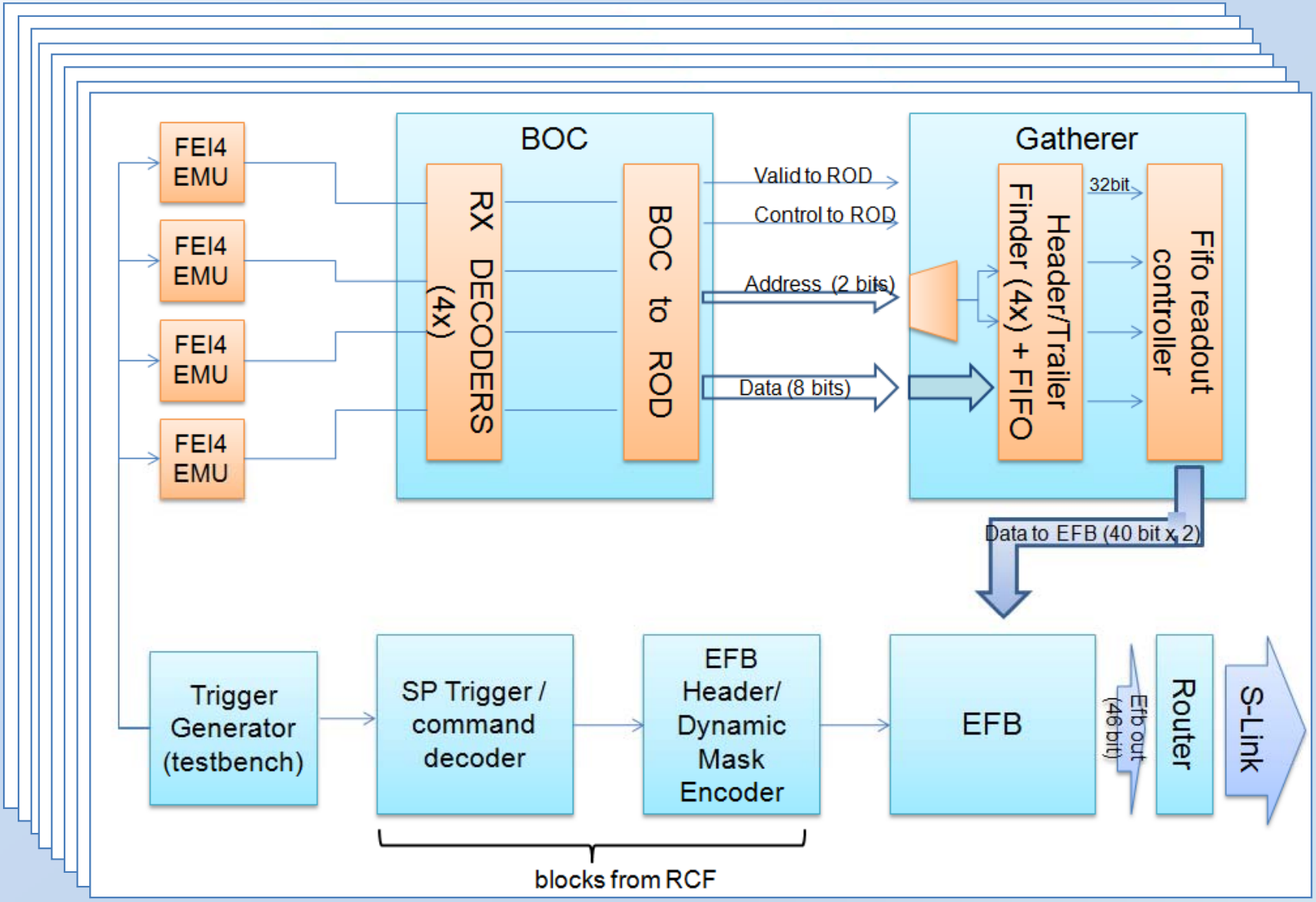
BOC-ROD Intercommunication



New vs Old System

- 4-fold integration (1 crate, 14 RODs for the full IBL system) keeping the same ATLAS environment (Trigger Timing Control and VME Single Board Computers)
- 4 Slave DSP + Master DSP ➔ Embedded PowerPC (in Virtex 5 FPGA)
  - homogeneous simulation environment (Master DPS still available)
  - New external GB links for external Calibration farm and programming
- Common off the shelf products (calibration farm, Tx Rx plugins)
- Backward compatibility (new ROD/BOC can be used for old Strip and Pixel det.)
- BOC ROD SSTL-3 or CMOS communication
- *Duplicated S-Link Output for existing DAQ (ROS) + FTK (Fast Tracking upgrade)

BOC–ROD Block Diagram



- Simulation of full chain
- Final system: One BOC-ROD pair: 8 of the above slices

FE Chip Calibration

- The analog part of the read-out electronics on the FE chips allows to adjust the threshold and the feedback current of the pixel read-out circuits to create homogeneous behavior
- For calibration well defined charges are injected into the preamplifier of each circuit and the comparator response is measured, this is repeatedly done for different charge values
- Measurement results are collected in histograms and analyzed

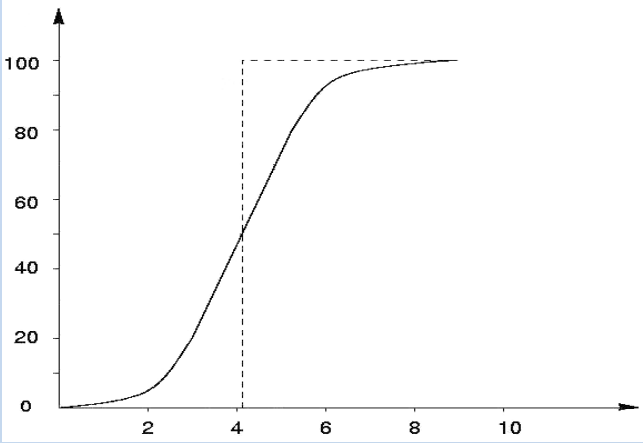
Present System:

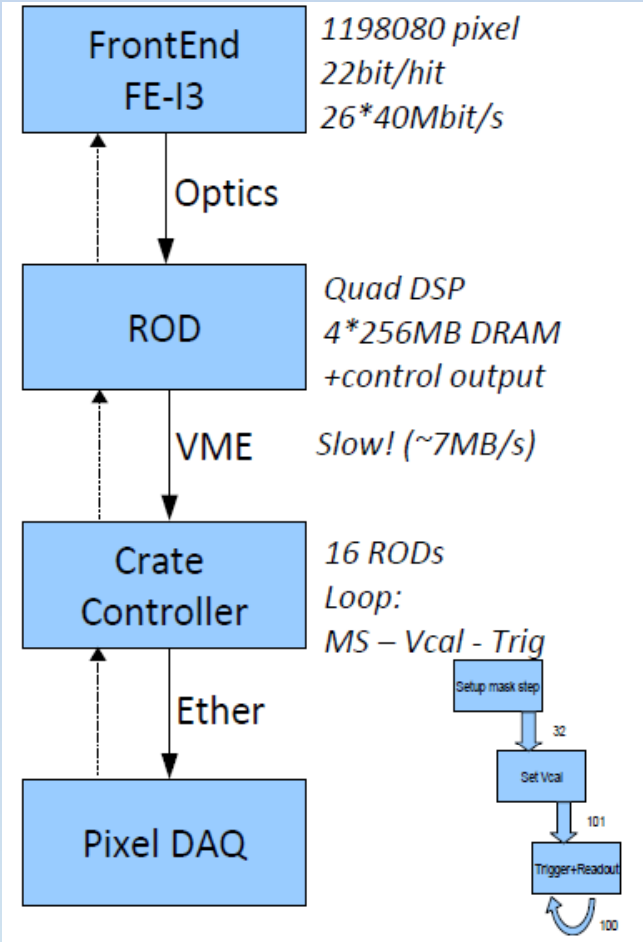
~10 minutes for one scan of 100 Vcals/Triggers

- Bandwidth Limitations (VME, fitting procedure)
- Occupancy, Time over threshold, $(ToT)^2$

New System:

- Faster control and data transmission to/from FE-I4
- Collect partial histograms on FPGA (for selected scans)
- Accumulate OCC, optional ToT and ToT^2 data per Vcal step
- No DSP use
- fast interface (GE) to DAQ + execute fit on remote processing unit, PC and/or GPU
- Improved flexibility for code development, more convenient tools compared to DSP environment





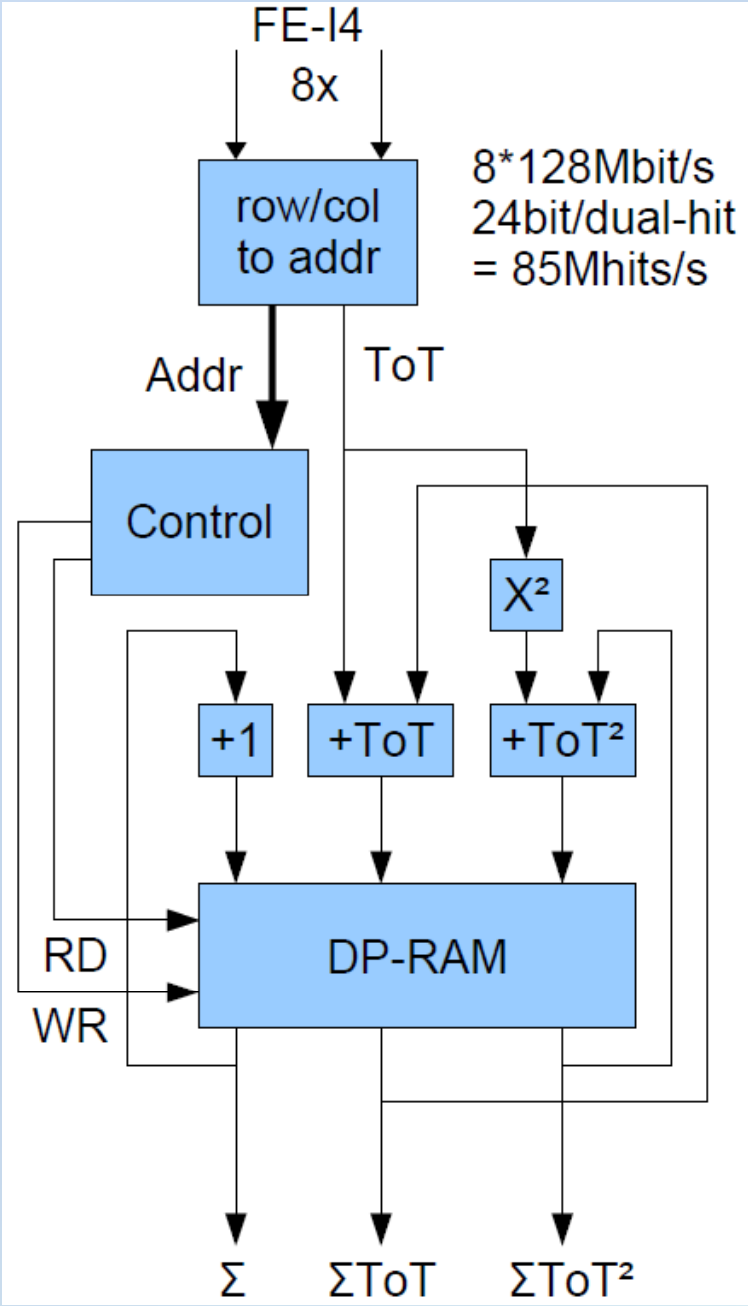
Histogramming on FPGA

Full simulation of histogramming on FPGA

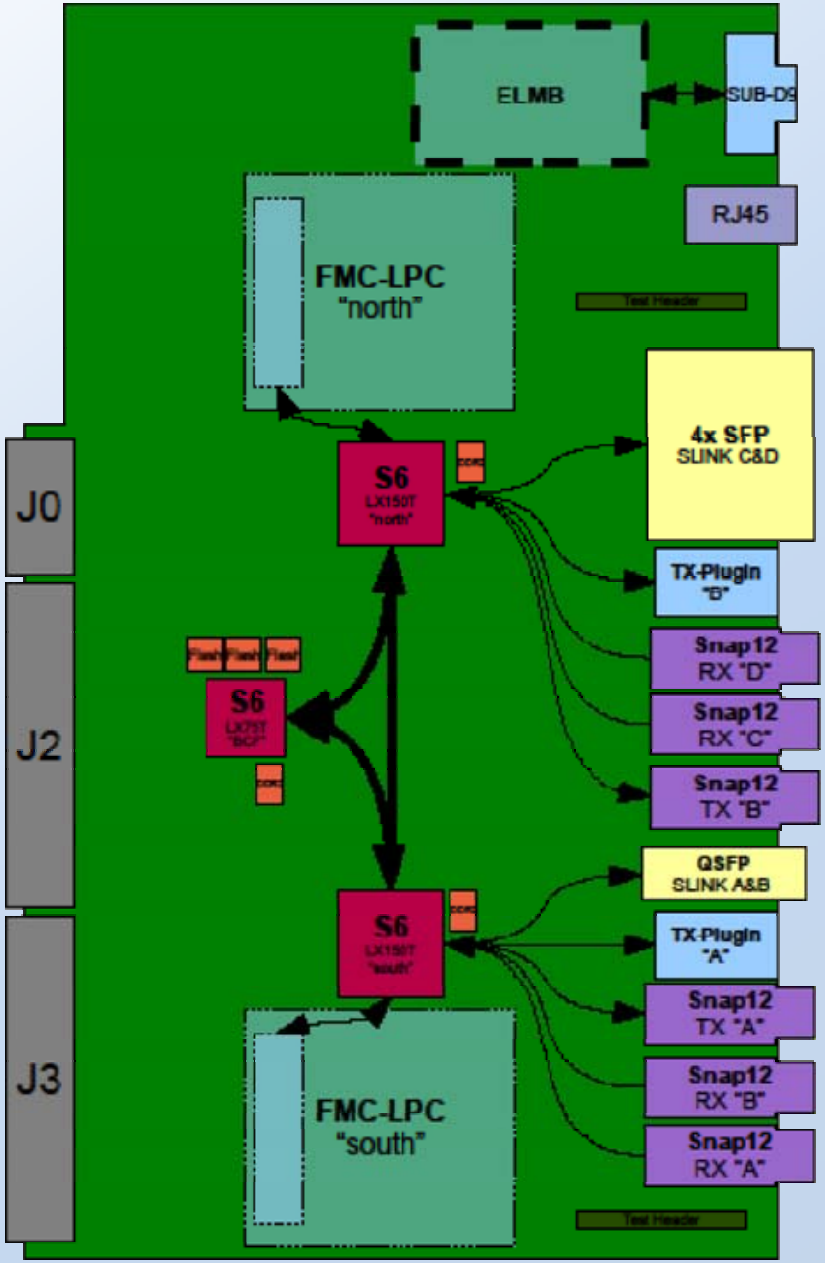
- Convert 24 bit FE-I4 format to direct addresses
- Pipelined update of Occupancy, ToT and ToT² sums
- RAM init during setup and readout
- 32k pixel on Spartan6-LX150T
  - DSP48A1s: 1%, 1 out of 180
  - BRAMs: 32%, 86 out of 268
  - slices: 1%, 191 out of 23,038
  - 100MHz operation
  - FE-I4: 2 units/FPGA & slower or 8 mask steps
- Readout after each Vcal step to GE/PCI

Histogramming

- Feasible on FPGAs with very little resource consumption (except for BRAM)
- Histogramming yields good data reduction, thus validating data transfer and analysis on remote processing units
- A lot of potential to accelerate the analysis by optimization of the code

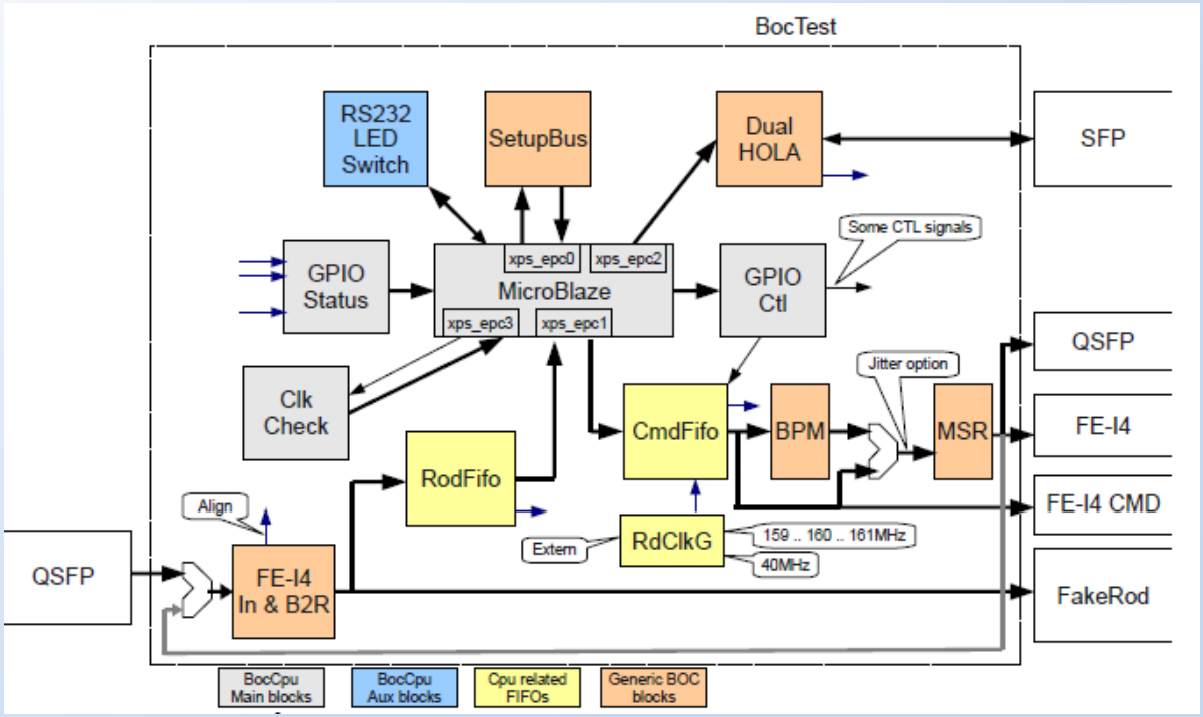


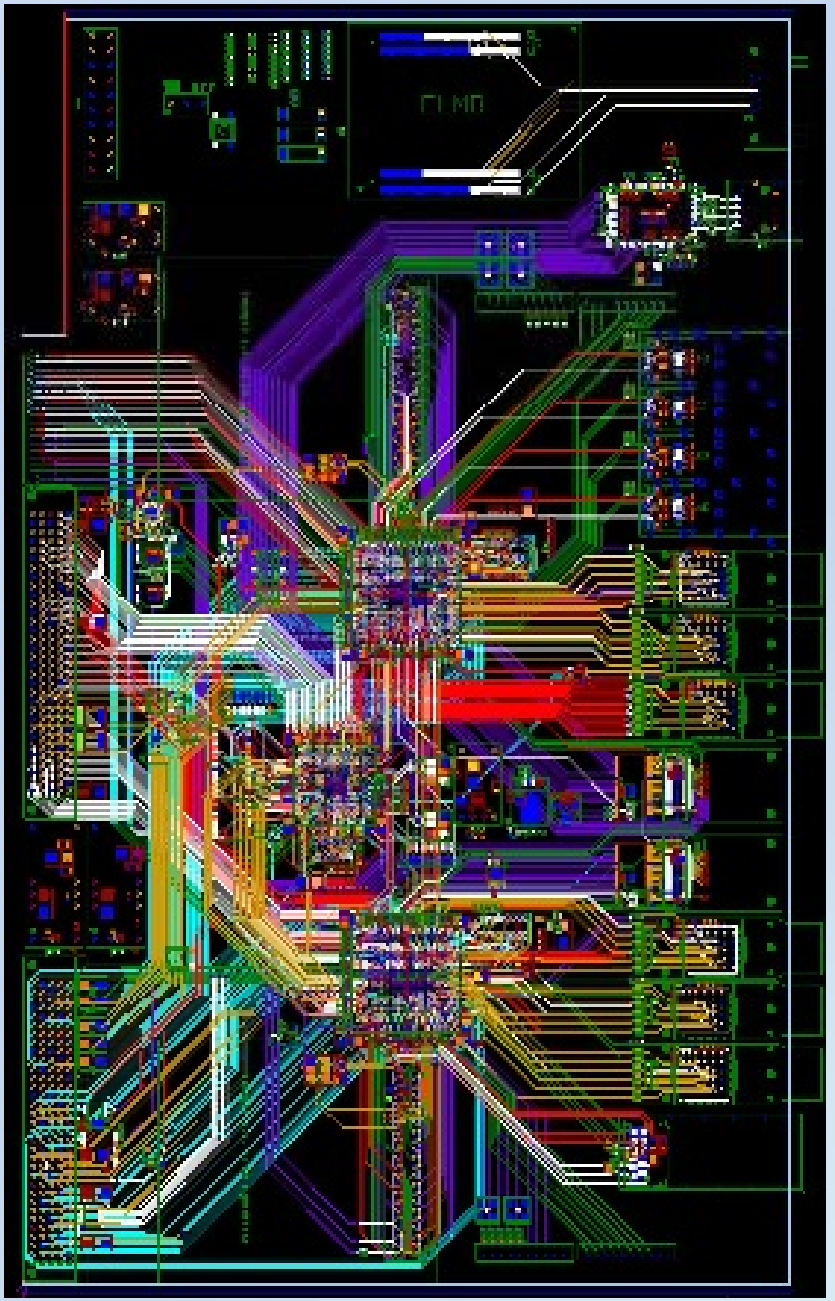
BOC Design



- Segmented into two functionally equivalent sections called “north” & “south”
- The heart/brain of each section is a Spartan6 LX150T device (BPM, synch)
- Receiving data from the FE via two Snap12 RX modules
- Configuration data is sent to the FE either by a Snap12 TX module or a TX plugin like the ones used on the current BOC
- The SLINK connection to the ROS is established either via a QSFP or four SFP transceivers (Small Form-factor Pluggable)
- For testing & debugging a *low pin count FPGA mezzanine connector* (LPC FMC), SE/diff pin header, SMA connectors and GPIO LEDs are available
- Configuration of the two Spartan6 devices is handled by a third Spartan 6 (LX75T), the Board Control FPGA (BCF)
- FLASH memory for configuration data
- MicroBlaze soft processor core
- DDR2 memory
- GbE interface, CAN (ELMB)

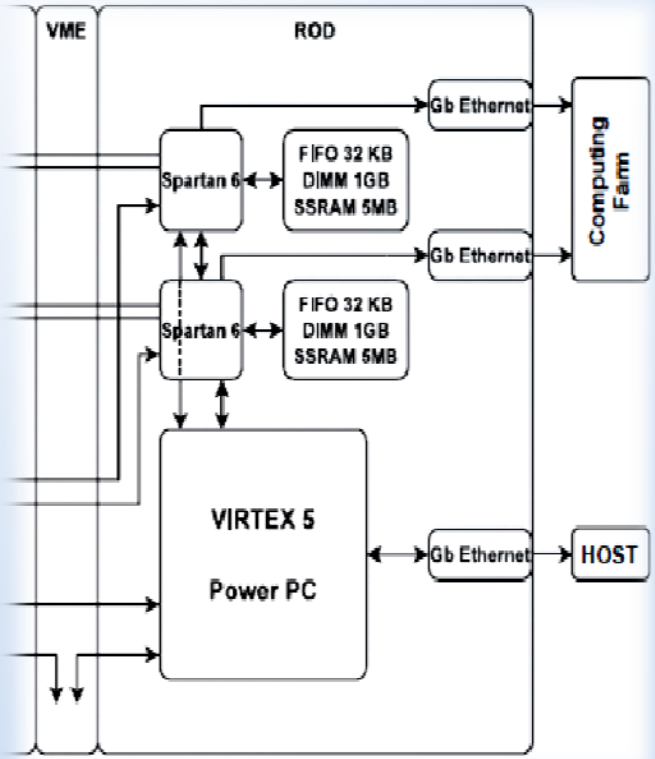
BOC Status





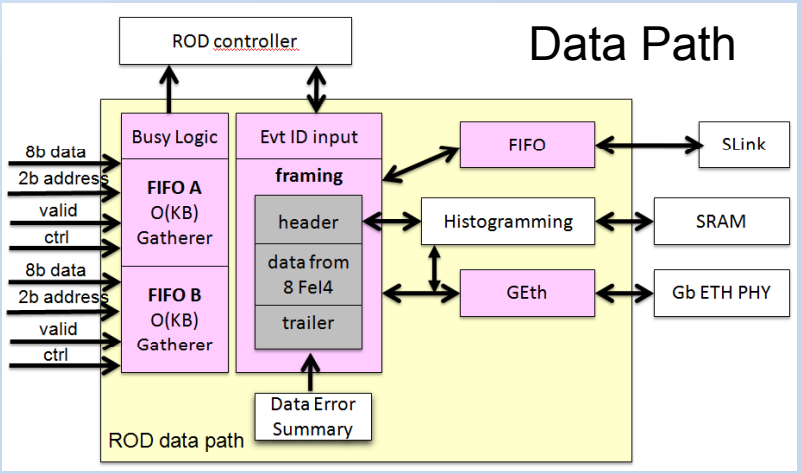
- BOC demonstrator:
  - based on the XILINX SP605 evaluation card
  - All Firmware blocks loaded and simulated
- Prototype layout is almost complete
  - PCB production will start in June

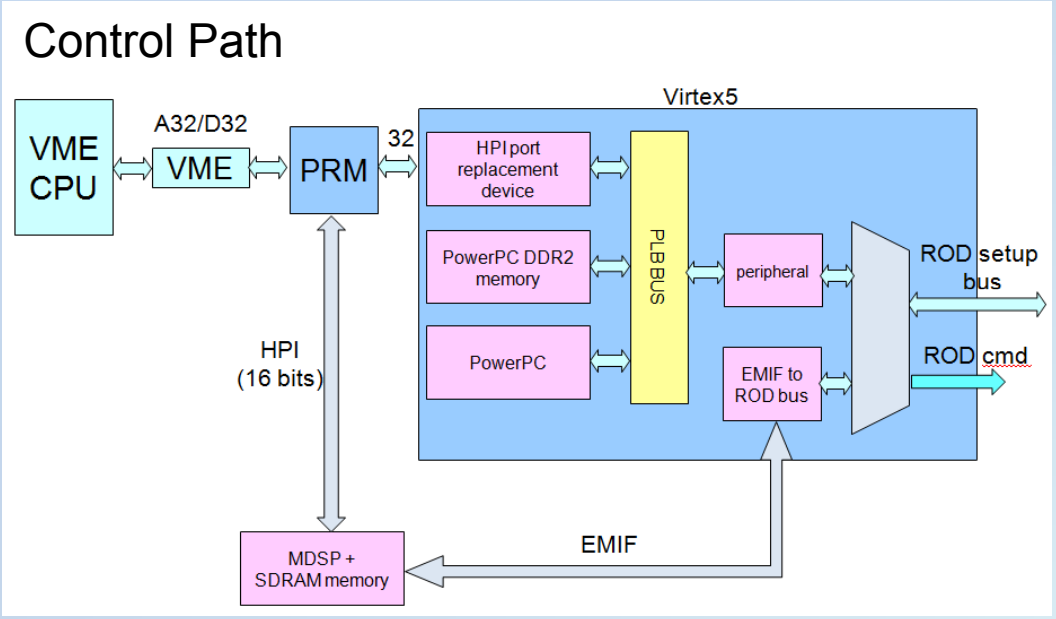
ROD Design



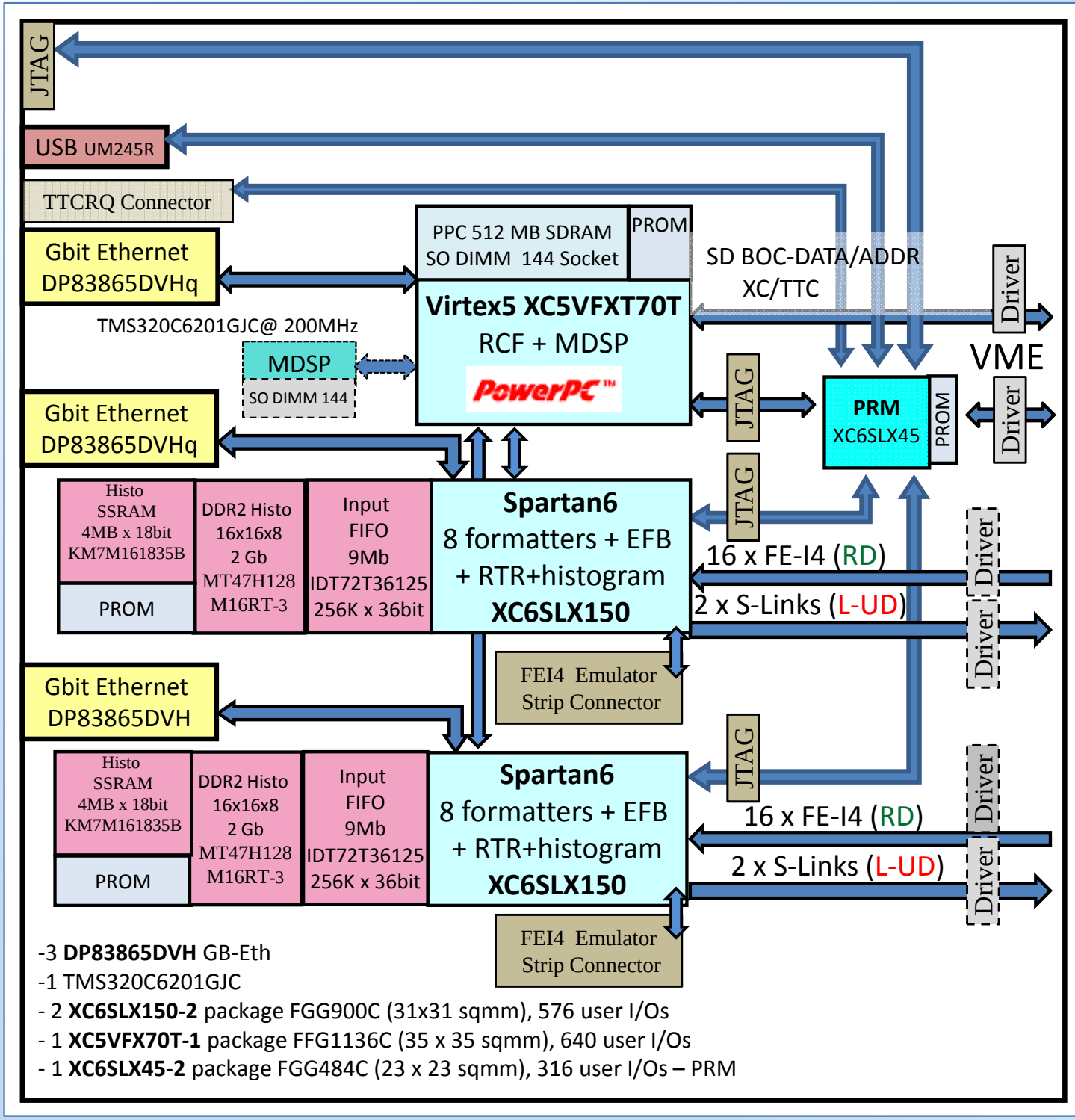
Versatile design:

- Control via VME or GB Ethernet
- Possibility of use w/o VME crate (TTC input, extern
- Avoid the use of DSPs
- Move the task of 4 slave DSP to off ROD processing
- Master DSP or Embedded PPC (Virtex 5)
- External data processing (for calibration)
- Backward compatibility with FE-I3 old DAQ chain
- Conceptually software running on the VME CPU would require minimal modifications





New ROD Block Schematics



P1

P0
5 rows

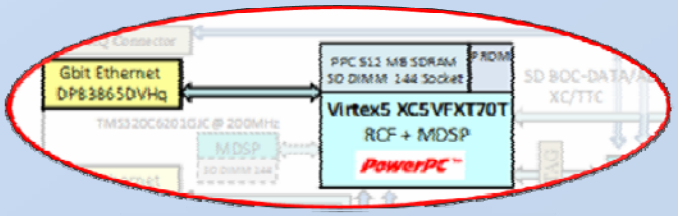
data from/to BOC

40 – 80 MHz LVTTL
> 80 MHz SSTL3-I

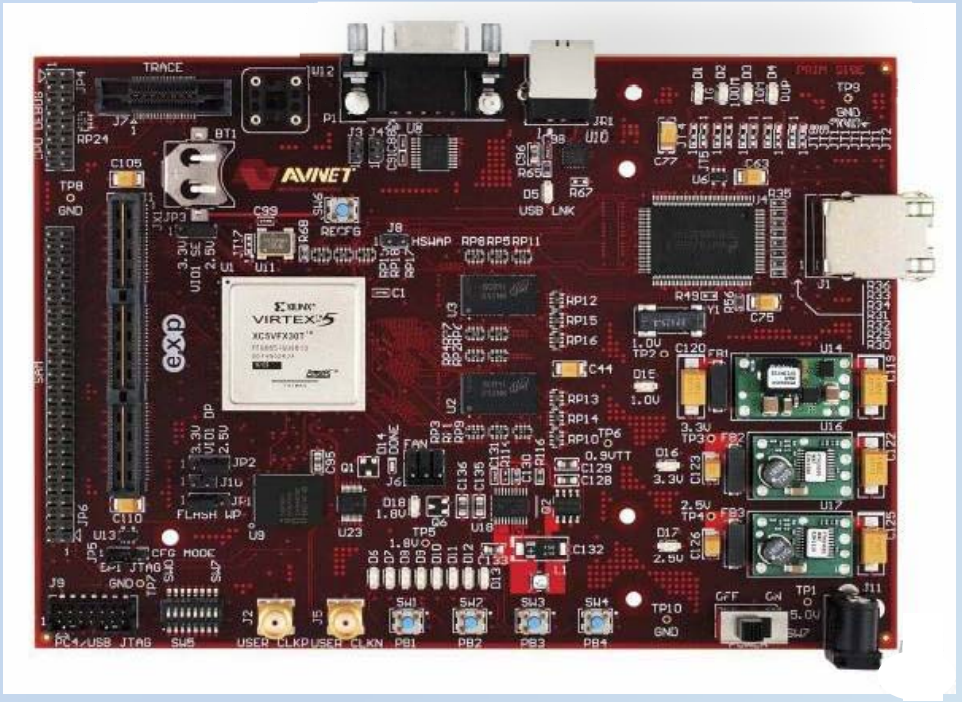
P2

P3

PowerPC-based Control

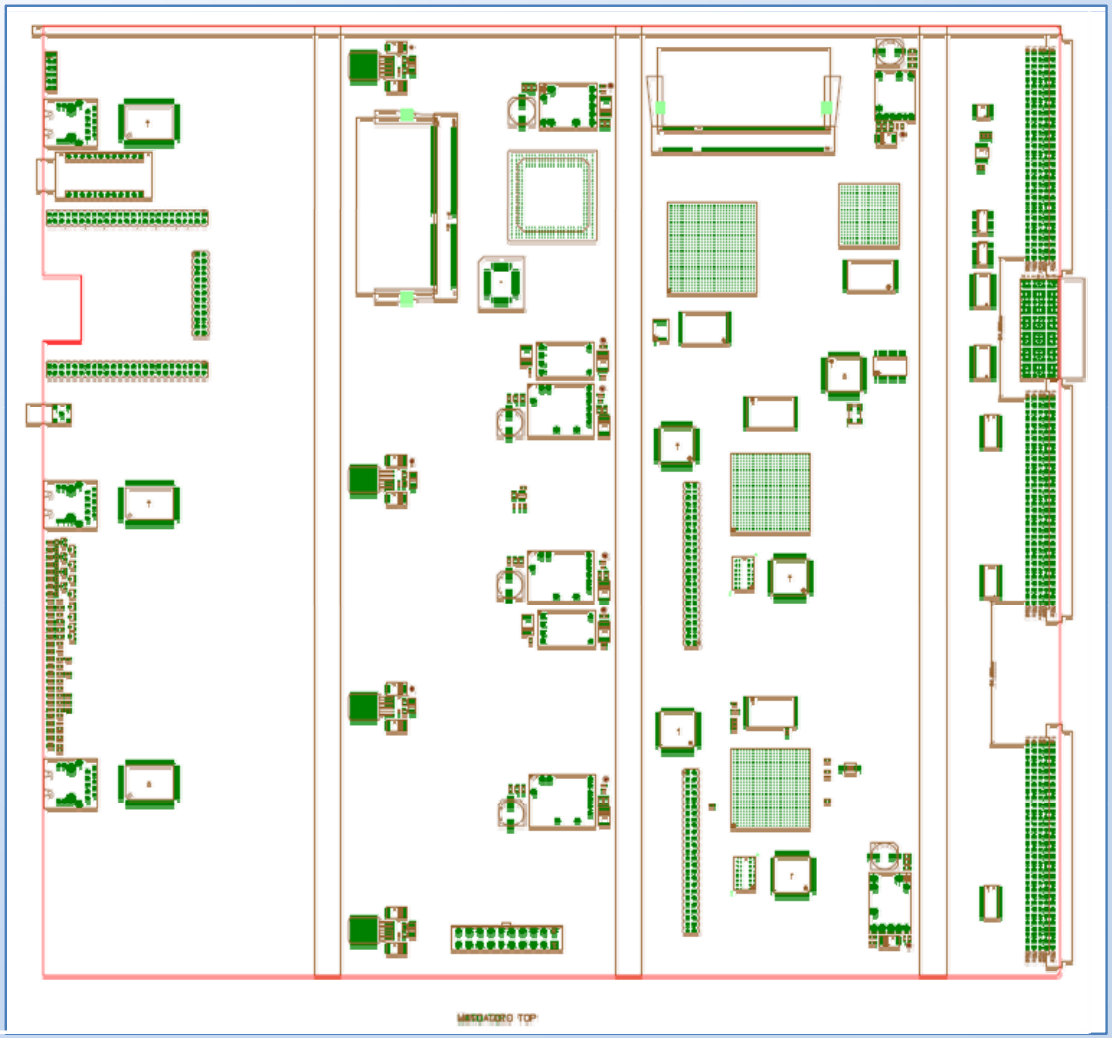


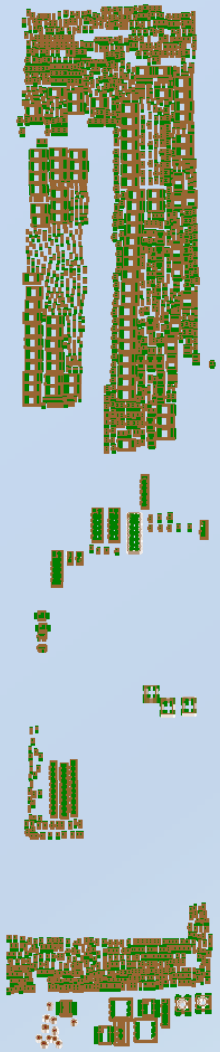
- Rationale:
  - Enhancing ROD control and monitoring (w.r.t. DSPs)
  - Adding Gigabit Ethernet control interface
  - Provide a development environment common with the custom FPGA firmware
- Main activities:
  - Increase knowledge on sw and fw design
  - Developing ad-hoc peripherals in order to manage custom fw
  - Running embedded Linux on PPC (could speed-up Lab and integration tests)
  - Provide an integrated hw/sw simulation testbench (FPGA → ROD → whole system)



- Status:
  - Development system: AVNET: XILINX Virtex-5 FXT Evaluation Kit
  - Ad-hoc peripheral connecting PPC with actual-ROD VHDL modules is working well
  - Able to run and customize Linux on *PowerPC*
  - Development of kernel modules for new peripherals ongoing
  - Tools providing hw/sw optimized and synchronized simulation is under study (menthor CodeLink)

ROD Layout & Prototype





- ROD schematic close and ROD layout submitted
- 2 fully assembled prototypes expected by end of June
- Firmware, test environment and DAQ software update being addressed
- First BOC – ROD integration of prototypes by mid-end of Summer

Conclusions

- For the ATLAS IBL which is expected to be installed in 2013 a new readout system has been designed.
- The system provides higher bandwidth and integration while keeping fully compatible to the present ATLAS DAQ
- New histogram readout path via GB Ethernet will increase the calibration speed and maintainability
- Total bandwidth of building blocks increases, leading to smaller size systems (IBL readout fits in a single crate)
- Industrial components will replace the custom-made components, recently failing within ATLAS pixel and SCT
- Production of prototypes has been submitted
- First integration of all components expected in mid-end of summer