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Design of the ATLAS IBL Readout System

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An Insertable B-Layer is planned for the upgrade of the ATLAS detector and will add a fourth and innermost silicon layer to the existing Pixel detector. 12 million pixels attached to new FE-I4 readout ASICs will require new off-detector electronics which is currently realized with two VME-based boards: a Back Of Crate module implementing optical I/O functionality and a Readout Driver module for data processing. This paper illustrates the new read-out chain, focusing on the design of new the Readout Driver Card, which, with a fourfold integration with respect to the previous design, builds up the detector data, controls the calibration procedures and interacts via Gigabit links with a novel calibration farm. Future prospects and back compatibility to the existing system are also addressed.

Author: Dr POLINI, Alessandro (INFN - Bologna)

Co-authors: GABRIELLI, Alessandro (Bologna University); KUGEL, Andreas (ZITI, LS Informatik V, Heidelberg University, Mannheim,); ZOCCOLI, Antonio (University of Bologna & INFN Bologna); FALCHIERI, Davide (Bologna University); BRUNI, Graziano (INFN Bologna); DANTONE, Ignazio (INFN Bologna); DOPKE, Jens (CERN); GROSSE-KNETTER, Joern (II. Physikalisches Institut, Universitaet Goettingen); JOSEPH, John (LNBL, Berkeley, U.S.A); BRUSCHI, Marco (INFN Bologna); RIZZI, Matteo (INFN Bologna); SCHROER, Nicolai (ZITI, LS Informatik V, Heidelberg University, Mannheim); KRIEGER, Nina (II. Physikalisches Institut, Universitaet Goettingen); MORETTINI, Paolo (INFN Genova, Italy); TRAVAGLINI, Riccardo (INFN Bologna); ZANNOLI, Samuele (University of Bologna & INFN Bologna); FLICK, Tobias (Fachbereich C Physik, Bergische Universitaet Wuppertal)

Presenter: Dr POLINI, Alessandro (INFN - Bologna)

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