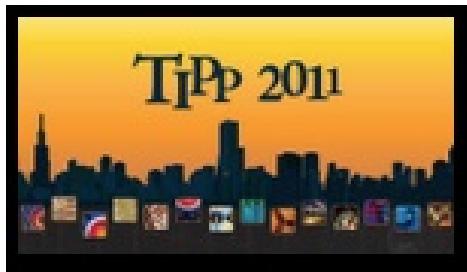


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Design of the ATLAS IBL Readout System

Saturday 11 June 2011 14:00 (20 minutes)

An Insertable B-Layer is planned for the upgrade of the ATLAS detector and will add a fourth and innermost silicon layer to the existing Pixel detector. 12 million pixels attached to new FE-I4 readout ASICs will require new off-detector electronics which is currently realized with two VME-based boards: a Back Of Crate module implementing optical I/O functionality and a Readout Driver module for data processing. This paper illustrates the new read-out chain, focusing on the design of new the Readout Driver Card, which, with a fourfold integration with respect to the previous design, builds up the detector data, controls the calibration procedures and interacts via Gigabit links with a novel calibration farm. Future prospects and back compatibility to the existing system are also addressed.

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