Advanced pixel sensors and readout electronics based on 3D integration for the SuperB Silicon Vertex Tracker

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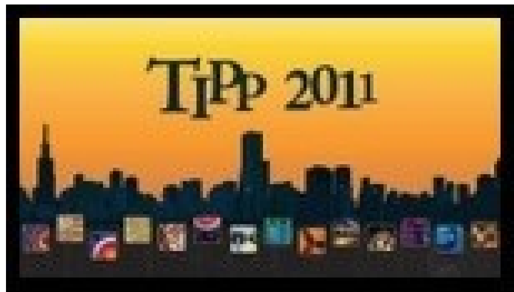
on behalf of the VIPIX collaboration



Technology and Instrumentation in Particle Physics 2011

June 9-14, 2011, Chicago

Outline

- The SuperB project and the Silicon Vertex Tracker
- Pixels in the SuperB SVT
- Evolution from 2D devices to 3D integration for advanced SuperB pixels

The SuperB Project

- The physics case for a high luminosity B Factory is clearly established.
  - Flavour physics is rich, promises sensitivity to New Physics ... but large statistics (50-100 ab^{-1}) is needed
- First generation of B-Factories (PEP-II and KEKB) exceeded their design goals ($\mathcal{L}$ ~1.2-1.7 $\times 10^{34}$ cm^{-2} s^{-1} , integrated 1.2 ab^{-1}) but an upgrade of ~2 orders of magnitude in $\mathcal{L}$ is needed to get 50ab^{-1} .
- Increasing Luminosity by brute-force (higher currents) is expensive and difficult
  - wall plug power and detector background explosion
  - effective limitation around 5×10^{35} cm^{-2} s^{-1}
- The SuperB italian accelerator concept allows to reach $\mathcal{L}$ $=10^{36}$ cm^{-2} s^{-1} with moderate beam current (2A) using very small beam size (~1/100 of present B-Factories beams exploiting the ILC R&D on damping rings & final focus) with the help of the Crab Waist scheme at the IP to keep the beams small & stable after collision (verified with tests on Dafne)
- This approach allows to (re-) use parts of existing detectors and machine components.

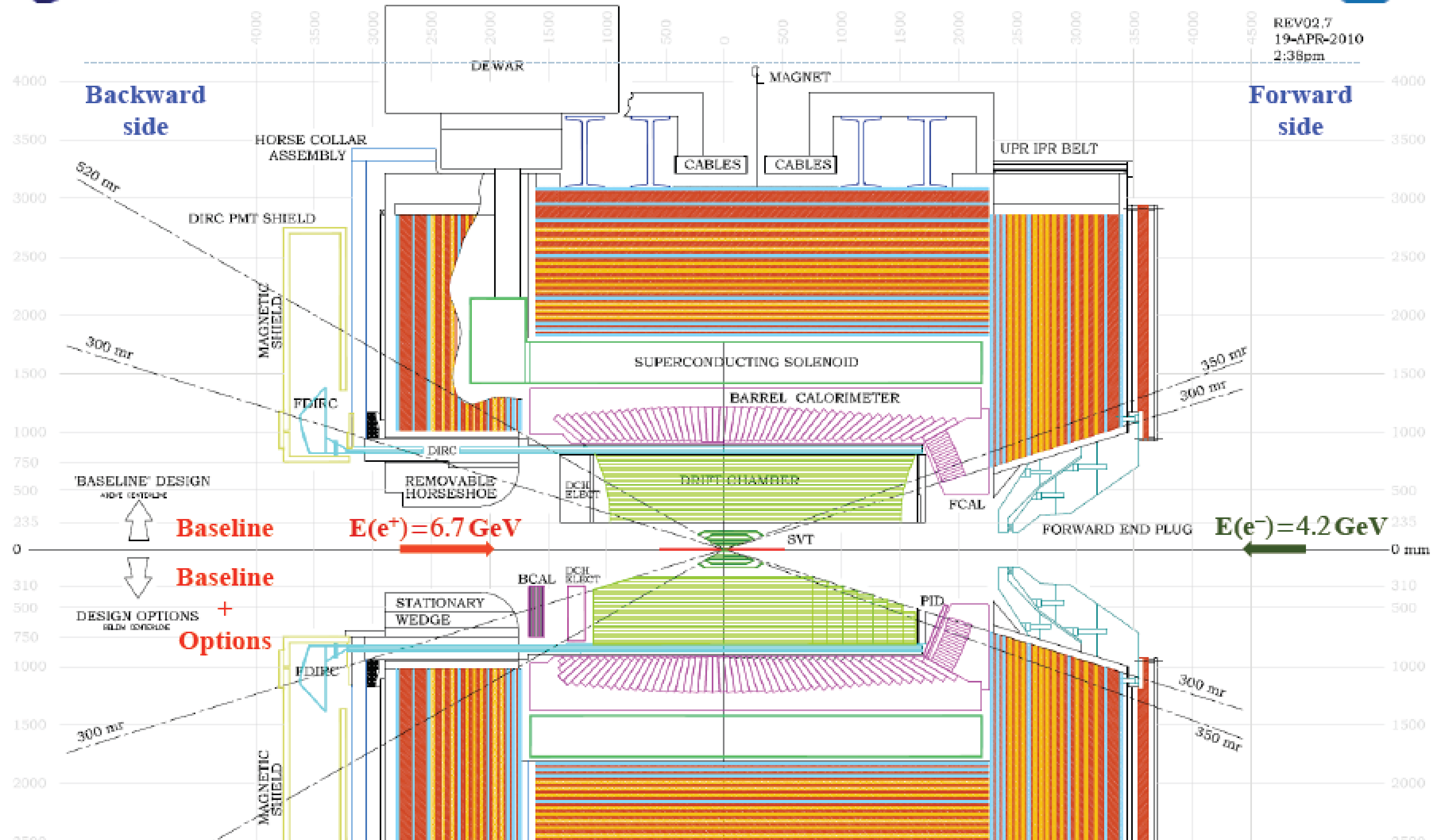
SuperB approval and site

- SuperB has been approved by the Italian Government as the first in a list of 14 "flagship" projects within the new national research plan.
- A financial allocation of 250 Million Euros in about five years has been approved for the "superb flavour factory"
- The site was decided: SuperB will be built in the campus of the Tor Vergata University campus near Rome
- Beam lines for synchrotron light (very high brightness) experiments will be available at the SuperB facility
- First collisions: mid 2016

Machine parameters

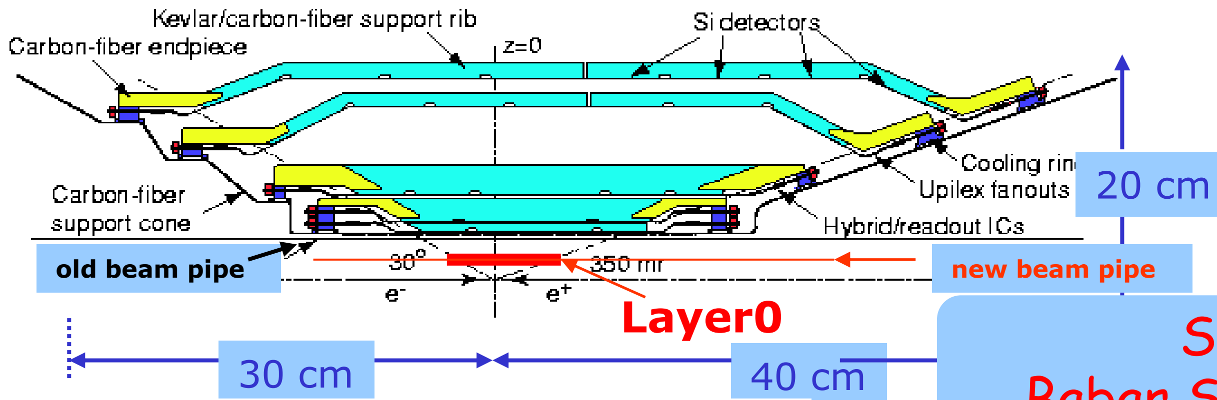
	Units	HER	LER	HER	LER	HER	LER
Machine		Super B		PEP II		Super KEKB	
Circumference	***m***	***1258.4***		***2200***		***3016.3***	
Frequency turn	Hz	2.38E+05		1.36E+05		9.95E+04	
# bunch		978		1732		2500	
Frequency collision	MHz	233		236		249	
Full crossing angle	Rad	0.066		0.000		0.083	
Energy	GeV	6.7	4.18	9.0	3.1	7	4
Energy ratio		1.60		2.90		1.75	
βx	cm	2.6	3.2	35	40	2.4	3.2
βy	***µm***	***253***	***205***	***9000***	***10800***	***410***	***270***
coupling	%	0.25	0.25	0.24	0.45	0.35	0.40
Radial emittance εx	nm	2.07	2.37	55	33	2.4	3.1
Vertical emittance εy	pm	5.18	5.93	1300	1500	8.4	12.4
Bunch length	cm	0.5	0.5	1.15	1.25	0.5	0.6
Current	A	1.89	2.44	2.07	3.21	2.6	3.62
# particles/bunch	10^{10}	5.08	6.56	5.49	8.52	6.55	9.13
Hor. size @ IP σx	µm	7.34	8.71	43.87	36.33	7.75	10.62
Ver. size @ IP σy	***nm***	***36.2***	***34.9***	***3421***	***4025***	***59.0***	***59.0***
Piwinsky angle		22.50	18.95	0.00	0.00	26.79	23.46
Horizontal tune shift	%	0.21	0.33	5		0.28	0.28
Vertical tune shift	%	9.89	9.55	5		8.75	9.00
Luminosity	***10^{36} Hz/cm^2***	***1.02***		***0.012***		***0.80***	

SuperB Detector (with options)



The SuperB Silicon Vertex Tracker

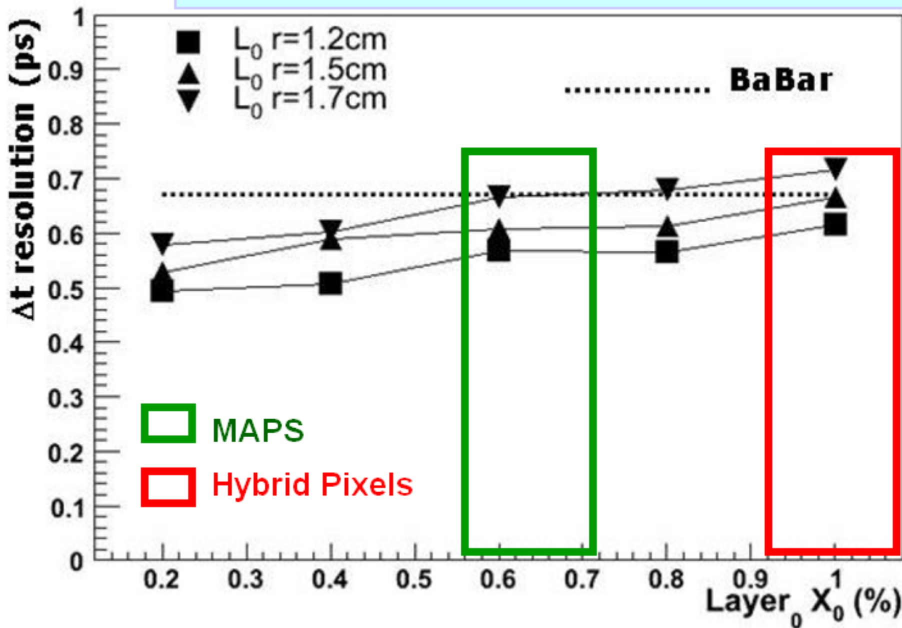
The SVT provides precise tracking and vertex reconstruction, crucial for time dependent measurements.



BaBar SVT

- 5 Layers of double-sided Si strip sensor
- Low-mass design. (P_t < 2.7 GeV)
- Stand-alone tracking for slow particles.
- 97% reconstruction efficiency
- Resolution ~15μm at normal incidence

B→π π decay mode, βγ=0.28, beam pipe X/X0=0.42%, hit resolution =10 μm



SuperB SVT based on Babar SVT design for R>3cm. BUT:

1) reduced beam energy asymmetry (6.7x4.2 GeV vs. 9x3.1 GeV) requires an improved vertex resolution (~factor 2)
   - Layer0 very close to IP (@1.5 cm) with low material budget (<1% X_0) and fine granularity (50 μm pitch)
   - Layer0 area 100 cm^2

2) bkg levels depend steeply on radius
   - Layer0 needs to be fast and rad hard (>20x5 MHz/cm^2, >3x5 MRad/yr)

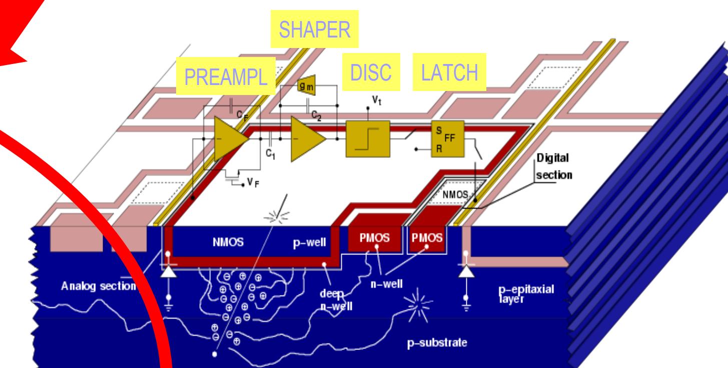
SuperB SVT Layer 0 technology options

- Striplets option: mature technology, not so robust

MAPS and 3D vertically integrated pixels are the two most advanced options considered for Layer0 upgrade:

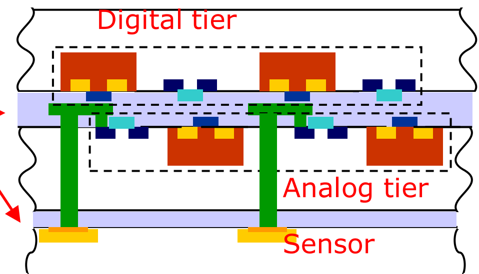
- Reduction of front-end pitch to 50x50 µm²
  - → Produced and tested FE prototype chip with 50x50 µm² pitch & fast data push readout (already developed for DNW MAPS) - (4k pixels, ST 130 nm)

- CMOS MAPS option: new & challenging technology.
  - Sensor & readout in 50 µm thick chip
  - Extensive R&D (SLIM5-INFN Collaboration) on
    - Deep N-well devices 50x50µm² with in-pixel sparsification.
    - Fast readout architecture implemented
  - CMOS MAPS (4k pixels) successfully tested with beams.



- Thin pixels with Vertical Integration: **reduction of material and improved performance.**
  - Two options are being pursued (VIPIX – INFN Collab.)
    - DNW MAPS with 2 tiers
    - Hybrid Pixel: FE chip with 2 tiers + high resistivity sensor

Wafer bonding & electrical intercon.



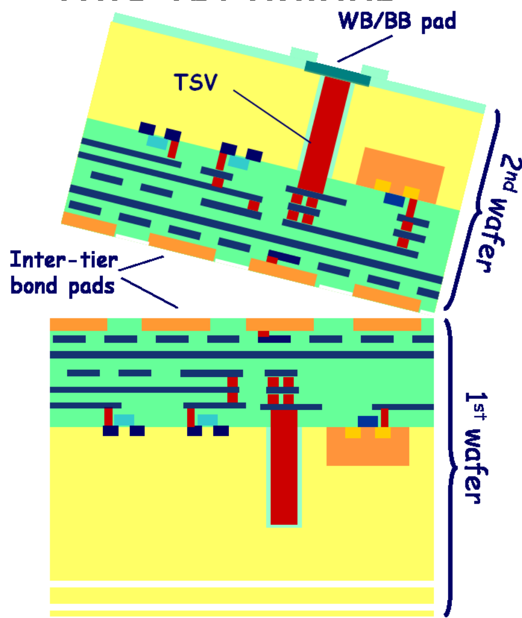
Complexity

Evolving from 2D to 3D

- We are targeting 50 x 50 μm^2 pixels (resolution requirement) with pixel-level sparsified readout and time stamping (background tolerance)
- If readout CMOS chips can expand to 2 (or more…) layers, more advanced and optimized functions can be integrated in smaller pixels
- In a 3D structure, one of the layers can be a high resistivity pixel sensor, or a CMOS sensor; several constraints can be removed with the help of 3D integration

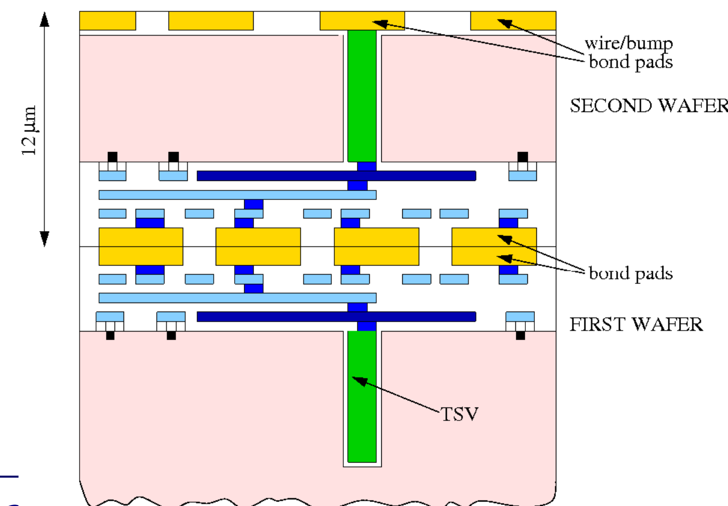
3D technology choices by SuperB-VIPIX

- Tezzaron "via middle" process for the face-to-face bonding between two 130 nm CMOS wafers by GlobalFoundries
- This approach is followed by the 3D-IC consortium promoted by Fermilab; the Italian VIPIX collaboration is a member of this consortium together with 17 international groups
- TSVs are drilled at the foundry in the early stages of CMOS wafers processing. Very high density interconnections (< 10 μm) are possible with this technique



e.g.: 2-layer CMOS chips for pixel readout

with many pixel-level interconnections



The SuperB-VIPIX way to 3D-integrated pixels

- **Readout of high resistivity pixels: from Superpix0 to Superpix1**

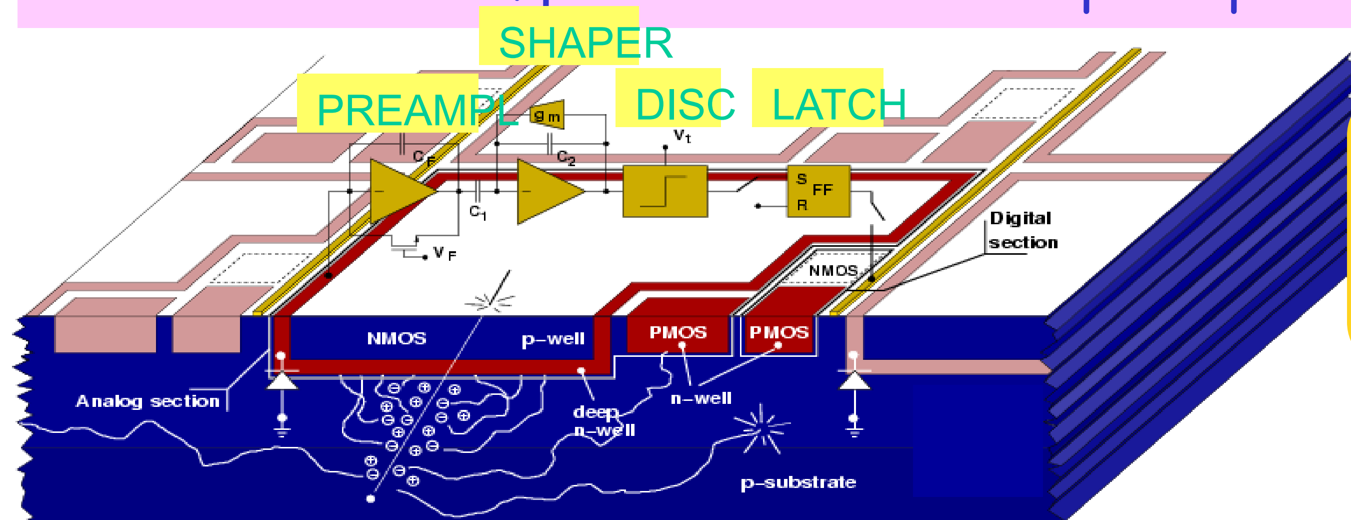
  Improve the performance of the analog section (e.g., gain uniformity and threshold dispersion), separate analog and digital, add logic functions for a more flexible readout architecture (triggerable, time-stamp ordered)

- **CMOS sensors: from 2D APSEL to 3D APSEL**

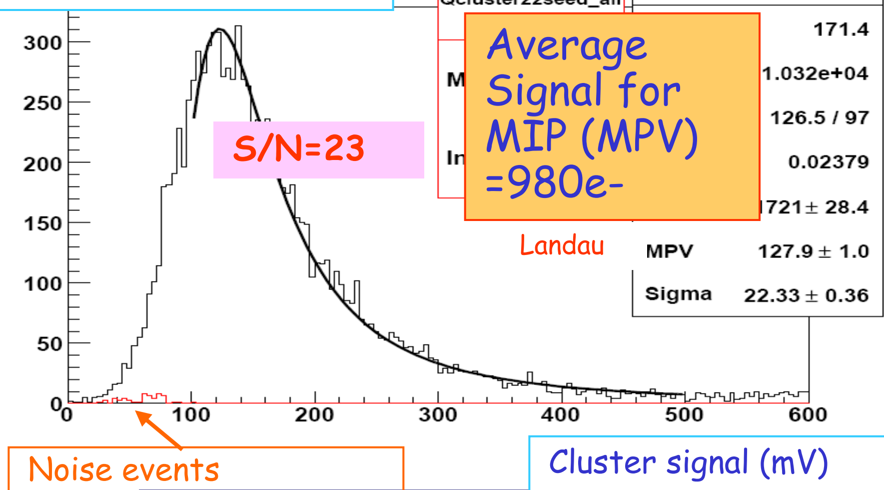
  Same as above, but also improving the sensor performance (smaller capacitance, better charge collection)

Deep N-Well (DNW) sensor concept

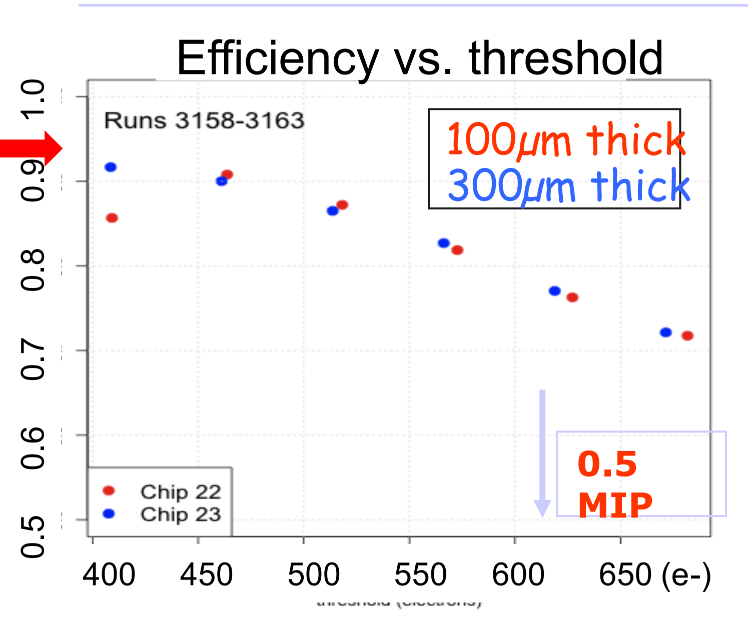
New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential



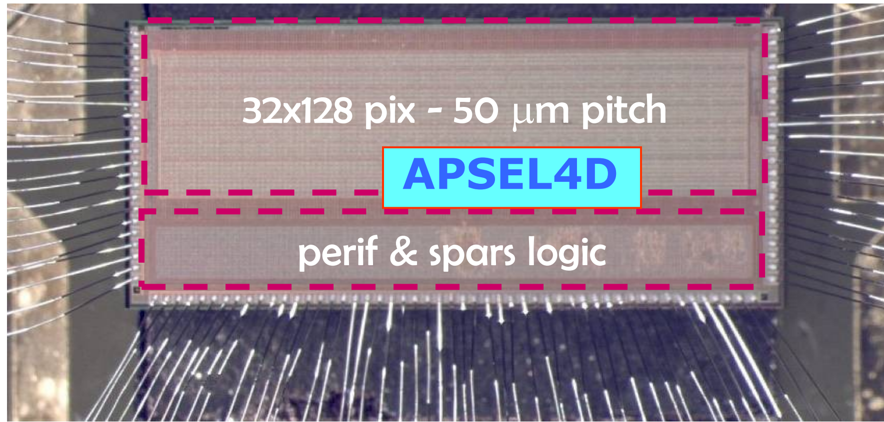
Developed in a 130 nm CMOS process, various different chips successfully tested with radioactive sources and in a beam



efficiency 92% because of PMOS N-wells in the pixel cell



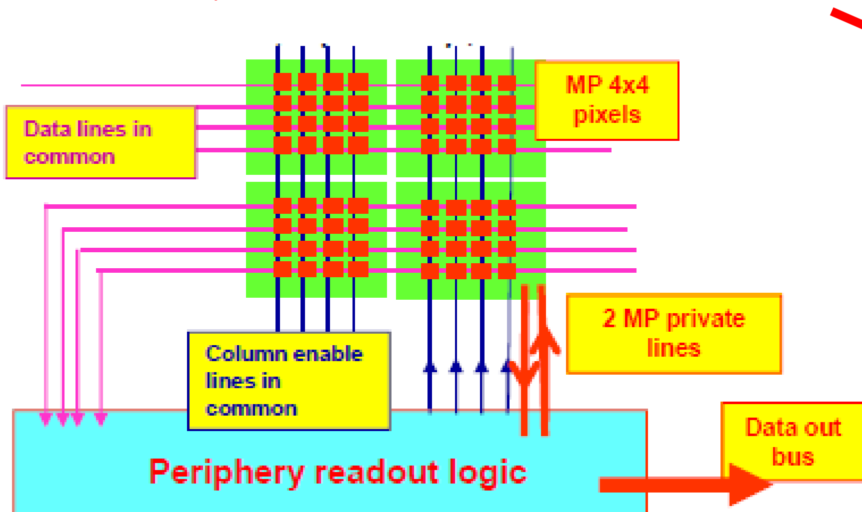
Latest 2D generation of deep N-well MAPS: APSEL4D and APSEL5T

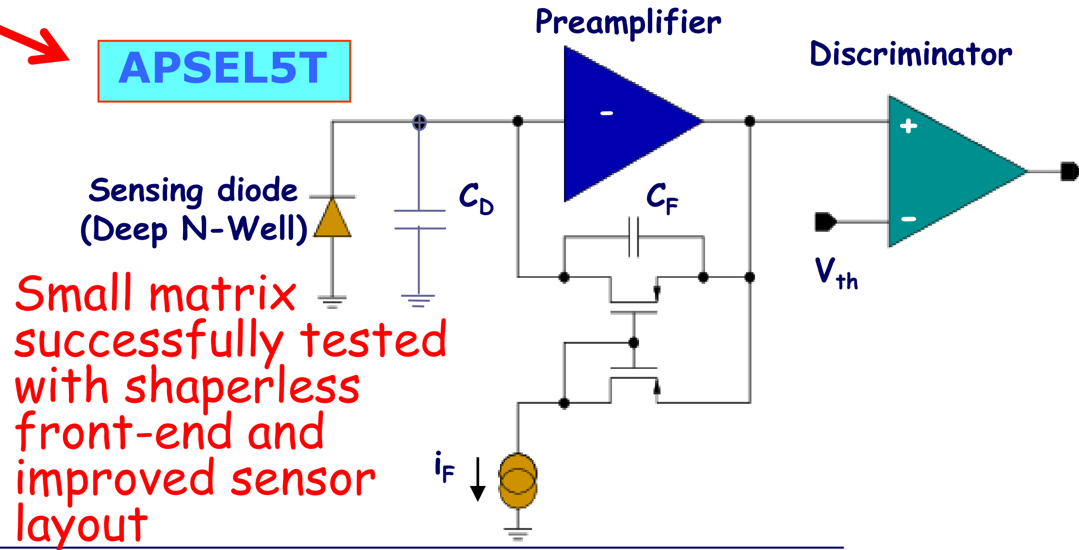


To reduce the area of logic blocks with PMOS in the pixel, the matrix is subdivided in MacroPixel (MP=4x4) with point to point connection to the periphery readout logic:

- Register hit MP & store timestamp
- Enable MP readout
- Receive, sparsify, format data to output bus

With respect to APSEL4D, scaling to larger matrix size dictates to remove the shaper stage to make room for additional macropixel private lines

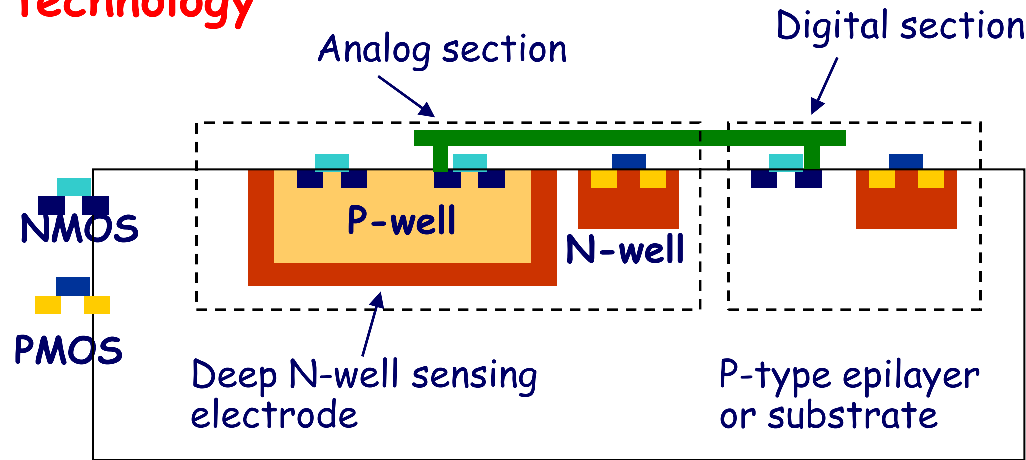




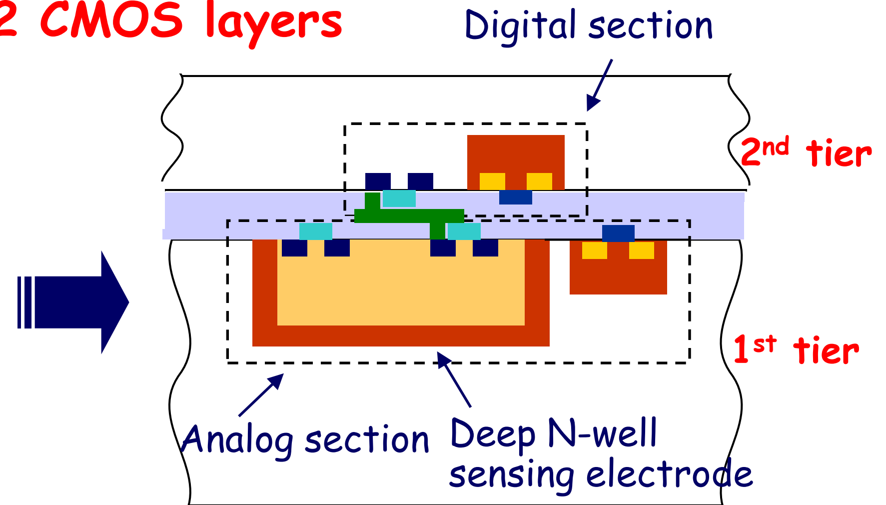
Small matrix successfully tested with shaperless front-end and improved sensor layout

3D integration for a large deep N-well MAPS matrix

2D CMOS technology



3D integration of 2 CMOS layers

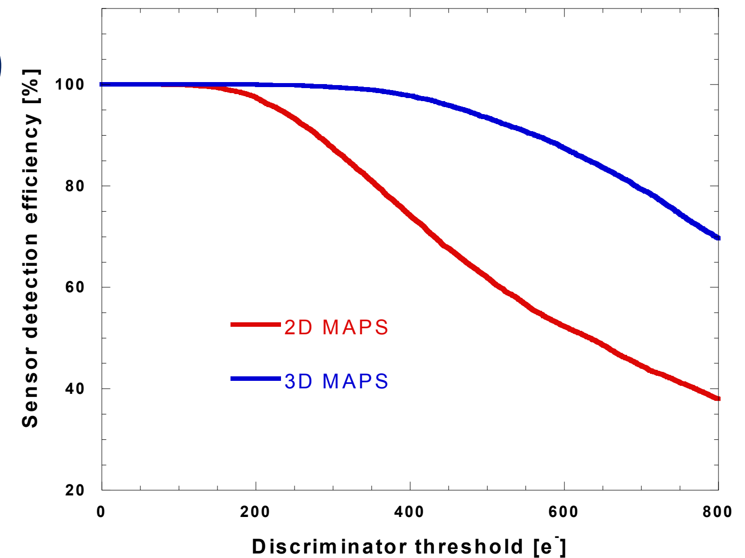


Sensor performance:

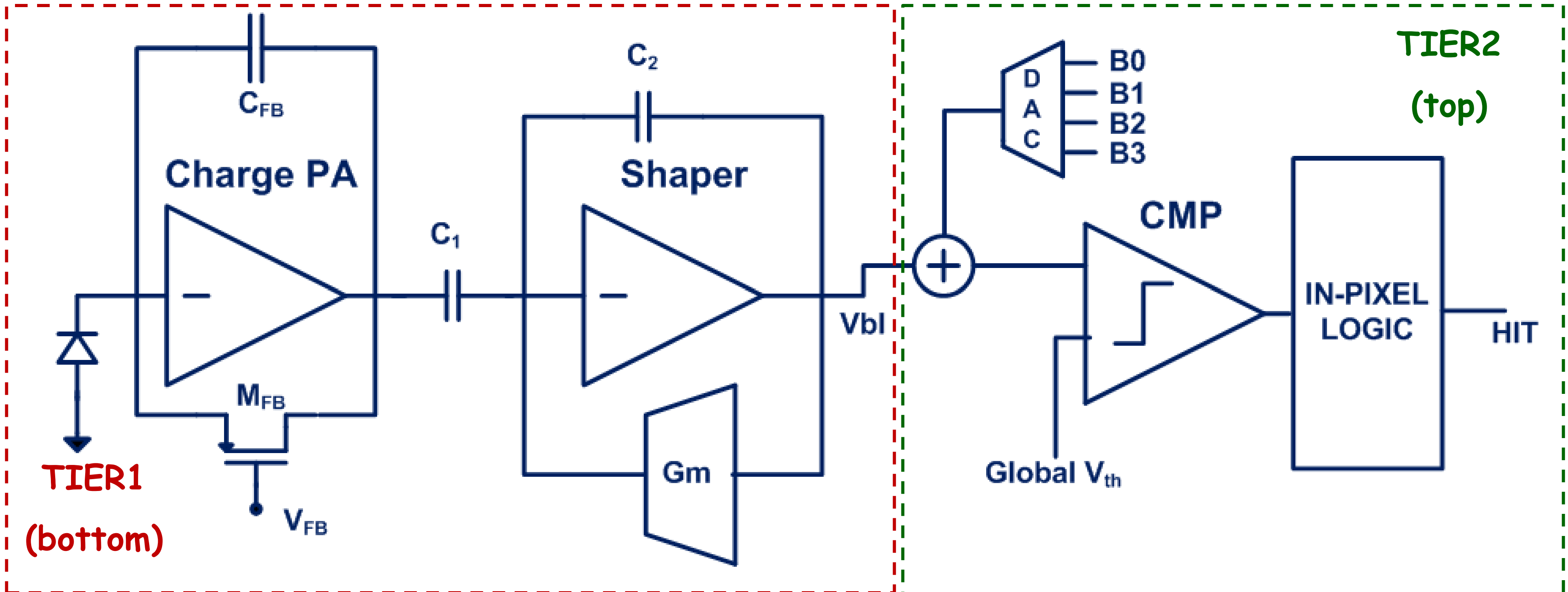
All the PMOS (and their competitive N-wells) of the digital section are removed from the sensing layer.

According to device simulation, efficiency ramps up to 99%.

Deep N-well area can be reduced, decreasing the sensor capacitance and allowing for a better noise/power trade-off.



The analog section in a 3D deep N-well MAPS



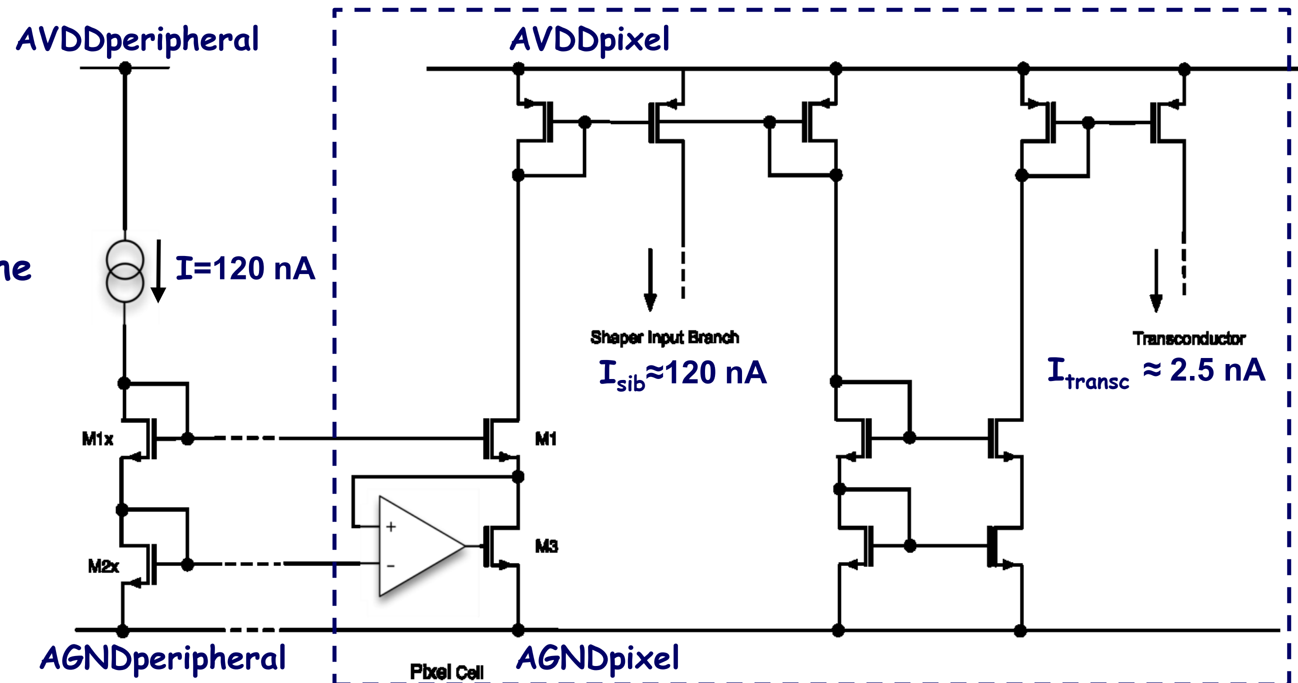
- Charge preamplifier with a C_{FB} countinously discharged by an NMOS biased in deep subthreshold region.
- RC-CR shaper with a transconductor feedback network:
  - V_{bl} chip wide distributed by an external voltage reference (not affected by voltage drop issues)

Thanks to 3D integration: use MiM capacitors, independently optimize noise and threshold dispersion (also DAC for local threshold adjustment), achieve a high charge sensitivity in a reliable way

Compensation of power supply voltage drops in a large matrix

- 3D Apsel features:
  - I_{analog_cell}=25 μA
  - 128x100 pixels matrix for the next run
  - Considering the case of a larger matrix (i.e. 256x256 elements), supplied from both sides, we obtain the following voltage drop on AVDD and AGND:

ΔV_d=15/20 mV (typ/max)



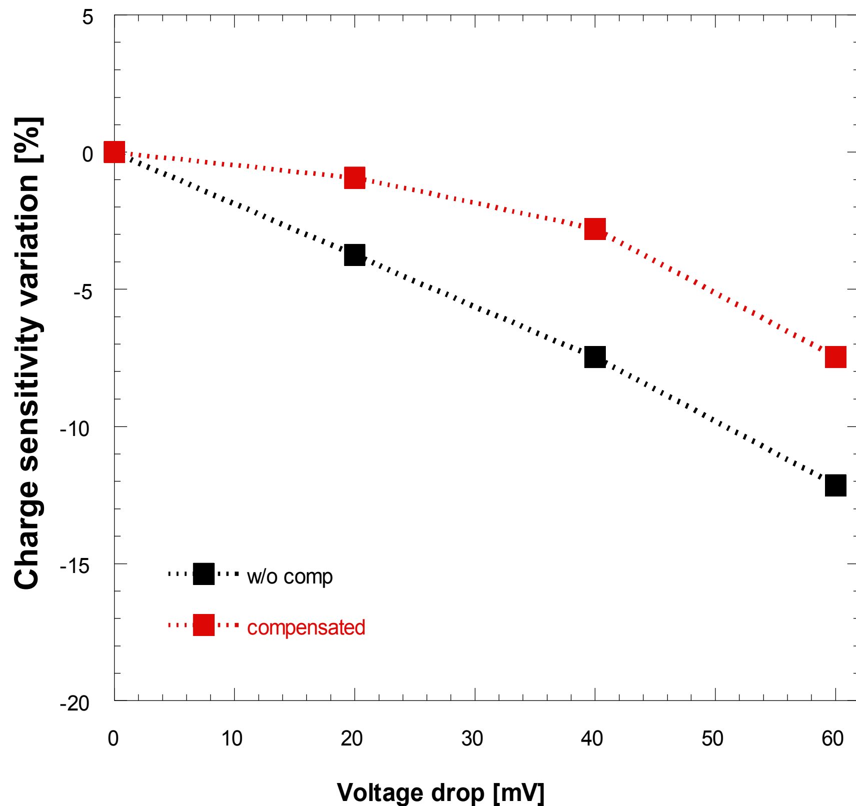
M. Manghisoni, E. Quartieri et al.,"High Accuracy Injection Circuit for Pixel-Level Calibration of Readout Electronics" presented at the *2010 IEEE Nuclear Science Symposium Conference*, Knoxville, USA, October 30 - November 6 2010.

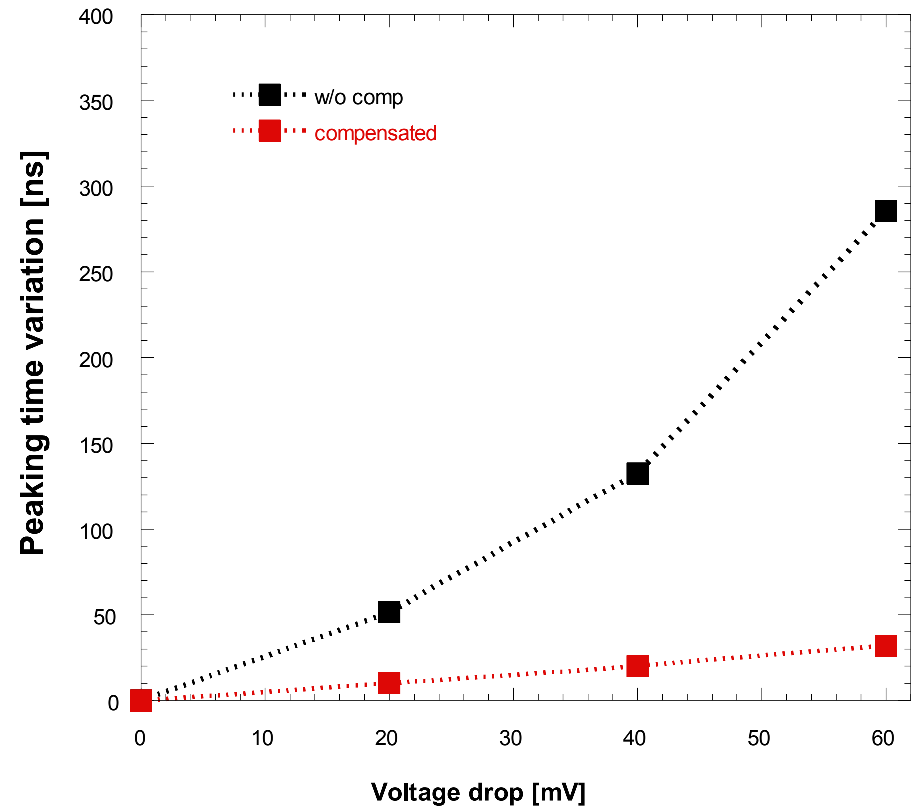
- Voltage drop on the AVDD and AGND lines causes changes in some pixel current sources, in particular in the **shaper input branch** and in the **transconductor**. These current changes lead to a degradation of the front-end performance (i.e. charge sensitivity and peaking time).
- **This problem is overcome by distributing a reference voltage to each pixel according to the schematic above.**

Effect of compensation of power supply voltage drops on peaking time and charge sensitivity

- Voltage drop is simulated as a symmetrical voltage variation in the analog power (AVDD) and ground (AGND) lines.

$$AVDD=1.5\ V-\Delta V_d,\ AGND=\Delta V_d$$



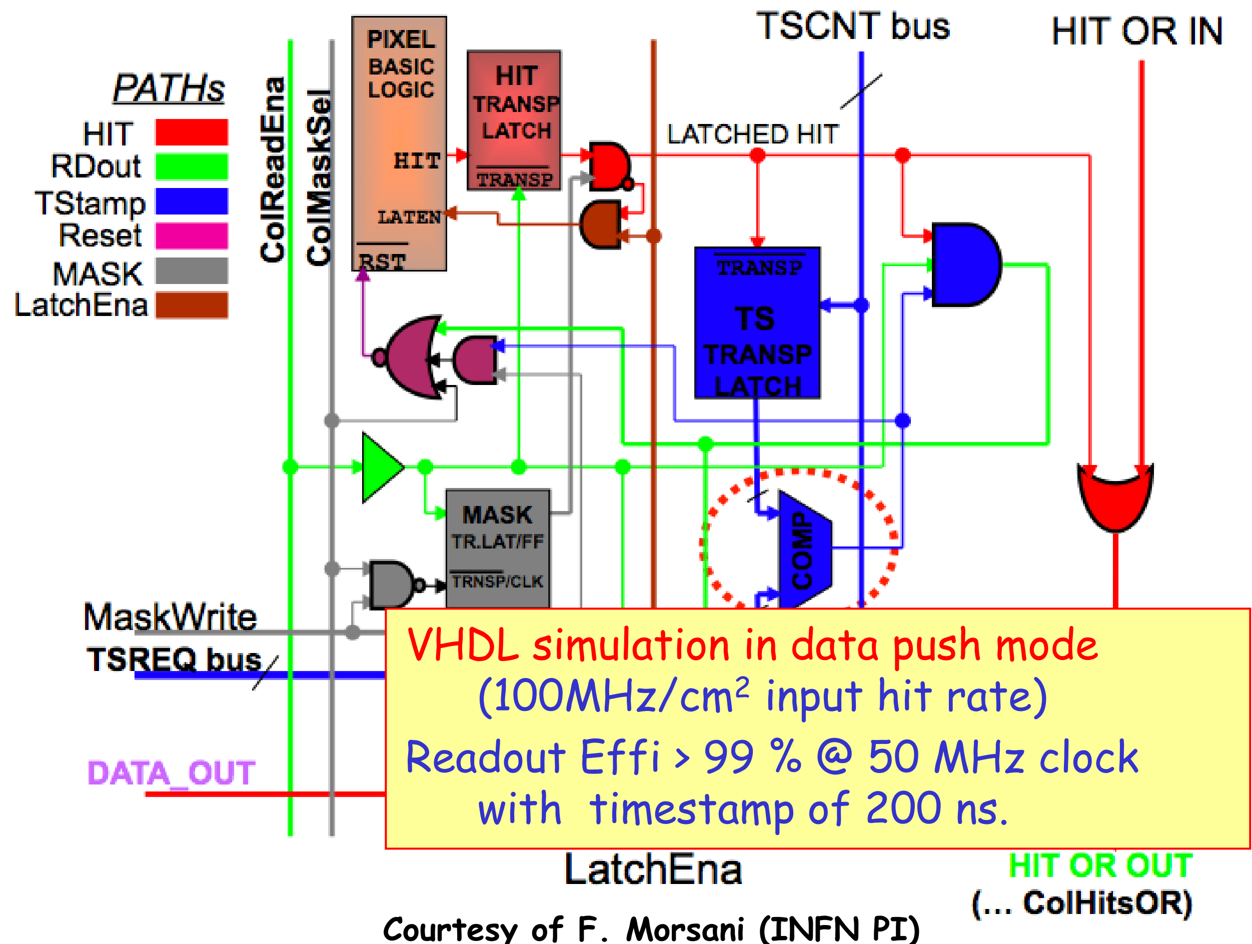


Readout architecture in a 3D MAPS pixel cell: time-stamp latch and comparator for a time-ordered triggered readout

- Complex in-pixel logic can be implemented without reducing the pixel collection efficiency; readout can be data push or triggered.

- Timestamp (TS) is broadcast to pixels and each pixel latches the current TS when fires.

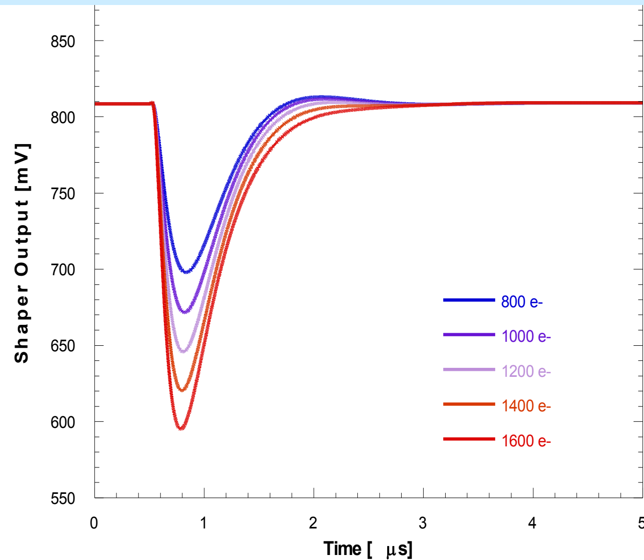
- Matrix readout is TS ordered
  - A readout TS enters the pixel and an HIT-OR-OUT is generated for columns with hits associated to that TS
  - A column is read only if HIT-OR-OUT=1
  - DATA_OUT is generated for pixels in the active columns with hits associated to that TS.

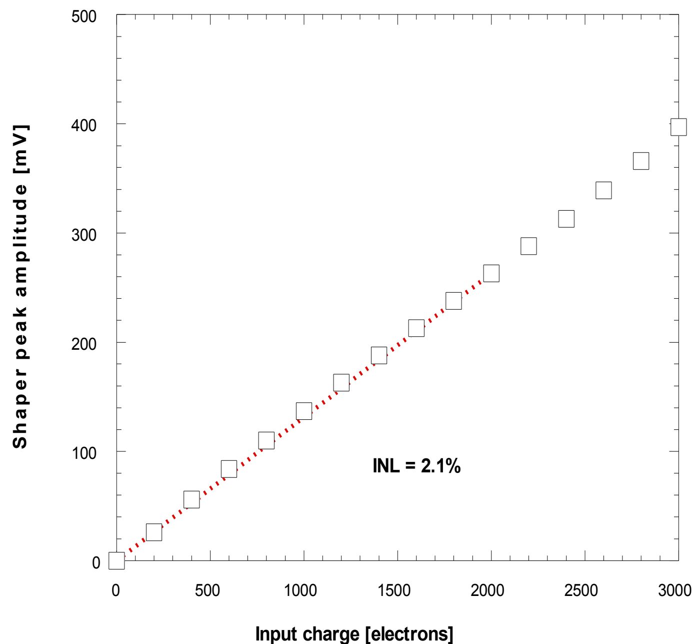


VHDL simulation in data push mode
($100 MHz/cm^2$ input hit rate)
Readout Effi > 99 % @ 50 MHz clock
with timestamp of 200 ns.

Courtesy of F. Morsani (INFN PI)

Design features and simulations for the 3D MAPS



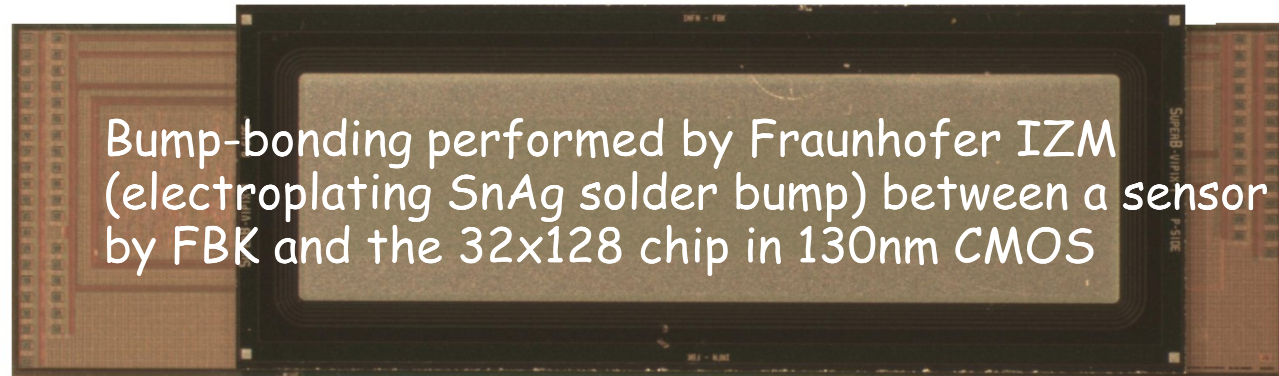


	3D Apsel
Charge sensitivity	850 mV/fC
Peaking time	320 ns
ENC	34 e-
Threshold dispersion before/after correction	103/13 e-
INL (@ 2000 e-)	2.1%
Analog power consumption	33 µW/pixel
Detector parasitic capacitance	300 fF
Matrix size	128x100 pixels
Pixel pitch	50 µm

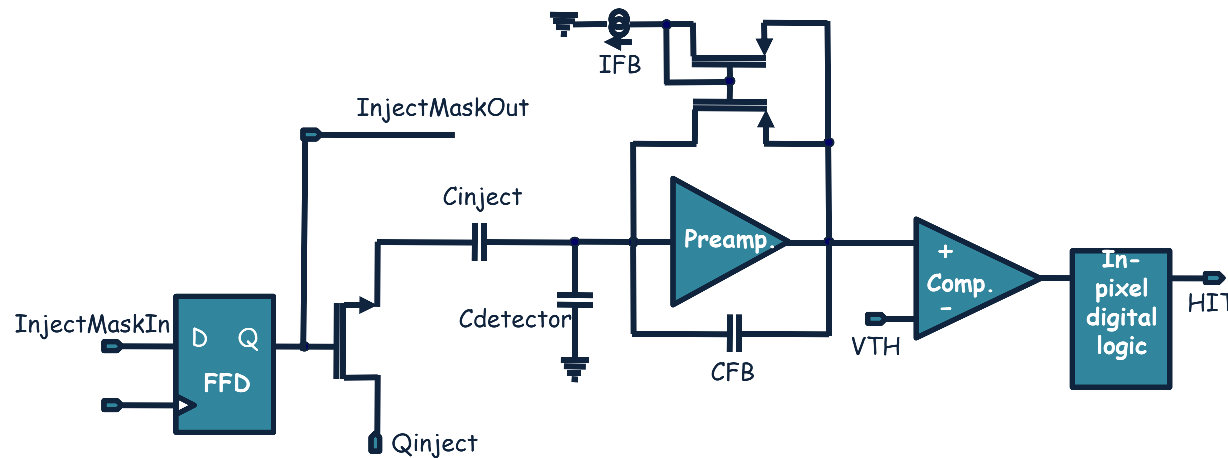
Superpix0: performance and limitations of a 2D CMOS readout chip for 50x50 um^2 high resistivity pixels

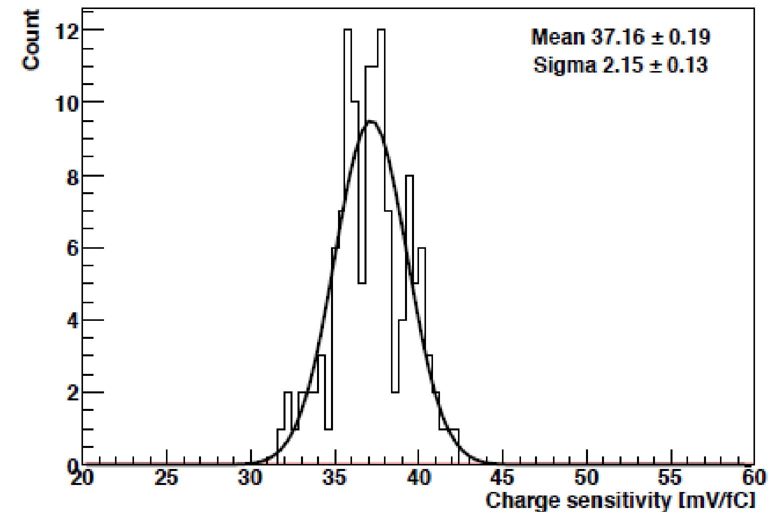
Test results with sensor:

ENC: 100 e rms
Threshold dispersion: 500 e-
Gain: 40 mV/fC
(with ~5% dispersion)
Power: 2 μW/pixel

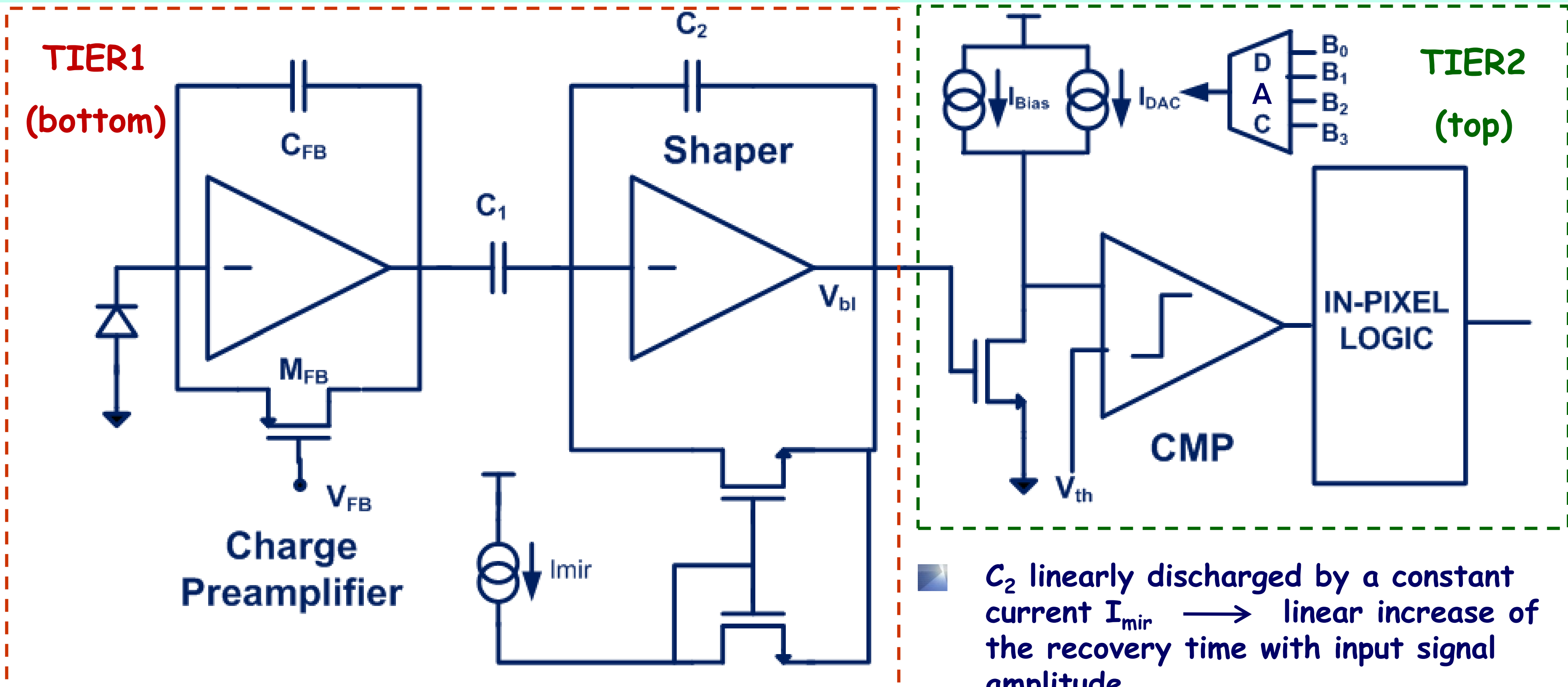


The chip architecture is derived from the 2D APSEL MAPS, with a shaperless front-end and a 2x8 MacroPixel readout structure.





Superpix1: a 3D CMOS chip for 50x50 um^2 pixels

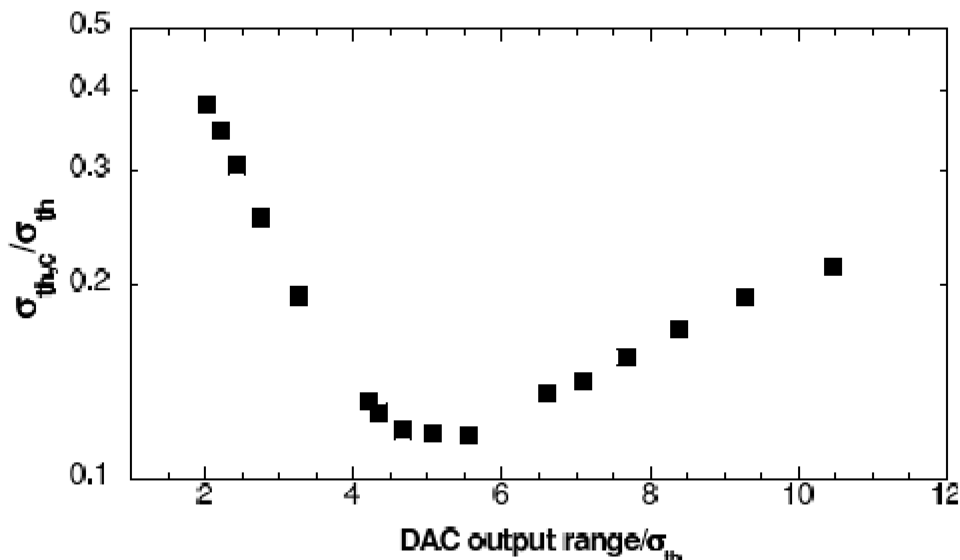


- C_2 linearly discharged by a constant current I_{mir} ⟶ linear increase of the recovery time with input signal amplitude.
- Lower detector parasitic capacitance ($C_D \approx 150$ fF): lower noise and power consumption
- Fine tuning system in order to reduce the threshold dispersion:
  - I_{DAC} is set by a 4 bit current steering DAC in each channel.
  - DAC driven by a thermometric code decoder.

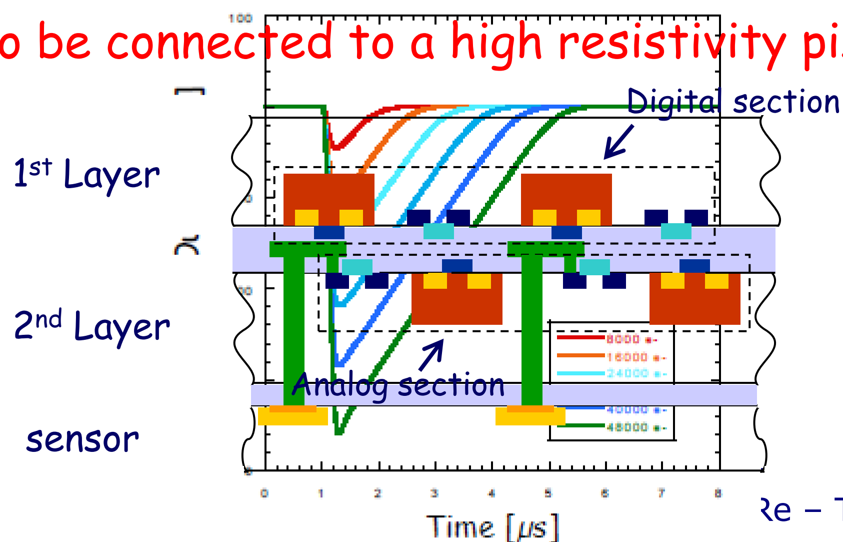
  All in a 50 µm pixel pitch
- Lower power consumption ($I_{cell} \approx 7\mu A$) reduces the voltage drop effects on the channel-to-channel baseline voltage (V_{bl}) dispersion ⟶ current mirror, also less noisy than transconductor.

Superpix1: a 3D CMOS chip for 50x50 um² pixels

- This plot shows that an optimum condition exists for the threshold correction operation (DAC output range $\approx 5\sigma_{th}$):



To be connected to a high resistivity pixel sensor



	Superpix1
Charge sensitivity	48 mV/fC
Peaking time @ 16000 injected electrons	260 ns
ENC	130 e-
Threshold dispersion before/after correction	560/65 e-
Analog power consumption	10 μW/pixel
Detector capacitance	150 fF
Matrix size	128x32 pixels
Pixel pitch	50 μm

- **The readout architecture is the same as in the 3D MAPS device**

Status of 3D integration of pixel sensors and electronics for the SuperB SVT (3D APSEL)

Cell layout (schematic v3) – analog layer

Voltage drop compensation

Sensor area: 716 μm^2

Area of NW PMOS: 95 μm^2

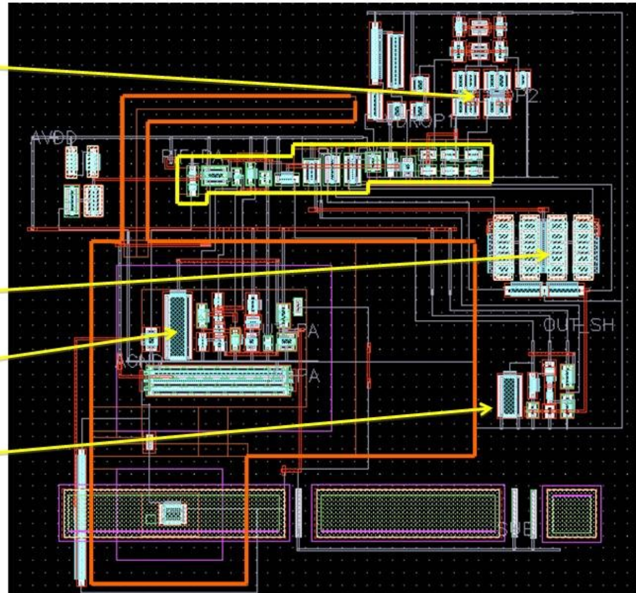
Fill factor: 0.88

Gm

PA

Shaper

Estimated sensor capacitance ≈ 290 fF



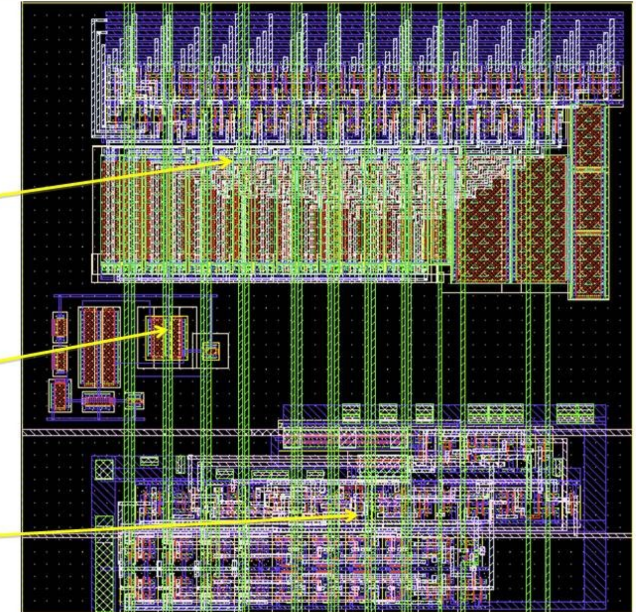
ApselVI 3D MAPS - Analog FE

Cell layout – digital layer (draft)

DAC

Threshold discriminator

In-pixel logic



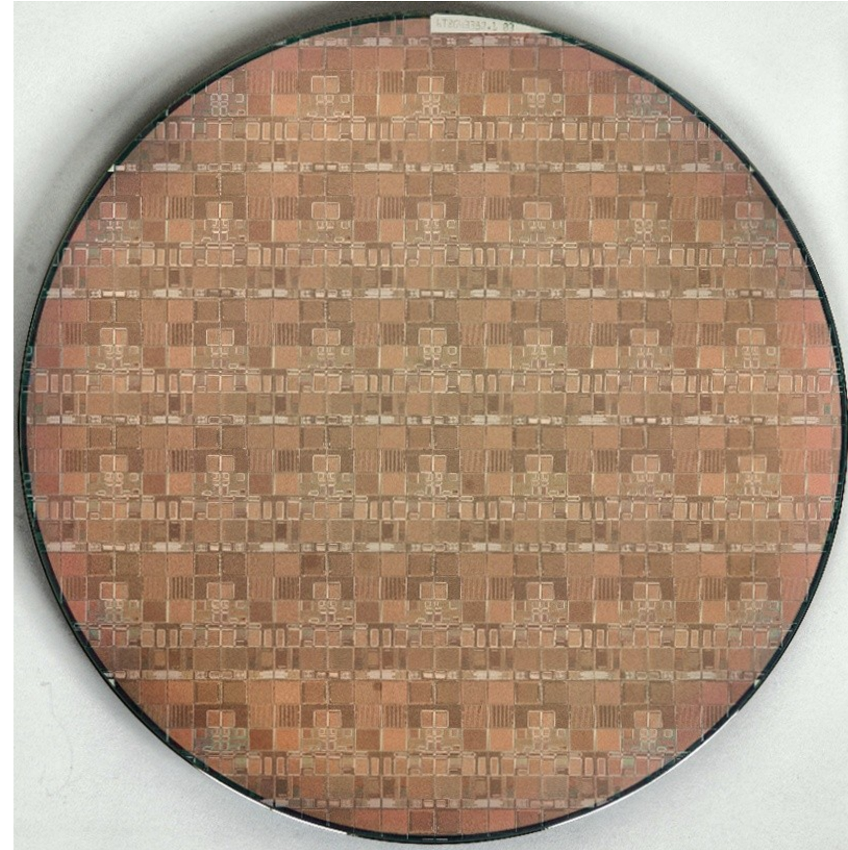
ApselVI 3D MAPS - Analog FE

We are getting ready for a submission in the Tezzaron/GlobalFoundries technology, which will be organized by CMC/CMP/MOSIS.

But, before this, we would like to test the chips from the first run of the 3D-IC consortium.

The first 3D-IC run

- In 2009, the Italian VIPIX collaboration submitted 3D active pixel devices in the first run of the 3DIC Consortium.



- In January 2011, we received the first samples, before the interconnection. These 2D devices were successfully tested.

- These chips include MAPS devices with two different designs:

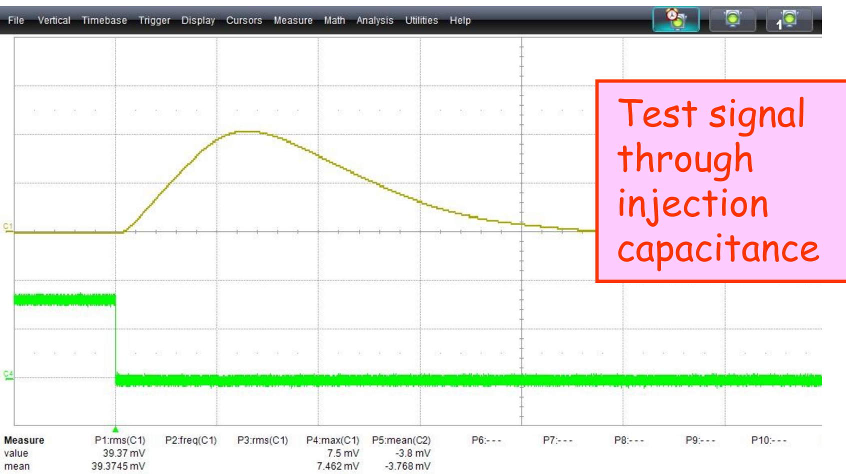
  - 1) APSEL-like chip (data driven continuous sparsified readout, 40 x 40 μm^2 pixels)

  - 2) Chip for the ILC Vertex (intertrain sparsified readout, 20 x 20 μm^2 pixels)

Tests of the layer with sensing electrode and analog front-end in APSEL chips from the first run of the 3D-IC consortium

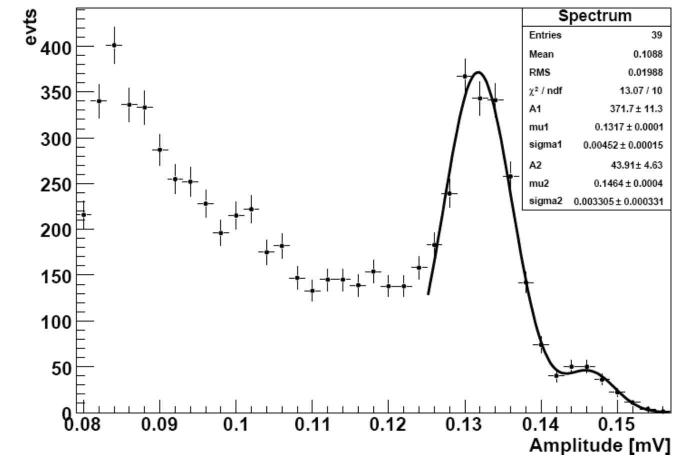
Analog signals, electronic noise (ENC ~ 50 e) and spectra from radioactive sources have been measured.

Signal at shaper output



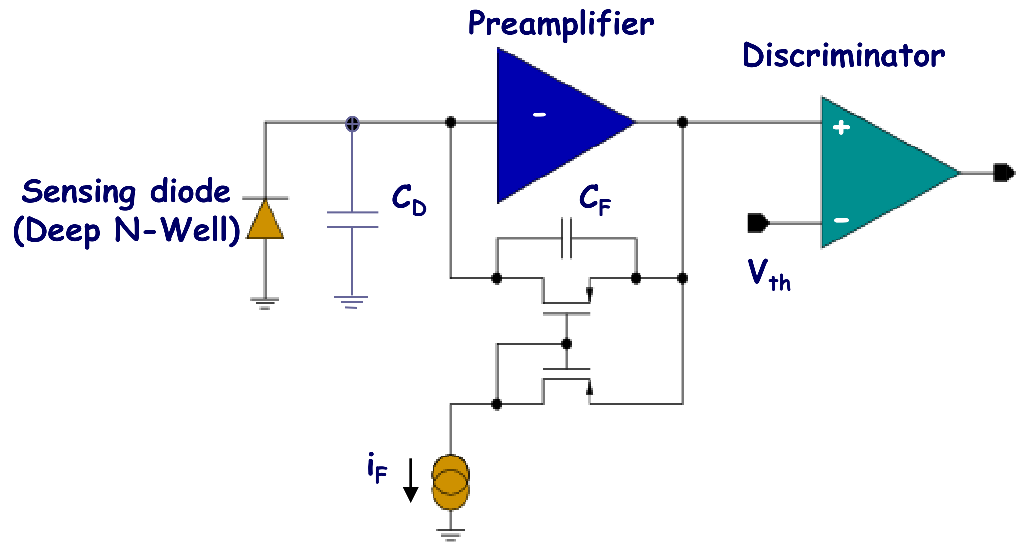
Test signal through injection capacitance

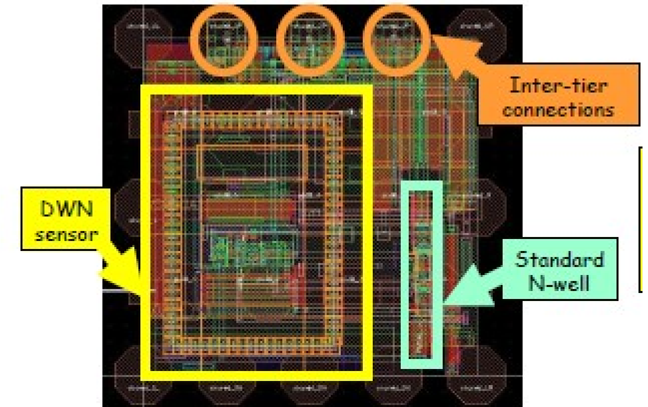
^{90}Sr event



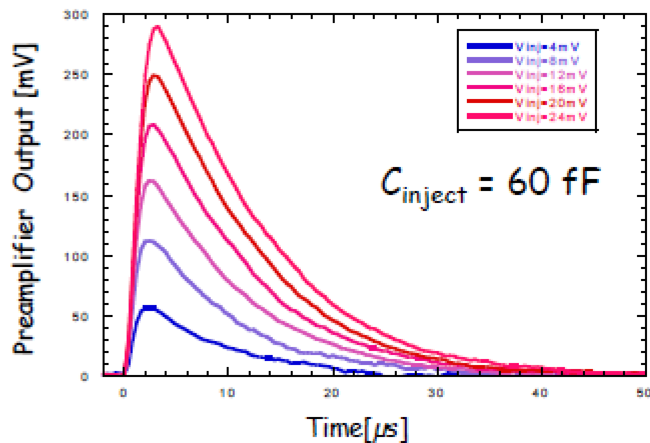
From ^{90}Sr spectra, average signal from MIPS is close to 900 electrons (MPV).

Tests of the the analog layer in a 64x64 matrix (ILC VTX design) in the first run of the 3D-IC consortium

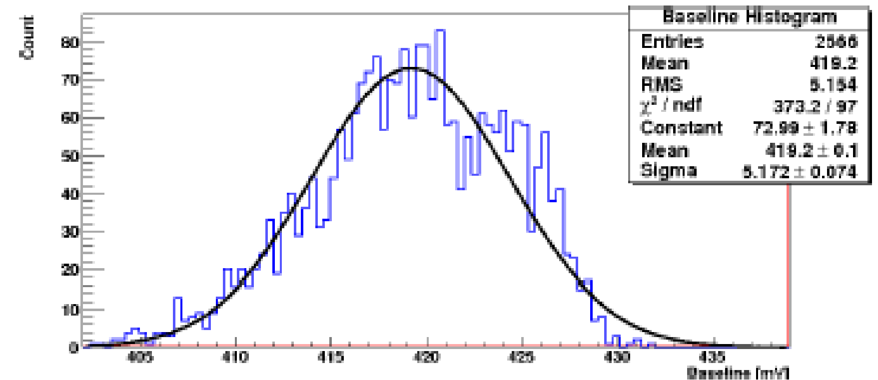




Measured ENC ~ 70 e at 5 μW/pixel power dissipation



threshold dispersion ~ 50 e

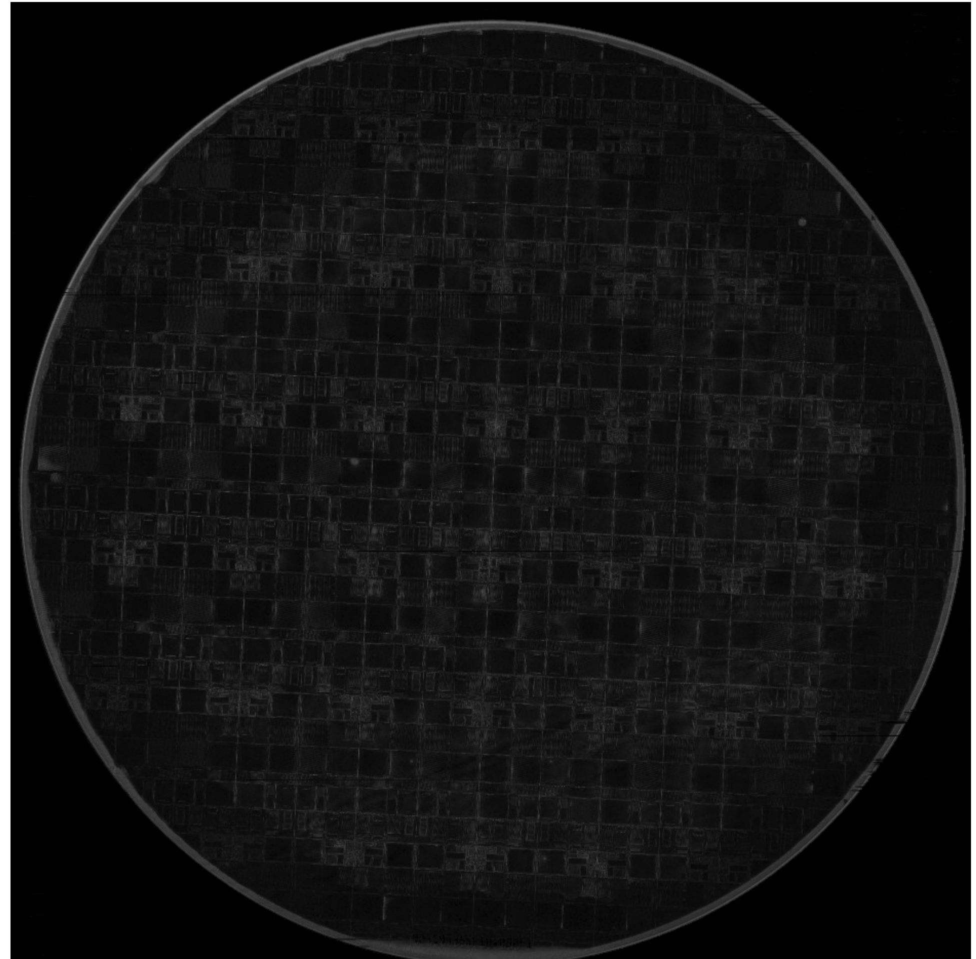


3D processing is slowly progressing

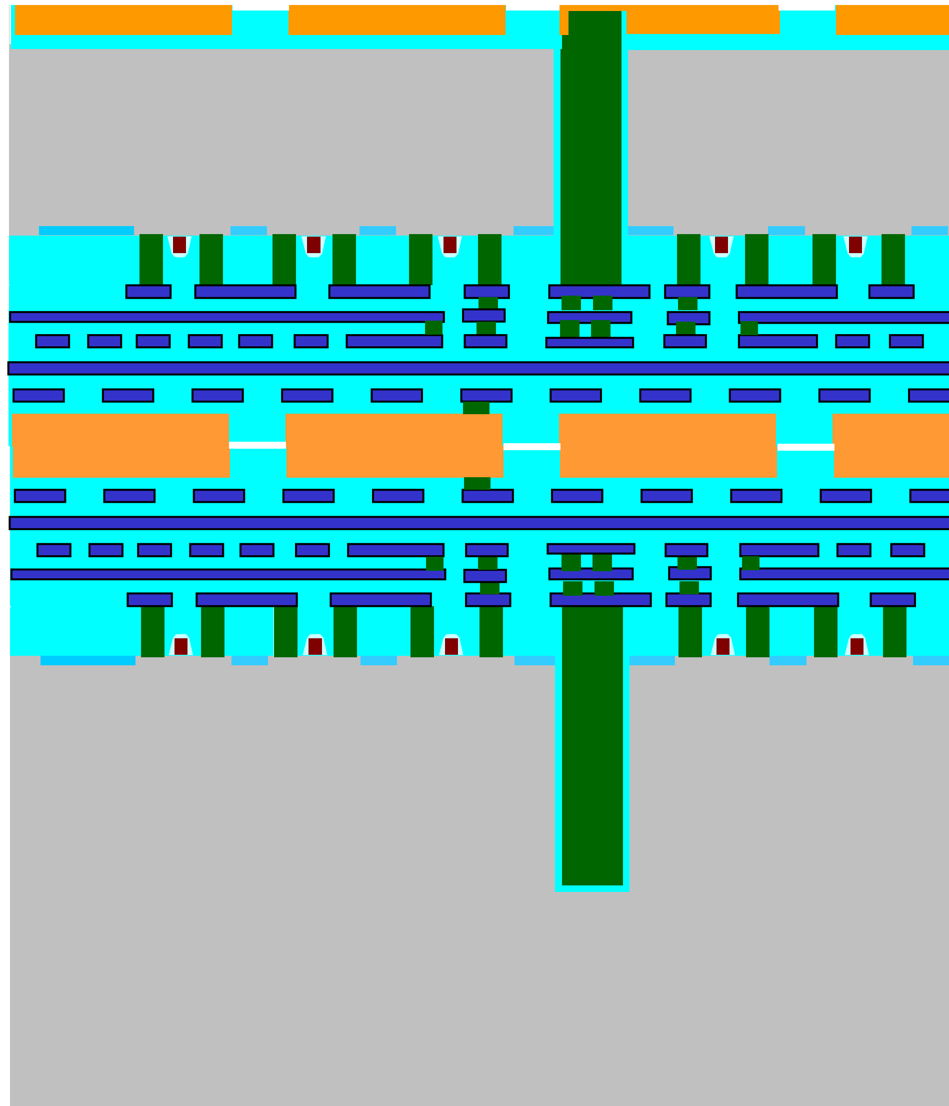
All tested 2D circuits are working, suggesting that 3D bonded circuits should work.

By May 17 two wafer pairs were bonded with good bonding results. Thinning is the next step, followed by backside metal deposition and finally chip dicing.

The second 3D-IC run will start soon after the tests of chip from the first run.



Remaining 3D processing steps in the first run of the 3D-IC consortium

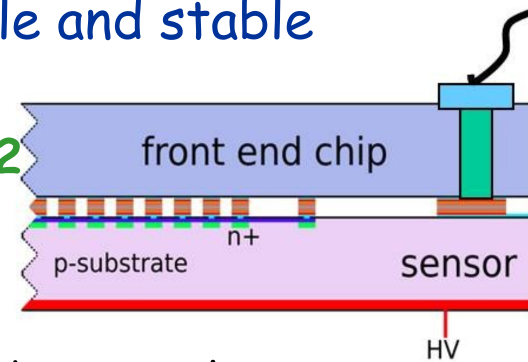


Thin wafer-2 to about 12 um to expose super via.

Add metallization on back of wafer-2 for bump bond or wire bond

Open issues and further R&D

- **3D integration:** can we access this technology in a reliable and stable way? Are there other useful approaches to 3D?

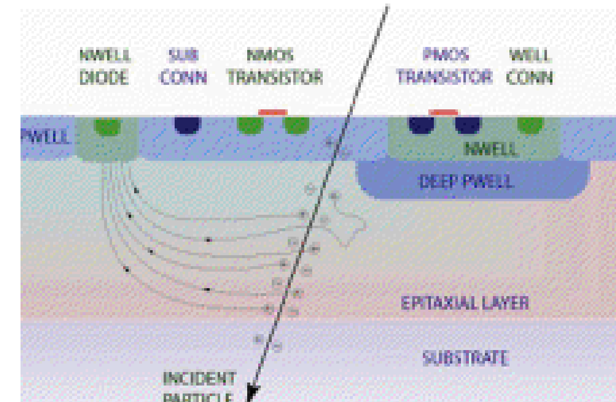


AIDA WP3: Advanced pixel sensors based on 3D integration of 2 layers in heterogeneous technologies (talk by H.-G. Moser on Tuesday in the satellite 3D meeting)

"**via last**" process, 4-side buttable device (reducing dead area and material budget) with low density interconnections in the device periphery.

- **Hybrid pixels:** can they be thin enough? Thinning studies of readout chips and sensors are being pursued by the pixel community

- **MAPS:** Tolerance to displacement damage could be a showstopper (estimated yearly fluence $\phi \sim 5 \times 10^{12}$ n/cm^2); a high-resistivity, fully depleted sensing layer with analog CMOS front-end might be the solution



CMOS sensor in the 180nm INMAPS process with high res. epilayer

Conclusions

- The performance of the innermost Layer0 of the Silicon Vertex Tracker at SuperB can greatly benefit from 3D integration in terms of both electronics and sensor
- An advanced pixelated detector will be required by Layer0 when SuperB operates at full luminosity (about 2 years after first collisions) because of high background
- R&D will proceed to a technology choice on Layer0 pixels in about two years from now

The INFN VIPIX collaboration

VIPIX - Vertically Integrated PIXels

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L. Bissi[8], P. Ciampolini[8], A. Marras[8], G. Matrella[8], P. Placidi[8], E. Pilicer[8], D. Passeri[8], L. Servoli[8], P. Tucceri[8]

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Backup slides

Exploiting 3D integration: readout architecture without MacroPixel

- The MacroPixel arrangement was adopted to reduce the pixel-level logic (limiting the area of competitive N-wells) and the digital switching lines running above pixel columns

- Reasons to eliminate the MacroPixel architecture:
  - **The routing of private lines (FastOR, Latch Enable) scales with matrix column dimension**
  - **Inefficiency due to dead time (freezed MP) depends on MP dimensions**
  - **Not-fired MP columns of fired MPs are also scanned (time consuming) by the sparsification logic**
  - **Only MP masking level can be reasonably implemented**

- Matrix readout speed can increase, also carrying along a readout logic simplification

- Removing the MacroPixel and implementing timestamp latching at the pixel level appears possible with 3D integration, without reducing the pixel efficiency

Tezzaron vertical integration process flow (VIA FIRST):

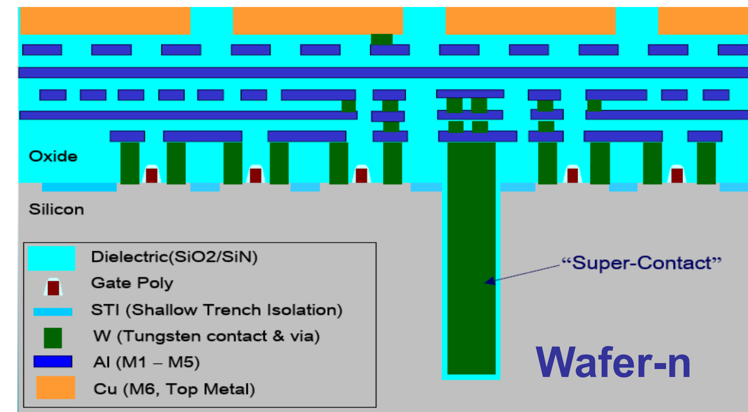
• multi-tier tier chip; Tezzaron includes standard CMOS process by Chartered Semiconductor, Singapore.

Step 1: Fabricate individual tiers; on all wafers to be stacked: complete transistor fabrication, form super via Fill super via at same time connections are made to transistors

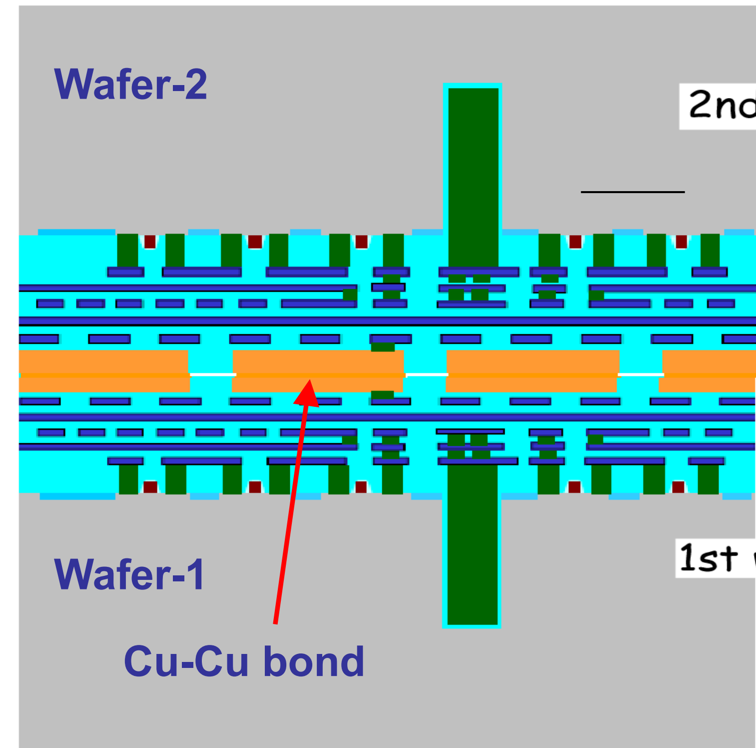
Oxide
Silicon
Dielectric(SiO2/SiN)
Gate Poly
STI (Shallow Trench Isolation)
W (Tungsten contact & via)
Cu Al (M1 – M5)
Cu (M6, Top Metal)
"Super-Contact"
6 μm
Wafer-n

All wafers are bulk

Step2: Complete back end of line (BEOL) process by adding Al metal layers and top Cu metal (0.7 μm)

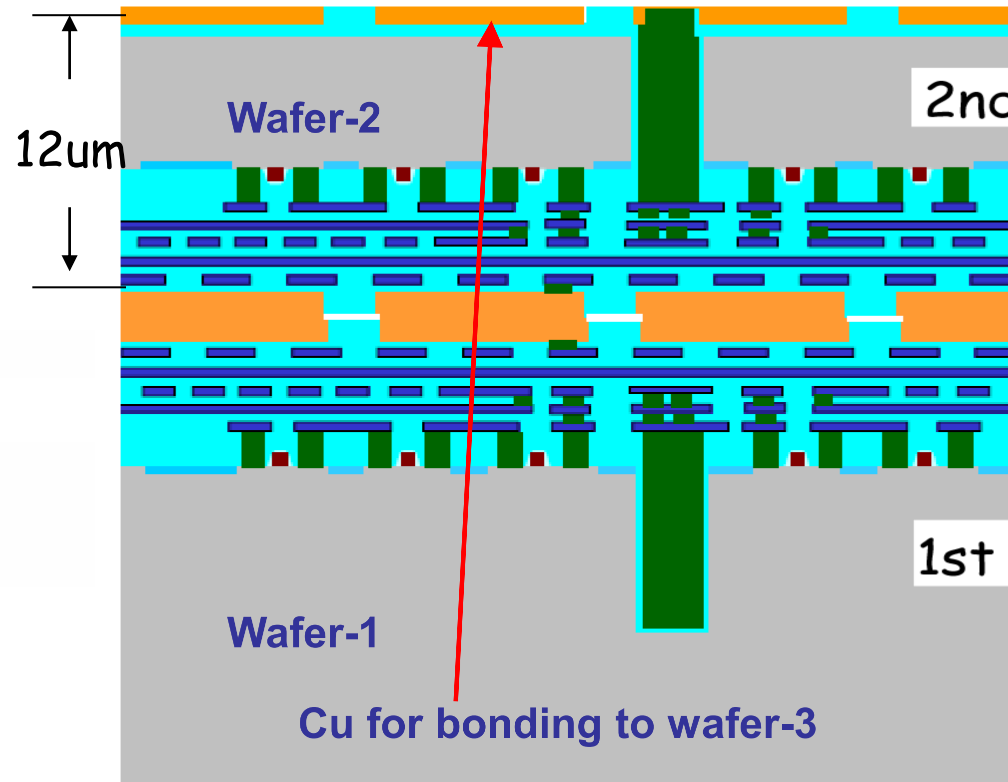


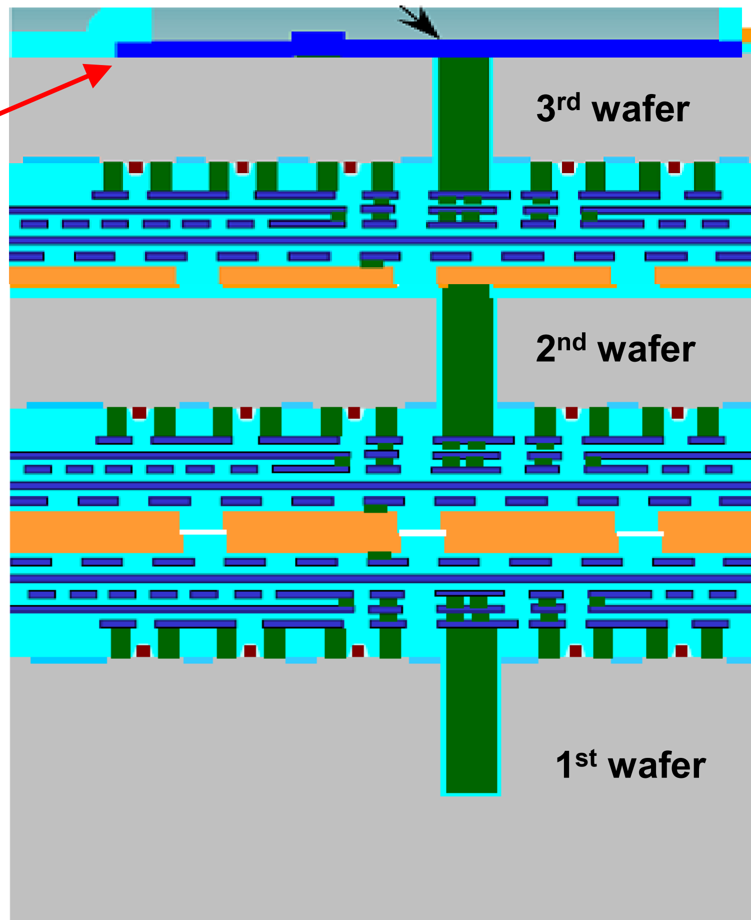
Step 3: Bond wafer-2 to first wafer-1 Cu-Cu thermo-compression bond



Tezzaron vertical integration process flow:

Step 4: Thin the wafer-2 to about 12 um to expose super via. Add Cu to back of wafer-2 to bond wafer-2 to wafer-3
OR stop stacking now! add metallization on back of wafer-2 for bump bond or wire bond

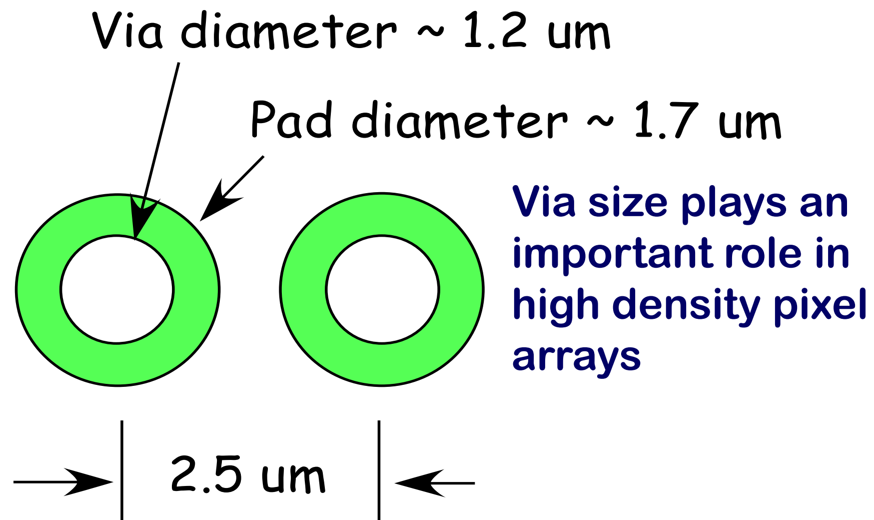




Step 5: Stack wafer-3, thin wafer-3 (course and fine fine grind to 20 um and finish with CMP to expose W filled vias)
Add final passivation and metal for bond pads

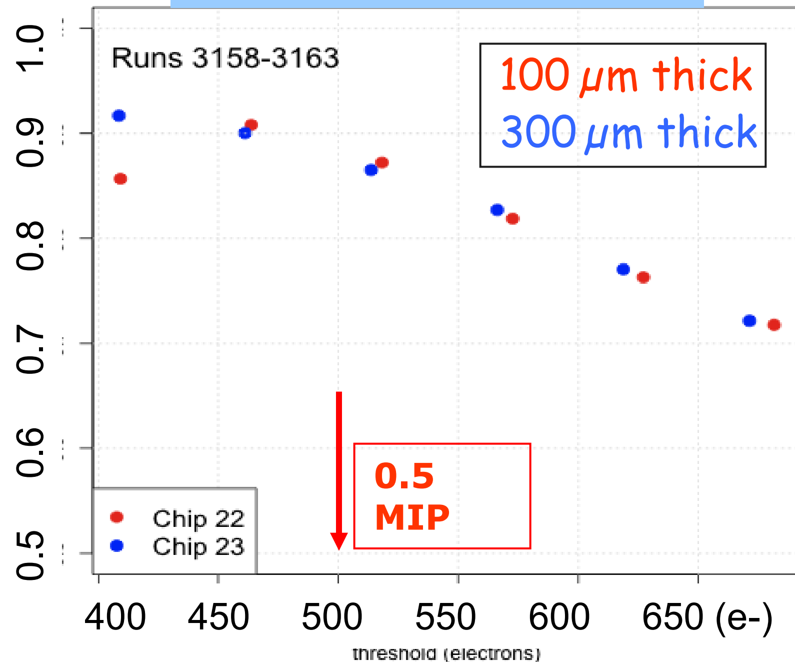
Advantages of Tezzaron process

- No handle wafers needed
- No extra space allotment in BEOL processing for vias
- Vias are very small
- Vias can be placed close together
- Minimal material added with bond process
  - 35% coverage with 1.6 um of Cu gives Xo=0.0056%
  - No material budget problem associated with wafer bonding.
- Good models available for Chartered transistors
- Thinned transistors have been characterized
- Process supported by commercial tools and vendors
- Fast assembly
- Lower cost



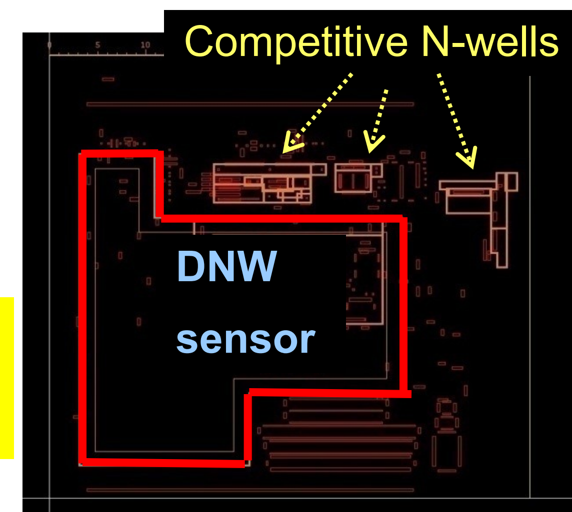
Via size plays an important role in high density pixel arrays

DNW MAPS Hit Efficiency measured in a CERN beam test (APSEL4D)



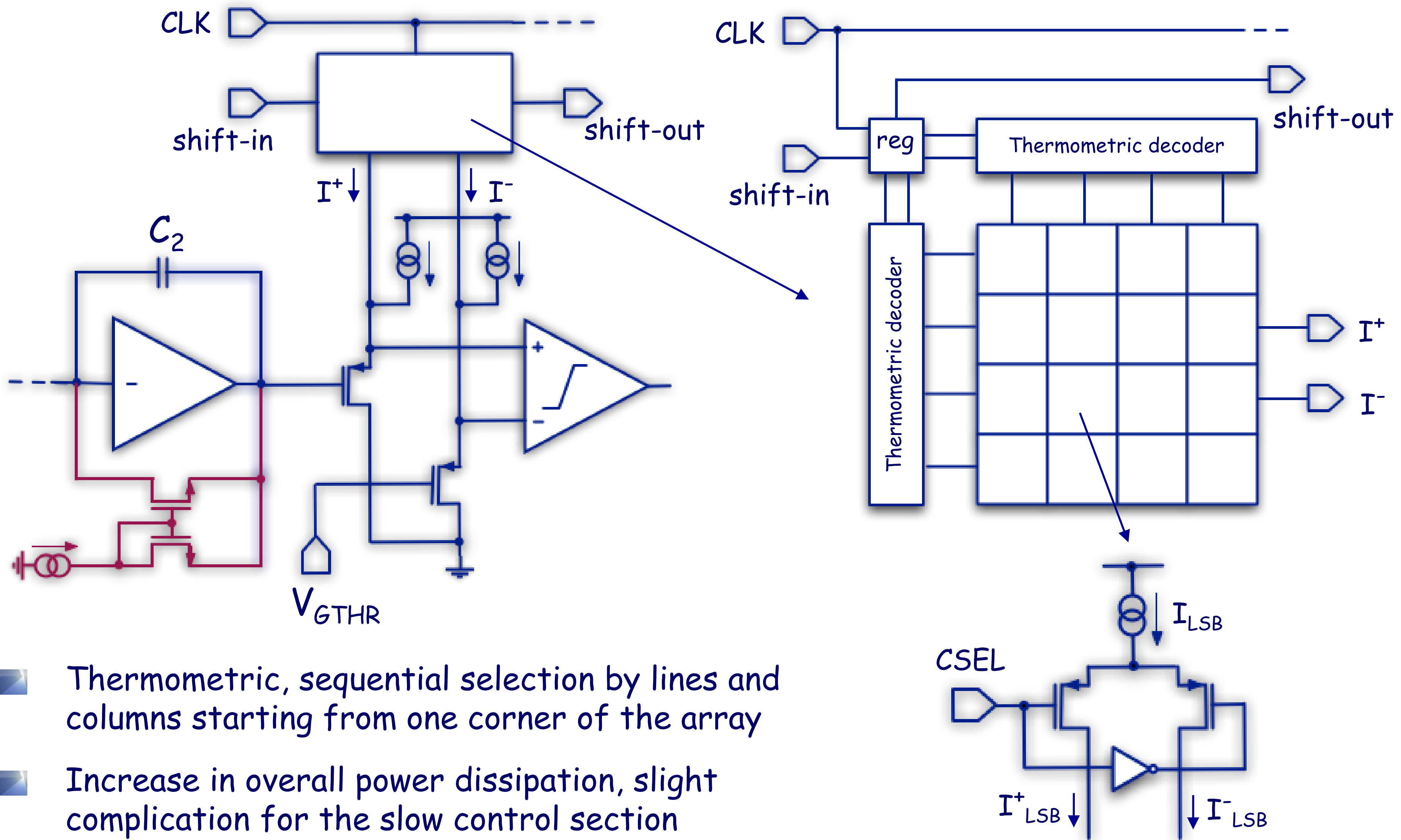
Measured with tracks reconstructed with the reference telescope extrapolated on MAPS matrix

- MAPS hit efficiency up to 92 % with threshold @ 400 e- (~ 4σ_noise+2σ_thr_disp)
- 300 and 100 μm thick chips give similar results
- Intrinsic resolution ~ 14 μm compatible with digital readout.



- Competitive N-wells (PMOS) in pixel cell can steal charge reducing the hit efficiency

4-bit current steering DAC



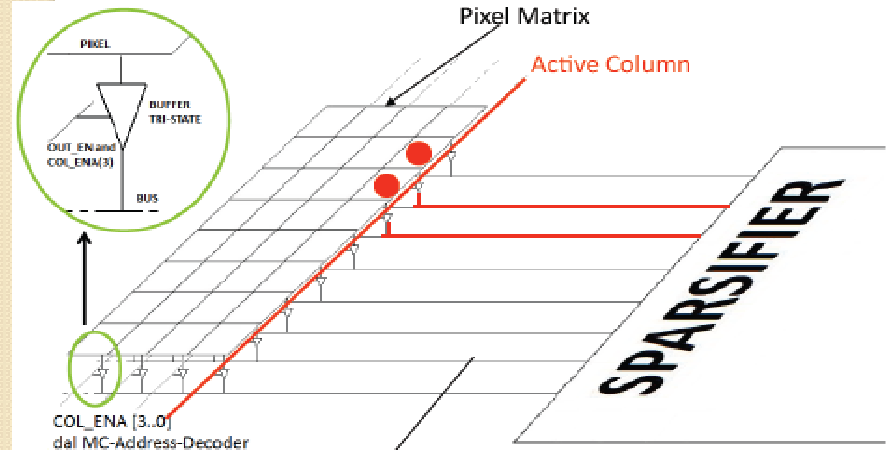
- Thermometric, sequential selection by lines and columns starting from one corner of the array
- Increase in overall power dissipation, slight complication for the slow control section

FE Chip architecture

- Use data push readout architecture developed for MAPS chip, now optimized with target rate (100 MHz/cm2) for full chip size (~1.3 cm2)
- VHDL simulation: readout efficiency > 98% @ 60 MHz RDclock
- Space time coordinates with time granularity 0.2-5.0 us (BCO clock)

Matrix overview

- Binary **pixels matrix**
- Column-wide **shared data-bus**
- **One column read per clock cycle**

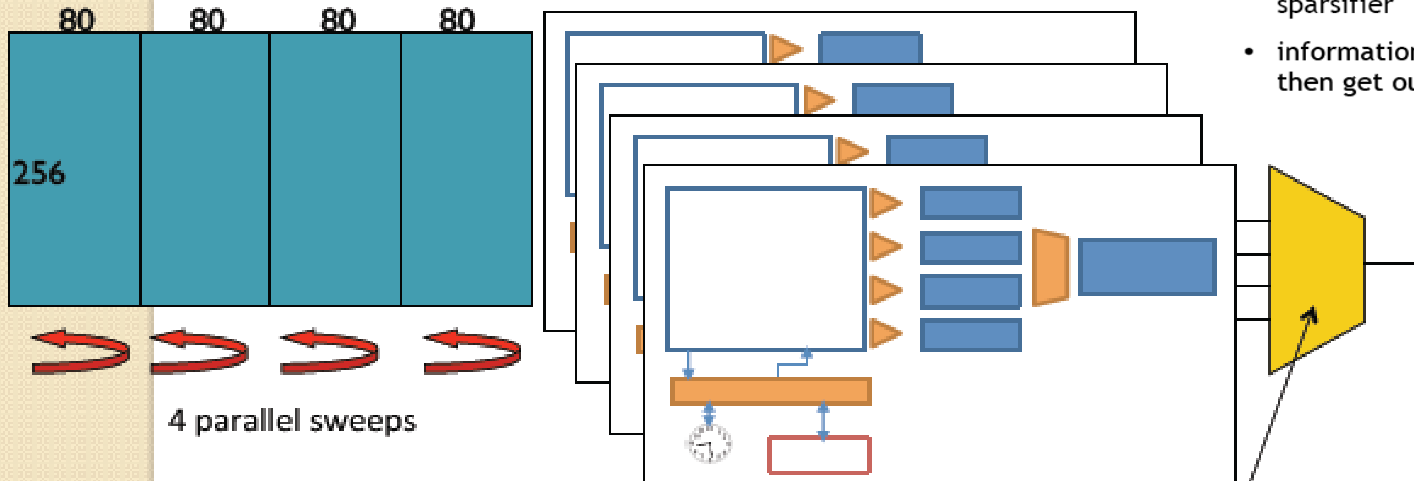


Common Pixel Data Bus – Active 1 column of pixel at a time

- the per-column readout starts at the arrival of a BC which increase also the time counter
- for each column, each MP is read by a sparsifier
- informations are collected in barrels and then get out of the submatrix

6

- Each sub-matrix scan has its own readout & scan logic
- All readout working in parallel
- Queuing output system



Common output stage

- Data from the final barrel are sent to a common bus with a faster clock ~ 160 MHz

- Each readout sweeps a portion of the matrix with 60 MHz clock.

Vertically integrated MAPS in the second 3D-IC run: APSEL