The Front-end Electronics for the Daya Bay Neutrino Experiment

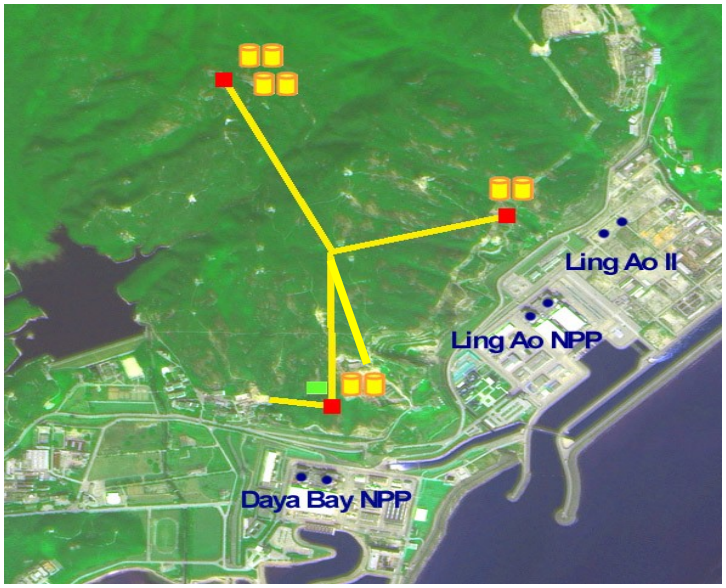
for Daya Bay Collaboration

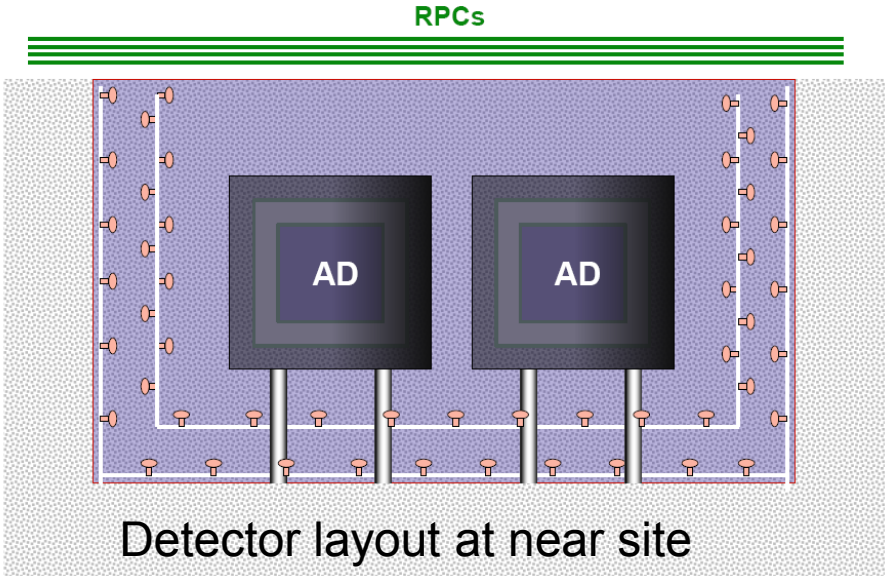
WANG Zheng
wz@ihep.ac.cn
Institute of High Energy Physics, Chinese Academy of Sciences

Outline

- Introduction on Daya Bay experiment
- PMT electronic system
- RPC electronic system
- Current status of the electronic system
- Summary

The Experiment





- **Near-far relative meas. to cancel correlated syst. errors**
  - **2 near cites + 1 far cite**
- **Multiple neutrino detector modules at each site to cross check and reduce un-correlated syst. errors**
  - **Gd-loaded liquid scintillator**
  - **Stainless steel tank+ 2 nested acrylic vessel + reflectors**
- **Multiple muon-veto to reduce bkgd-related syst. errors**
  - **4-layer RPC + 2-layer water Cerenkov detector**

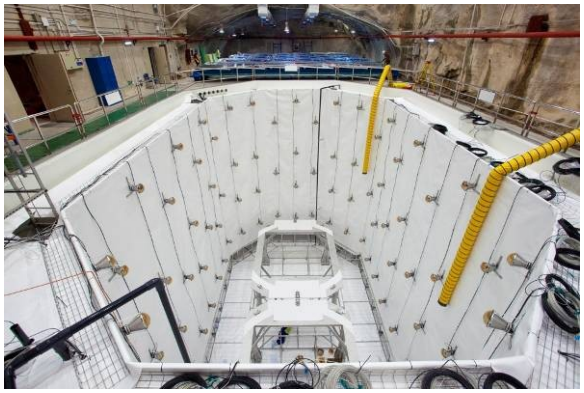
Detectors and electronics each site

Antineutrino Detector

(192 8'PMTs)

X2 near site
X4 far site

2 or 4 PMT readout systems

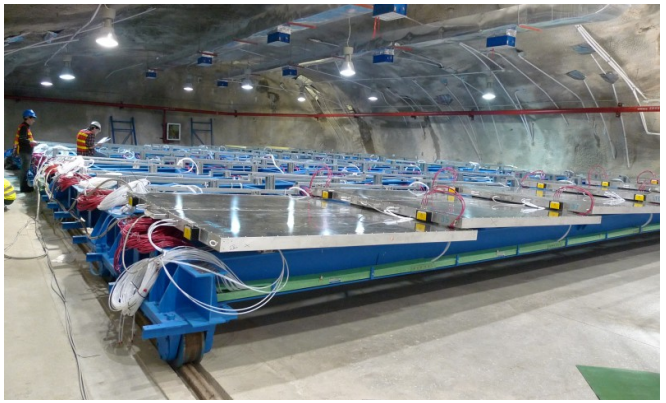


Inner and outer Water Cherenkov Detectors

(289 or 392 8'PMTs)

289 near site
392 far site

2 PMT readout systems



RPC Detector

(1728 readout strips)

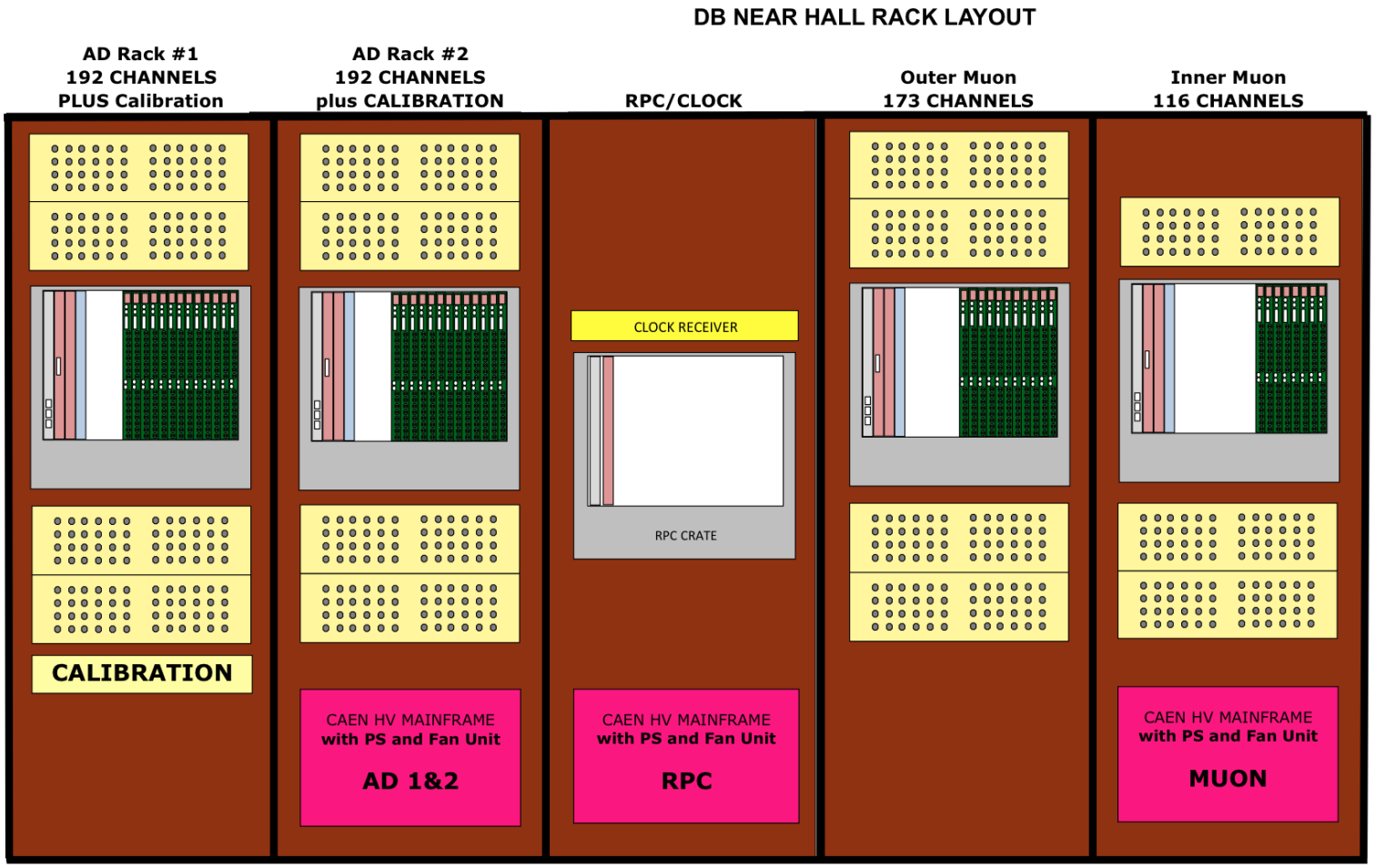
1 RPC readout system

Electronic system

Each detector has standalone readout electronic system. Each system is a single 9U VME crate and it can do data taking individually.

Readout system	Antineutrino Detector	Water Cherenkov Detector	RPC detector	Site subtotal
Daya Bay near site	2	2	1	5
Ling Ao near site	2	2	1	5
Far site	4	2	1	7
Detector subtotal	8	6	3	17

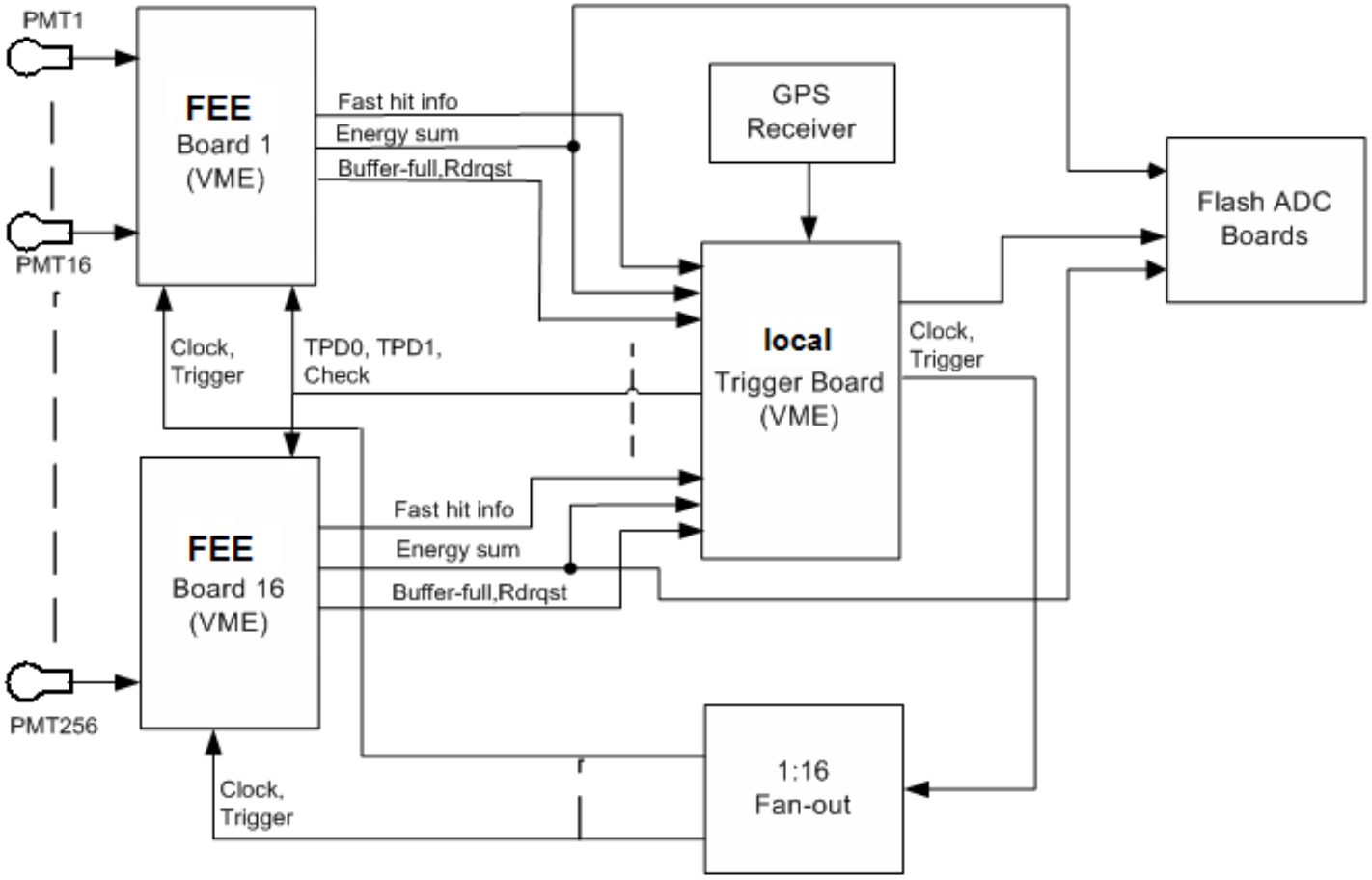
Electronic system for DB near site



PMT Electronic System

- **The PMT Electronic System is designed to process the PMT signals from either Antineutrino Detector (AD) or Water Cherenkov Detector (WCD).**
- **Functions:**
  - **Determine the *charge* (energy) of each PMT signal**
  - **Provide precision *timing* information (from PMT hit to trigger) that can be used to reconstruct the location of the antineutrino interaction**
  - **Generate multiplicity (nPMT) trigger**
  - **Generate total energy (ESUM) trigger**
  - **Energy Sum waveform of each 32 PMTs is digitized using 1GHz flash ADC for cross check.**

PMT Electronic System



Each PMT electronic system sits in single 9U VME crate

FEE Specifications

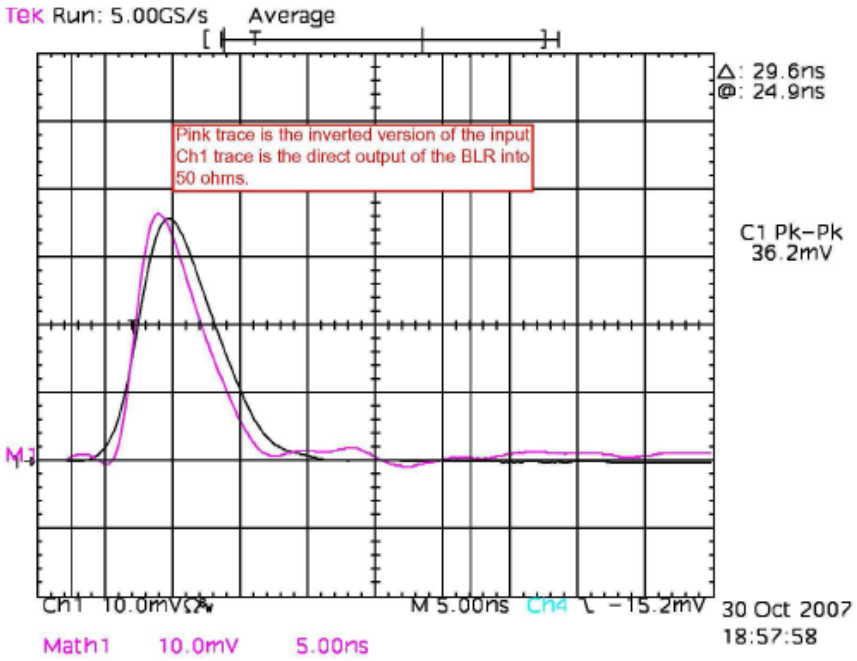
Quantity		Specification
Charge dynamic range		0-1800 pC
	Fine Range	0-160 pC (100pe@PMTgain 2E7)
	Coarse range	160-1800 p.C
Shaping width		<325ns down to 1%
Peak error		< 4% @ 40MSPS
ADC bit resolution		< 10% @ 1.6 pC
ADC Bits		12 bits for fine range 12 bits for coarse range
ADC Sampling rate		40 MSPS
Disc. threshold		0.25 p.e. (programmable each chnl.)
Time range		0-1.3 us
Time bin		1.5625ns
Timing Precision (RMS)		<1 ns
Multi-hit separation		Yes
Multi-hit resolution		50 ns

FEE Specifications (cont.)

Quantity	Specification
Real time nPMT to LTB	5-bit LVDS @ 80M
ESUM to LTB	2-wire LEMO (2.5V@100p.e.)
ESUM to FADC Bd.	2-wire LEMO (2.5V@100p.e.)
Clock input	receiving 40M clock from fan-out bd. 2-wire LEMO (lvPECL)
Trigger input	receiving trigger from LTB (lvPECL)
Signal input connector	BNC
Signal input impedance	50 Ohm
Channels/board	16
Data Readout	CBLT (Chained Block Transf.)
VME standard	9U VME 64Xp (340mm)
Power backplane	Wiener defined power pins (P3)

PMT signal characteristics

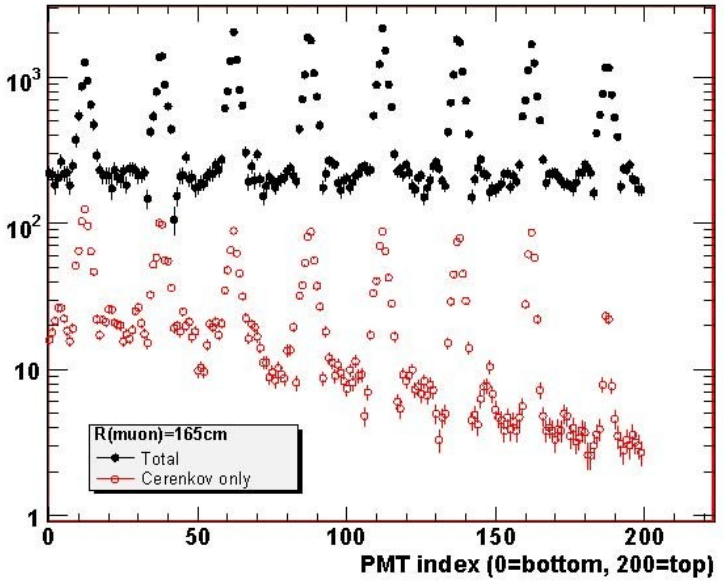
from TDR 4.5 PMT System



rising edge : 4ns

falling edge : 10ns

# of p.e. versus PMT number



MC of muons passing through the AD

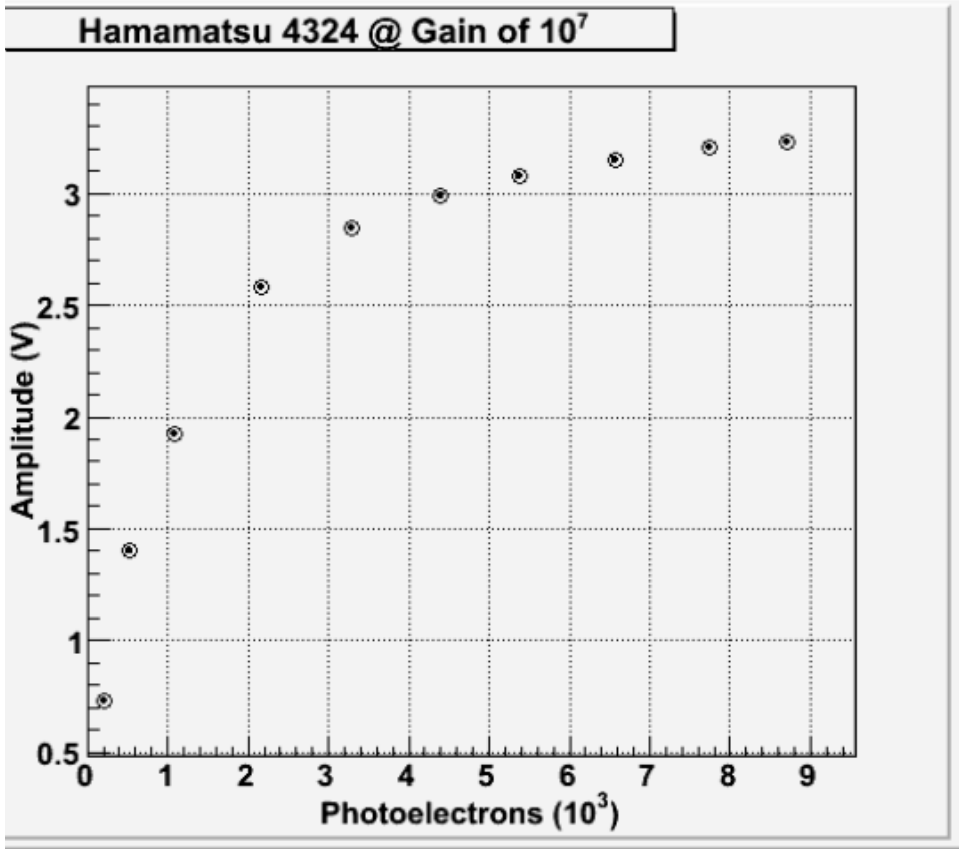
dynamic range : 2000 p.e.

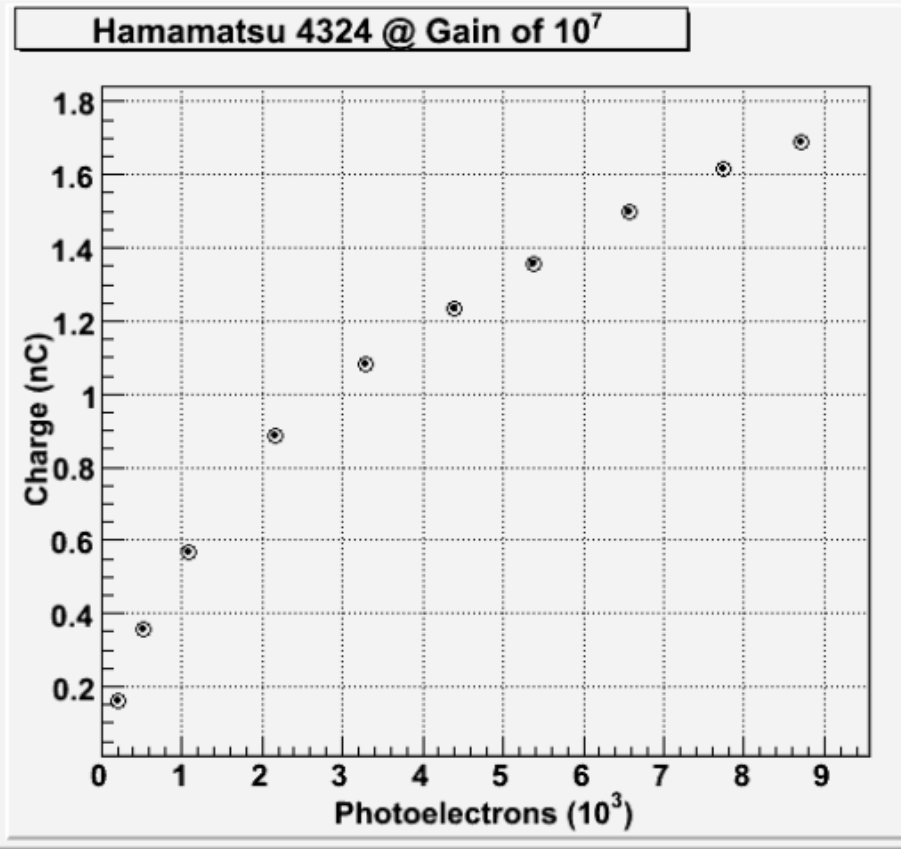
Gain	$\geq 10^7$ for all PMTs with appropriate tapered resistive base. — PMTs must achieve a gain of 3×10^7 at V0 $\leq$2 kV
Pulse Linearity	— PMT anode pulse linearity must be better than 5% over the dynamic range of 0–1 nC at a gain of 10^7

gain: 2×10^7

linearity: 5%@(0－625p.e.)

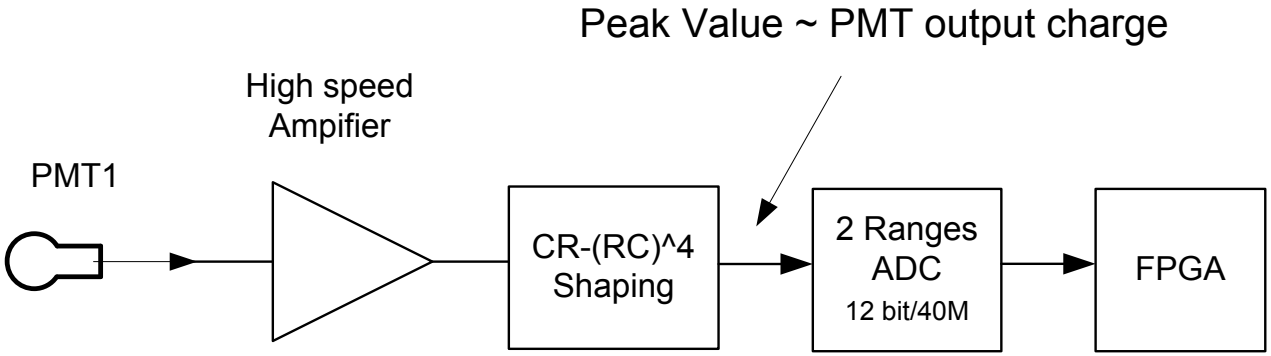
Linearity of PMT output

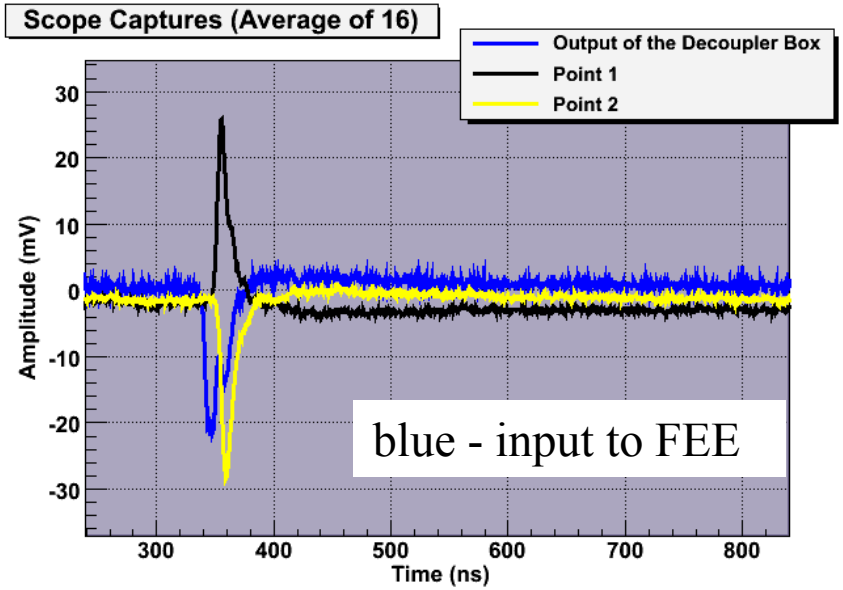


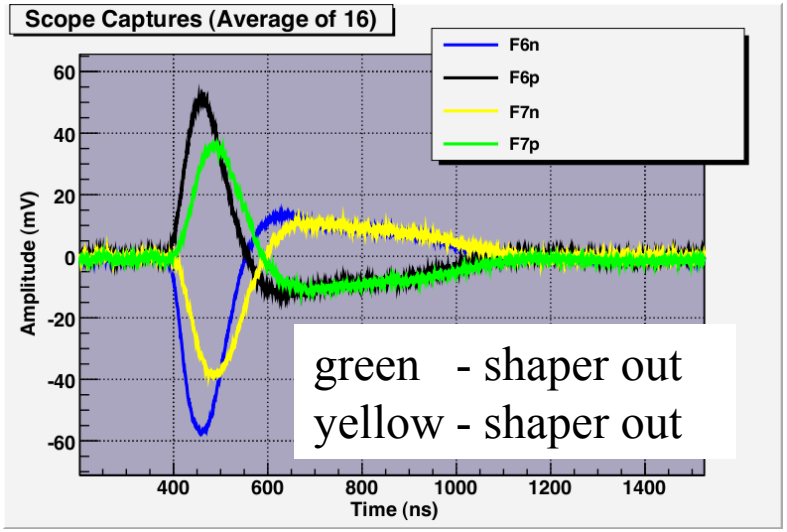


Hamamatsu R5912 PMT response to large light signals

Charge Measure Solution

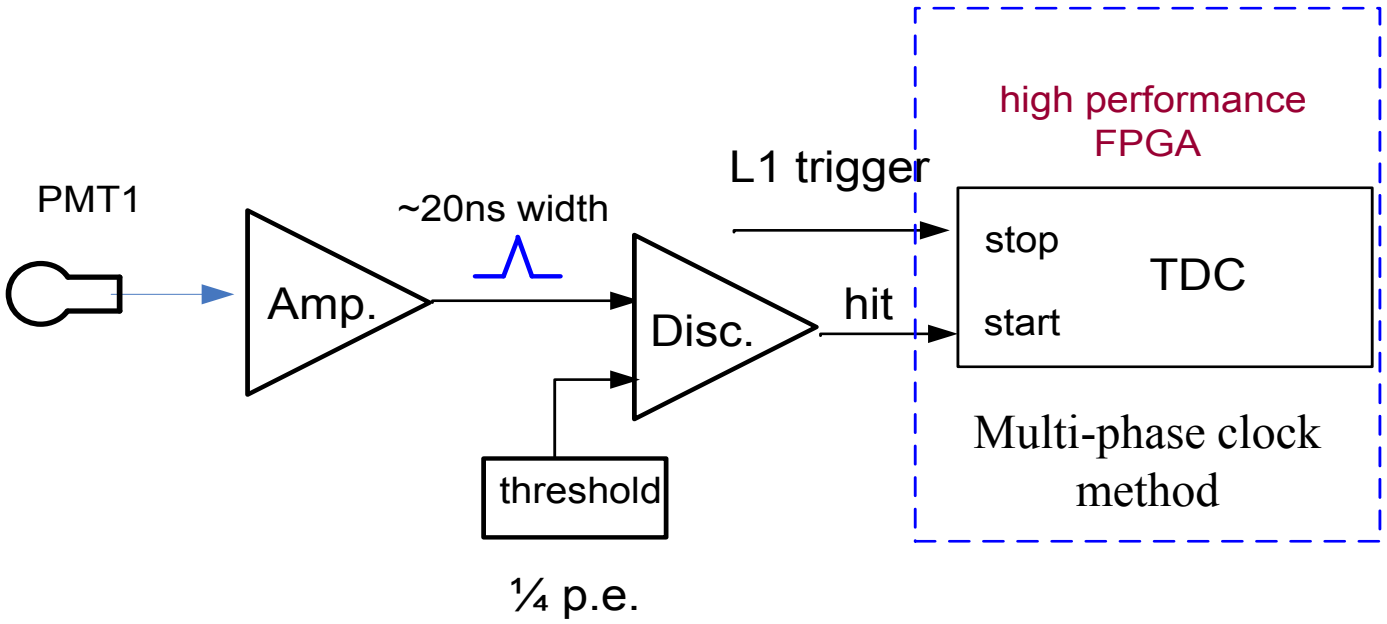






- Amplitude of shaper output is in scale of input charge

Time measure scheme

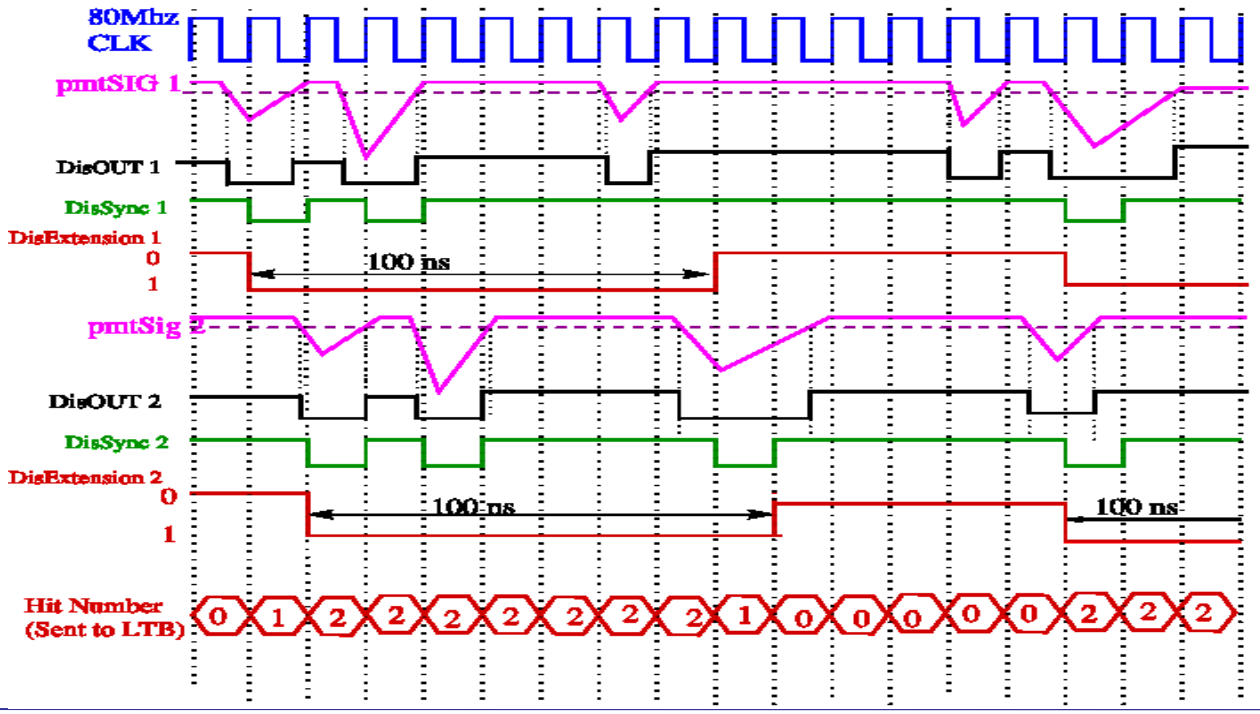


- Measuring the time from PMT over threshold/hit to trigger
- Rising edge timing method
- Multi-hit TDC
  - Two hits separation >= 50 ns

Time bin: 1.5625ns

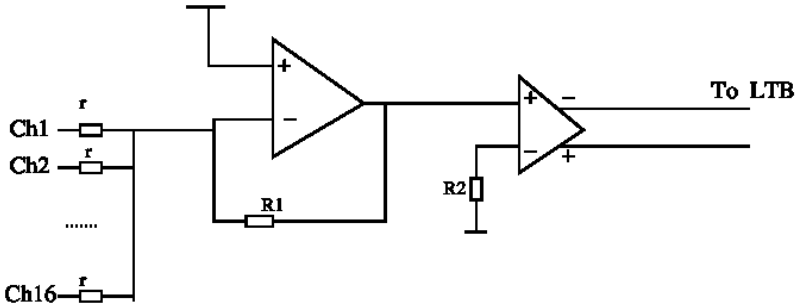
nPMT Generation

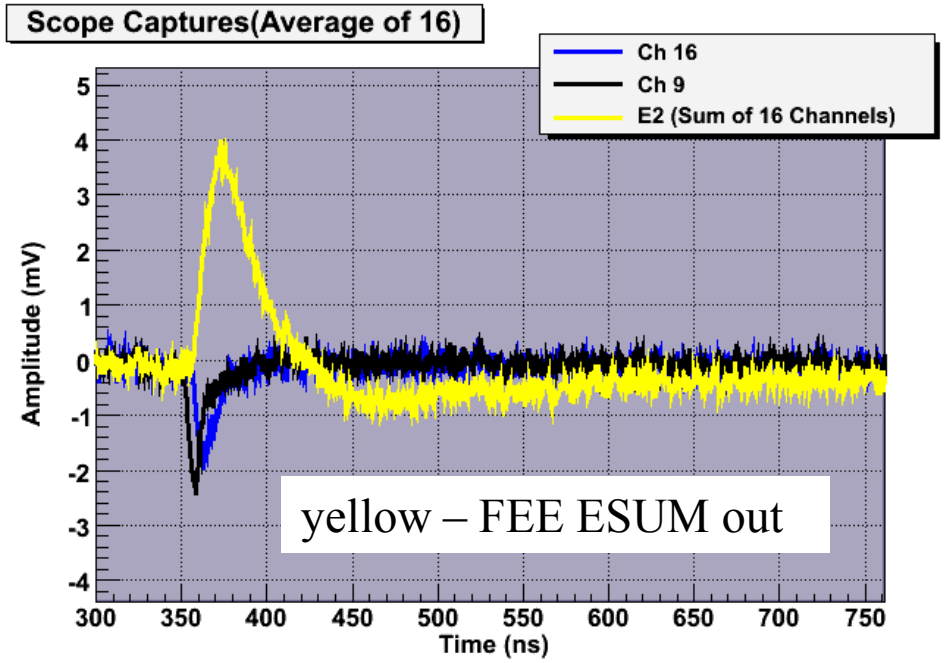
- PMT pulses are amplified and sent to a fast discriminator
- The DisOUT is then synchronized with the 80 Mhz clock be extent to 100 ns
- nPMT == coincidence among the 16 channels
- Sent to Local Trigger Board every 12.5ns to form multiplicity trigger



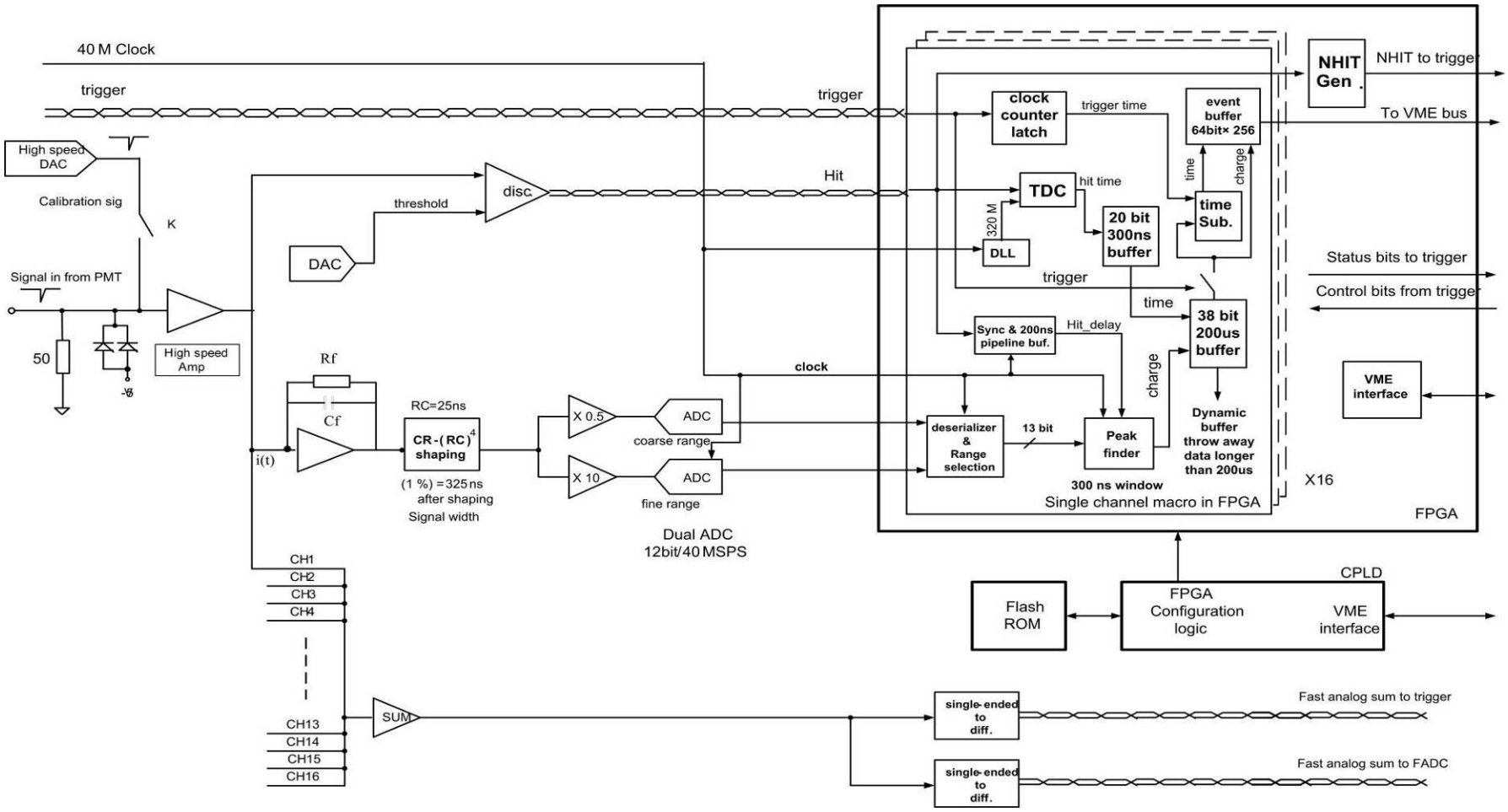
Esum

- PMT pulses in 16 channels are summed and converted to differential analog signal to LTB
- Diff. 2.5V @ 100 p.e.
- For total energy trigger





FEE block diagram



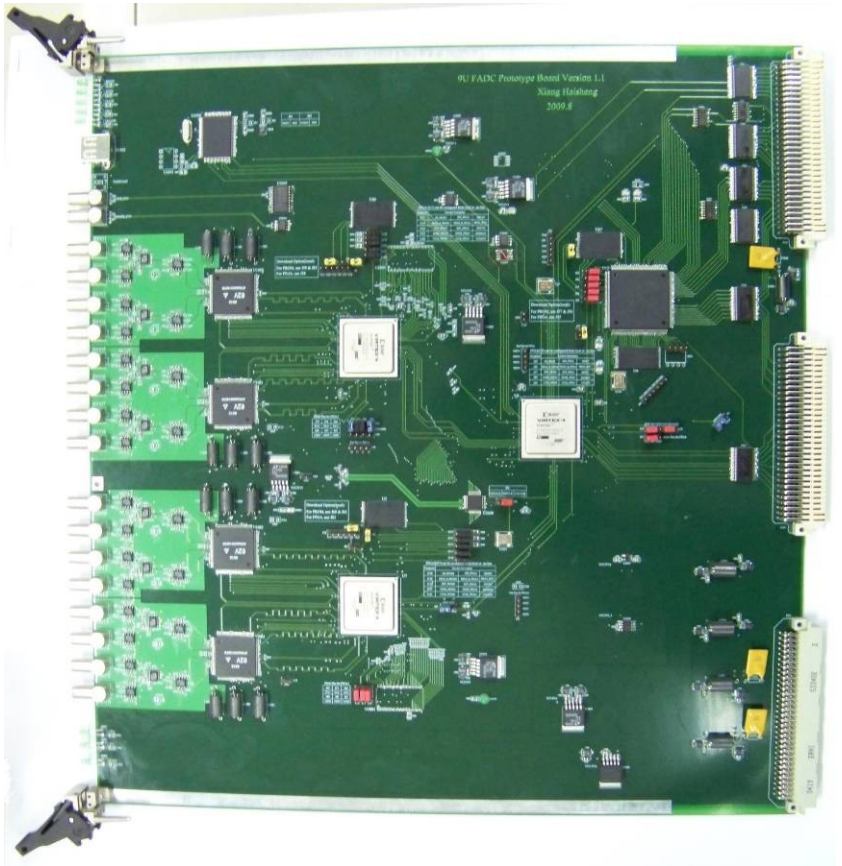
Flash ADC board

For cross check

Sampling the energy sum of every 32 PMTs at 1GHz

9U VME board

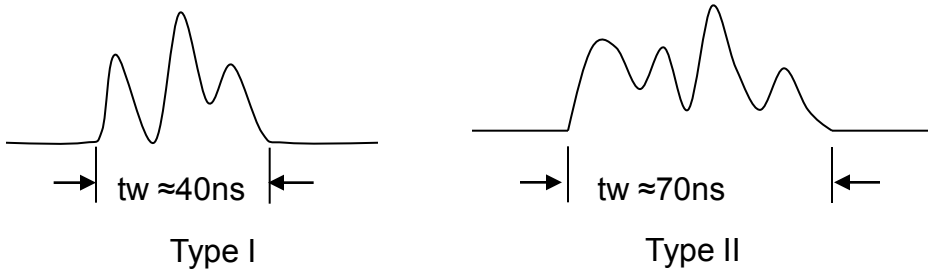
CBLT readout



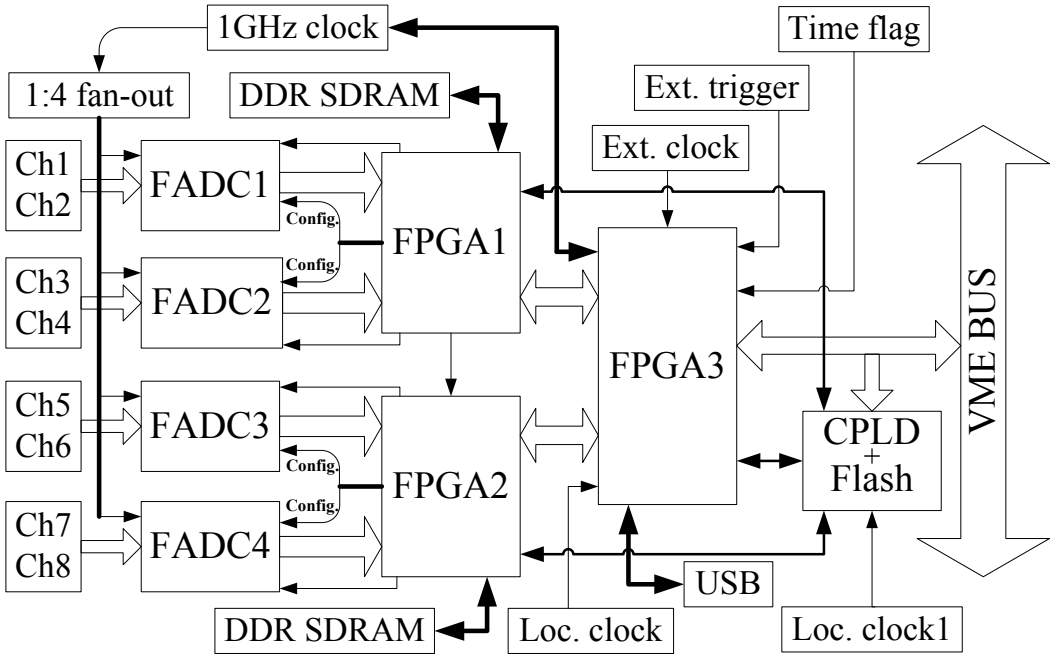
Flash ADC board

- Requirements
  - 8 channel, 1Gsps/ch
  - Local/external clock
  - Self/external trigger
  - Extended RAM
  - On-line configuration
  - VME/USB readout

- Analog input
  - Type I: 16-channel sum from FEE boards, width: ~40ns
  - Type II: total energy sum from trigger module, width: ~70ns
  - Signal rate: ~1KHz

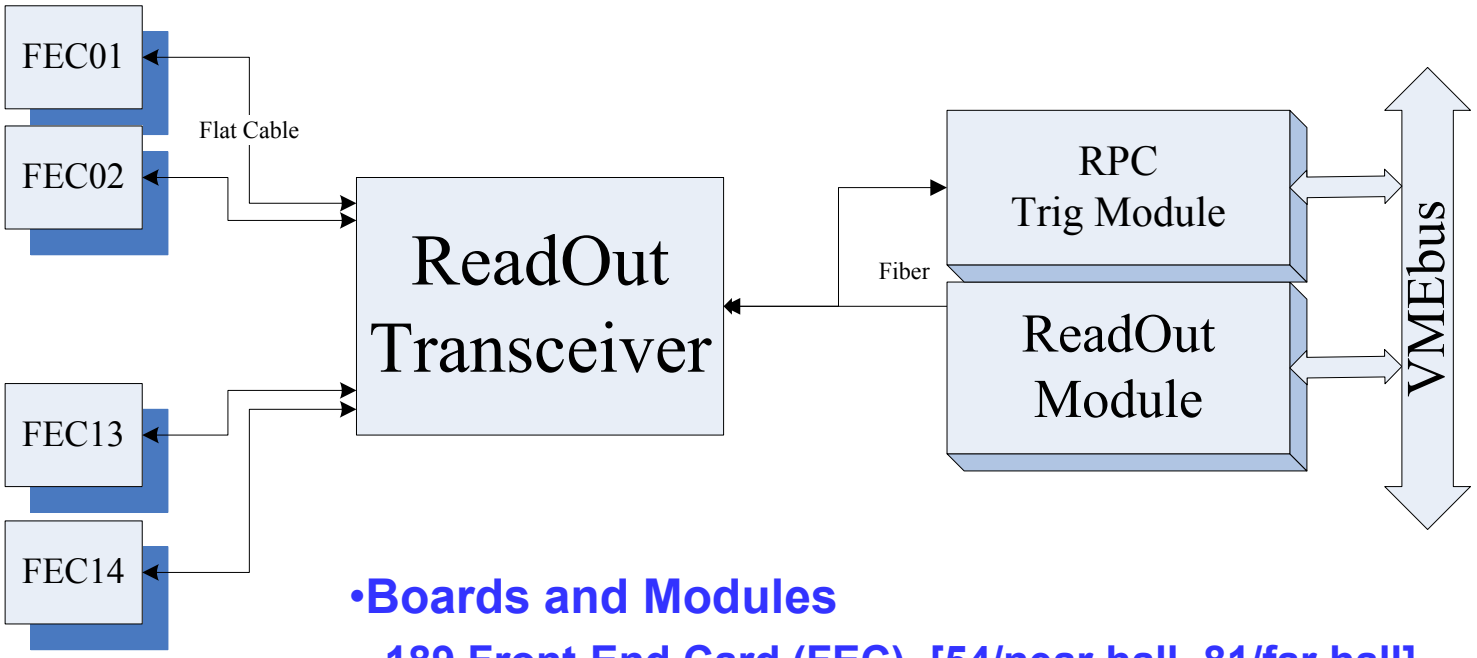


FADC board



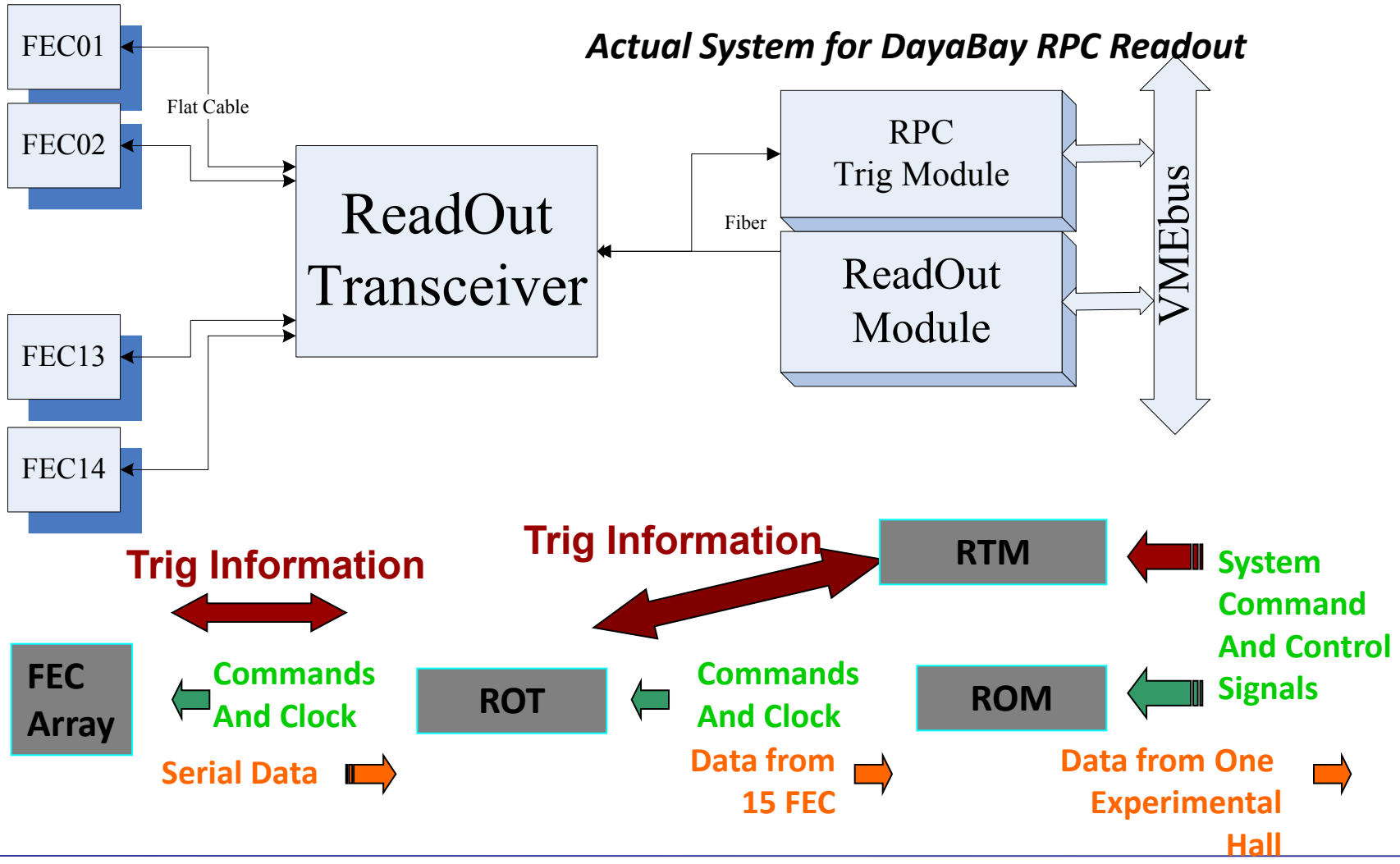
- FPGA1 and FPGA2 realizes pipelined capture, processing and primary packaging of sampling data
- FPGA3 realizes further packing and transmission of data
- Clock synthesizer is programmed by FPGA3 to generate 1GHz clock signal, clock fan-out chip distributes four identical copies of the 1GHz clock to four FADCs
- CPLD and Flash are used to realize on-line configuration of FPGAs

RPC electronic system



- **Boards and Modules**
  - **189 Front-End Card (FEC) [54/near hall, 81/far hall]**
  - **14 ReadOut Transceivers (ROT) [4/near hall, 6/far hall]**
    - **1 ROT connected from 12 to 15 FEC boards**
  - **3 ReadOutModule(ROM) [1 for each hall]**
  - **3 RpcTriggerModule(RTM) [1 for each hall]**

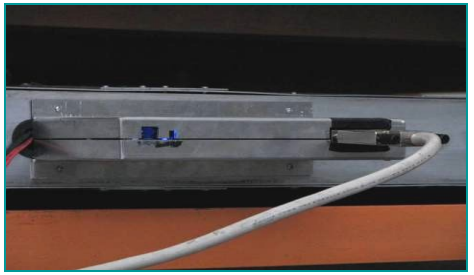
RPC electronic system



FEC (Front End Card) functions

- Front-end readout card for the RPC detector
  - 1 RPC module -> 1 FEC ~ 32 channels
- Marked each event with time stamp
- generate 2/4 or 3/4 trigger and sent to ROT/RTM;
- Transfer data to ROT when receiving trigger
- Up to 15 FECs send trigger information to RTM through ROT
- Up to 15 FECs collect and send data to ROM through ROT

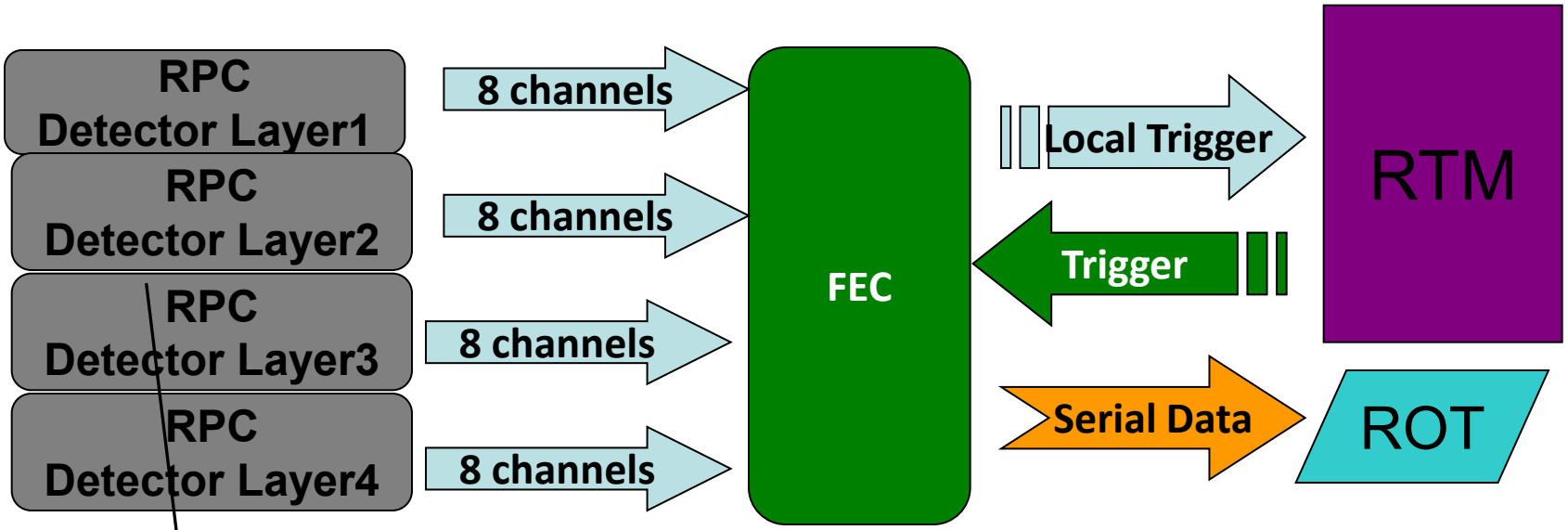
FEC



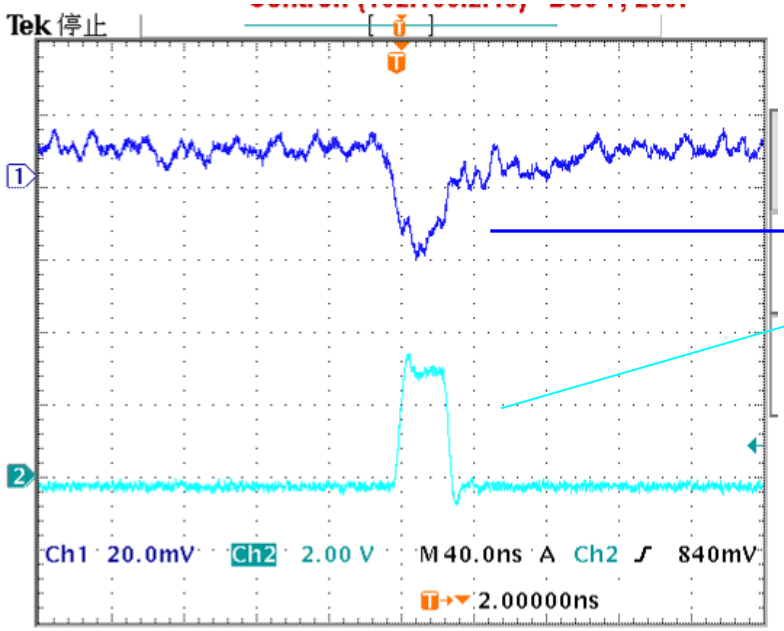
FEC mounted in a box

How does it work?

Core Functions



When 2 or more layers gives out hit signals, the FEC generates a 2/4 Local Trigger;
When 3 or more layers gives out hit signal,3/4 local trigger will be send out

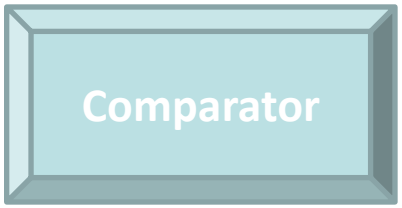


Blue signal: the output of a sample RPC,2007-12-08,IHEP

Marine signal: Output of comparator, version 1 FEC

MODE

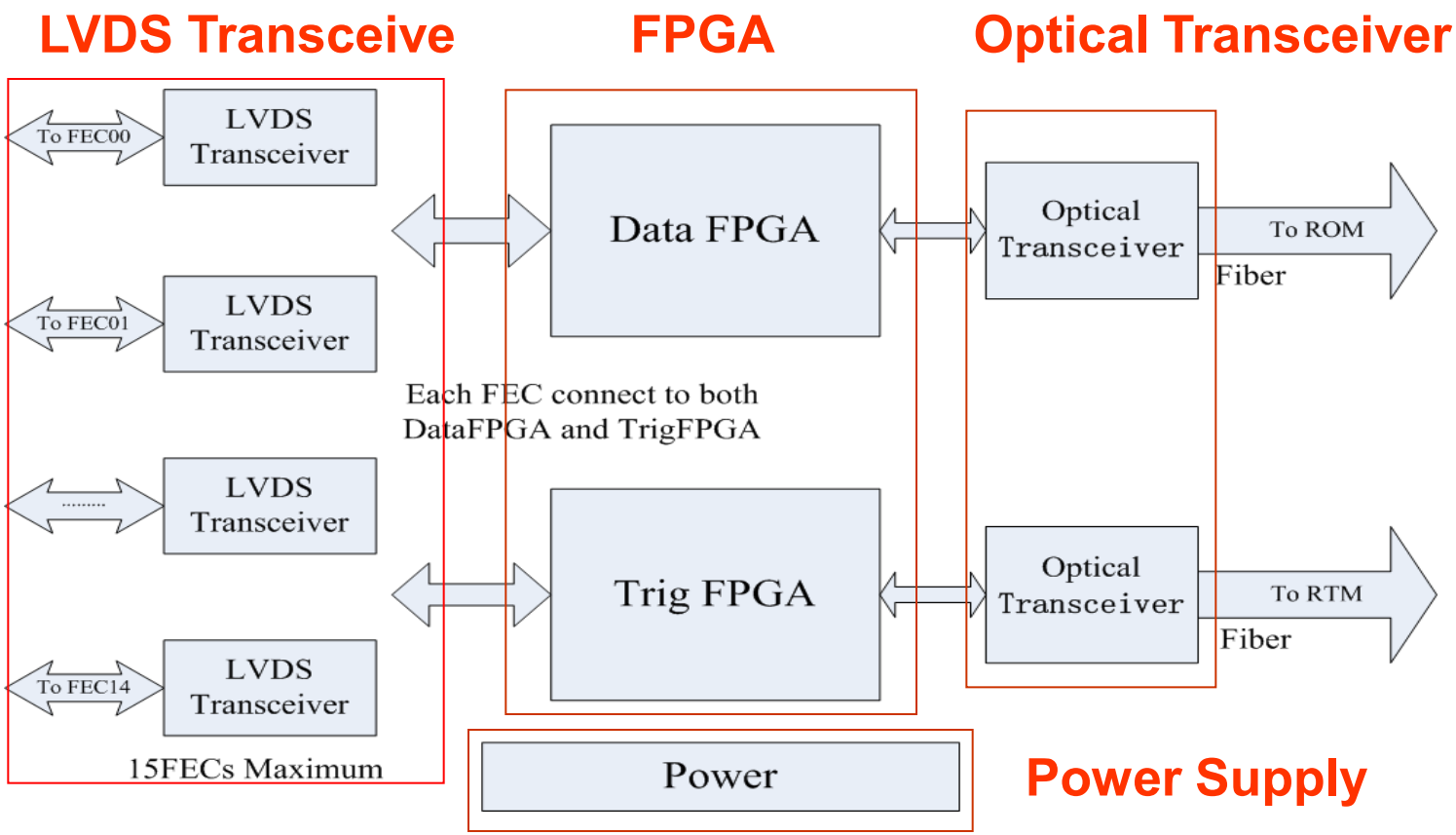
- RPC Hit Signal
- Threshold



A Logic “1” to FPGA

One Channel

Block Diagram of ROT



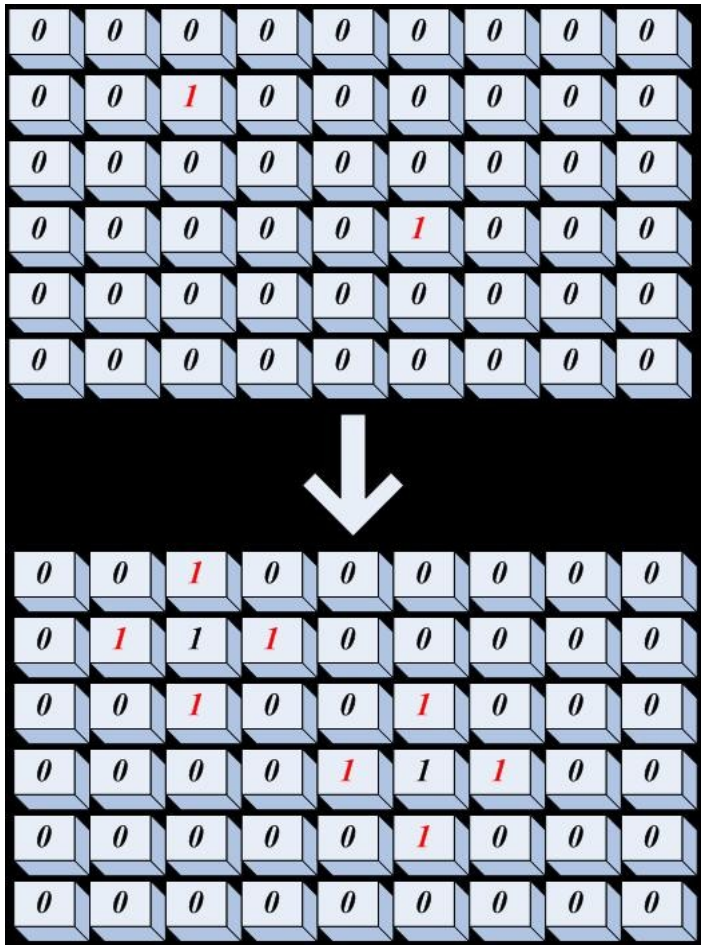
Module Function

- RTM (RPC Trigger Module)
  - 6 Optical link interfaces in 1 RTM
  - Accept system control signals including system clock and PPS
  - Accept cross trigger then distribute to all FECs
  - Accept Local Trigger from each FECs, generate a trigger matrix, process for neighbor FEC readout, then transfer processing result (*real* Trigger) to each FEC
  - Generate Trigger and send to each FEC when a ¾ Local Trigger received
  - Count seconds and add timestamp over second to dataflow
  - Optical links used to transfer signals between RTM and ROT, twisted pair cable used to accept system control signals (LVPECL)
  - Optical links used as virtual parallel bus, so RTM looks like to face to each FEC directly, 1 local trigger signal for each FEC

RTM local trigger processing

Input 2/4 Local Triggers' matrix for near hall (9×6FECs)

Output Triggers' matrix for each FEC



Module Function

- ROM (ReadOut Module)
  - 6 Optical link interfaces in 1 ROM, matched the readout requirement for 1 hall (1 ROM connected up to 6 ROTs)
  - Accept system control signals then distribute Fast Control Signal to all ROTs, including system clock and PPS
  - Distribute all commands to ROTs
  - Receive data from each ROT/FEC, buffer and organize dataflow
  - Count seconds and add timestamp over second to dataflow
  - Optical links used to transfer signals between ROM and ROT, twisted pair cable used to accept system control signals (LVPECL)
  - Optical links used as virtual parallel bus, so ROM looks like to face to each FEC directly

Dataflow

- RPC dataflow is organized by RPC Module. Each data package contains one module's hit map, with time information and module ID , trigger information maybe included also.
- Usually 1 local trigger 2/4 will result 5 neighbor RPC data package with same time information, except that when the module gives out local trigger is on edge or corner.
- If a ¾ local trigger arose or cross trigger arrived, all FECs will be readout, then the dataflow may contains 54 or 81 data package with same time information.

Status of Daya Bay Electronics

Milestones of Daya Bay electronics

- All boards are finalized at the end of 2010
- Installation for Daya Bay Near site done March 2011
- Start online integration test since March 2011
- Ready for near site data taking July 1st,2011

PMT electronics progress

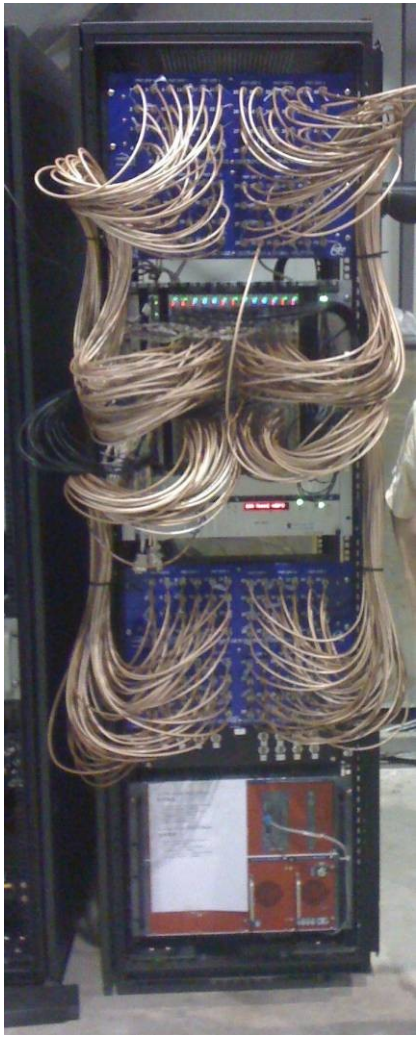
FEE

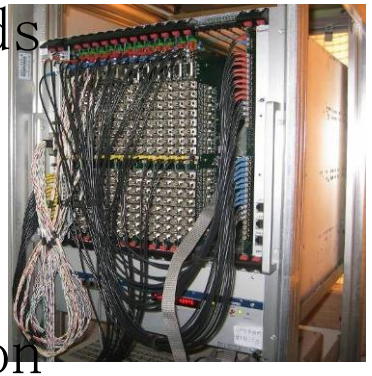
FADC

Fanout board

Local trigger board (LTB)

FEE system for AD dry run





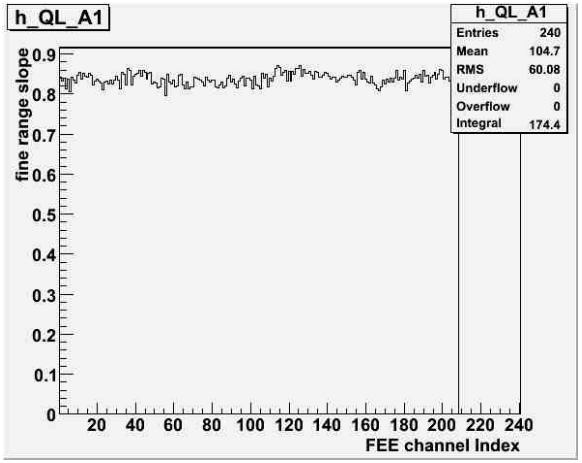
- Readout system w/ 13 FEE boards installed in SAB on June 7th.
  - 12 FEEs for AD + 1 LTB
  - 1 FEE for 2” Calibration PMTs
- Commissioning w/ LTB and DAQ
- Updated FEE firmware to version *12JUNE2010*
  - Fixed nPMT transmission problem
- Updated FEE firmware to version *1JULY2010*
  - Fixed CBLT interrupt data loss bug
- Upgraded FEE firmware update program
  - Parallel updating firmware for all FEEs
  - shorter time: 5 mins instead of 40 mins

System installation and test

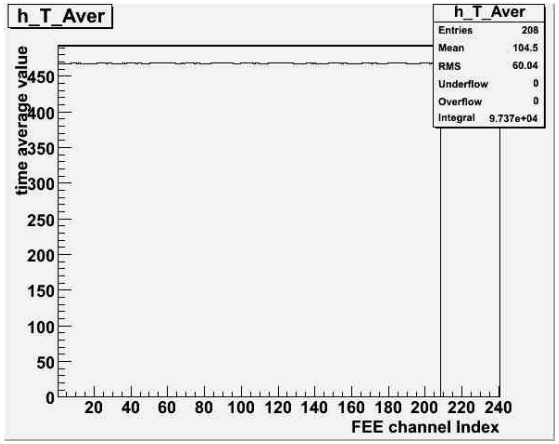
Testing @ IHEP

Installation and test in Daya bay Near site

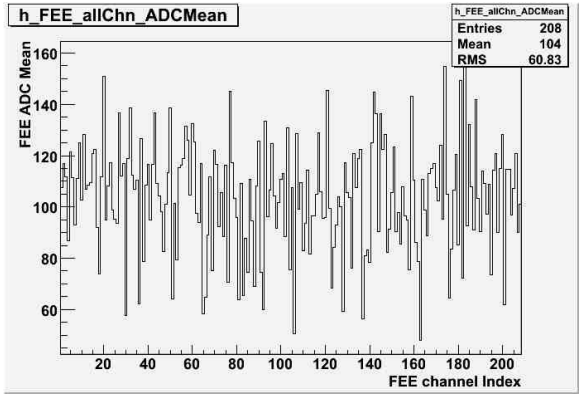
Performance of PMT electronics



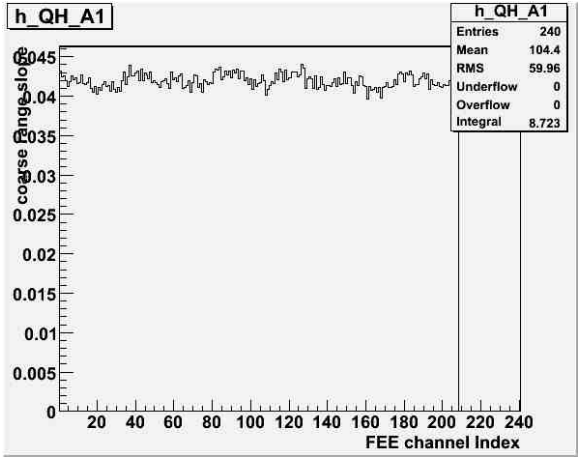
ADC fine range slope



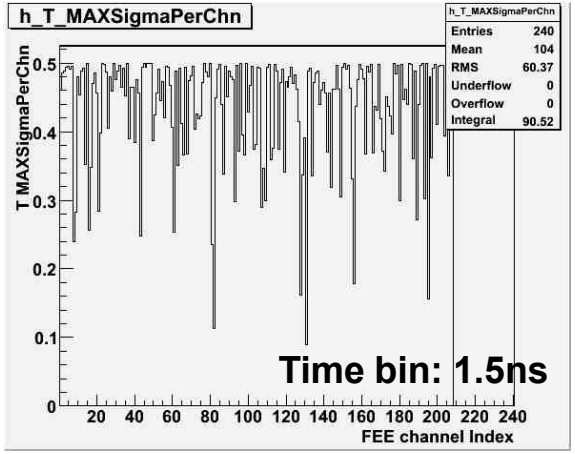
Time average



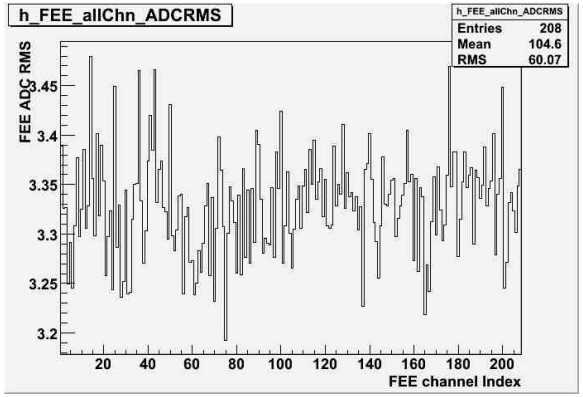
ADC pedestal



ADC coarse range slope



Time RMS

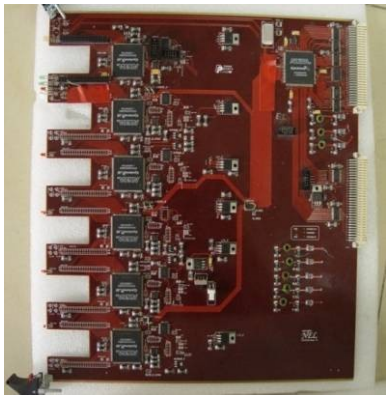


ADC RMS

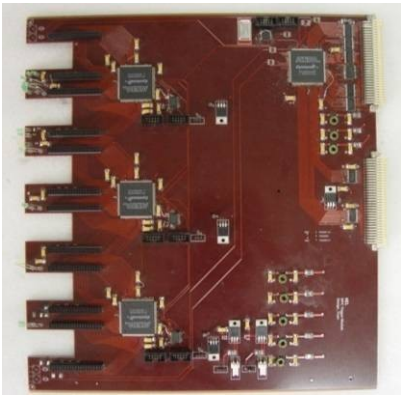
Status of RPC electronics

FEC

ROT

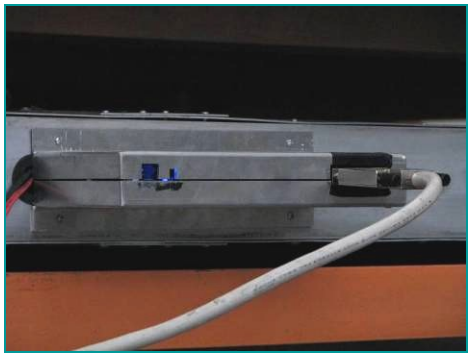


ROM



RTM

小系统测试

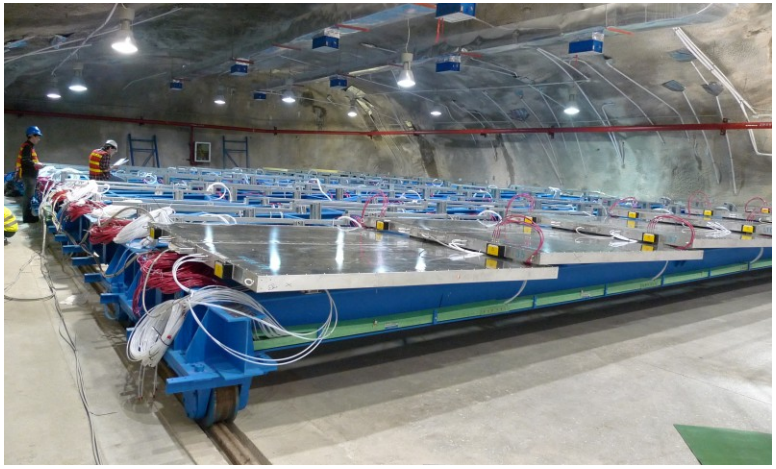


FEC电子学盒

ROM/USB机箱

RPC electronics integration test in IHEP

Installation of RPC electronics



Installation of FEC

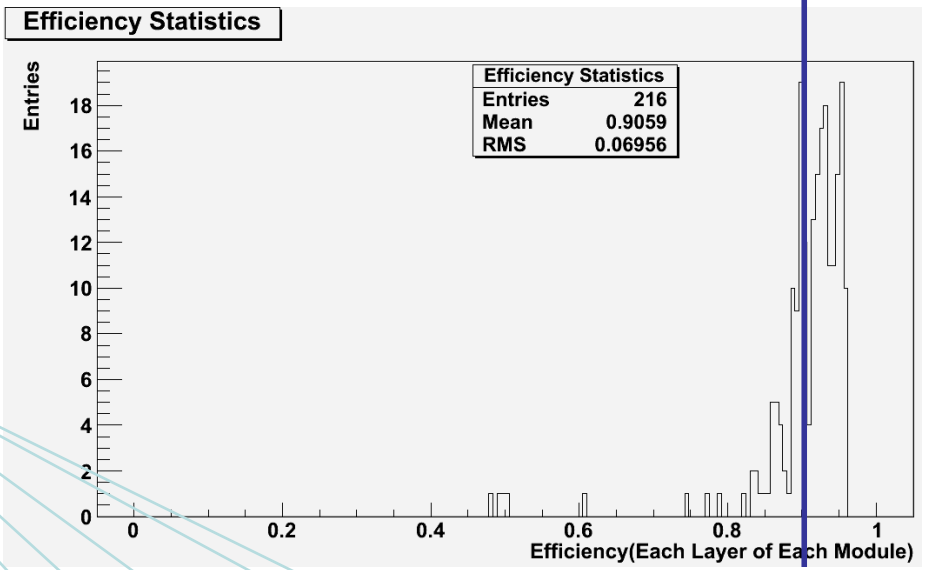
Installation of ROT

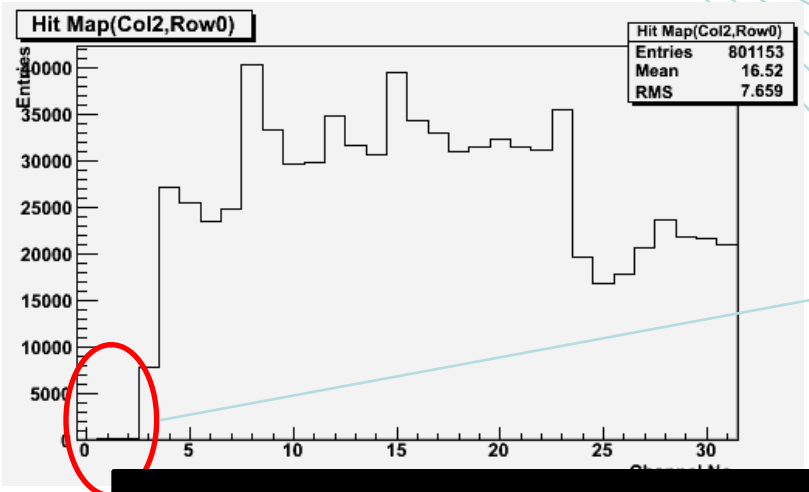
Installation of ROM and RTM

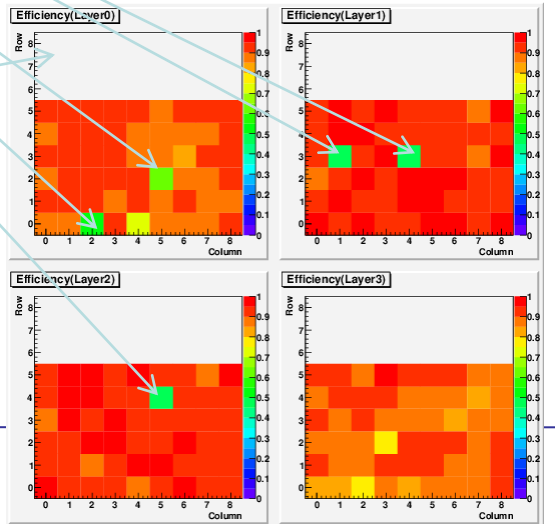
Test Results

90%

- **Efficiencies**
  - ✓ Majority: >90%
  - ✓ Top and bottom layers: sys. lower.
  - ✓ A few(5): ~50% (green pads)







For x-strip layers, we can know which RPC in that layer is dead, but not for y-strip layers

Summary

- PMT electronic system is designed for the antineutrino det. and water Cherenkov det. (identical hardware, different FPGA firmware)
  - Large charge dynamic range : up to 16 bits
  - Low dead time
  - Parallel processing in FPGA
- RPC electronic system
  - Low threshold
  - High efficiency
- Electronic system ready for Daya Bay near site data taking.

Thank you.