The Front-end Electronics for the Daya Bay Neutrino Experiment for Daya Bay Collaboration

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Outline

• Introduction on Daya Bay experiment
• PMT electronic system
• RPC electronic system
• Current status of the electronic system
• Summary
The Experiment

- Near-far relative meas. to cancel correlated syst. errors
  - 2 near cites + 1 far cite
- Multiple neutrino detector modules at each site to cross check and reduce un-correlated syst. errors
  - Gd-loaded liquid scintillator
  - Stainless steel tank + 2 nested acrylic vessel + reflectors
- Multiple muon-veto to reduce bkgd-related syst. errors
  - 4-layer RPC + 2-layer water Cerenkov detector
Detectors and electronics each site

Antineutrino Detector
(192 8’PMTs)
X2 near site
X4 far site
2 or 4 PMT readout systems

Inner and outer Water Cherenkov Detectors
(289 or 392 8’PMTs)
289 near site
392 far site
2 PMT readout systems

RPC Detector
(1728 readout strips)
1 RPC readout system
Electronic system

Each detector has standalone readout electronic system. Each system is a single 9U VME crate and it can do data taking individually.

<table>
<thead>
<tr>
<th>Readout system</th>
<th>Antineutrino Detector</th>
<th>Water Cherenkov Detector</th>
<th>RPC detector</th>
<th>Site subtotal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Daya Bay near site</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>Ling Ao near site</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>Far site</td>
<td>4</td>
<td>2</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>Detector subtotal</td>
<td>8</td>
<td>6</td>
<td>3</td>
<td>17</td>
</tr>
</tbody>
</table>
Electronic system for DB near site

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**DB NEAR HALL RACK LAYOUT**

- **AD Rack #1**: 192 CHANNELS PLUS Calibration
- **AD Rack #2**: 192 CHANNELS plus CALIBRATION
- **Outer Muon**: 173 CHANNELS
- **Inner Muon**: 116 CHANNELS

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- **CALIBRATION**
- **CAEN HV MAINFRAME with PS and Fan Unit**: AD 1&2
- **CAEN HV MAINFRAME with PS and Fan Unit**: RPC
- **CAEN HV MAINFRAME with PS and Fan Unit**: MUON

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The PMT Electronic System is designed to process the PMT signals from either Antineutrino Detector (AD) or Water Cherenkov Detector (WCD).

Functions:

- Determine the *charge* (energy) of each PMT signal
- Provide precision *timing* information (from PMT hit to trigger) that can be used to reconstruct the location of the antineutrino interaction
- Generate multiplicity (*nPMT*) trigger
- Generate total energy (*ESUM*) trigger
- Energy Sum waveform of each 32 PMTs is digitized using 1GHz flash ADC for cross check.
Each PMT electronic system sits in single 9U VME crate
# FEE Specifications

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Charge dynamic range</td>
<td>0-1800 pC</td>
</tr>
<tr>
<td><strong>Fine Range</strong></td>
<td>0-160 pC (100pe@PMTgain 2E7)</td>
</tr>
<tr>
<td><strong>Coarse range</strong></td>
<td>160-1800 pC</td>
</tr>
<tr>
<td>Shaping width</td>
<td>&lt;325ns down to 1%</td>
</tr>
<tr>
<td>Peak error</td>
<td>&lt; 4% @ 40MSPS</td>
</tr>
<tr>
<td>ADC bit resolution</td>
<td>&lt; 10% @ 1.6 pC</td>
</tr>
<tr>
<td>ADC Bits</td>
<td>12 bits for fine range</td>
</tr>
<tr>
<td></td>
<td>12 bits for coarse range</td>
</tr>
<tr>
<td>ADC Sampling rate</td>
<td>40 MSPS</td>
</tr>
<tr>
<td>Disc. threshold</td>
<td>0.25 p.e. (programmable each chnl.)</td>
</tr>
<tr>
<td>Time range</td>
<td>0-1.3 us</td>
</tr>
<tr>
<td>Time bin</td>
<td>1.5625ns</td>
</tr>
<tr>
<td>Timing Precision (RMS)</td>
<td>&lt;1 ns</td>
</tr>
<tr>
<td>Multi-hit separation</td>
<td>Yes</td>
</tr>
<tr>
<td>Multi-hit resolution</td>
<td>50 ns</td>
</tr>
</tbody>
</table>
### FEE Specifications (cont.)

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real time nPMT to LTB</td>
<td>5-bit LVDS @ 80M</td>
</tr>
<tr>
<td>ESUM to LTB</td>
<td>2-wire LEMO (<a href="mailto:2.5V@100p.e">2.5V@100p.e</a>.)</td>
</tr>
<tr>
<td>ESUM to FADC Bd.</td>
<td>2-wire LEMO (<a href="mailto:2.5V@100p.e">2.5V@100p.e</a>.)</td>
</tr>
<tr>
<td>Clock input</td>
<td>receiving 40M clock from fan-out bd. 2-wire LEMO (lvPECL)</td>
</tr>
<tr>
<td>Trigger input</td>
<td>receiving trigger from LTB (lvPECL)</td>
</tr>
<tr>
<td>Signal input connector</td>
<td>BNC</td>
</tr>
<tr>
<td>Signal input impedance</td>
<td>50 Ohm</td>
</tr>
<tr>
<td>Channels/board</td>
<td>16</td>
</tr>
<tr>
<td>Data Readout</td>
<td>CBLT (Chained Block Transf.)</td>
</tr>
<tr>
<td>VME standard</td>
<td>9U VME 64Xp (340mm)</td>
</tr>
<tr>
<td>Power backplane</td>
<td>Wiener defined power pins (P3)</td>
</tr>
</tbody>
</table>
PMT signal characteristics
from TDR 4.5 PMT System

# of p.e. versus PMT number

MC of muons passing through the AD
dynamic range : 2000 p.e.

gain: $2 \times 10^7$
linearity: 5%@(0–625p.e.)

<table>
<thead>
<tr>
<th>Gain</th>
<th>$\geq 10^7$ for all PMTs with appropriate tapered resistive base.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>— PMTs must achieve a gain of $3 \times 10^7$ at $V_0 \leq 2$ kV</td>
</tr>
</tbody>
</table>

| Pulse Linearity | — PMT anode pulse linearity must be better than 5% |
|-----------------| over the dynamic range of 0–1 nC at a gain of $10^7$ |
Linearity of PMT output

Hamamatsu 4324 @ Gain of $10^7$

Hamamatsu R5912 PMT response to large light signals
Charge Measure Solution

Peak Value ~ PMT output charge

- Amplitude of shaper output is in scale of input charge
Time measure scheme

- Measuring the time from PMT over threshold/hit to trigger
- Rising edge timing method
- Multi-hit TDC
  - Two hits separation $>= 50$ ns
  - Time bin: 1.5625 ns
nPMT Generation

- PMT pulses are amplified and sent to a fast discriminator
- The DisOUT is then synchronized with the 80 Mhz clock by extent to 100 ns
- nPMT == coincidence among the 16 channels
- Sent to Local Trigger Board every 12.5ns to form multiplicity trigger
Esum

- PMT pulses in 16 channels are summed and converted to differential analog signal to LTB
- Diff. 2.5V @ 100 p.e.
- For total energy trigger
FEE block diagram
Flash ADC board

For cross check
Sampling the energy sum of every 32 PMTs at 1GHz
9U VME board
CBLT readout
Flash ADC board

- Requirements
  - 8 channel, 1Gsp/ch
  - Local/external clock
  - Self/external trigger
  - Extended RAM
  - On-line configuration
  - VME/USB readout

- Analog input
  - Type I: 16-channel sum from FEE boards, width: ~40ns
  - Type II: total energy sum from trigger module, width: ~70ns
  - Signal rate: ~1KHz
FADC board

- FPGA1 and FPGA2 realizes pipelined capture, processing and primary packaging of sampling data
- FPGA3 realizes further packing and transmission of data
- Clock synthesizer is programmed by FPGA3 to generate 1GHz clock signal, clock fan-out chip distributes four identical copies of the 1GHz clock to four FADCs
- CPLD and Flash are used to realize on-line configuration of FPGAs
RPC electronic system

- **Boards and Modules**
  - 189 Front-End Card (FEC) [54/near hall, 81/far hall]
  - 14 ReadOut Transceivers (ROT) [4/near hall, 6/far hall]
    - 1 ROT connected from 12 to 15 FEC boards
  - 3 ReadOutModule (ROM) [1 for each hall]
  - 3 RpcTriggerModule (RTM) [1 for each hall]
RPC electronic system

Actual System for DayaBay RPC Readout

FEC01
FEC02
FEC13
FEC14

Flat Cable

ReadOut Transceiver

RPC Trig Module

ReadOut Module

Fiber

VMEbus

RPC electronic system

FEC Array

Trig Information

Commands And Clock

Serial Data

ROT

Commands And Clock

ROM

RTM

Trig Information

Data from 15 FEC

System Command And Control Signals

Data from One Experimental Hall

Menu

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FEC (Front End Card) functions

- Front-end readout card for the RPC detector
  - 1 RPC module -> 1 FEC ~ 32 channels
- Marked each event with time stamp
- Generate 2/4 or 3/4 trigger and sent to ROT/RTM;
- Transfer data to ROT when receiving trigger
- Up to 15 FECs send trigger information to RTM through ROT
- Up to 15 FECs collect and send data to ROM through ROT

FEC

FEC mounted in a box
How does it work?

**Core Functions**

When 2 or more layers gives out hit signals, the FEC generates a 2/4 Local Trigger; When 3 or more layers gives out hit signal, 3/4 local trigger will be send out.
Blue signal: the output of a sample RPC, 2007-12-08, IHEP

Marine signal: Output of comparator, version 1 FEC

- **RPC Hit Signal**
- **Threshold**

One Channel

Comparator

A Logic “1” to FPGA

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Block Diagram of ROT

LVDS Transceiver

FPGA

Optical Transceiver

Power Supply

LVDS Transceiver
LVDS Transceiver
LVDS Transceiver
LVDS Transceiver
LVDS Transceiver
LVDS Transceiver
LVDS Transceiver
LVDS Transceiver
LVDS Transceiver

Data FPGA

Trig FPGA

Optical Transceiver

Power

Each FEC connect to both Data FPGA and Trig FPGA

To FEC00
To FEC01
To FEC14

15 FECs Maximum

To ROM Fiber
To RTM Fiber

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Module Function

- RTM (RPC Trigger Module)
  - 6 Optical link interfaces in 1 RTM
  - Accept system control signals including system clock and PPS
  - Accept cross trigger then distribute to all FECs
  - Accept Local Trigger from each FECs, generate a trigger matrix, process for neighbor FEC readout, then transfer processing result (real Trigger) to each FEC
  - Generate Trigger and send to each FEC when a ¾ Local Trigger received
  - Count seconds and add timestamp over second to dataflow
  - Optical links used to transfer signals between RTM and ROT, twisted pair cable used to accept system control signals (LVPECL)
  - Optical links used as virtual parallel bus, so RTM looks like to face to each FEC directly, 1 local trigger signal for each FEC
RTM local trigger processing

Input 2/4 Local Triggers’ matrix for near hall
(9 × 6FECs)

Output Triggers’ matrix for each FEC
Module Function

- ROM (ReadOut Module)
  - 6 Optical link interfaces in 1 ROM, matched the readout requirement for 1 hall (1 ROM connected up to 6 ROTs)
  - Accept system control signals then distribute Fast Control Signal to all ROTs, including system clock and PPS
  - Distribute all commands to ROTs
  - Receive data from each ROT/FEC, buffer and organize dataflow
  - Count seconds and add timestamp over second to dataflow
  - Optical links used to transfer signals between ROM and ROT, twisted pair cable used to accept system control signals (LVPECL)
  - Optical links used as virtual parallel bus, so ROM looks like to face to each FEC directly
Dataflow

• RPC dataflow is organized by RPC Module. Each data package contains one module’s hit map, with time information and module ID, trigger information maybe included also.

• Usually 1 local trigger 2/4 will result 5 neighbor RPC data package with same time information, except that when the module gives out local trigger is on edge or corner.

• If a ¾ local trigger arose or cross trigger arrived, all FECs will be readout, then the dataflow may contains 54 or 81 data package with same time information.
Status of Daya Bay Electronics
Milestones of Daya Bay electronics

- All boards are finalized at the end of 2010
- Installation for Daya Bay Near site done March 2011
- Start online integration test since March 2011
- Ready for near site data taking July 1st, 2011
PMT electronics progress

- FEE
- FADC
- Fanout board
- Local trigger board (LTB)
FEE system for AD dry run

- Readout system w/ 13 FEE boards installed in SAB on June 7th.
  - 12 FEEs for AD + 1 LTB
  - 1 FEE for 2” Calibration PMTs
- Commissioning w/ LTB and DAQ
- Updated FEE firmware to version 12JUNE2010
  - Fixed nPMT transmission problem
- Updated FEE firmware to version 1JULY2010
  - Fixed CBLT interrupt data loss bug
- Upgraded FEE firmware update program
  - Parallel updating firmware for all FEEs
  - shorter time: 5 mins instead of 40 mins
System installation and test

Testing @ IHEP

Installation and test in Daya bay
Near site
Performance of PMT electronics

ADC fine range slope

Time average

ADC pedestal

ADC coarse range slope

Time RMS

ADC RMS
Status of RPC electronics

FEC               ROT                    ROM                  RTM

FEC 电子学盒     ROM/USB 机箱

小系统测试

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RPC electronics integration test in IHEP
Installation of RPC electronics

Installation of FEC

Installation of ROM and RTM

Installation of ROT
Test Results

- **Efficiencies**
  - Majority: >90%
  - Top and bottom layers: sys. lower.
  - A few (5): ~50% (green pads)

For x-strip layers, we can know which RPC in that layer is dead, but not for y-strip layers.
Summary

- PMT electronic system is designed for the antineutrino det. and water Cherenkov det. (identical hardware, different FPGA firmware)
  - Large charge dynamic range: up to 16 bits
  - Low dead time
  - Parallel processing in FPGA
- RPC electronic system
  - Low threshold
  - High efficiency
- Electronic system ready for Daya Bay near site data taking.

Thank you.