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HIPPO, a Flexible Front-End Signal Processor for High-Speed Image Sensor Readout

Carl Grace, Dario Gnani, Jean-Pierre Walder, and Bob Zheng

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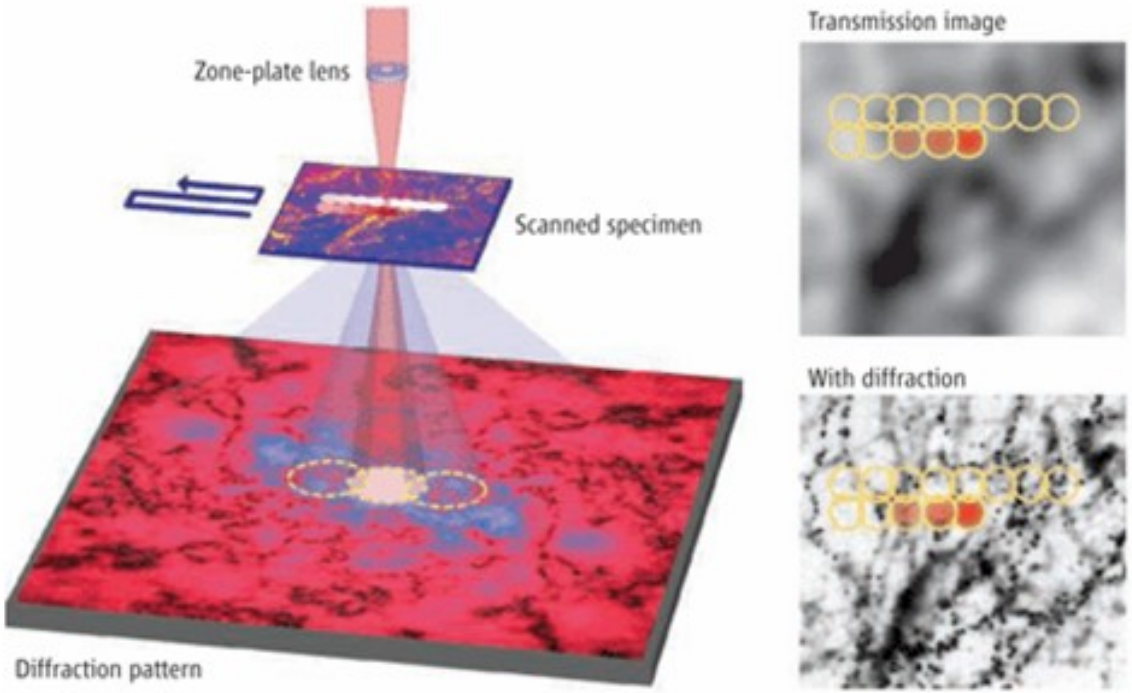
Outline of Presentation

- Motivation for HIPPO
- LBNL thick, fully column-parallel CCDs
- HIPPO Design
- Layout and Results

High-Speed Image Pre-Processor with Oversampling (HIPPO)

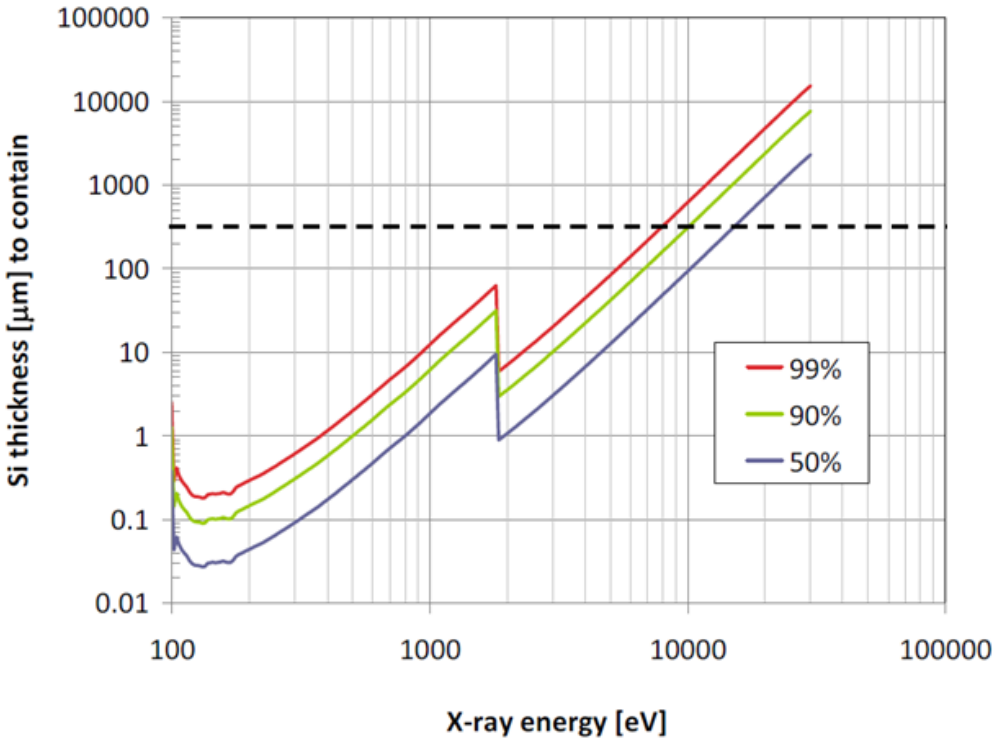
Emerging soft x-ray imaging applications for dynamic processes require greatly increased readout speeds

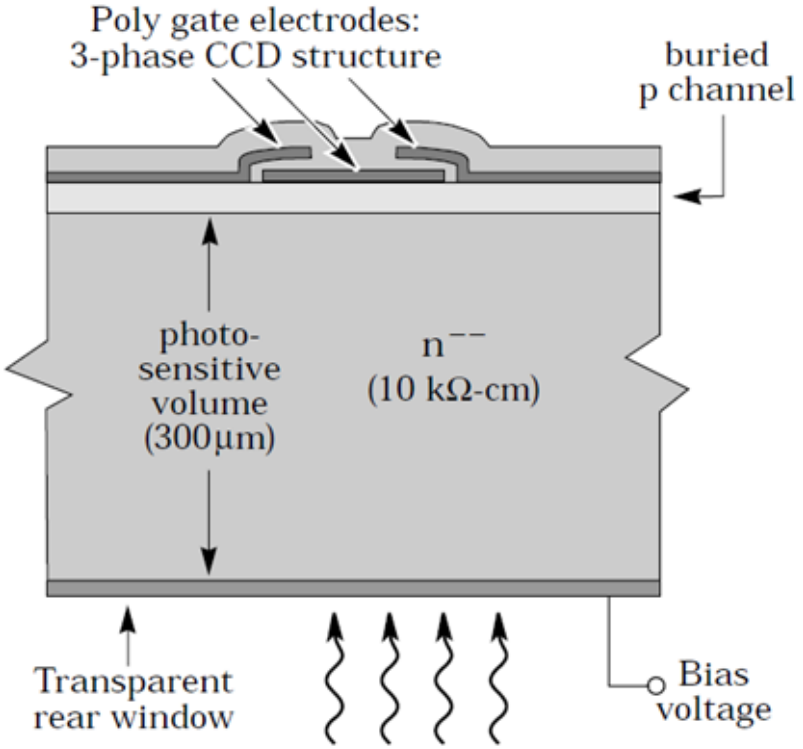


Ptchyographic x-ray microscopy

Figure: H.N. Chapman, **Science** 321 352 (2008)

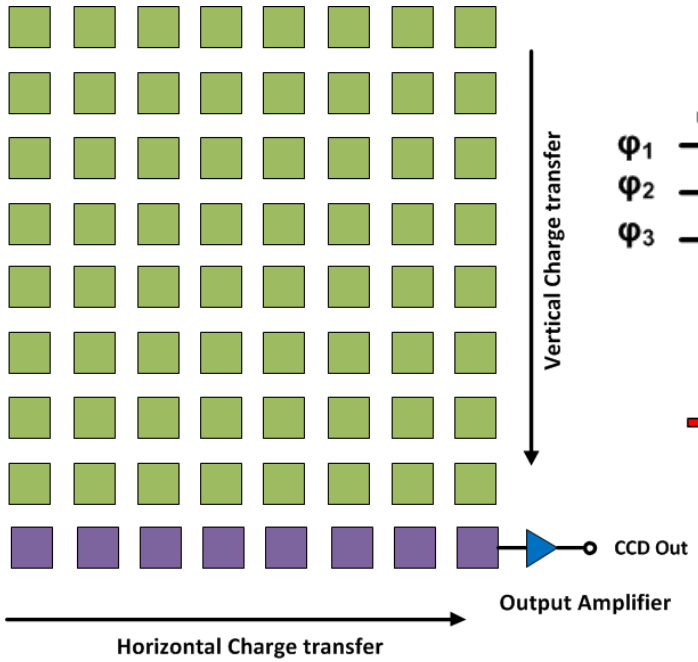
LBNL thick, high ρ, fully depleted CCDs

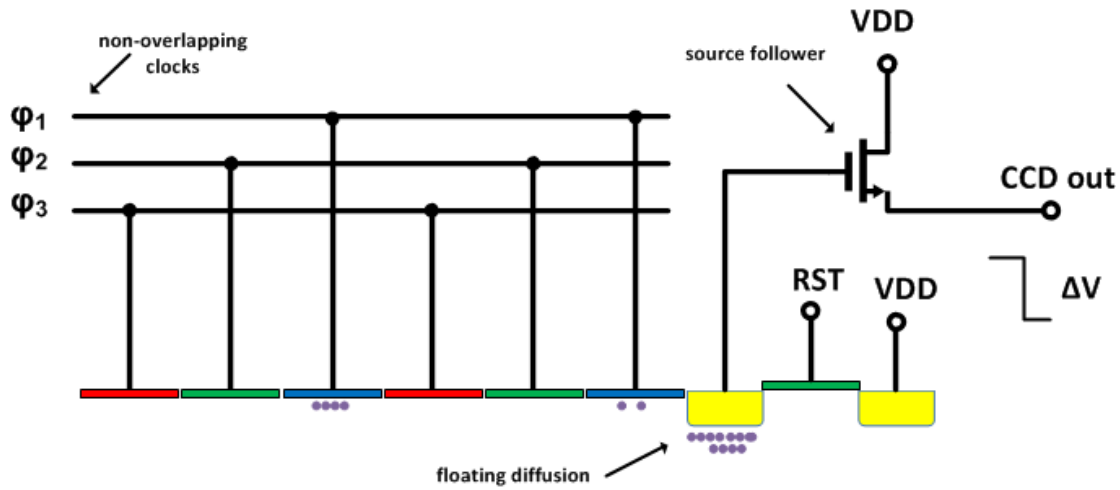




- LBNL-developed thick CCDs provide excellent soft x-ray response
- Lack of field-free region provides excellent point spread function

Conventional Charge-Coupled Devices

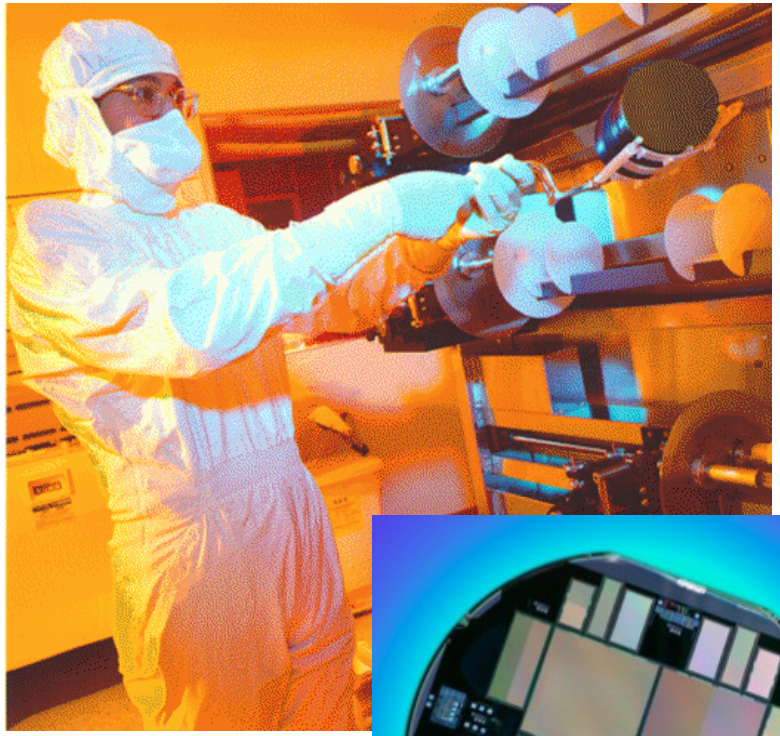


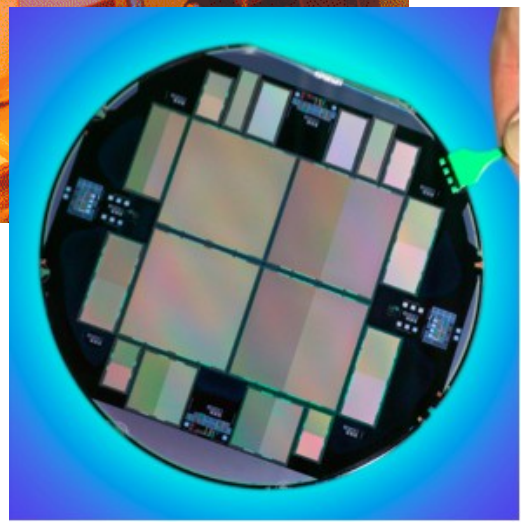


Horizontal output shift register

- Noiseless, nearly lossless charge transfer (high SNR)
- Improved DR*Size*Speed product compared to CMOS sensors
- Speed limited by serial output
- Solution → Parallelize column readout (column readout up to 10 MHz)

CCDs @ LBNL Micro Systems Lab (MSL)





4 e^- @ 100 kpix/s

LBNL 2k x 4k CCD:
Blue: H- at 656 nm Green: SIII at 955 nm Red: 1.02 nm

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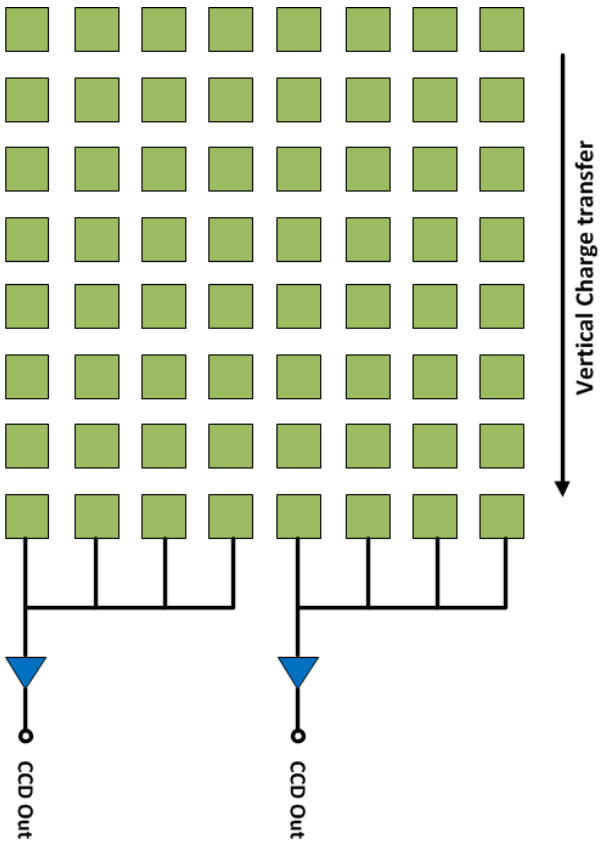
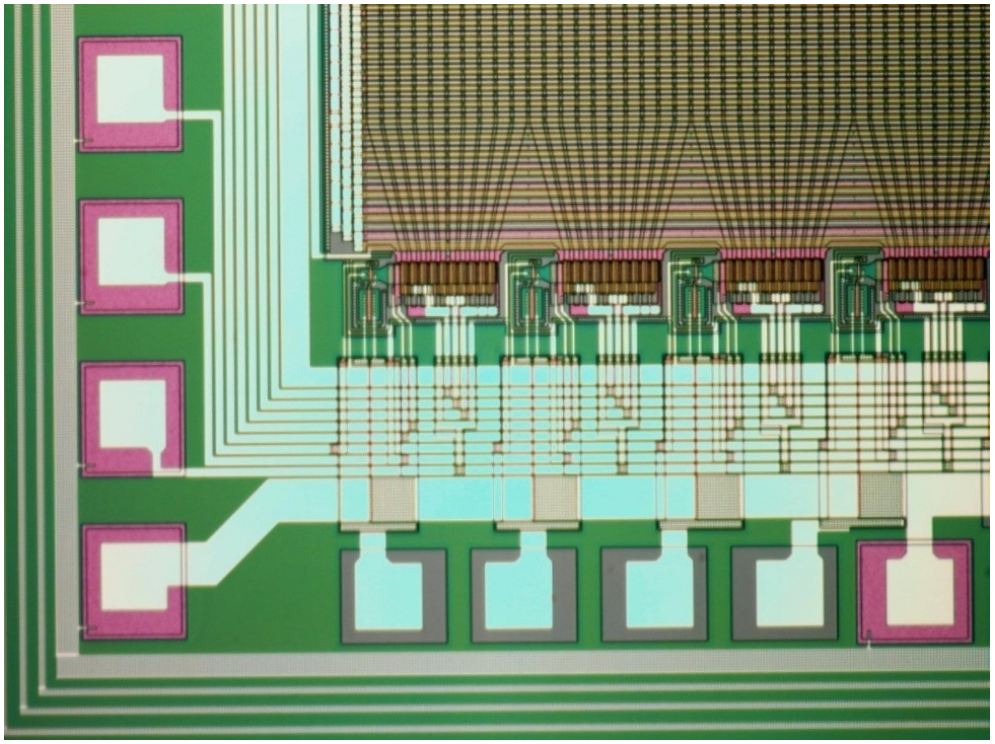
“Almost” Column-Parallel LBNL CCD



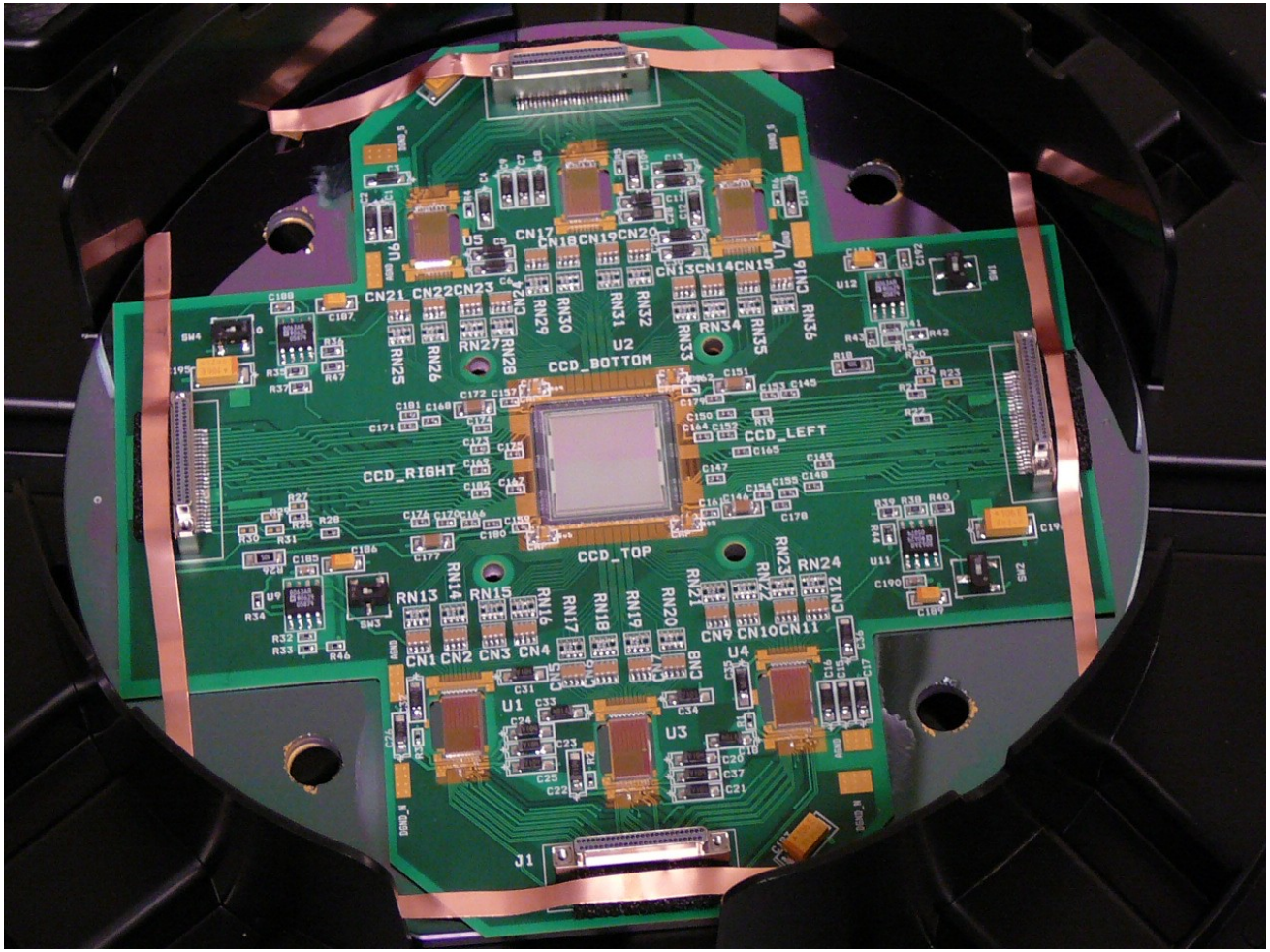


Almost Column-Parallel LBNL CCD

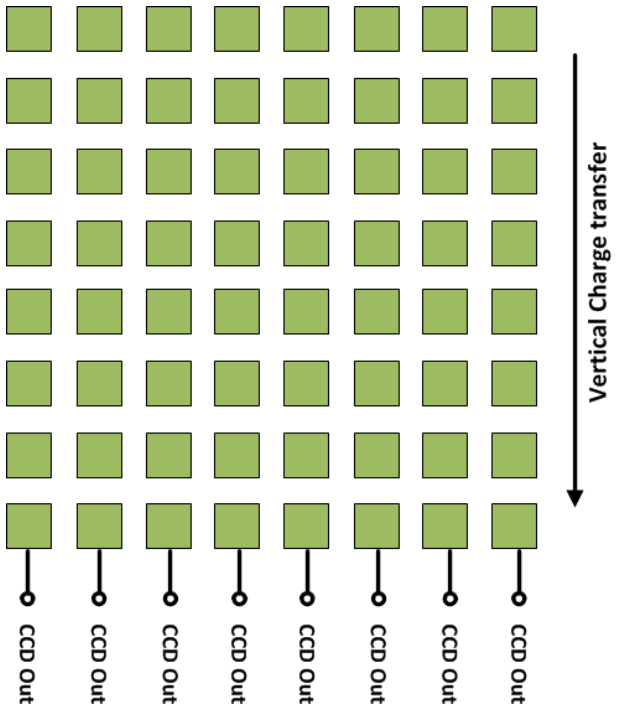
- Each output stage shared by ten columns
- Not practical to make more parallel with on-CCD charge conversion
- Solution → Fully column-parallel CCD

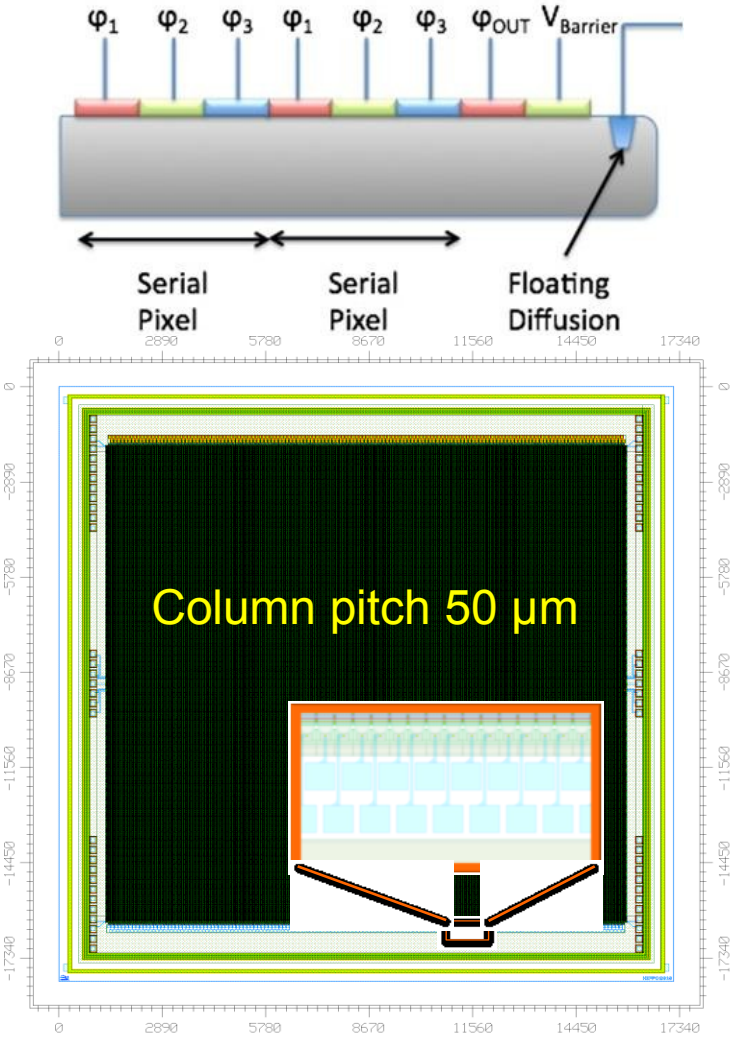
Fast CCD X-ray camera board

10 e^- @ 1 Mpix/s



Fully Column-Parallel LBNL CCD





Megapixel square sensor has ~1000 columns → need custom IC readout

No room for output amplifier → need charge-sensitive readout

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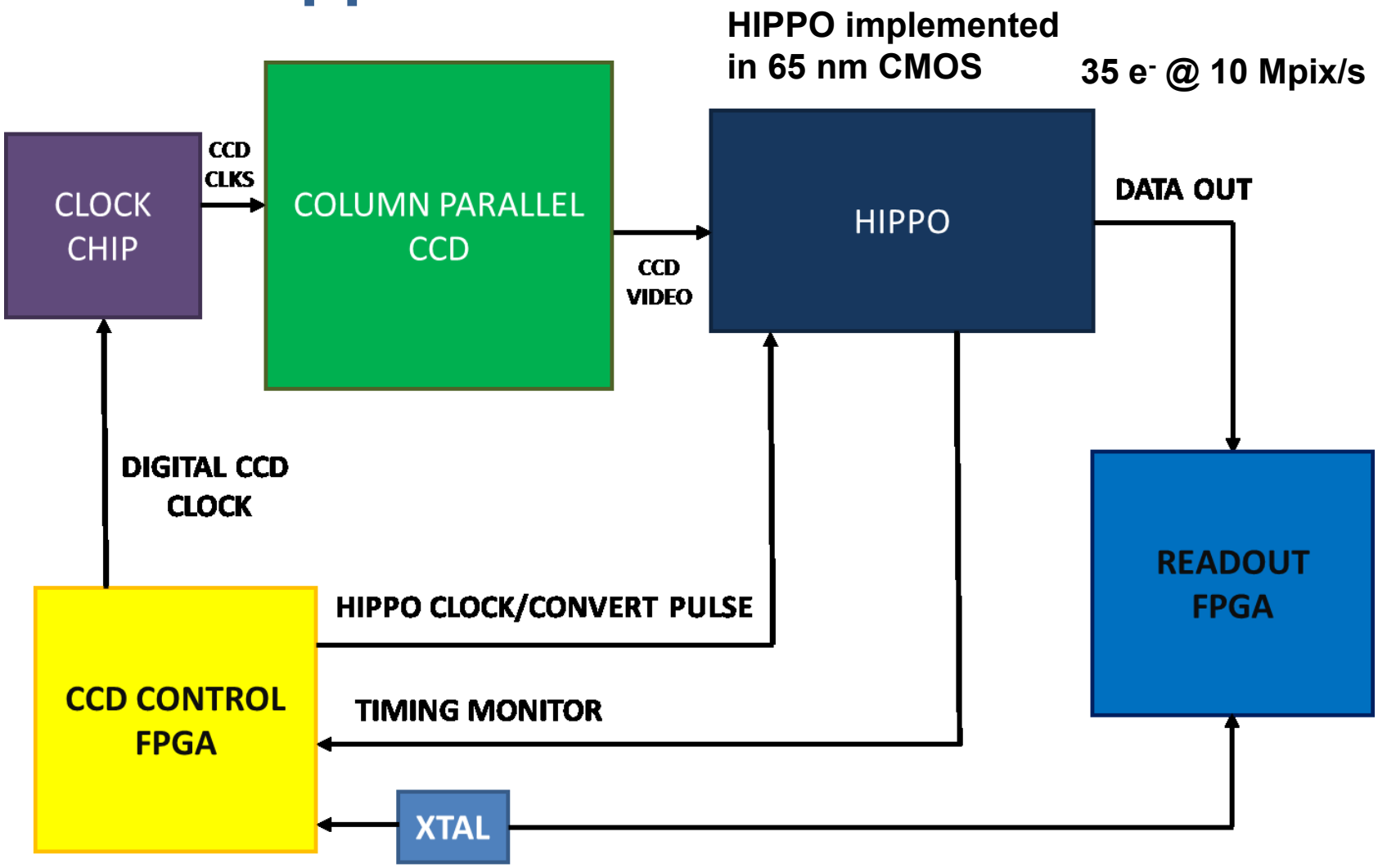
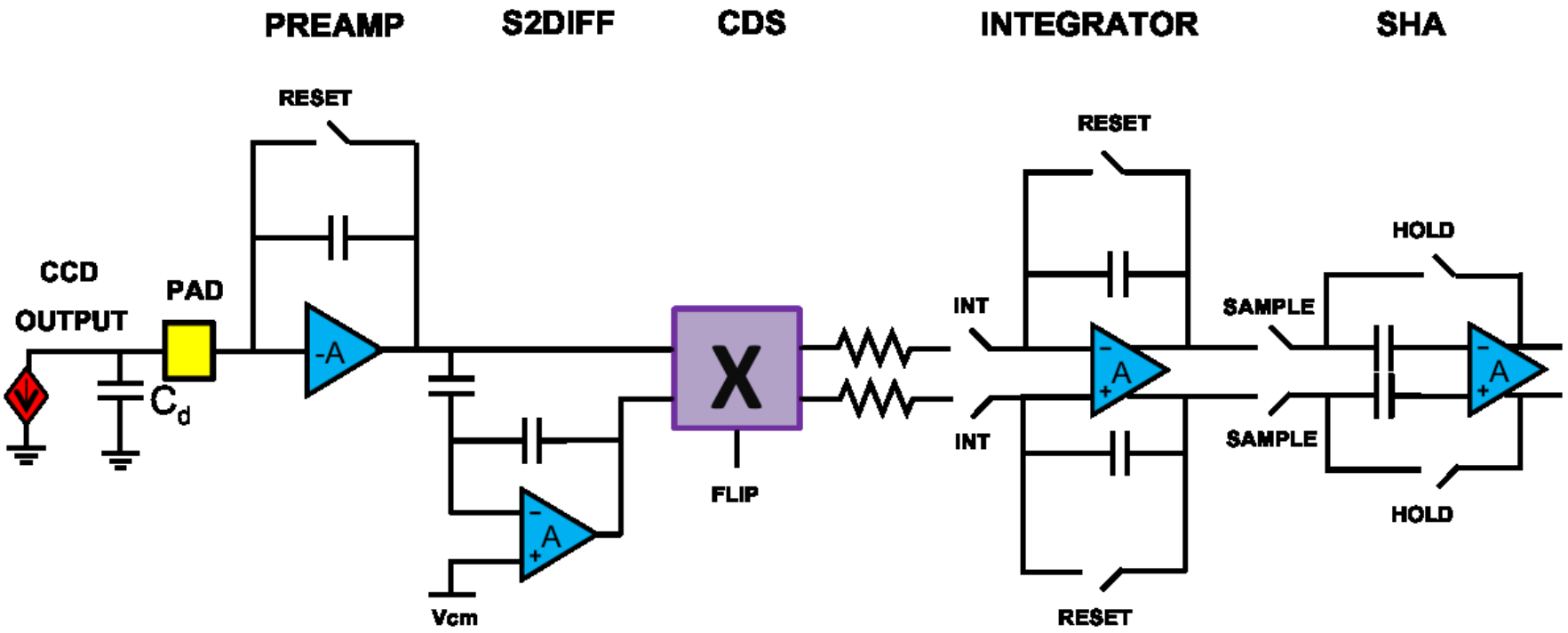
HIPPO Application

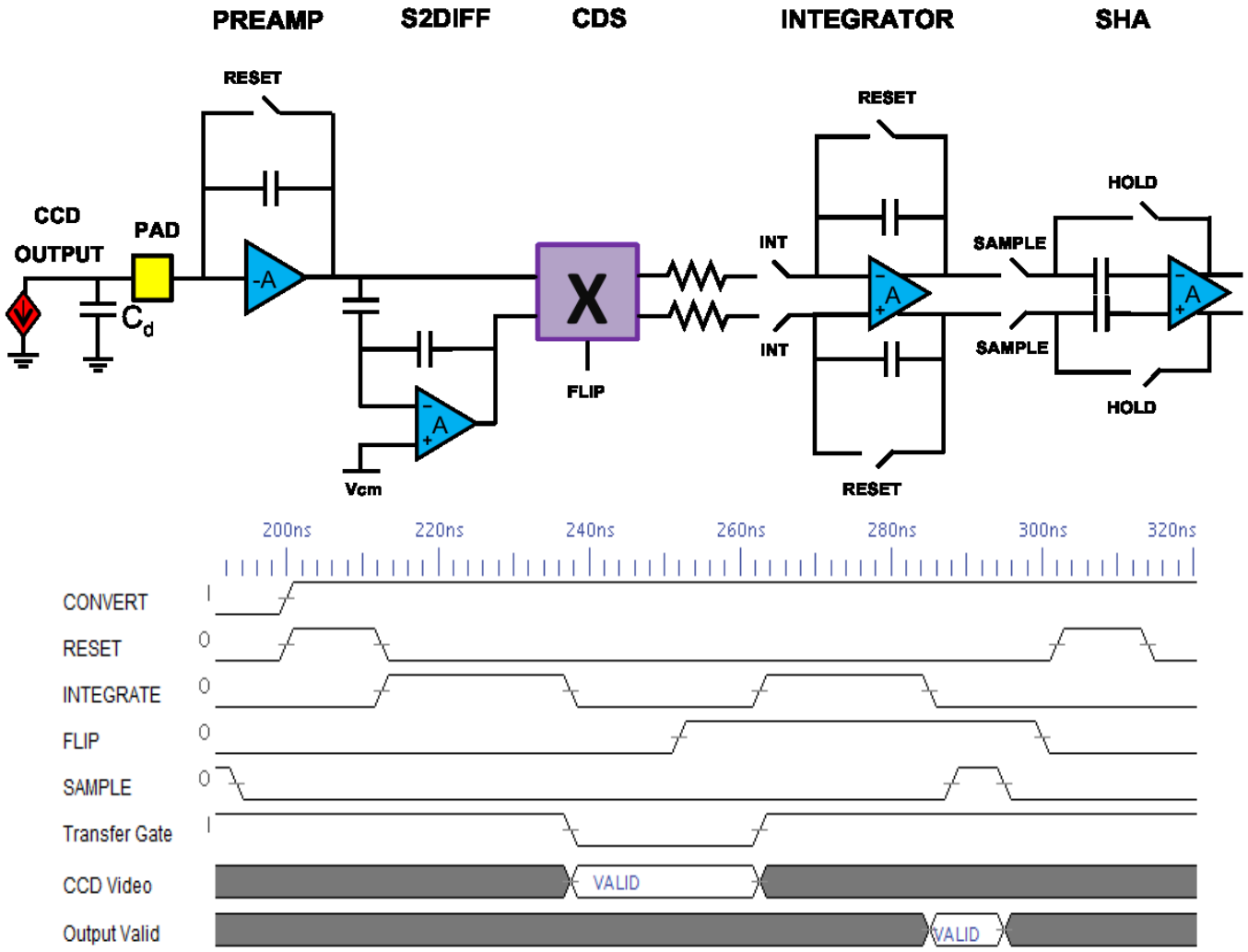


HIPPO Channel

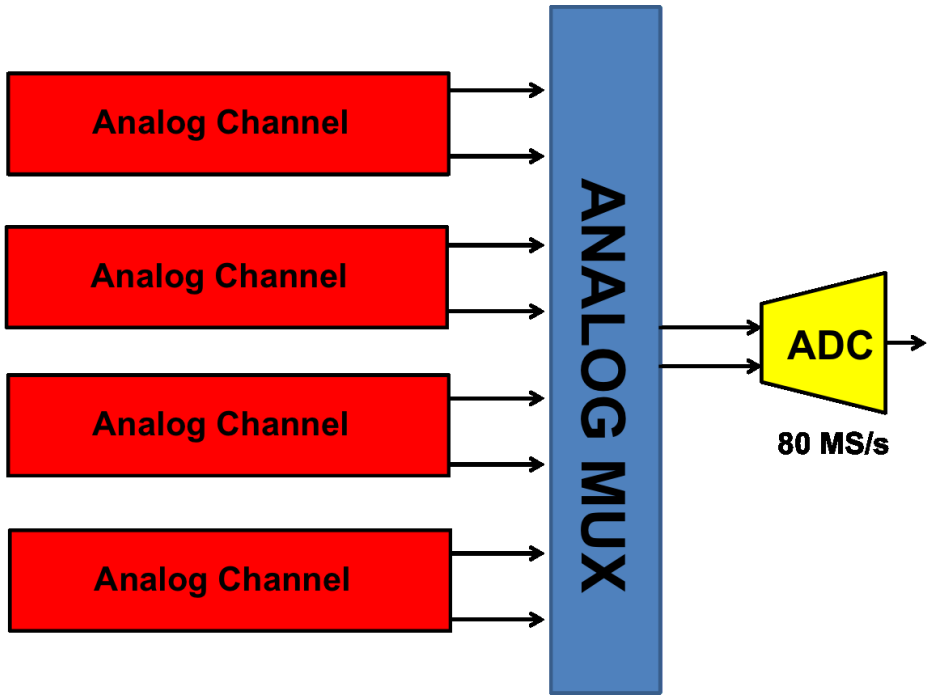


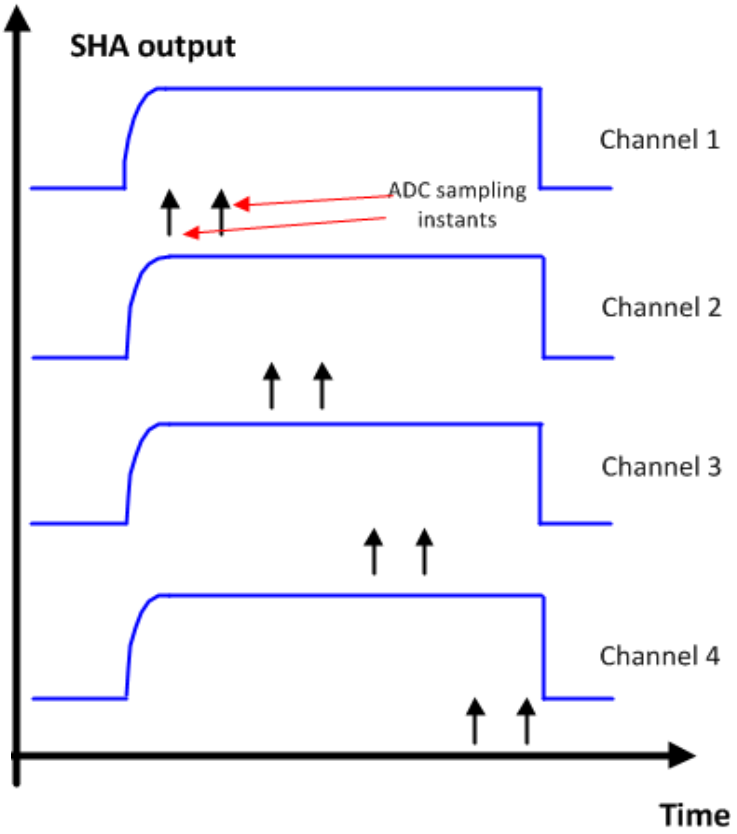
Channel pitch-matched to 50 μm CCD column
Need X4 ADC multiplexing

HIPPO Timing



HIPPO Architecture



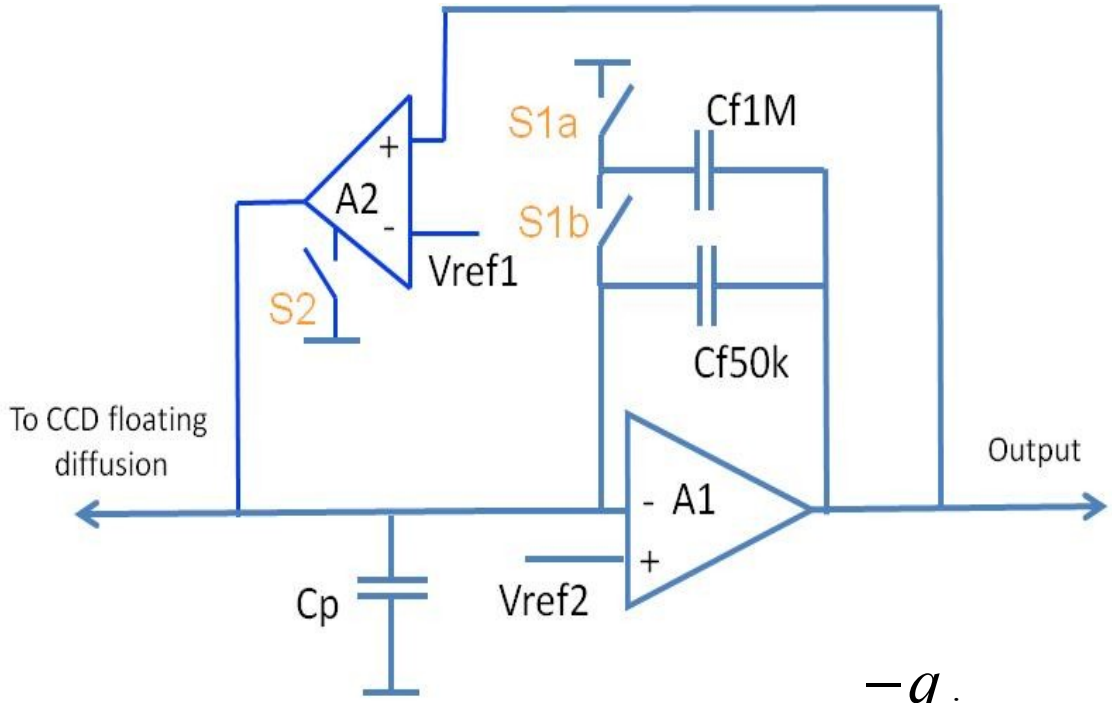


HIPPO contains 16 readout channels

One high-speed, oversampling ADC is multiplexed across each 4 channels

ADC noise reduced as $OSR^{1/2}$

HIPPO Preamplifier

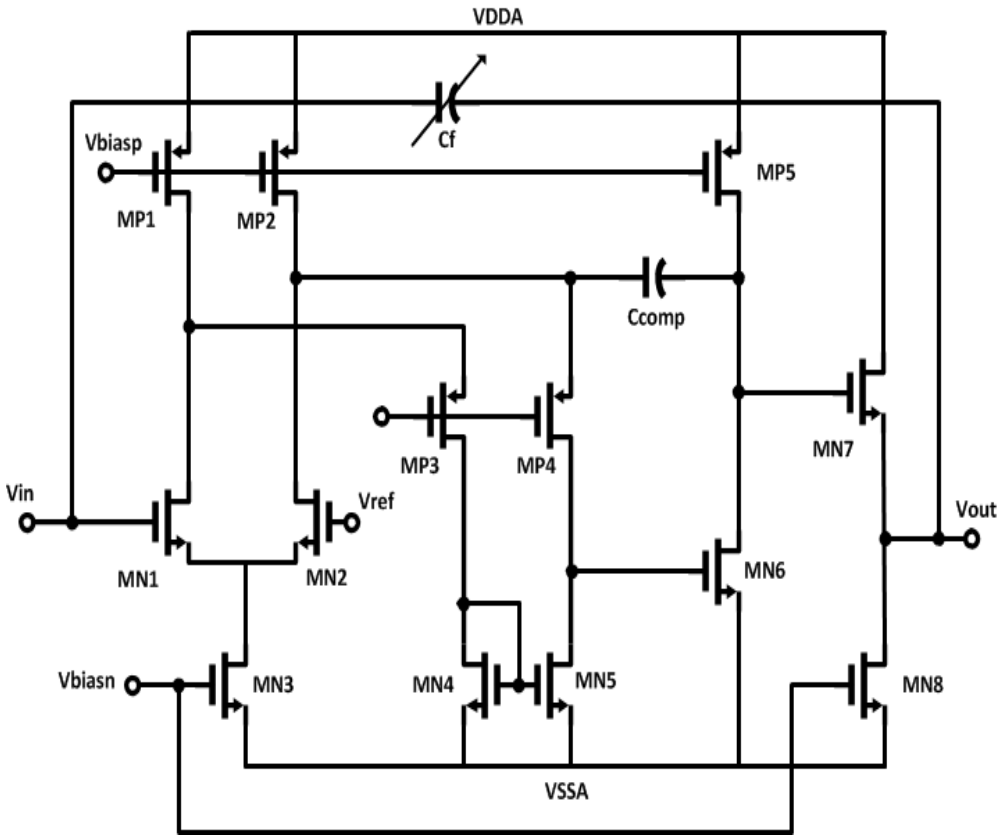


$$V_{out} = \frac{-q_{in}}{C_f + \frac{C_p}{A_{ol}}}$$

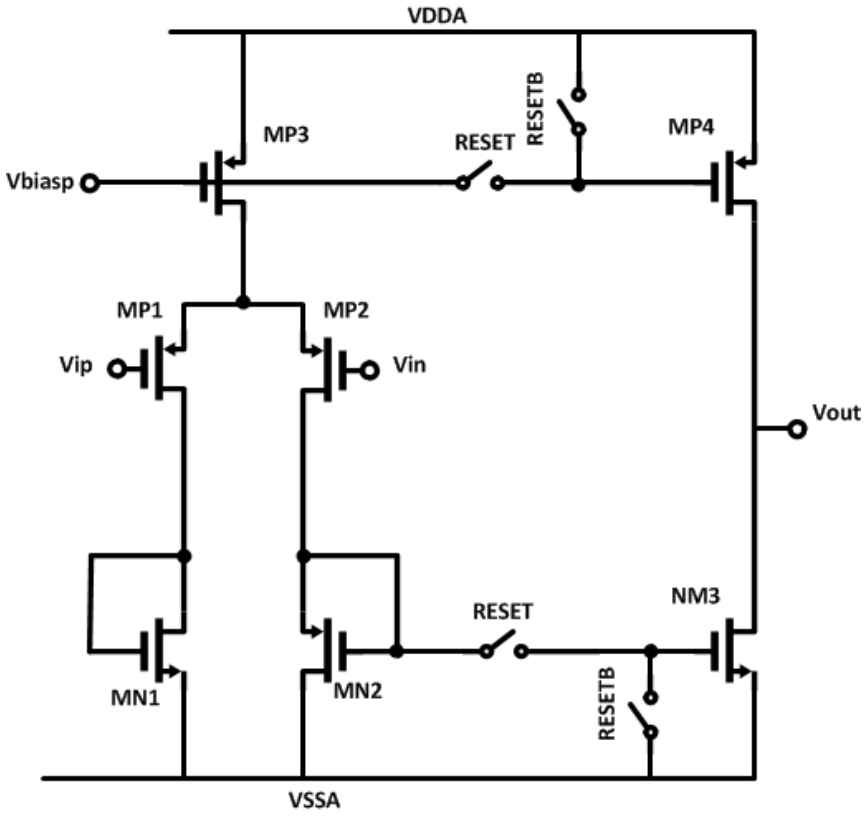
Preamp implemented with high-voltage devices

Parameter	Value	Units
Full Scale	50k / 1M	e^-
CCD charge injection	200k	e^-
Input noise	35 / 24	e^- (max / min speed)
Settling time	< 15	ns
Charge loss	< 1	%
Linearity	10	bits
Power	5	mW

HIPPO Preamplifier

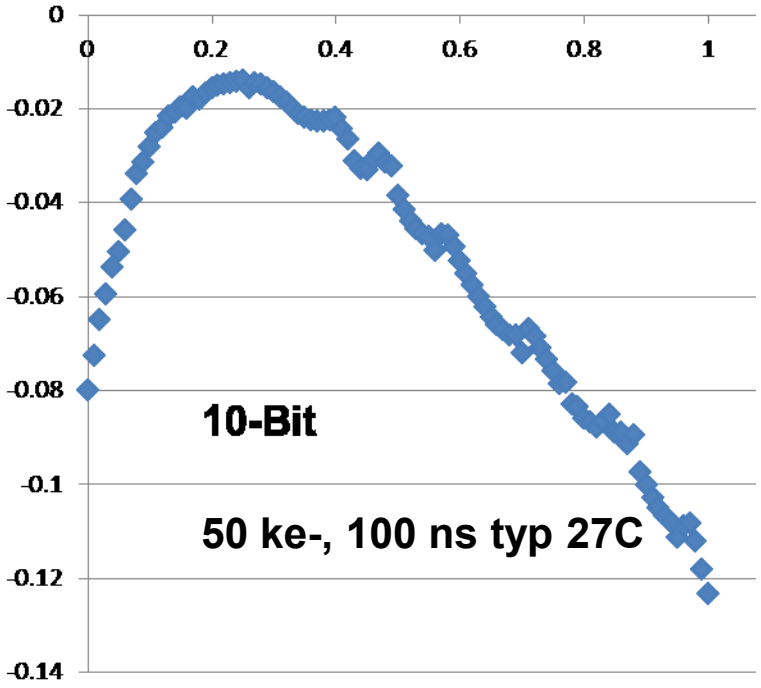


Forward Amplifier

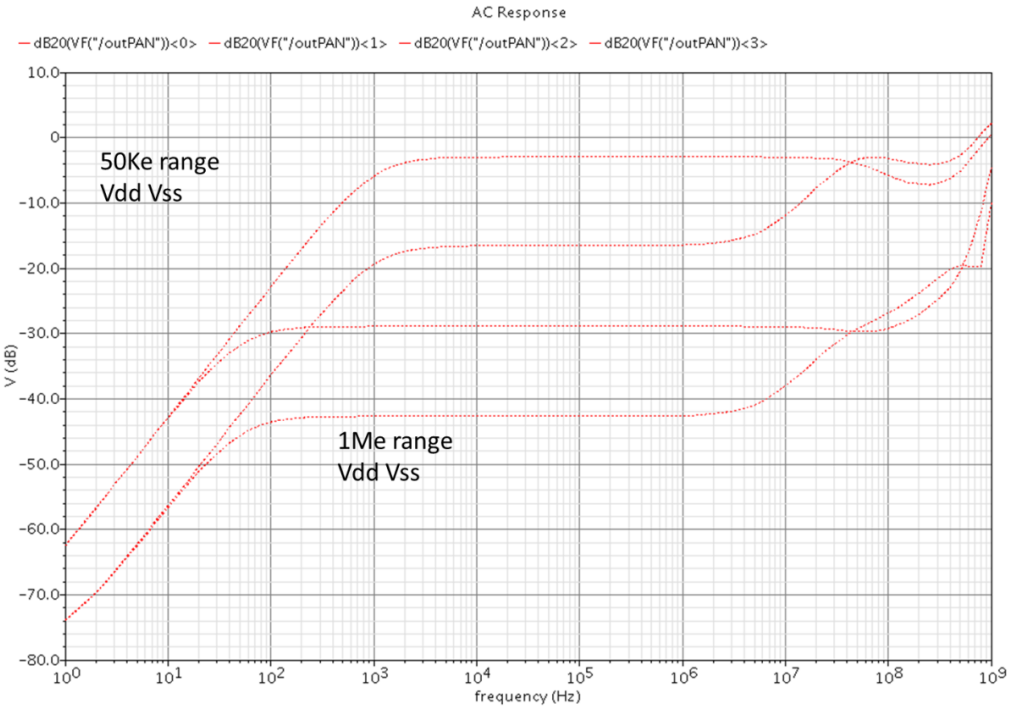


Reset OTA

HIPPO Preamplifier performance



LINEARITY



PSRR

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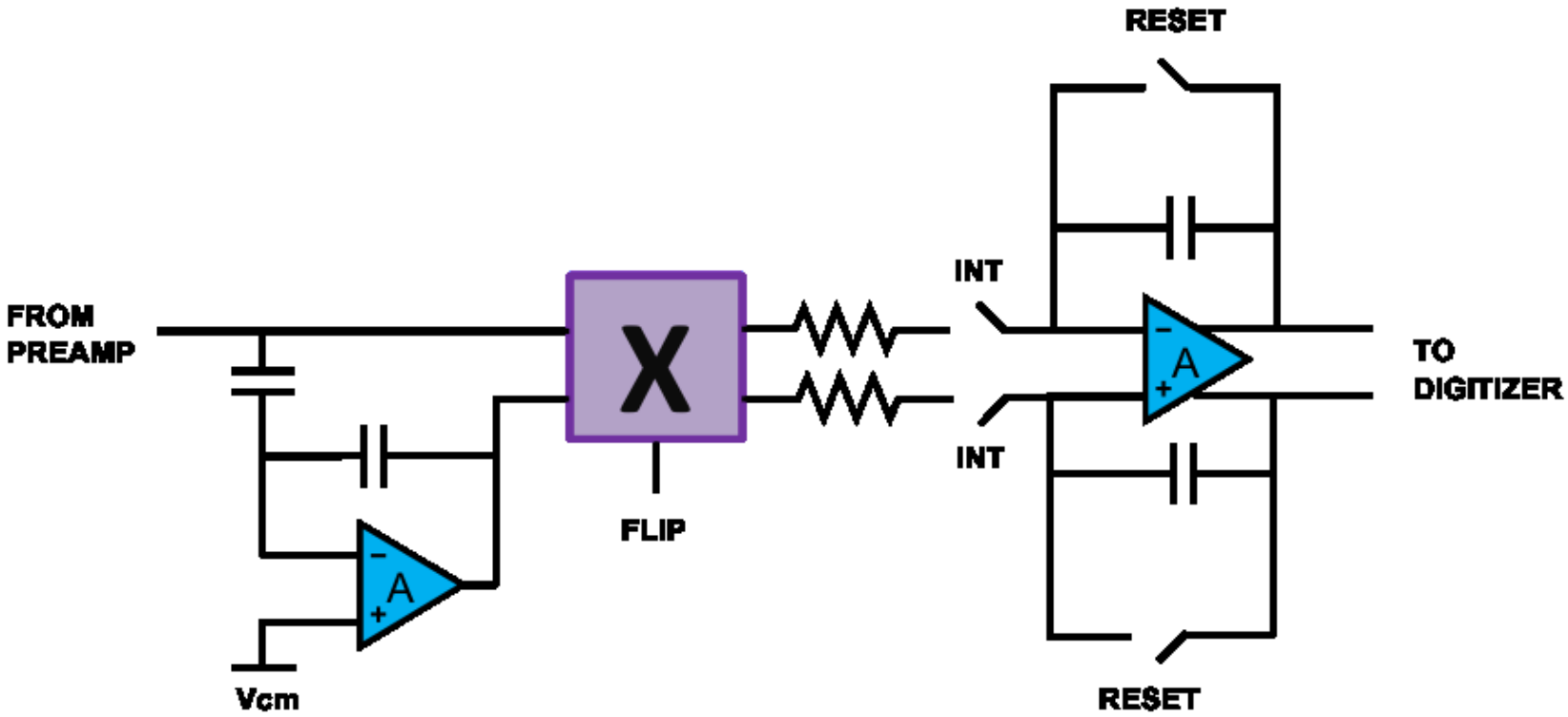
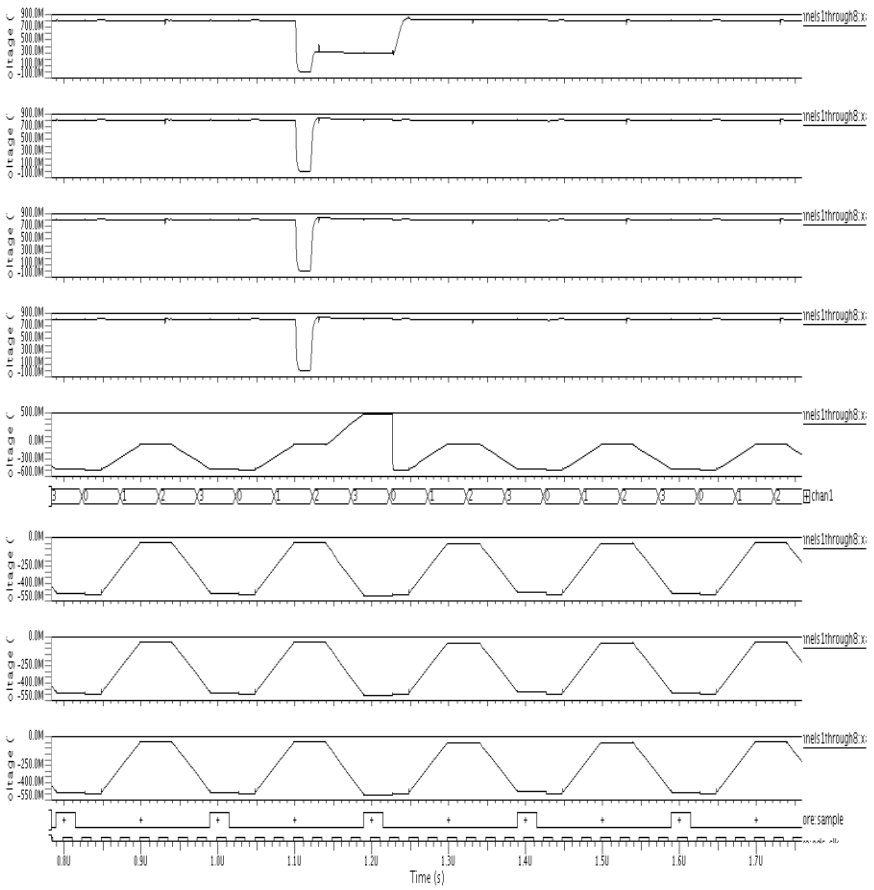
HIPPO Correlated Double-Sampler

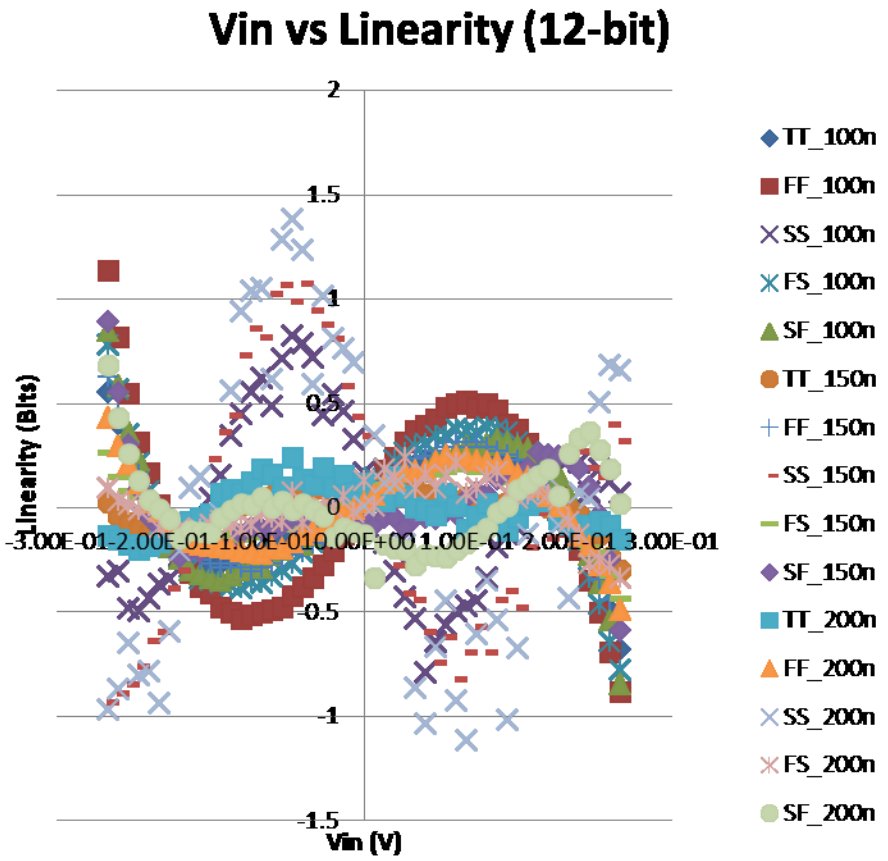


$$V_{out} = \int V_R\,dt - \int \left(V_R + V_S\right)dt$$

HIPPO Correlated Double-Sampler

Channel simulation





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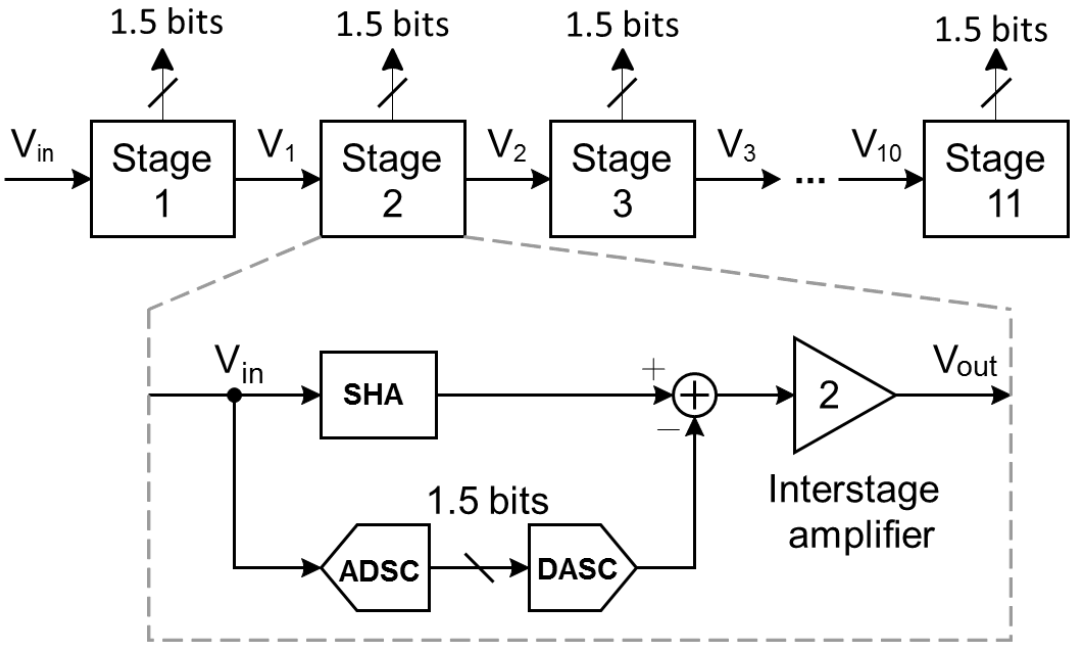
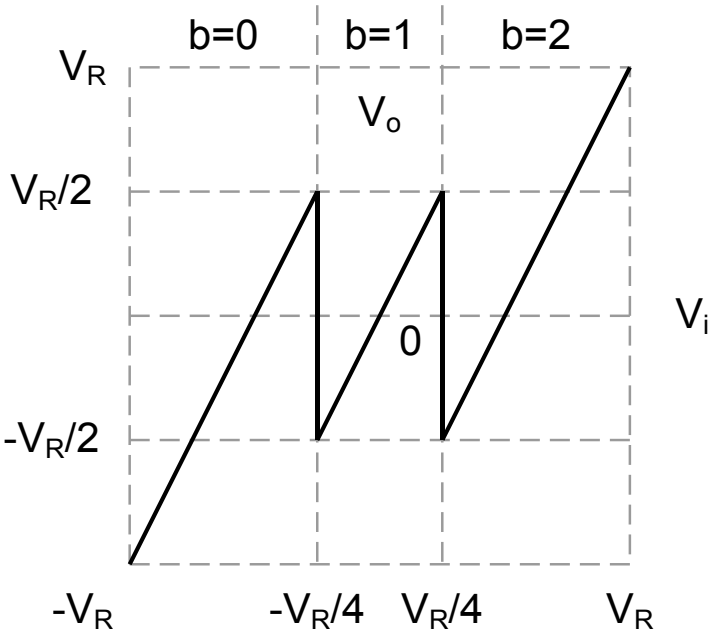
12-bit, 80 MS/s Pipelined ADC

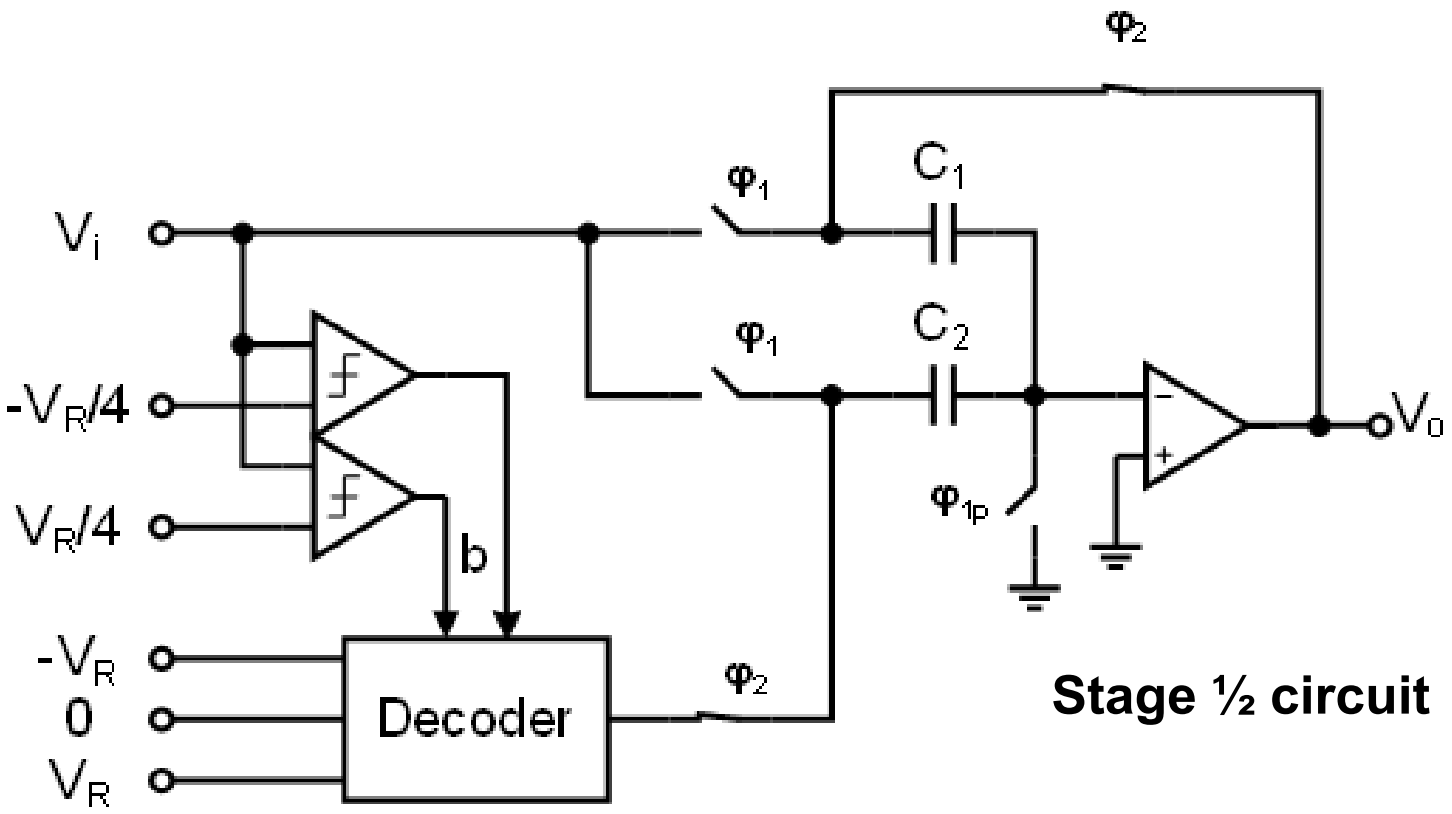


12-bit, 80 MS/s pipelined ADC



1.5-bit stage transfer characteristic

12-bit, 80 MS/s Pipelined ADC

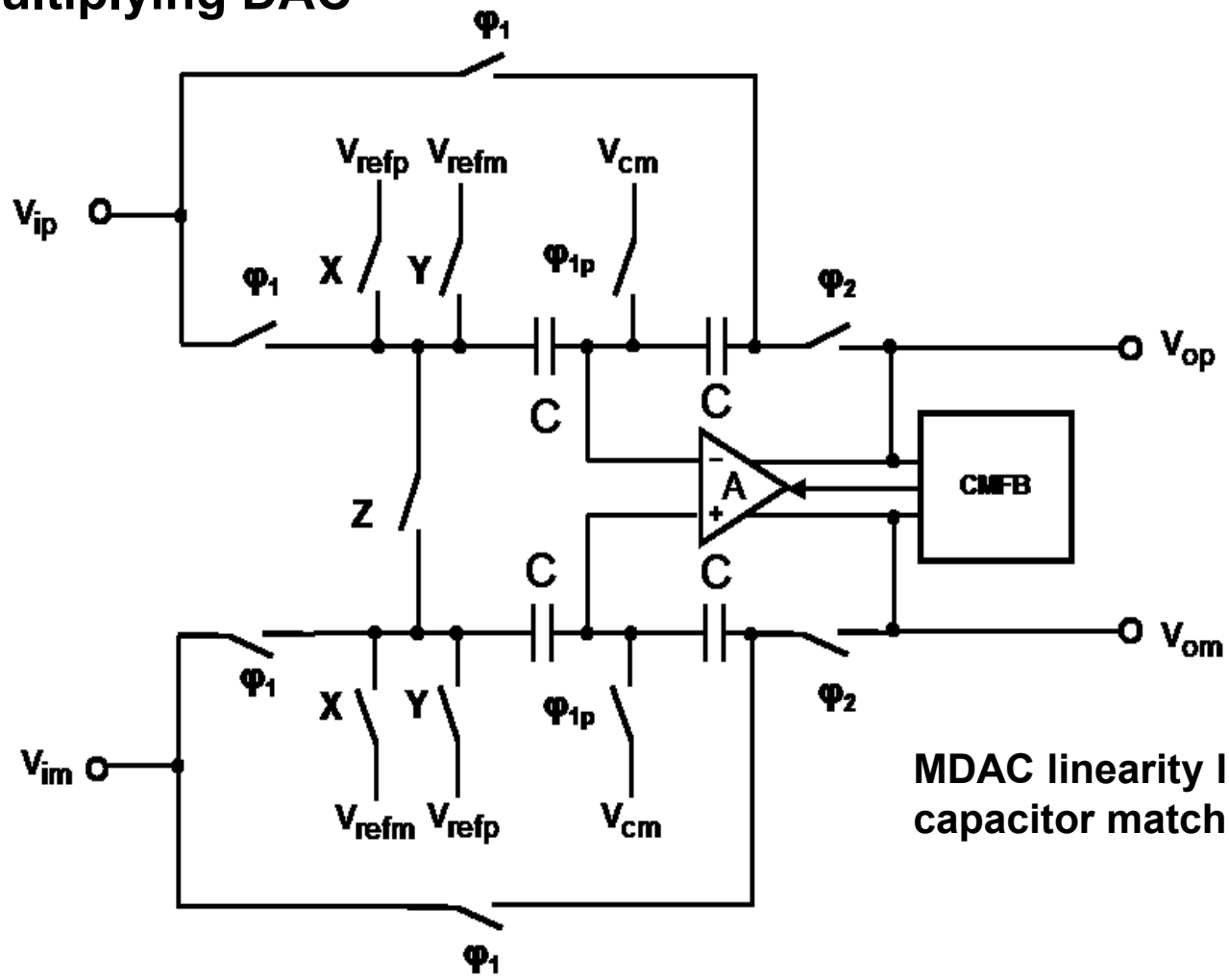


Stage ½ circuit

Flip-around MDAC architecture minimizes stage settling time

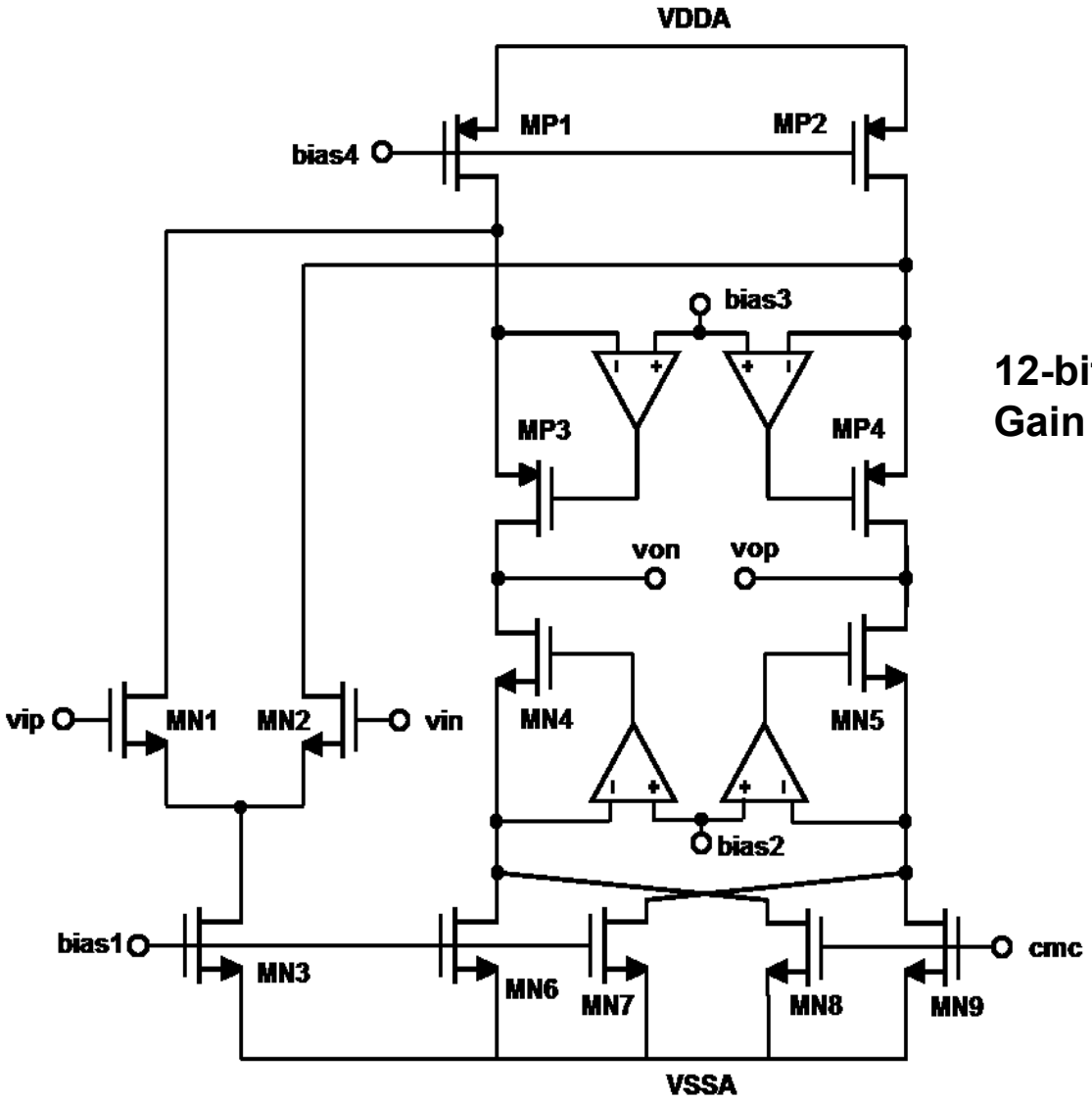
12-bit, 80 MS/s Pipelined ADC

Multiplying DAC



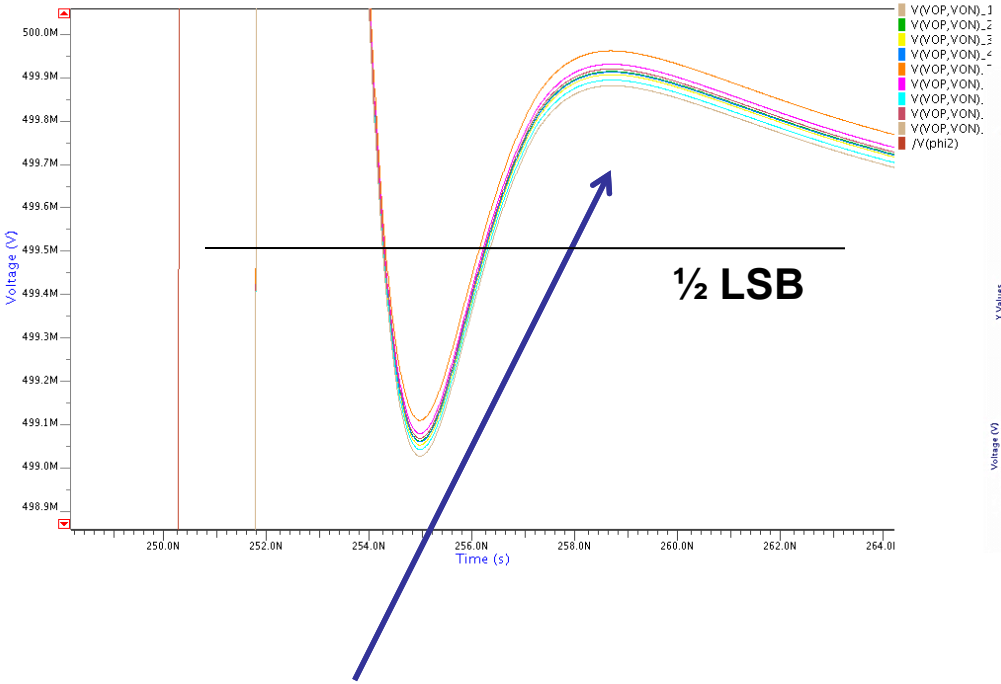
MDAC linearity limited by capacitor matching

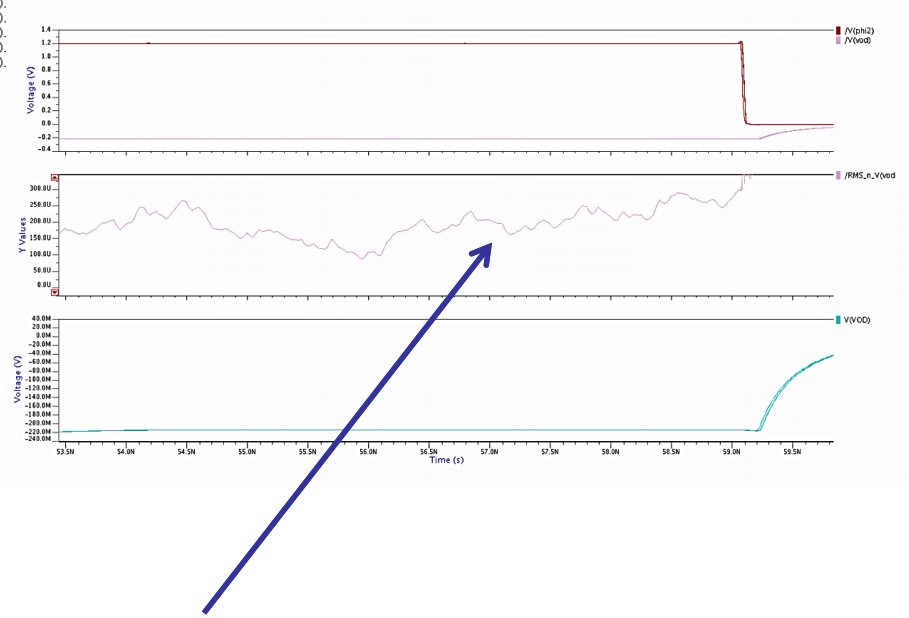
12-bit, 80 MS/s Pipelined ADC



12-bit linear gain-boosted OTA.
Gain = 72 dB, settling time < 6ns

MDAC performance





Settling to < ½ LSB in 6 ns

rms noise better than 11 bits

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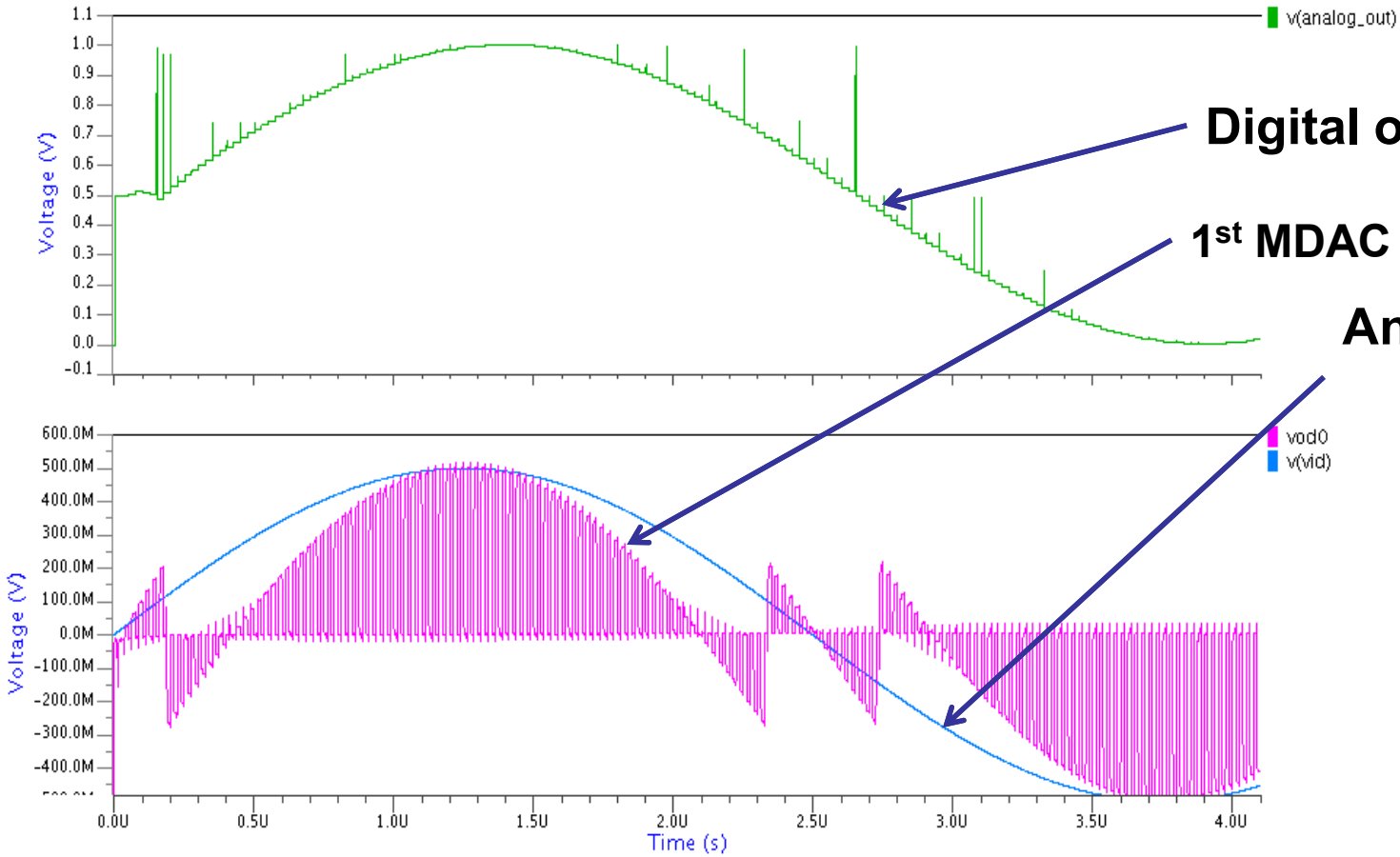
Post-layout ADC functional verification



Digital output

1st MDAC analog output

Analog input

Glitches due to Verilog-A monitor

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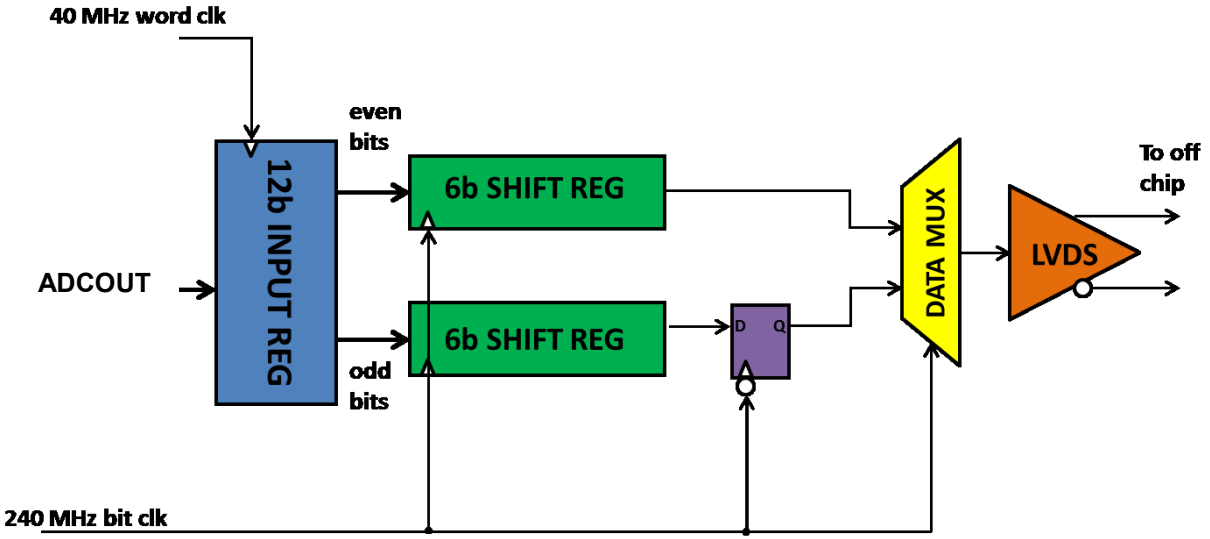
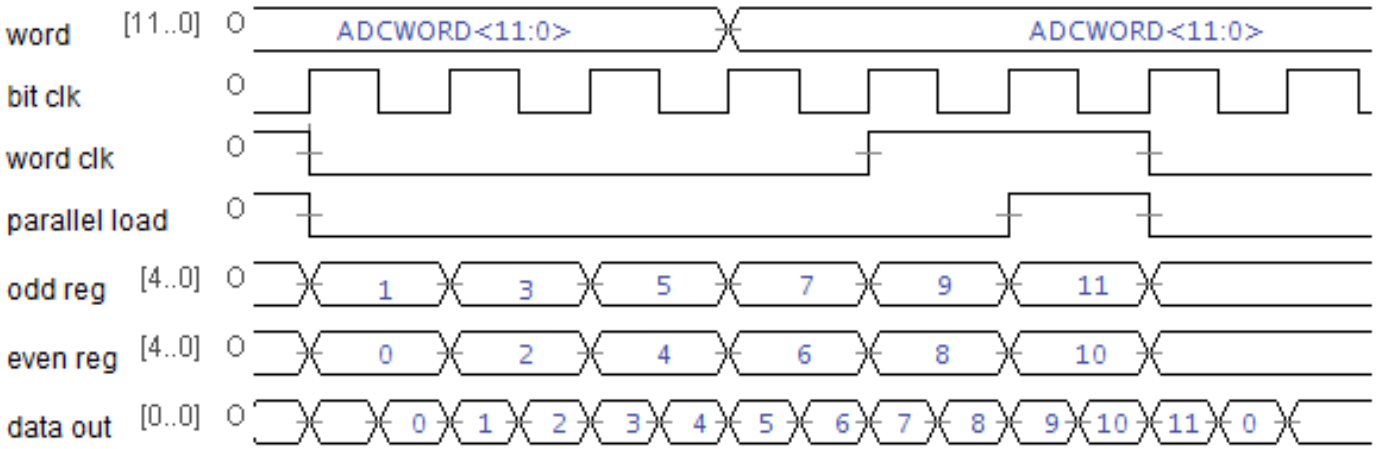
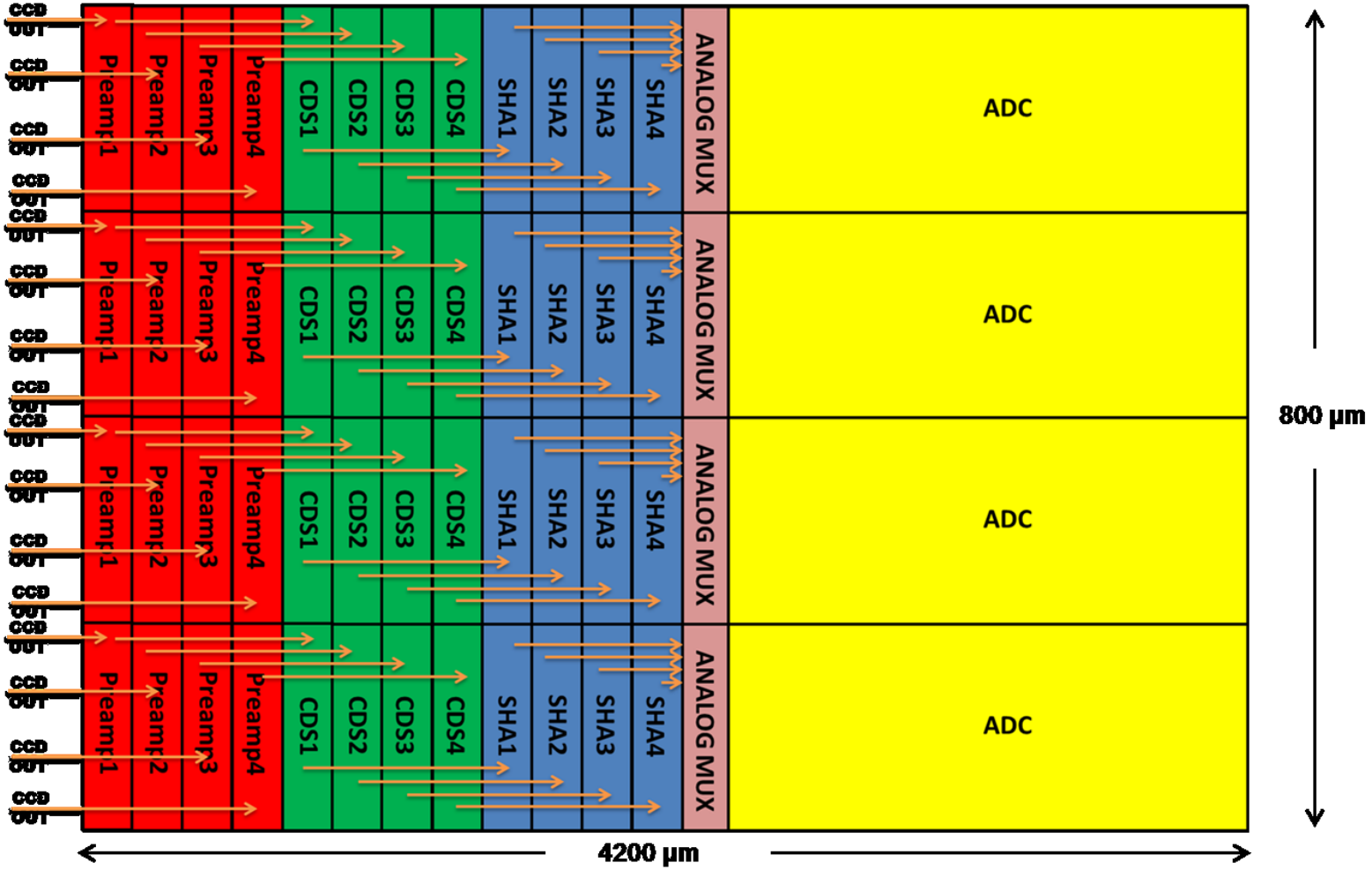
Serializer



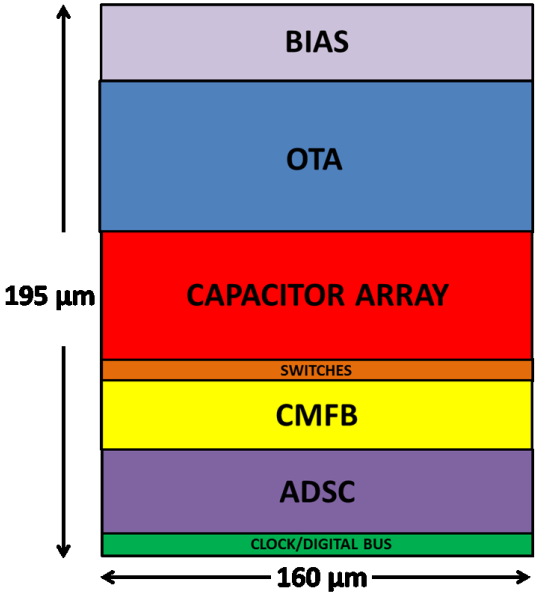


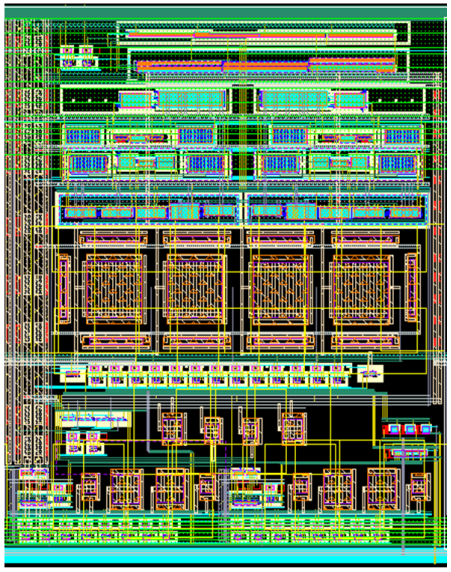
HIPPO layout strategy



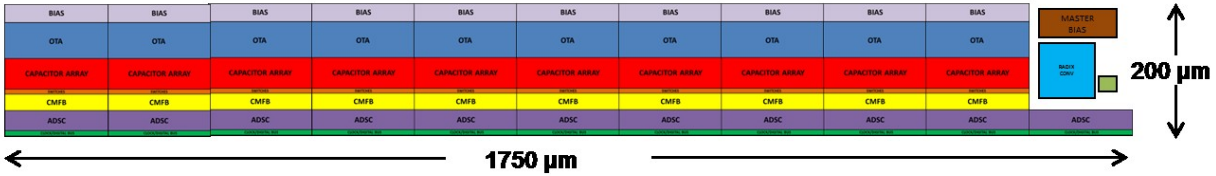
Pitch-matched ADC layout

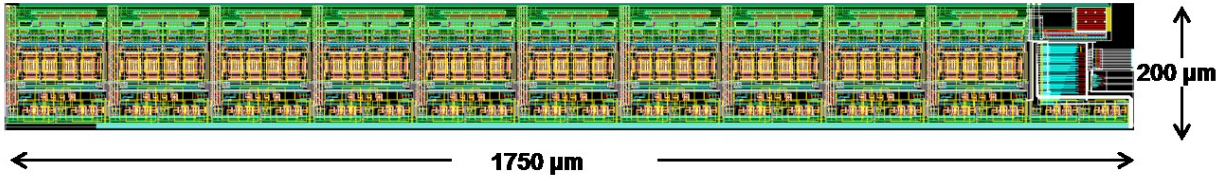
ADC stage



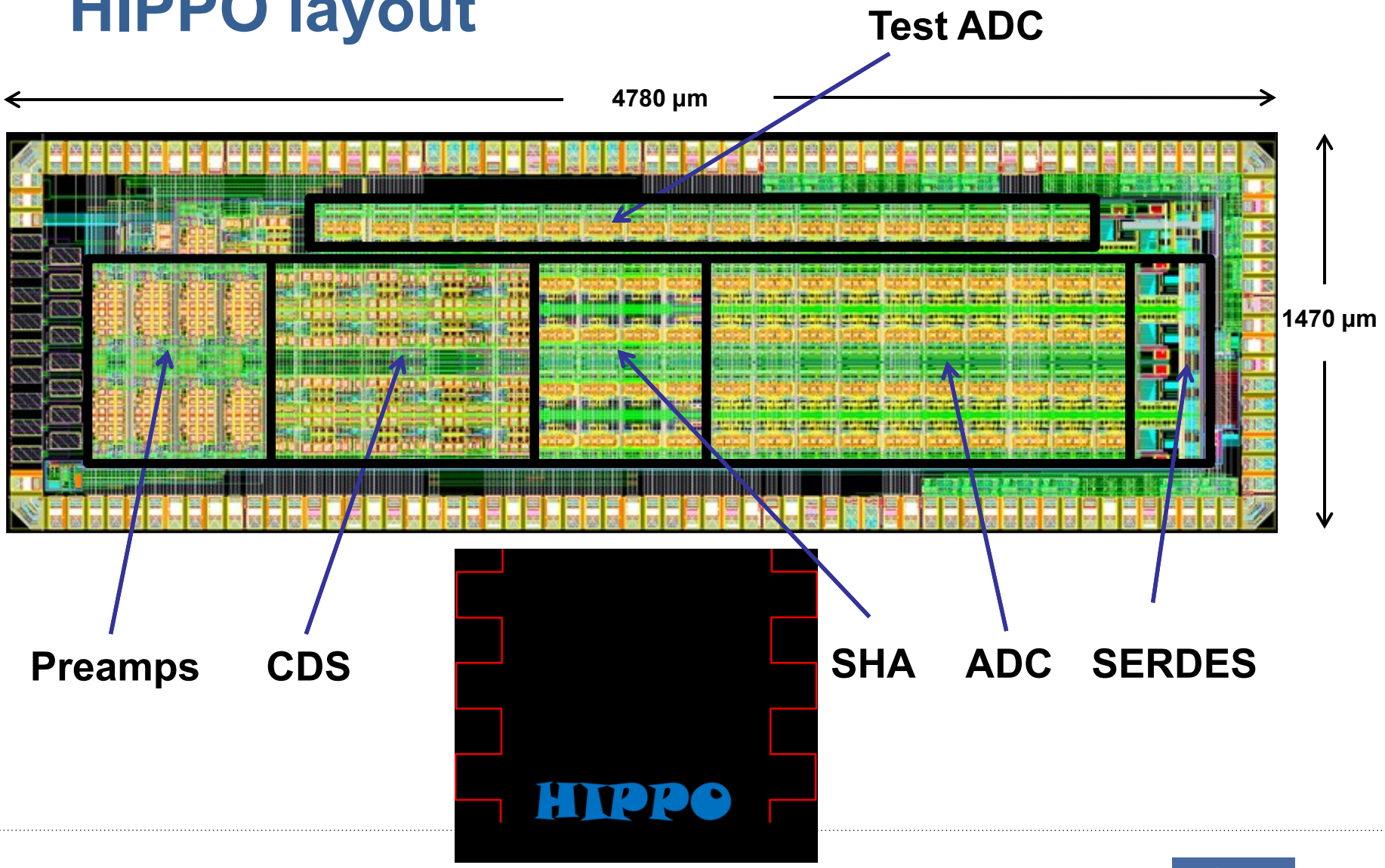


Pipeline

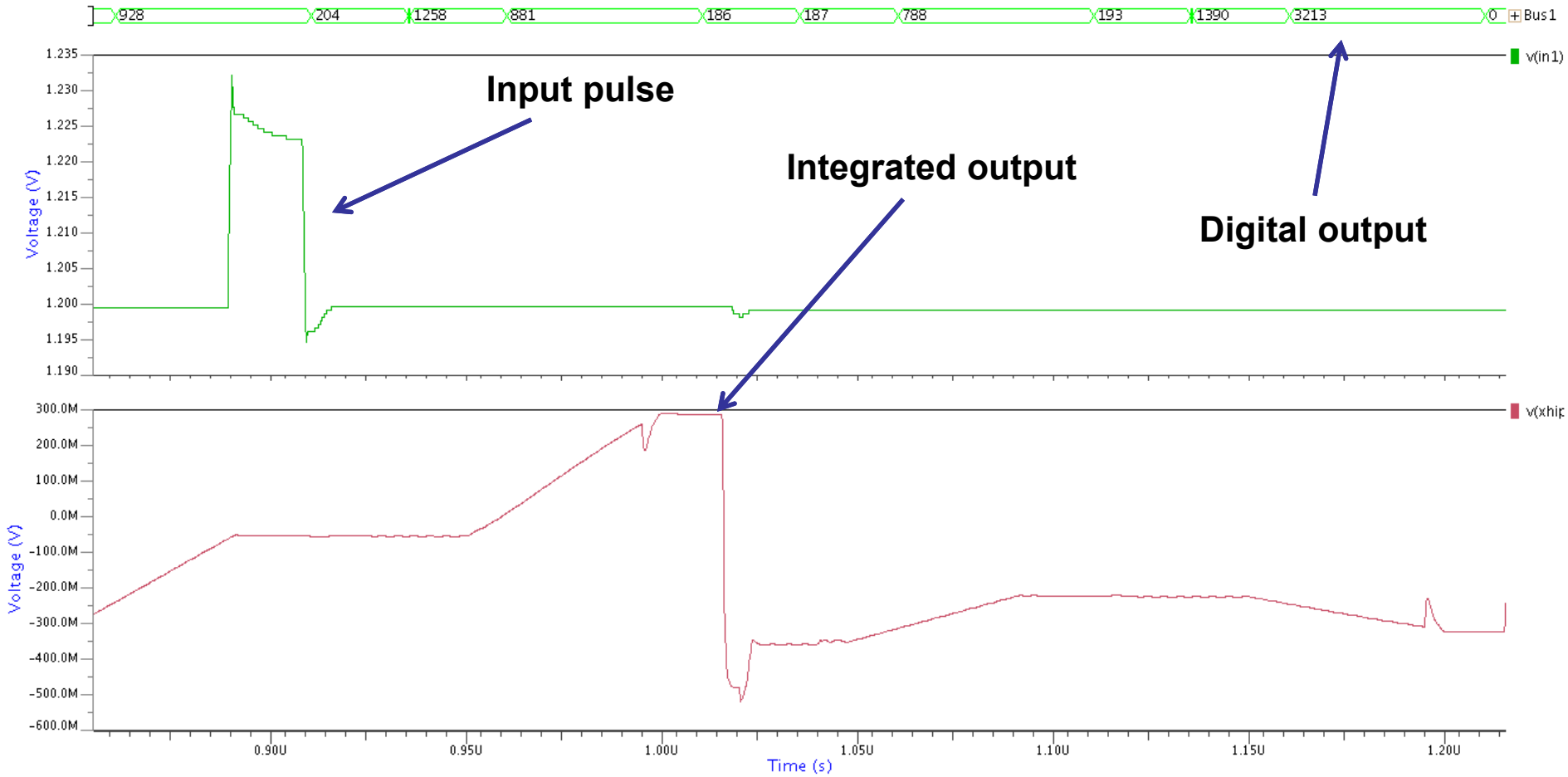




HIPPO layout



Post-layout full-chip functional simulation



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Summary

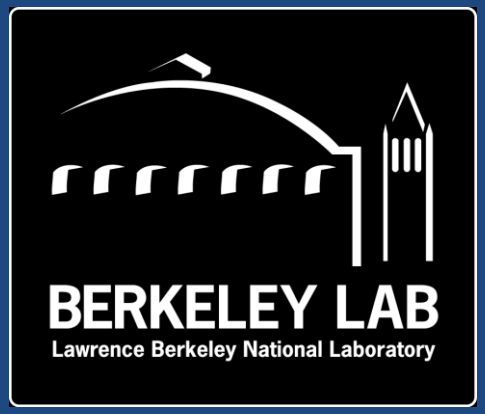
Requirement	Performance
Channel rates	10, 5, 2.5, 1.25, 0.625 MHz
ADC rates	80, 40, 20, 10 MS/s
Input Noise	35 e^- at 10 MHz, 24 e^- at 2.5 MHz @ C_{in} 500 fF
Output resolution	12 bits
Linearity	0.1 % (10 bits)
External Clock	240 MHz LVDS; fully differential
Output datarate	480 Mb/s
Channel pitch	50 μm
Power dissipation	25 mW / channel
Active area	3.5 mm^2
Technology	65 nm CMOS

Acknowledgements

- LBNL Detector Development Group

- LBNL Integrated Circuits Group

- Department of Energy Office of Basic Energy Sciences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