Recent progress of the pixel detectors R&D based on the SOI technology

Toshinobu Miyoshi (KEK IPNS)

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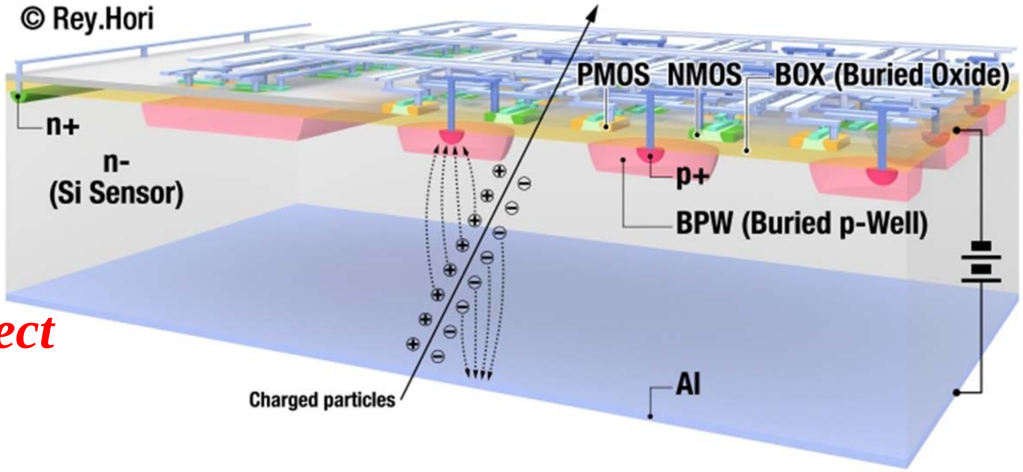
Outline

1. Overview
2. SOI pixel detectors
3. Progress & detector performance
4. Current issue
5. Conclusion & Schedule

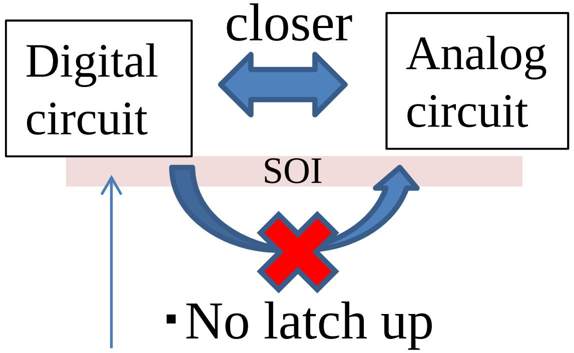
Overview of the SOI monolithic pixel detector R&D

Development of the SOI monolithic pixel detector has been started since 2005 as a project of the ***KEK Detector Technology Project (KEK DTP)***



The features of SOI monolithic pixel detector

- Use commercial SOI wafer
- High resistivity silicon --- sensor
  Low resistivity silicon --- circuit
  SiO_2 --- insulator
- No mechanical bump bonding
- Lower junction capacitance
- Full dielectric isolation
- Smaller parasitic capacitance
- Technology based on industry standards
→ lower cost



- No latch up
- less probability of SEE

SOI Process & MPW

Process (OKI Semiconductor Co. Ltd.)	0.2μm Low-Leakage Fully-Depleted (FD) SOI CMOS 1 Poly, 5 Metal layers, MIM Capacitor, DMOS option, Core (I/O) 1.8 (3.3) V
SOI wafer (200 mm ϕ =8 inch)	Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz ~700 Ω-cm (*n-type*), 650 μm thick FZ ~ 8 k Ω-cm (*n- or p- type*), 650 μm thick
Backside	Thinned to 260 μm and sputtered with Al (200 nm). (to be optimized)

Multi Project Wafer (MPW) run

- KEK organizes MPW runs
- Mask is shared to reduce cost of a design
- Including pixel detector chip and SOI-CMOS circuit chip
- Once a year in 2005-2008, 2011
- **Twice a year in 2009, 2010, (2012-?**

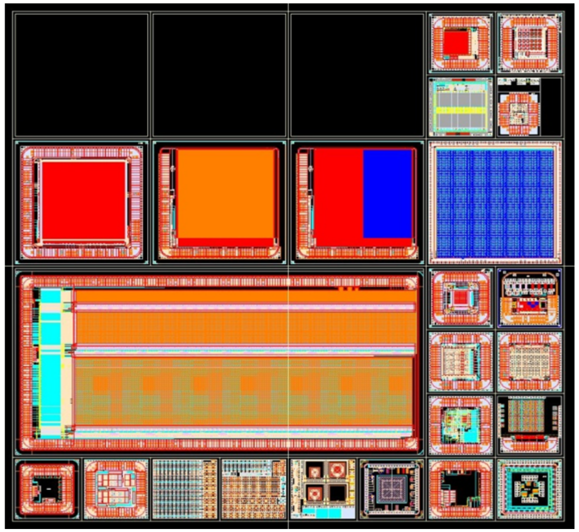
▪ University & institution

KEK, FNAL, LBNL, Kyoto Univ, Tohoku Univ, Univ. of Tsukuba, RIKEN, JAXA, Krakow, Hawaii, and more…

Supporting companies

OKI Semiconductor Co. Ltd. ,
OKI Semiconductor Miyagi Co. Ltd. , T-Micro Co. Ltd., Rigaku Co. Ltd

MPW FY10-1 (Aug. 2010)



20.8mm

KEK SOI Pixel detectors

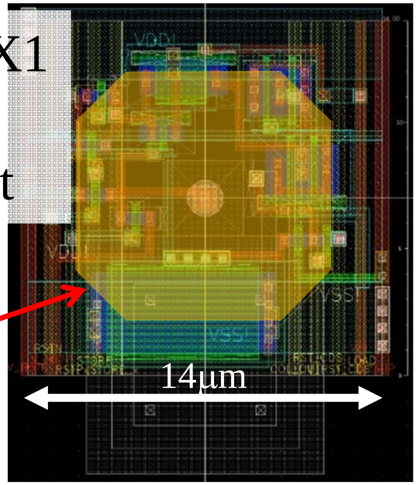
- Integration-type pixel detector
(INTPIX1,2,3a,3b,3c,3e,4 and Dual-mode INTPIX=DIPIX)
- Counting-type pixel detector (CNTPIX2,3,4,5)

A.Takeda's talk
ID=282, (11 Sat.)

Specification summary of integration-type pixel detector since 2008

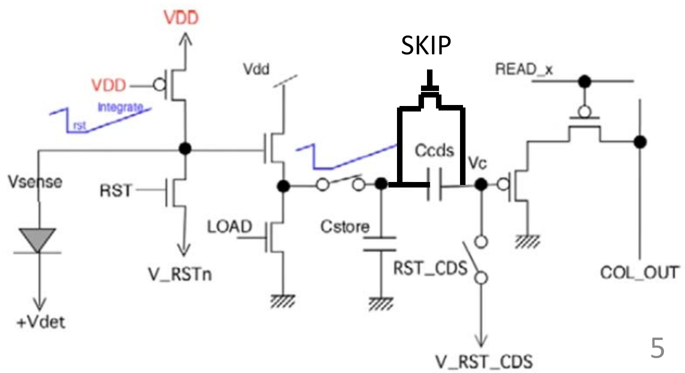
	pixel size [μm]	# of pixels	Effective Area [mm]	Chip area [mm]	Fabrication year	# of pixel type	CDS in pixel
INTPIX3a	20 x 20	128 x 128	2.56 x 2.56	5 x 5	FY08	8	No
INTPIX3b	20 x 20	128 x 128	2.56 x 2.56	5 x 5	FY09-1	8	No
INTPIX4	17 x 17	**832 x 512**	**14.144 x 8.704**	**15.3 x 10.2**	FY09-1	1	Yes
INTPIX3c	20 x 20	128 x 128	2.56 x 2.56	5 x 5	FY09-2	8	No
INTPIX3e	16 x 16	192 x 192	3.072 x 3.072	5 x 5	FY10-1	1	No
DIPIX1	**14 x 14**	256 x 256	3.584 x 3.584	5 x 5	FY10-1	1	Yes
DIPIX2	**14 x 14**	256 x 256	3.584 x 3.584	5 x 5	FY10-1	2	Yes

DIPIX1
pixel
layout

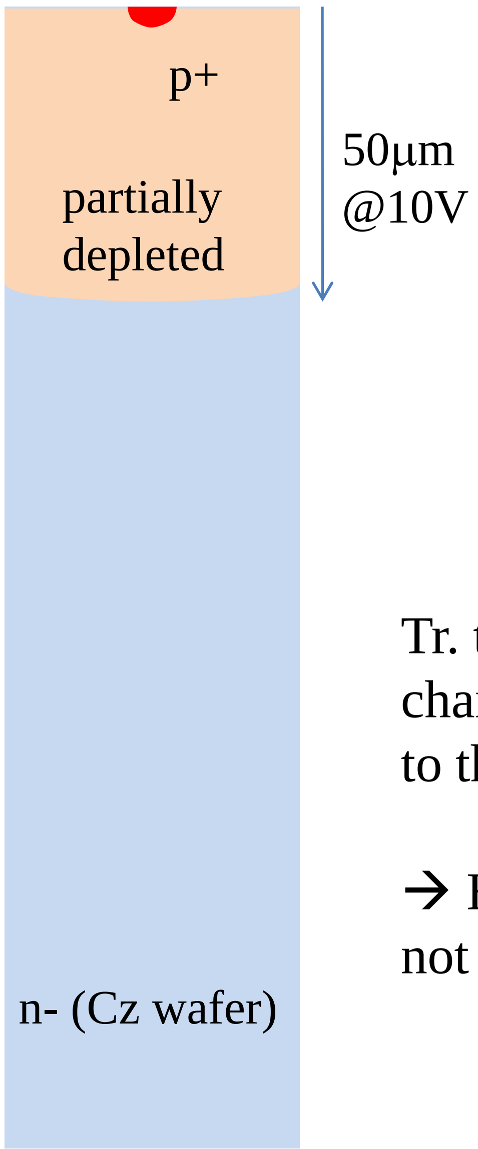


Buried
P-Well
(BPW)

DIPIX1 pixel circuit



Progress of SOI pixel detector R&D (1)



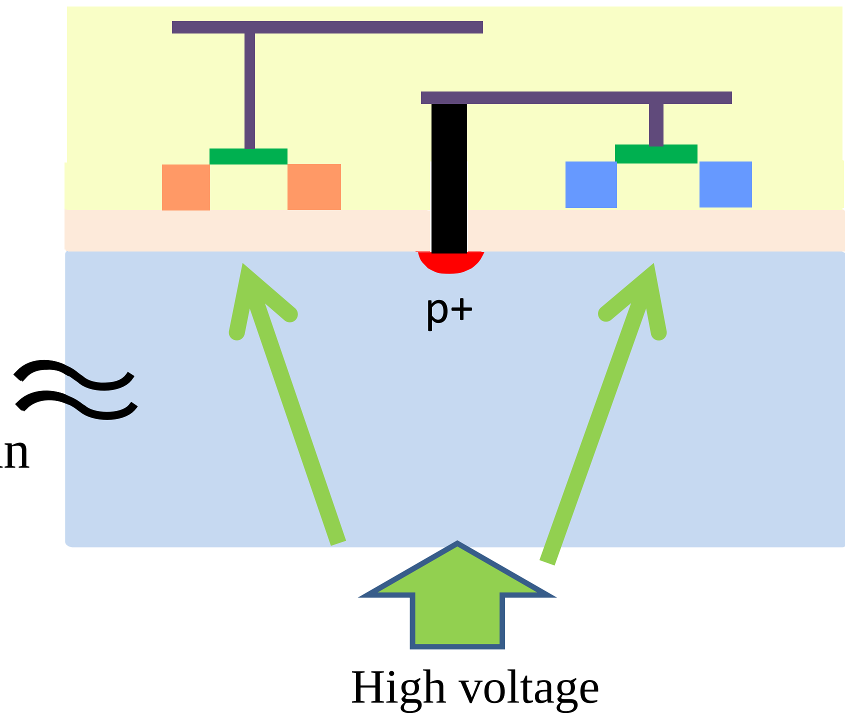
-2008

Sensor test with visible light laser
Partial depletion with lower back-bias voltage
Front illumination (from the circuit side)
<u>Back gate effect problem</u>

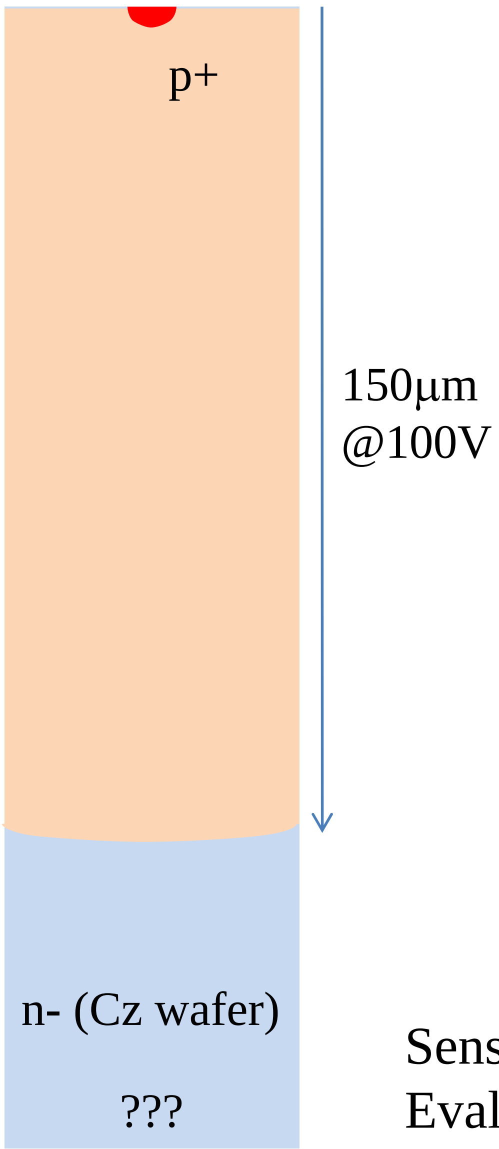
2D diagram of the SOI detector

Tr. threshold changes according to the back bias

→ High voltage can not be applied



Progress of SOI pixel detector R&D (2)

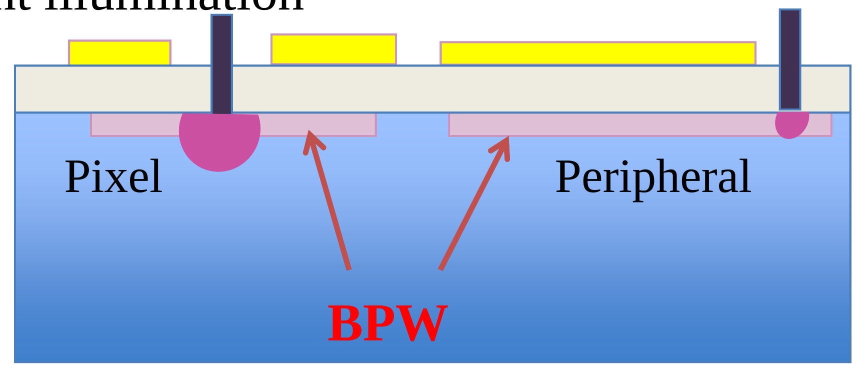


-2008

Sensor test with visible light laser
Partial depletion with lower back-bias voltage
Front illumination (from the circuit side)
Back gate effect problem

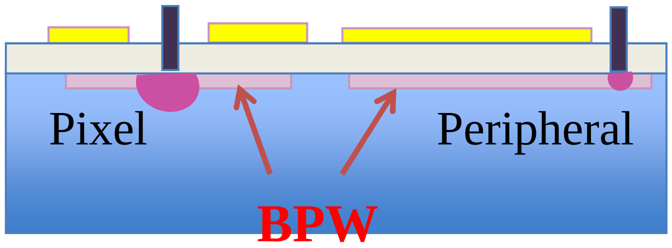
2009 -

Introduction of BPW process
Sensor test with IR laser, X-ray and charged particle
Partial depletion with higher back-bias voltage
Front illumination



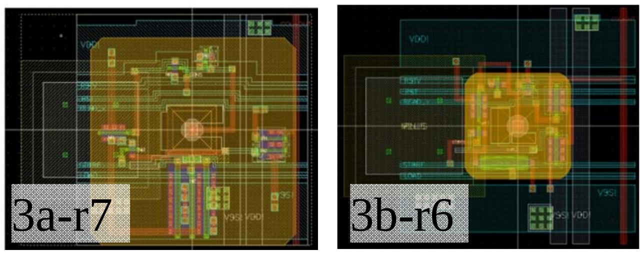
Sensor gain measurement
Evaluation of spatial resolution with BPW
@KEK-PF and X-ray generator

Sensor gain



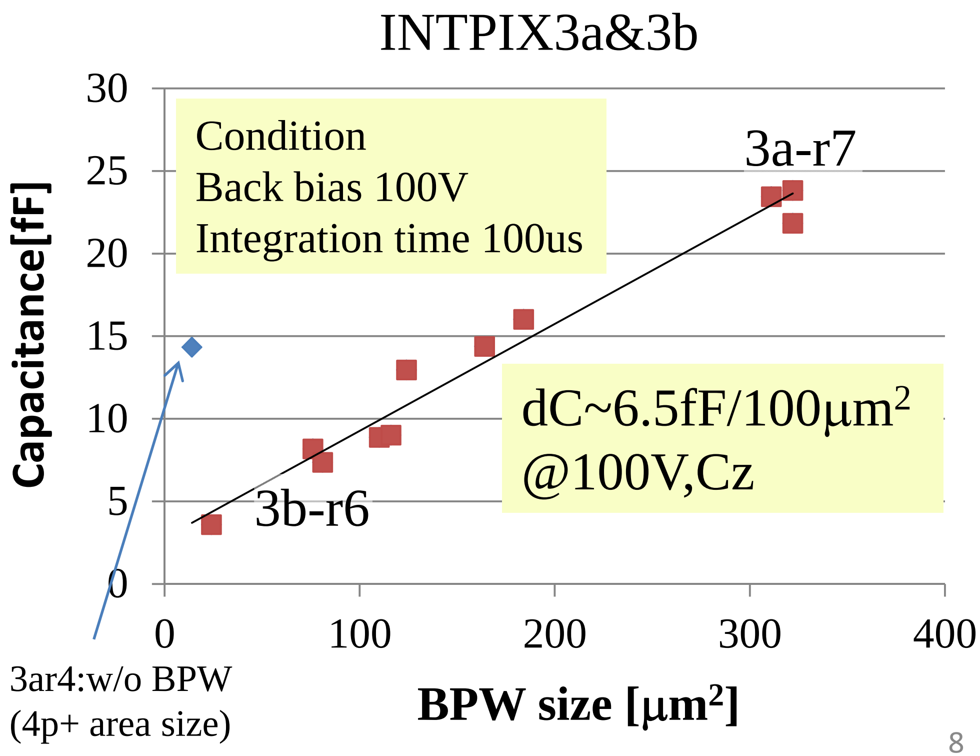
Pixel contact size ~ a few μm
"BPW-in-pixel" increases sensor capacitance
→ Sensor gain decreases

- Gain measurement was done using SR X-ray in KEK Photon Factory
- X-Ray from 6 keV – 18.5 keV in BL-14A
- Internal gain was measured and then calculated capacitance



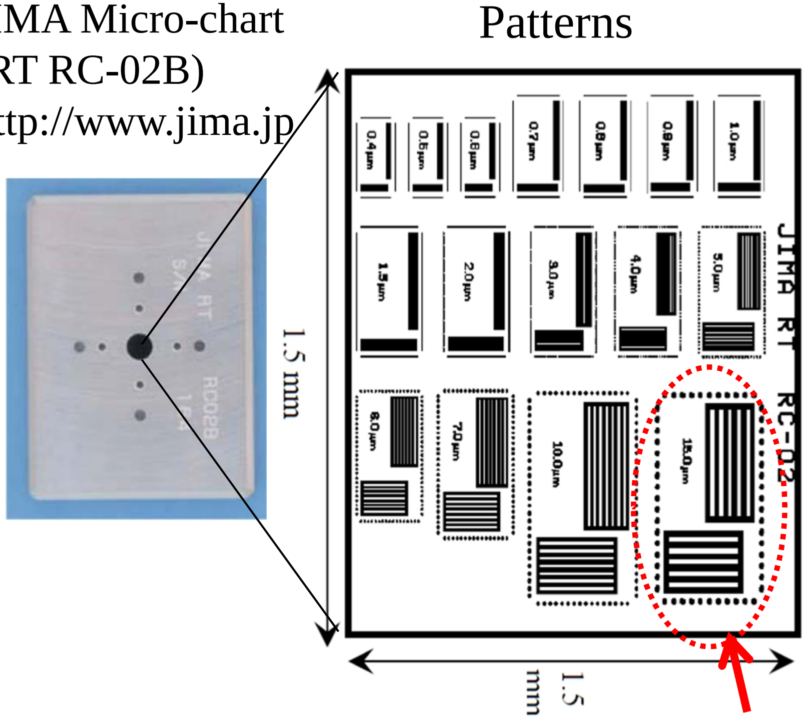
Pixel layout

-Gain decrease with "BPW-in-pixel" size
-Capacitance ~ 8fF
Gain ~ 20μV/e- @ 3b-r6 (optimized BPW size) →applied to INTPIX3e



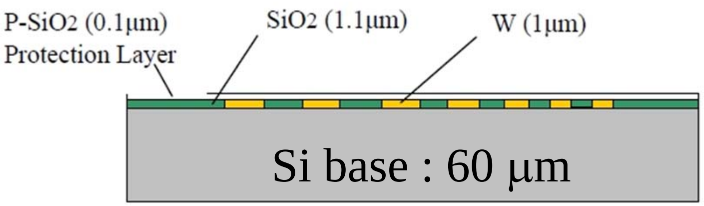
DIPIX1(14μm pixel) spatial resolution

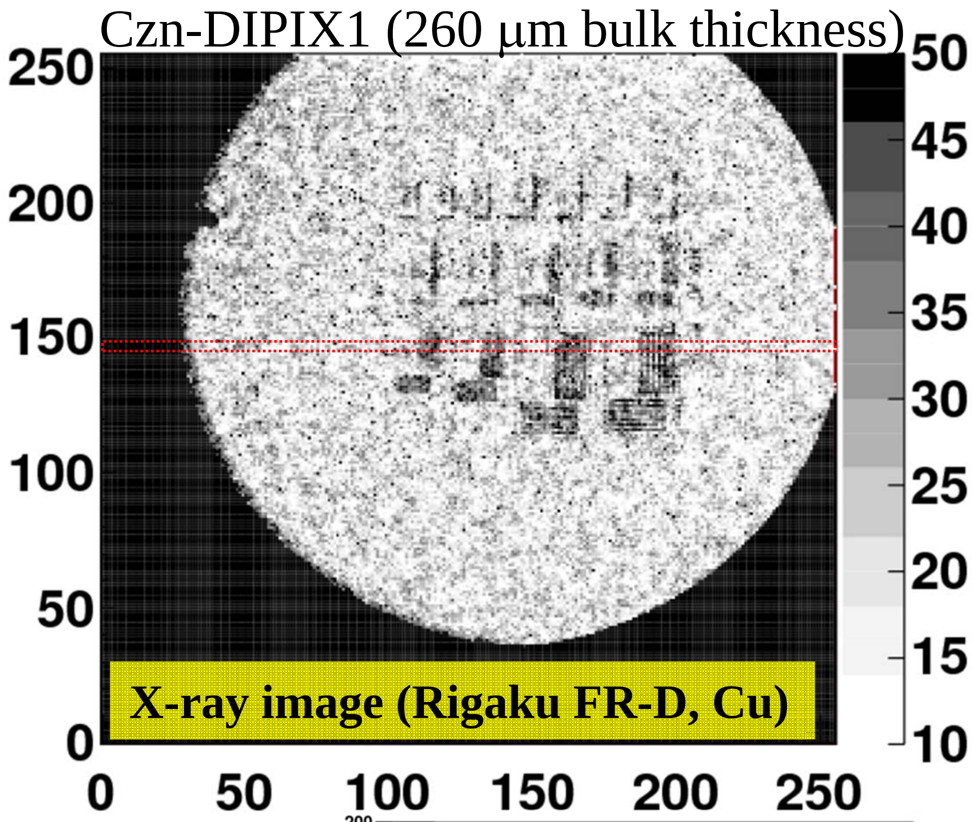
JIMA Micro-chart
(RT RC-02B)
http://www.jima.jp



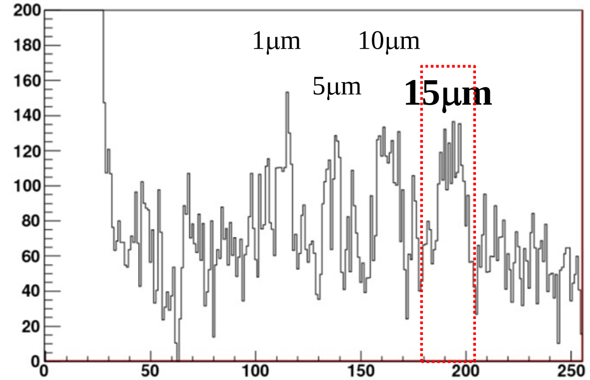
15μm slit x 5 lines

Thickness of Absorption material (W: Tungsten) : 1 μm





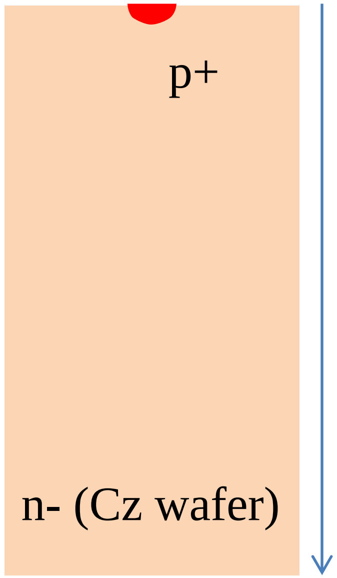
- FR-D 40kV-50mA
- T_{integ}=100μs x 1000 images
- Reverse contrast



RA145-147 line profile

15 μm-slit lines are seen

Progress of SOI pixel detector R&D (3)



-2008

Sensor test with visible light laser
Partial depletion with lower back-bias voltage
Front illumination
Back gate effect problem

2009 -

Introduction of BPW process
Sensor test with IR laser, X-ray and charged particle
Wafer thinning by TAIKO process
- 100µm bulk thickness
- High energy particle detection (MIP detection)
- Reduction of material budget
- Full depletion
- Back illumination

Photo: http://www.disco.co.jp/jp/solution/library/taiko.html

Thinned INTPIX3a evaluation experiment
- Red & IR laser
- High energy particle detection

Sensor response after wafer thinning

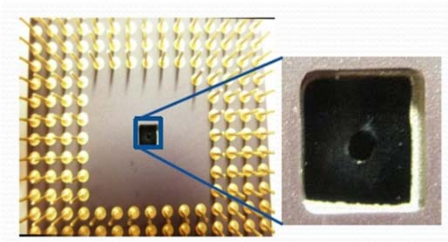
Front (IR) & back (red) illumination experiment

Univ. of Tsukuba

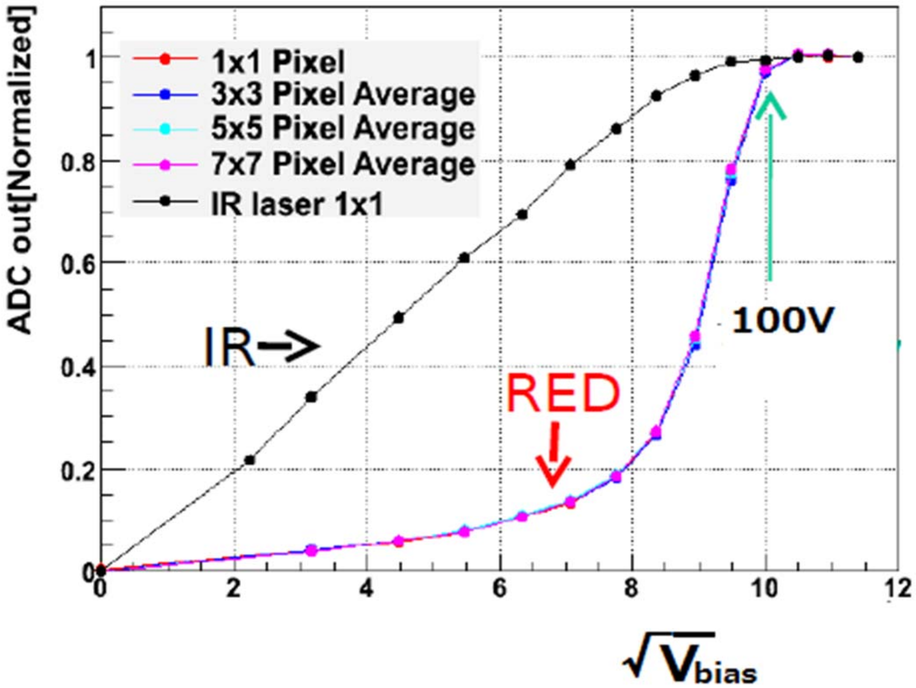
100 μm-INTPIX3a
-Integration time = 10 μs
-IR laser focused inside 5μm window
-1064nm IR : 3mm penetration depth

Pixel photo

- Red laser 634nm stops at surface
- Remove aluminum from the back side



Package photo



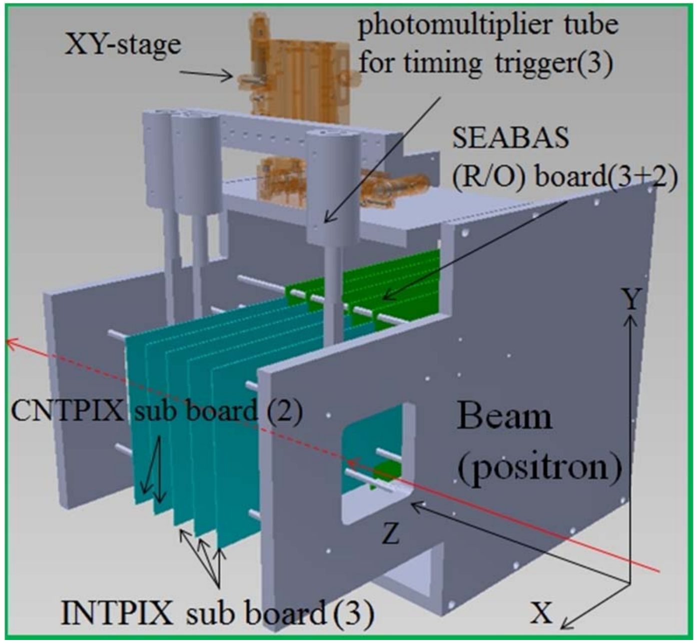
$(V_{bias}=V_{back}-V_{gnd=bias})$

Full depletion at ~100V

High energy particle tracking experiment

2010.9 CERN-SPS preliminary experiment with pion beam
<u>2010.9-10 Tohoku-LNS electron beam tracking experiment</u>
2011.10 CERN-SPS beam tracking experiment (scheduled)

Tohoku Univ.
Univ. of Tsukuba
Osaka Univ.

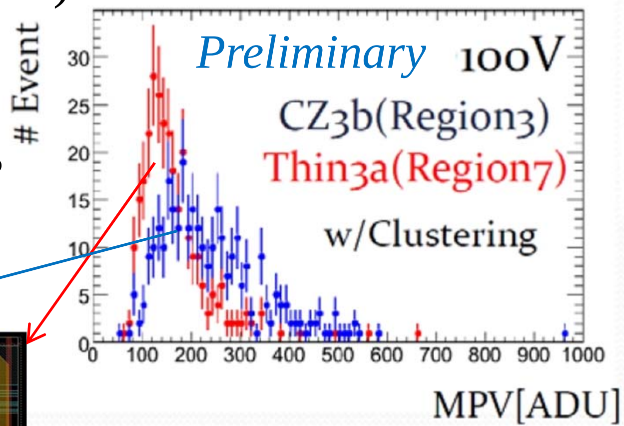


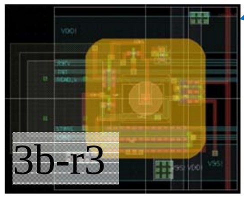
Tohoku LNS setup

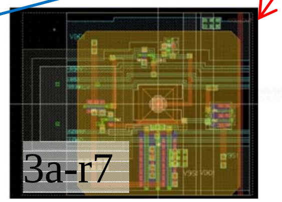
Positron beam energy
= 673 MeV

MIP distribution

- Peak position depends on the gain (BPW size)
- SNR > 20

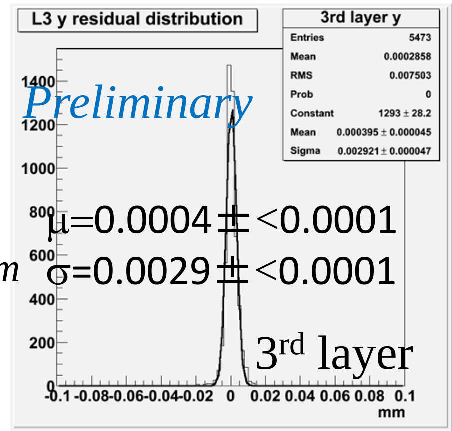






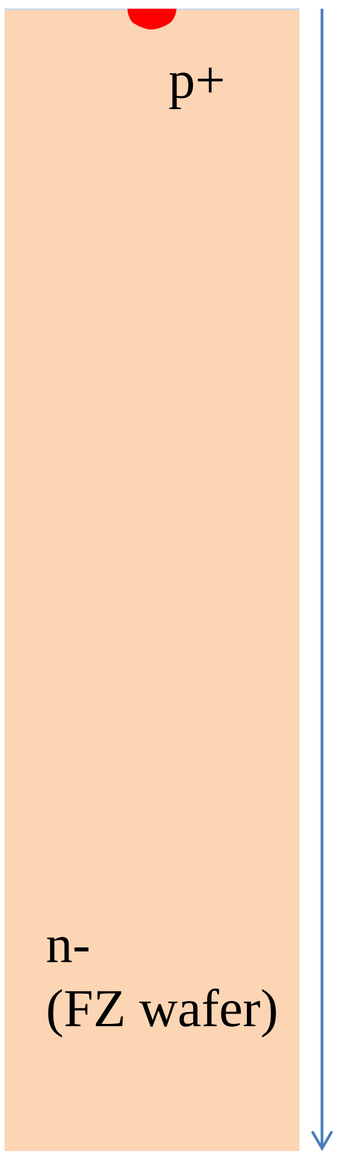
Tracking results

Position resolution 2.9-7.6 μm [rms] for 3 layers
Binary resolution [rms] $\frac{20}{\sqrt{12}} \sim 5.8\mu m$ is corresponding to experimental results



We had achieved the first high-energy particle tracking with KEK-SOI detector

Progress of SOI pixel detector R&D (4)



260µm
@~30V
or
500µm
@~100V

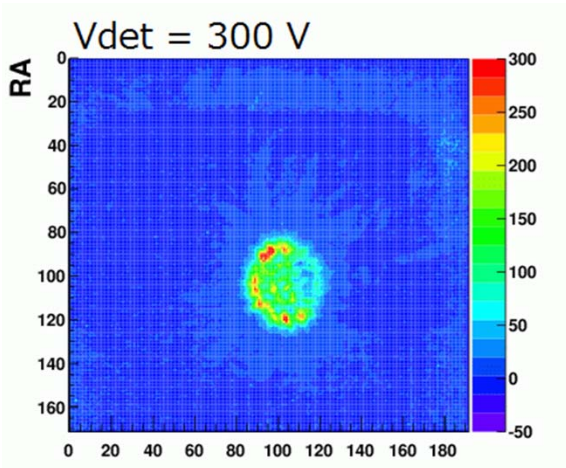
-2008
Sensor test with visible light laser
Partial depletion with lower back-bias voltage
Front illumination
Back gate effect problem

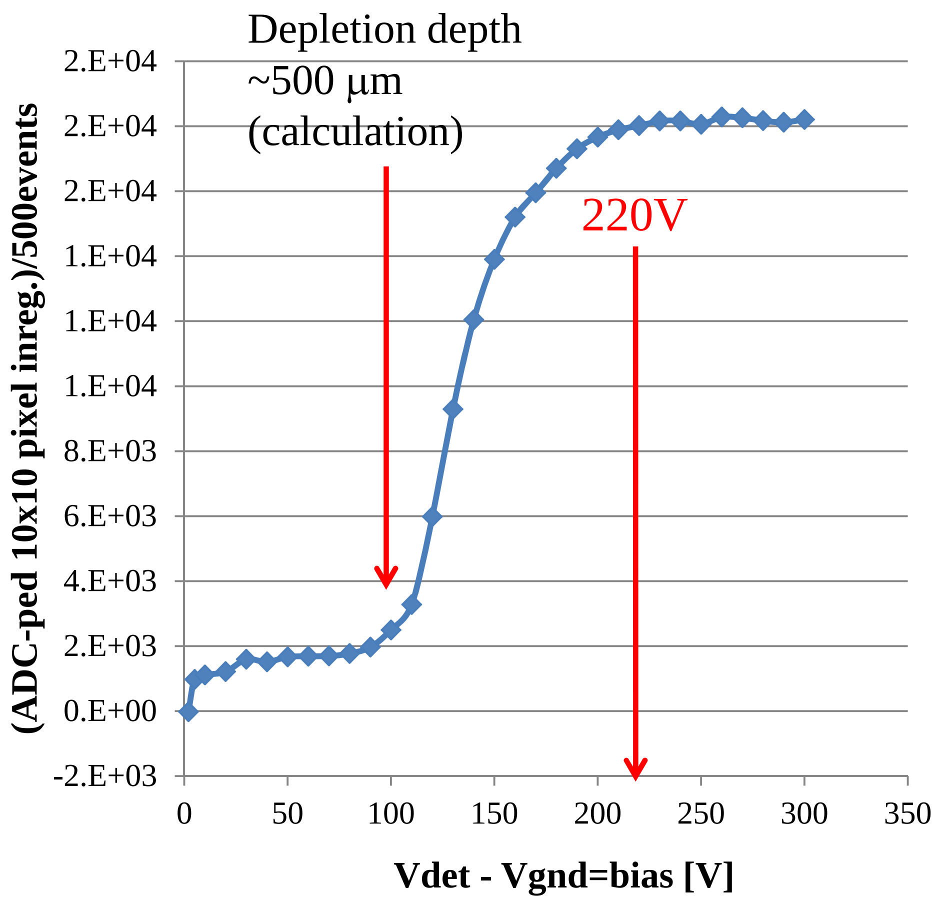
2009 -
Introduction of BPW process
Sensor test with IR laser, X-ray and charged particle
Partial depletion with higher back-bias voltage
Front illumination

2010 -
Introduction of FZ wafer
Sensor test with IR laser, X-ray and charged particle
Full depletion with lower back-bias voltage
Back illumination

FZn-INTPIX3e back illumination experiment

SOI sensor chip : FZn-INTPIX3e
- Resistivity ~8kΩ cm
- Bulk thickness 500 μm
- The back side open (3.1 x 3.1 mm)





Red laser was illuminated
from the back side
Red laser absorption ~ a few μm
1mmϕ Al collimator was used

The sensor is fully depleted > 220V

Improvement of the back-side process is required to reach plateau earlier

Full depletion at ~30V with 260 μm sensor is also confirmed

→ S. Nakashima's talk ID=348

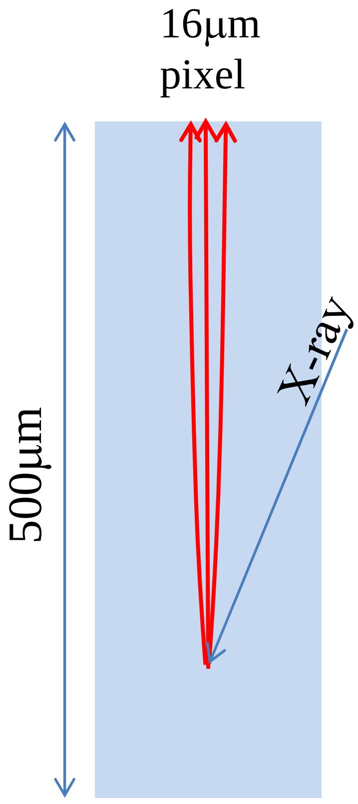
Charge sharing correction

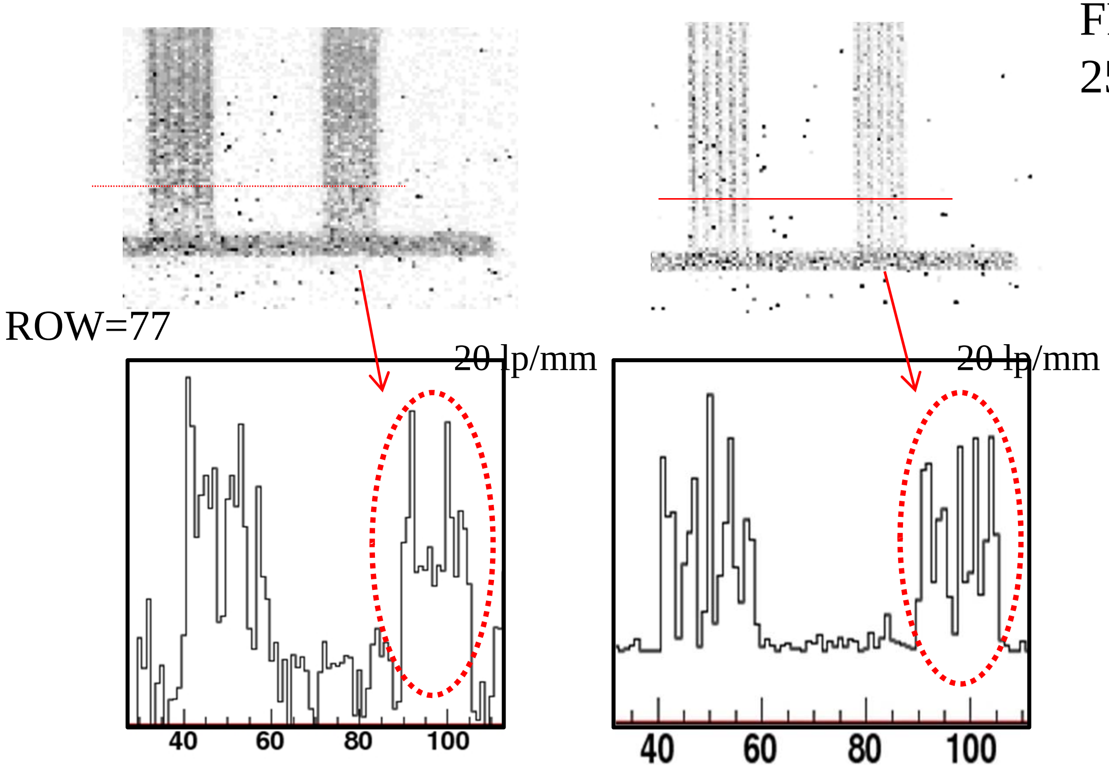
FZn-INTPIX3e

Pixel size 16 μm vs. 500 μm thickness → charge sharing increases

Charge sharing correction --- 3x3 clustering

FZn-INTPIX3e bias voltage 80 V (Vdet, partial depletion)
X-ray test chart images
(FR-D Cu target X-ray generator)





FR-D(Cu)
25 kV – 20 mA

Slit material
Pb 30 μm

After the correction, 20 lp/mm slit is clearly seen

Progress of SOI pixel detector R&D (5)

260µm
@~30V
or
500µm
@~100V

-2008

- Sensor test with visible light laser
- Partial depletion with lower back-bias voltage
- Front illumination
- Back gate effect problem

2009 -

- Introduction of BPW process
- Sensor test with IR laser, X-ray and charged particle
- Partial depletion with higher back-bias voltage
- Front illumination
- **We don't know what happens at the back side**

2010 -

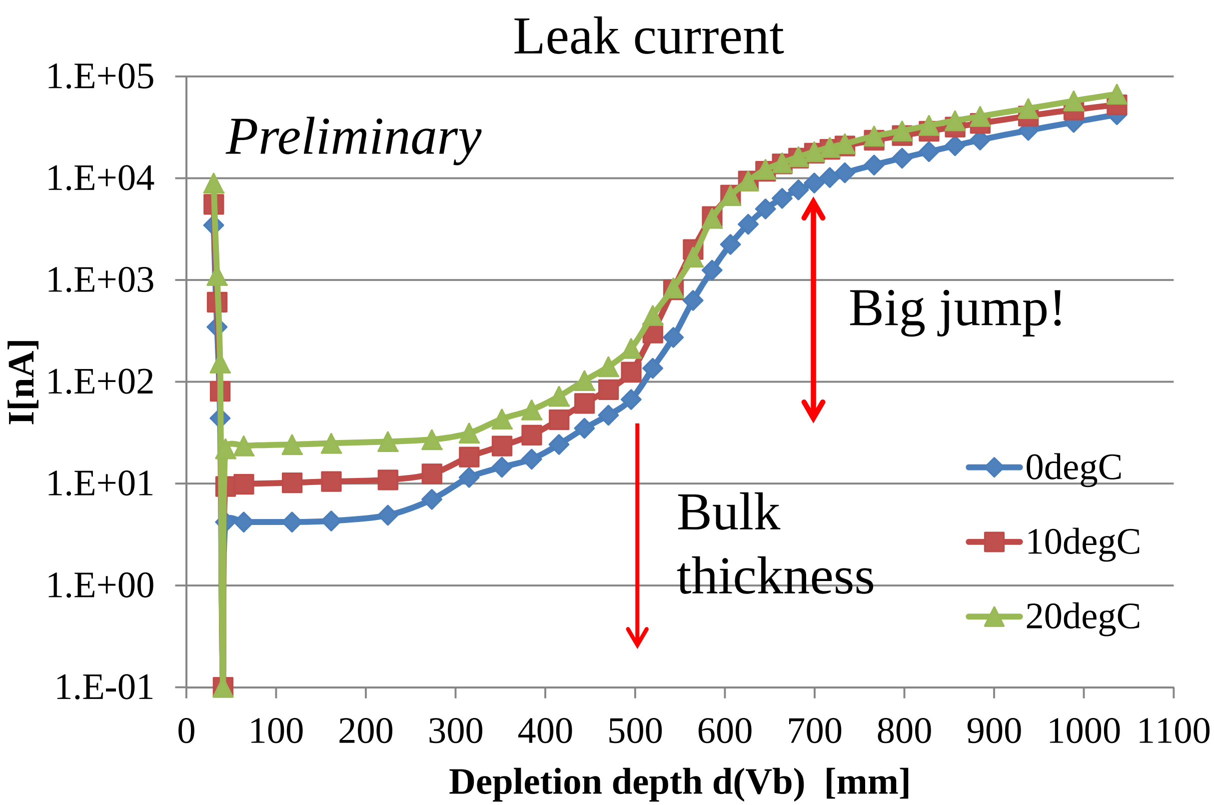
- Introduction of FZ wafer
- Sensor test with IR laser, X-ray and charged particle
- Full depletion with lower back-bias voltages
- Back illumination
- **We realized that proper back-side processes are required**

Current issue : Back-side process

Chip: FZn- INTPIX3e
a package for back illumination

CMP was applied at the back side

The chip was set in thermostat chambers



d: depletion depth as a function of back-bias voltage assuming very large bulk thickness

$$d(V_b) = \sqrt{\frac{2\varepsilon}{qN_d}(\varphi_B + V_b)}$$

N_d: n- side dope density
φ_B: build-in potential
V_b: back-bias voltage (V_{det}-$V_{bias=gnd}$)
q: elementary charge
ε: permittivity
$\rho_n = 1/qN_d\mu_N$: resistivity

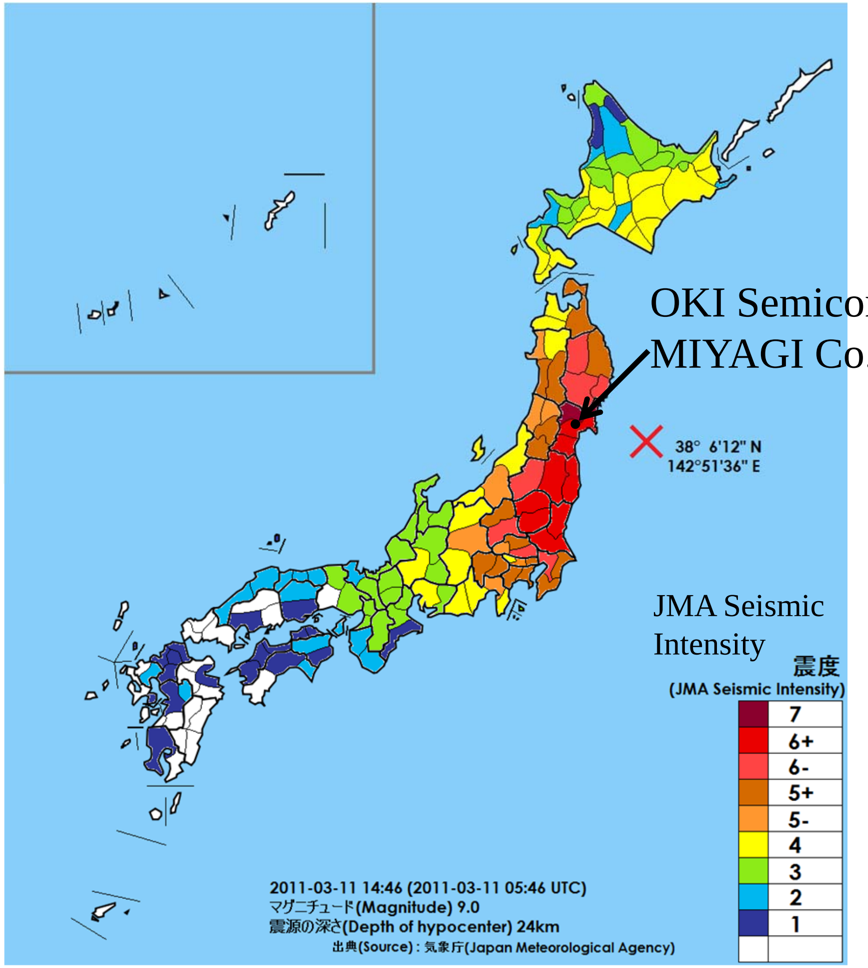
- When applied CMP, pixel dark current decreased at more than full depletion voltage (S. Nakashima's talk ID=348)
- However, there is a big jump in the I-V curve (above)
- **OKI Semi. started the optimization of proper back-side process**

Conclusion

- Thanks to BPW, higher back-bias voltage can be applied and therefore we started evaluation of SOI pixel detectors with spatial resolution, sensor gain and response to X-ray and high energy particles.
- Applying FZ wafer, SOI pixel detectors became operated with full depletion voltage
- A current issue is back-side process and OKI Semi. started the optimization of the back-side process.
- The SOI pixel detector R&D will move to application studies.

The next slide is the final one…

Schedule



- A large-scale earthquake occurred in Miyagi Prefecture at 2:46 PM on March 11th, 2011.
- No personal suffering and no large scale damage to the OKI Semiconductor Miyagi facilities have been observed
- Operations recommenced mid. of April, and therefore the delay of FY10-2 MPW run will be only 2 months!

FY10-2 MPW process: will complete hopefully in June 2011.
FY11 MPW run deadline: Oct. 3rd.

For further information, please attend 3D satellite meeting tomorrow, 16:25-16:50