Chicago Hawaii ASIC, Multi-Purpose [CHAMP] Overview

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Outline

- Chicago Designs:
  - VCDLs w/ delay locked loops (DLLs)
    - "Slow" (18 GHz)
    - "Fast" (25 GHz)
  - VCROs + counters
    - "Slow" (3 GHz)
    - "Fast" (4 GHz)
  - Independent DLL structure
- Hawaii Designs:
  - Digital-to-Analog Converter (DAC)
  - Analog Storage Cells with built in comparator
  - Voltage Controlled Delay Line (VCDL) (x2)
  - Voltage Controlled Ring Oscillator (VCRO)
  - Waveform sampler arrays (WFS) (x4)
  - D Flip Flops
  - LVDS receiver
  - Charge Sensitive Amplifier (CSA)

Discussed here.

Background

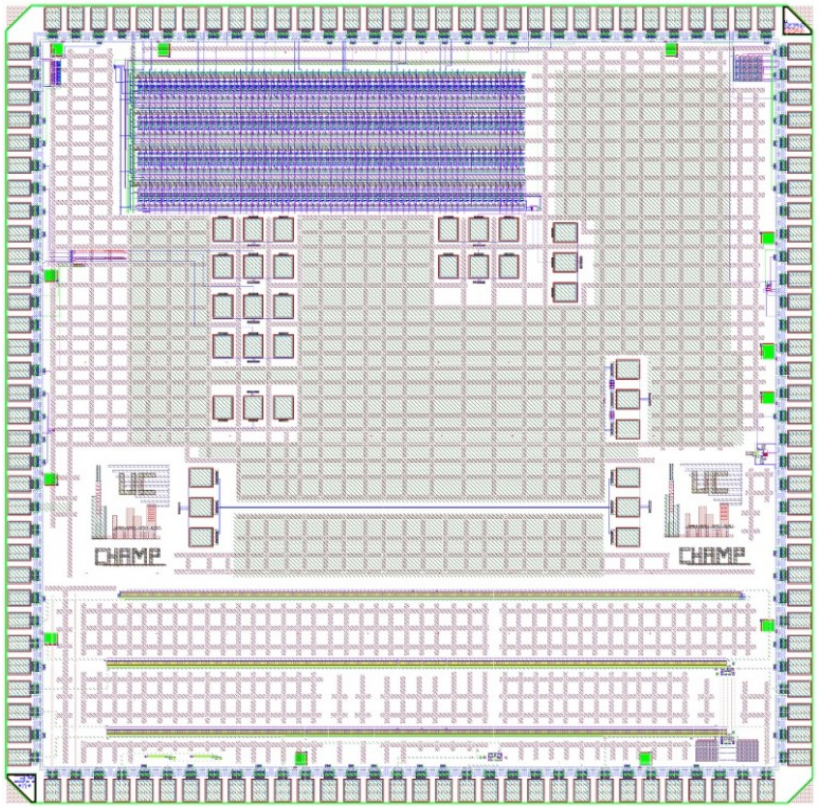
- CHAMP ASIC
  - Joint U. of Chicago and U. of Hawaii test structure submission
  - Lays groundwork for future submissions
- Process: IBM CMOS 8RF-DM 130nm
- First time in Hawaii using IBM process
- First time ASIC submission for most designers in Hawaii

Motivation

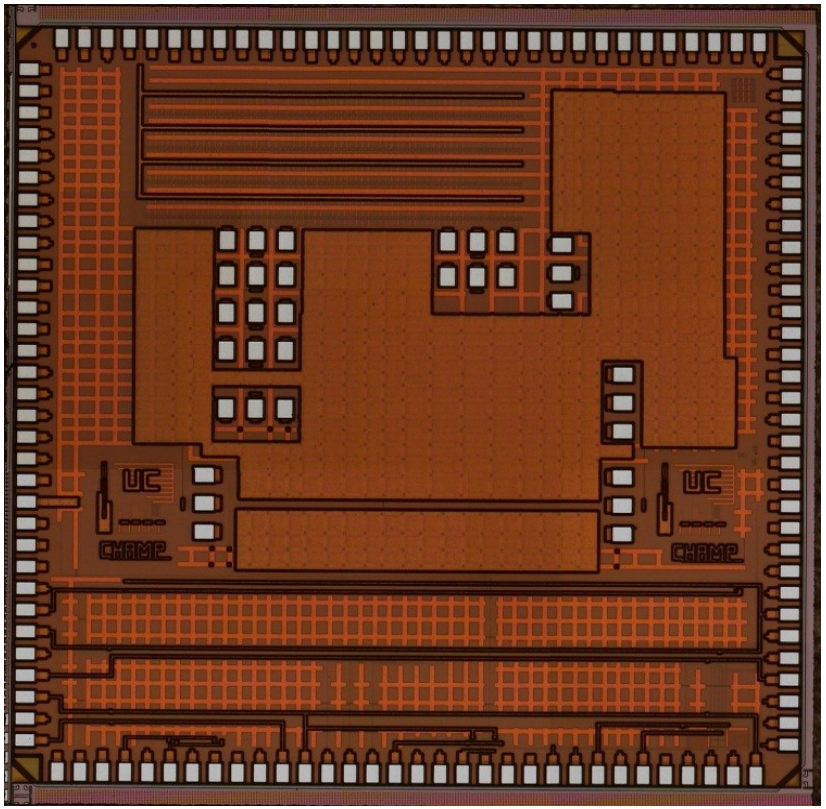
- Part of the Large Area Picosecond Photo-Detectors Project (LAPPD)
- Goal:
  - Measure time-of-arrival of relativistic particles with 1 pico-second resolution
- Requires high speed electronics

CHAMP Submission

- Submitted via CERN MPW May 2010
  - First die received Feb. 14, 2011



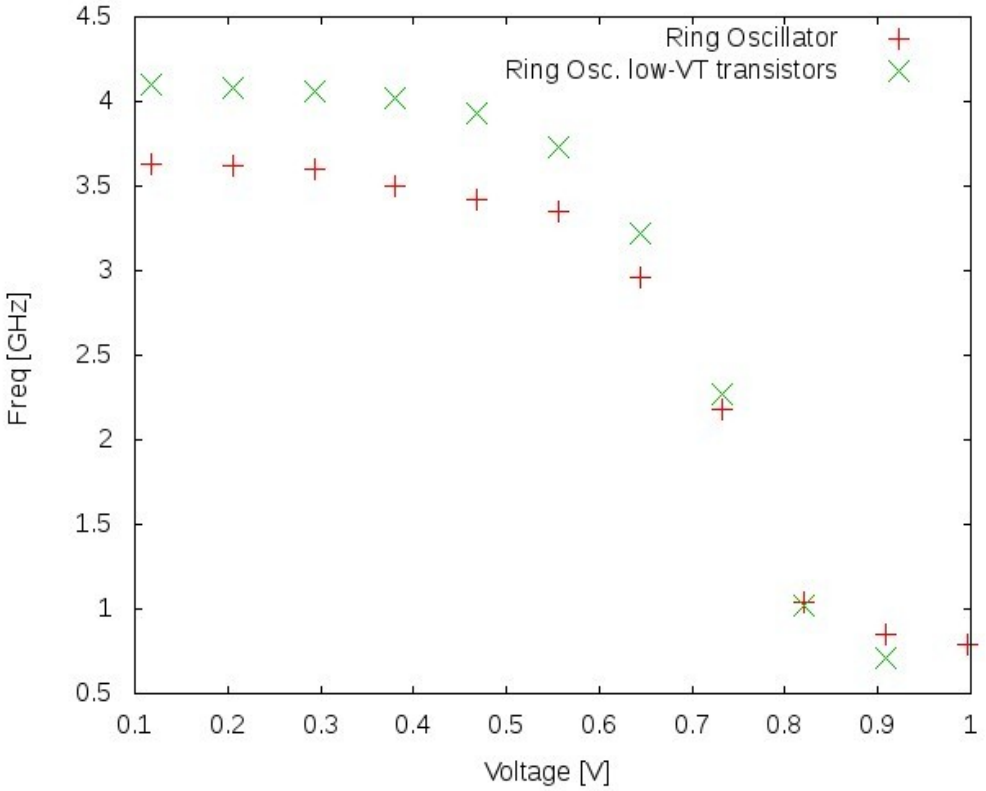
CHAMP Layout View.



CHAMP Die View. Overall size: 4mm x 4mm

Chicago: VCRO Results

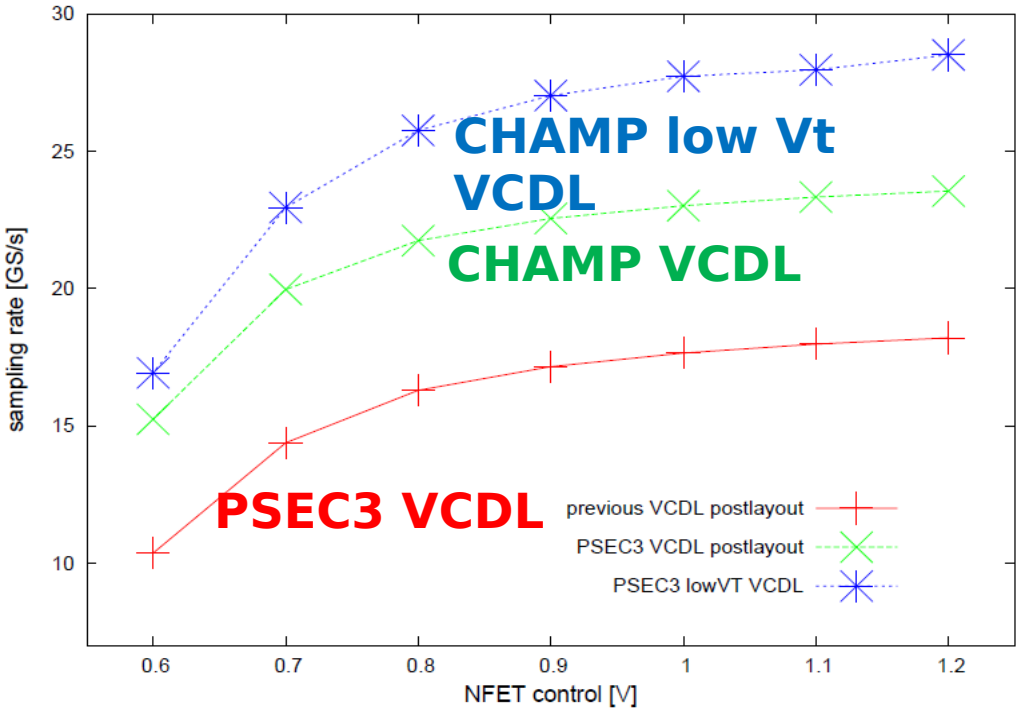
- Many structures tested on the PSEC3
  - Due to long delay in receiving CHAMP
- CHAMP includes faster versions than PSEC3*
  - Including low threshold transistors (green plot)



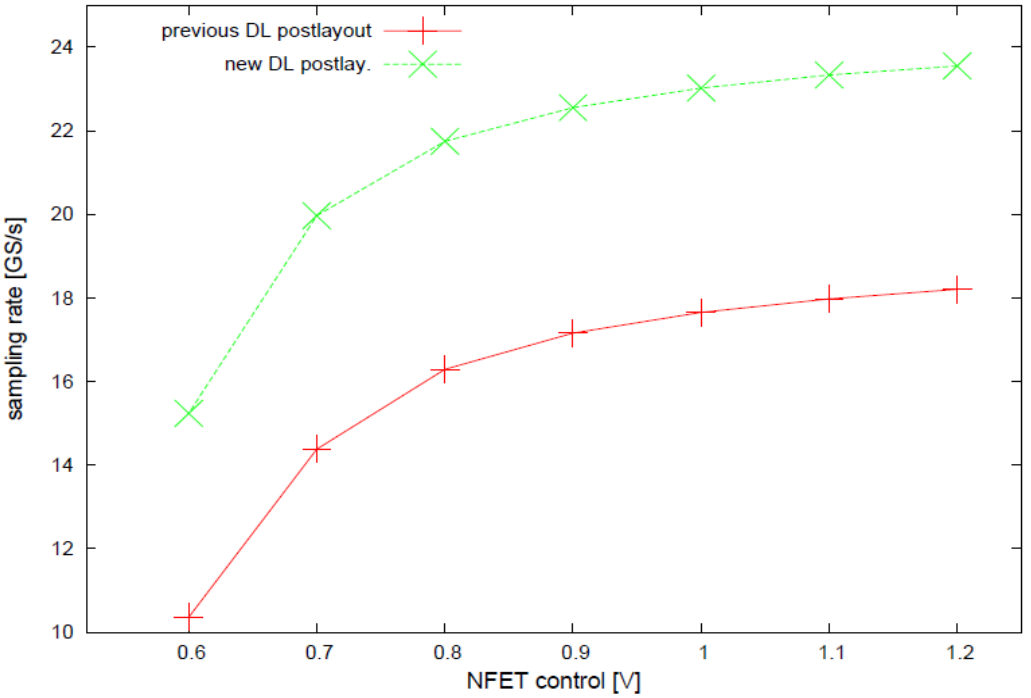
Results from two different ring oscillators.

* PSEC3 talk given during TIPP 2011 by Eric Oberla [ID 219]

Chicago: VCDL Results



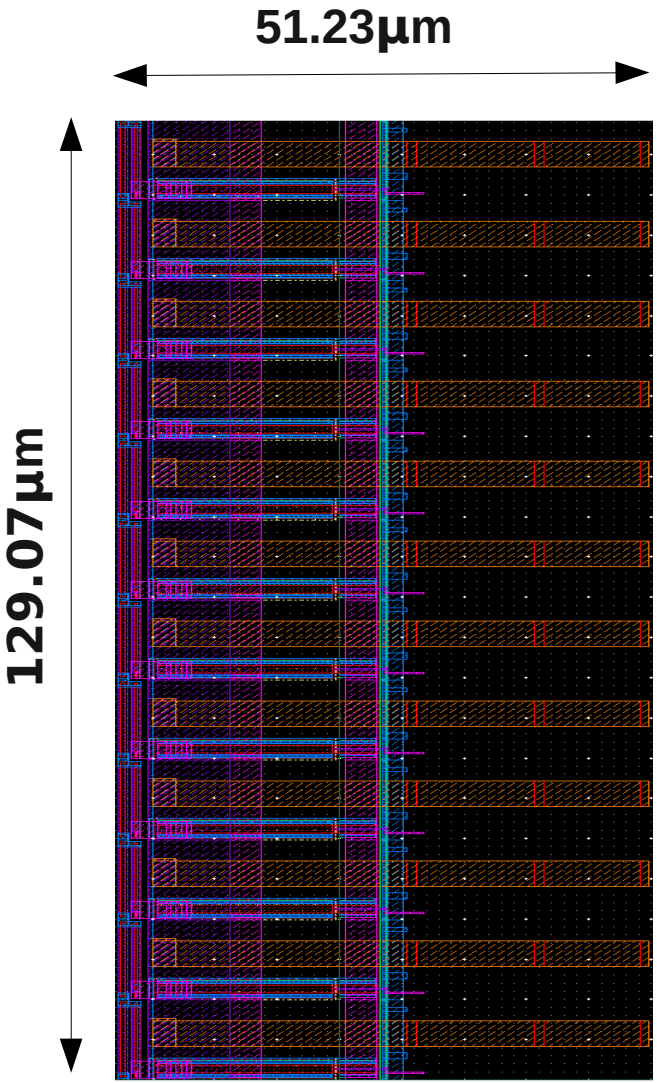
Post layout simulation results for VCDL for the PSEC3 and CHAMP designs.



Post layout simulation results for VCDL with improved simulation technique.

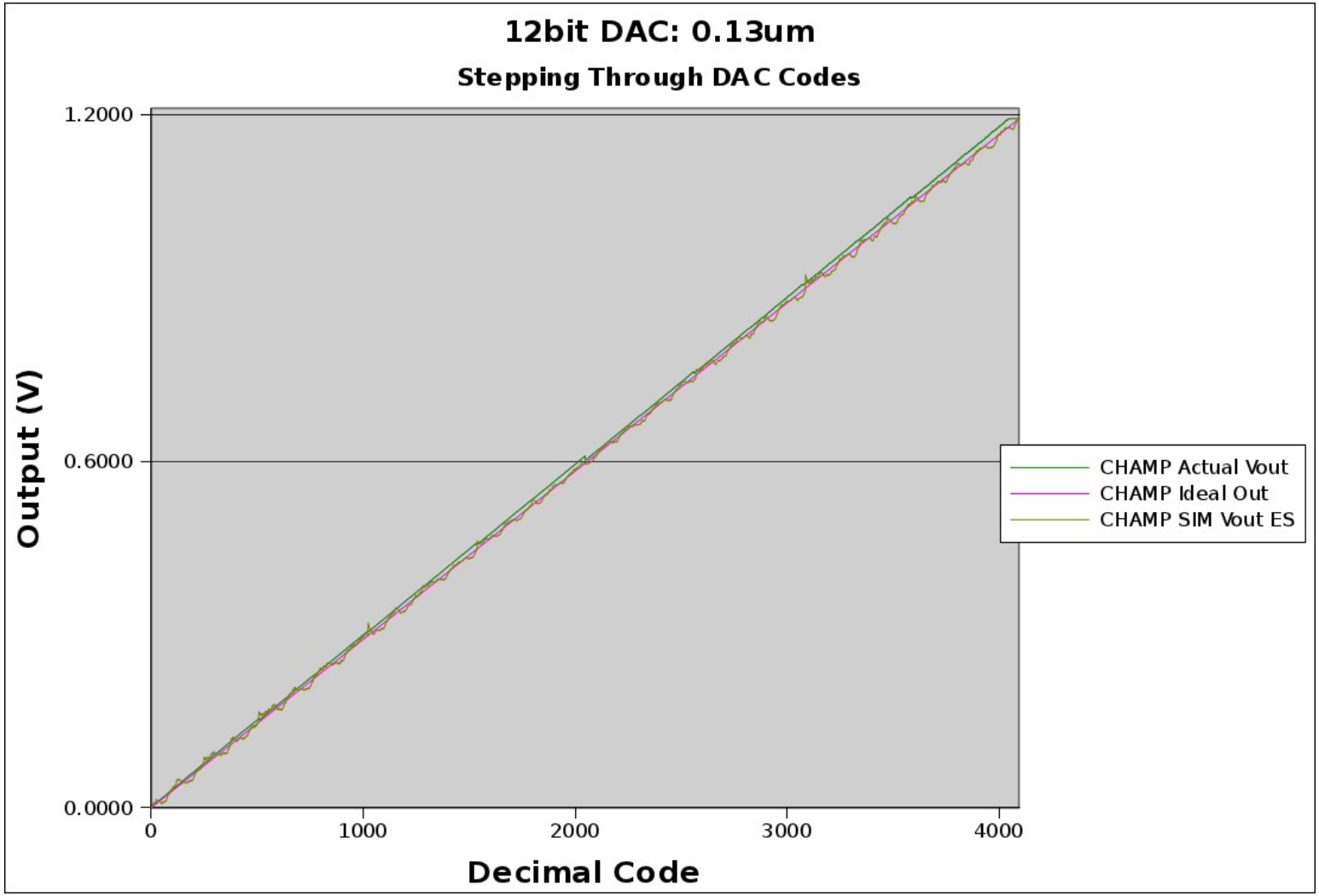
Hawaii: DAC

- Digital to Analog Converter:
  - R/2R design with serial Interface
  - 12 bit resolution
  - 6 external pins



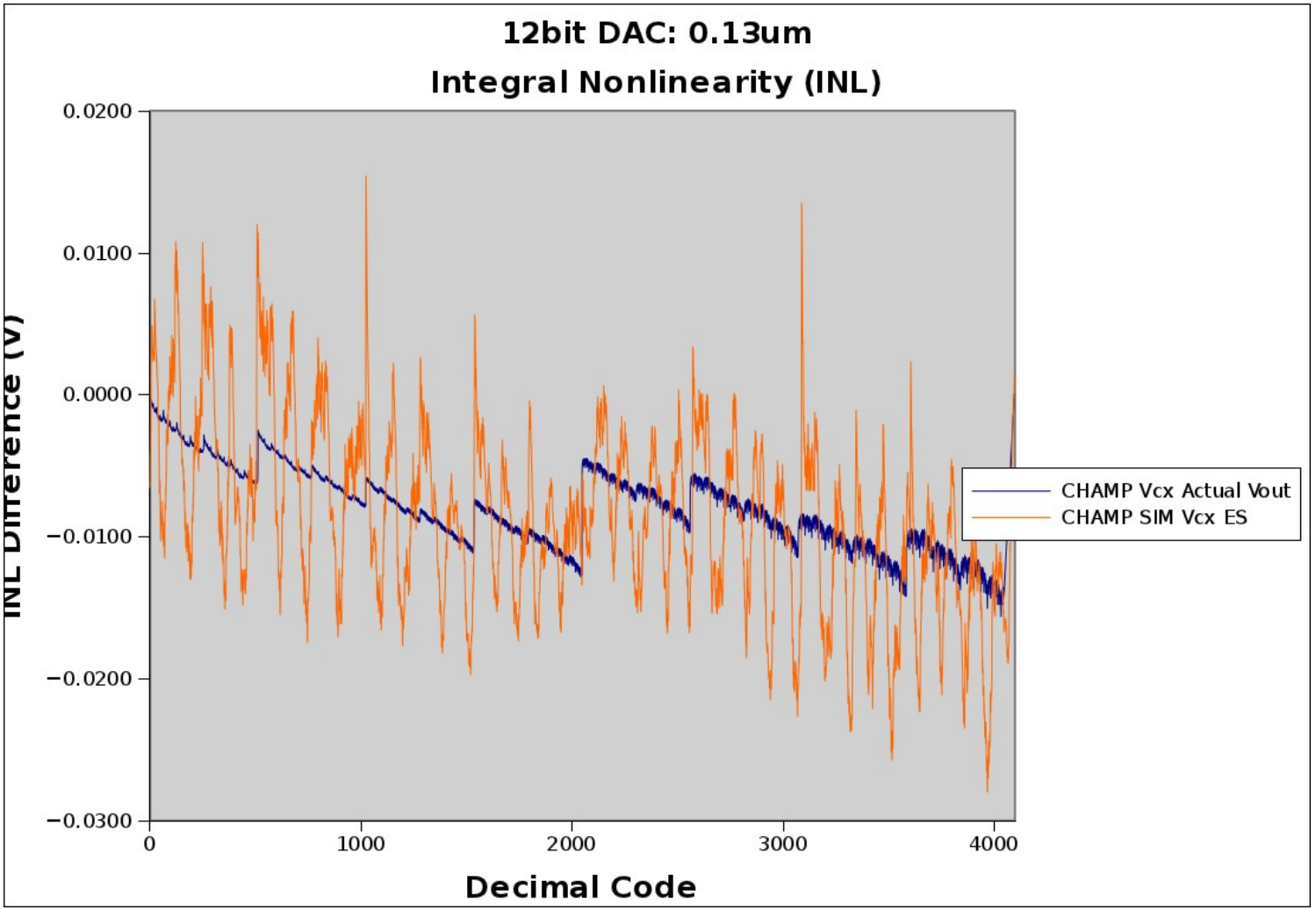
Layout view of 12bit DAC.

DAC: Ideal vs. Simulation Output



Plot for a 12bit CHAMP DAC showing ideal, simulation, and actual outputs. No gaps in output voltage coverage.

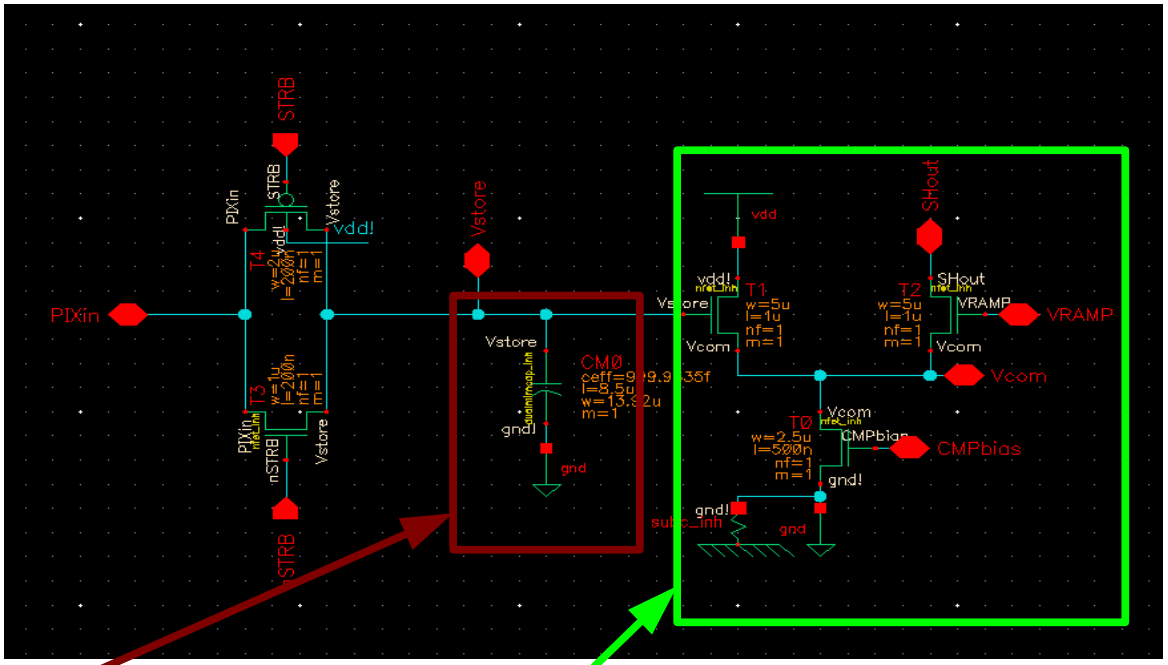
DAC: Nonlinearity



Plot for a 12bit CHAMP DAC showing integral nonlinearity. LSB = 0.29mV

Hawaii: Analog Storage Cells with built in comparator

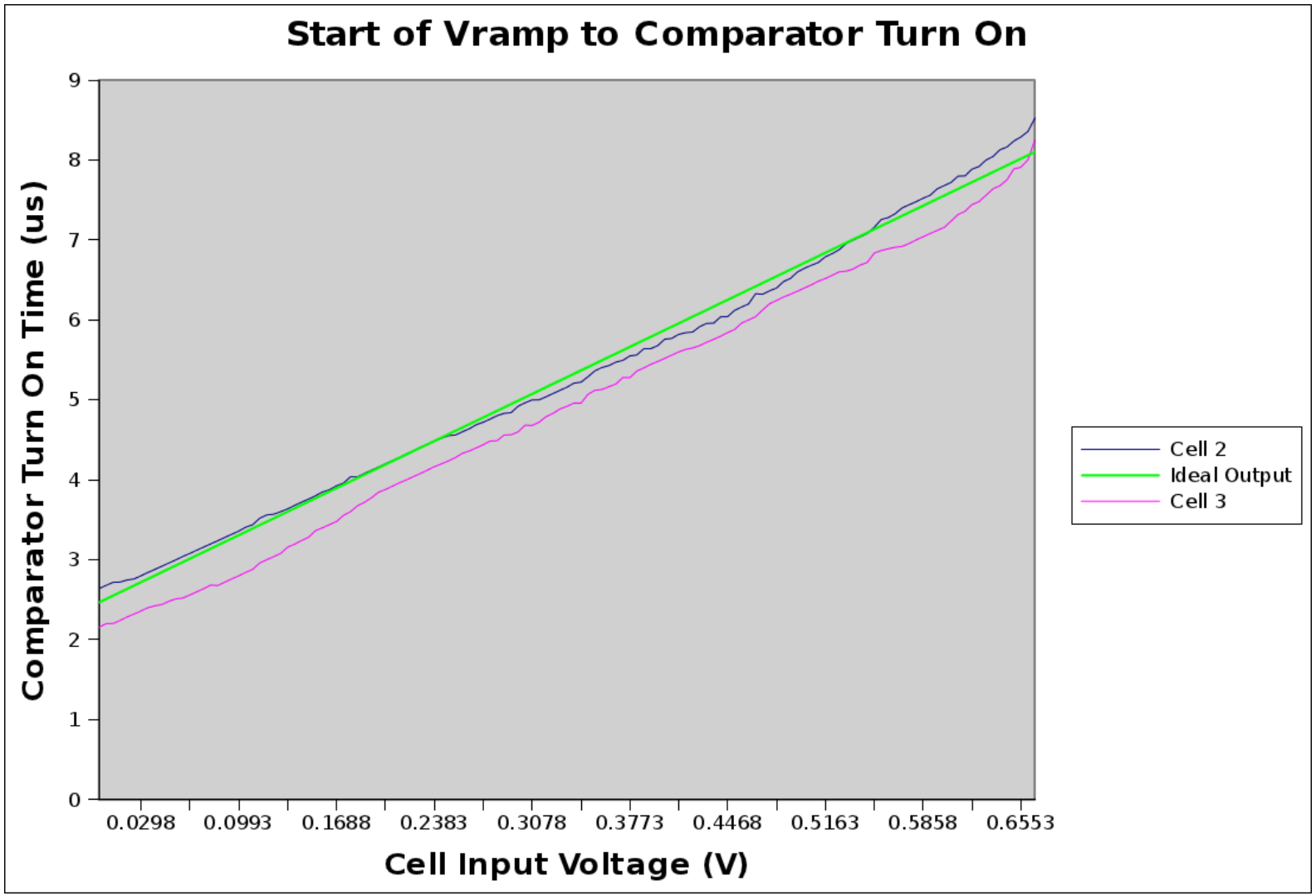
- Designed to minimize effects of large leakage currents in the 130nm CMOS process.
- Uses large storage capacitor (1pF).
- 138.11 um by 135.33 um
  - Includes address decoding
- Could be used for deep storage in a future waveform ASIC



Storage capacitor

Differential pair comparator

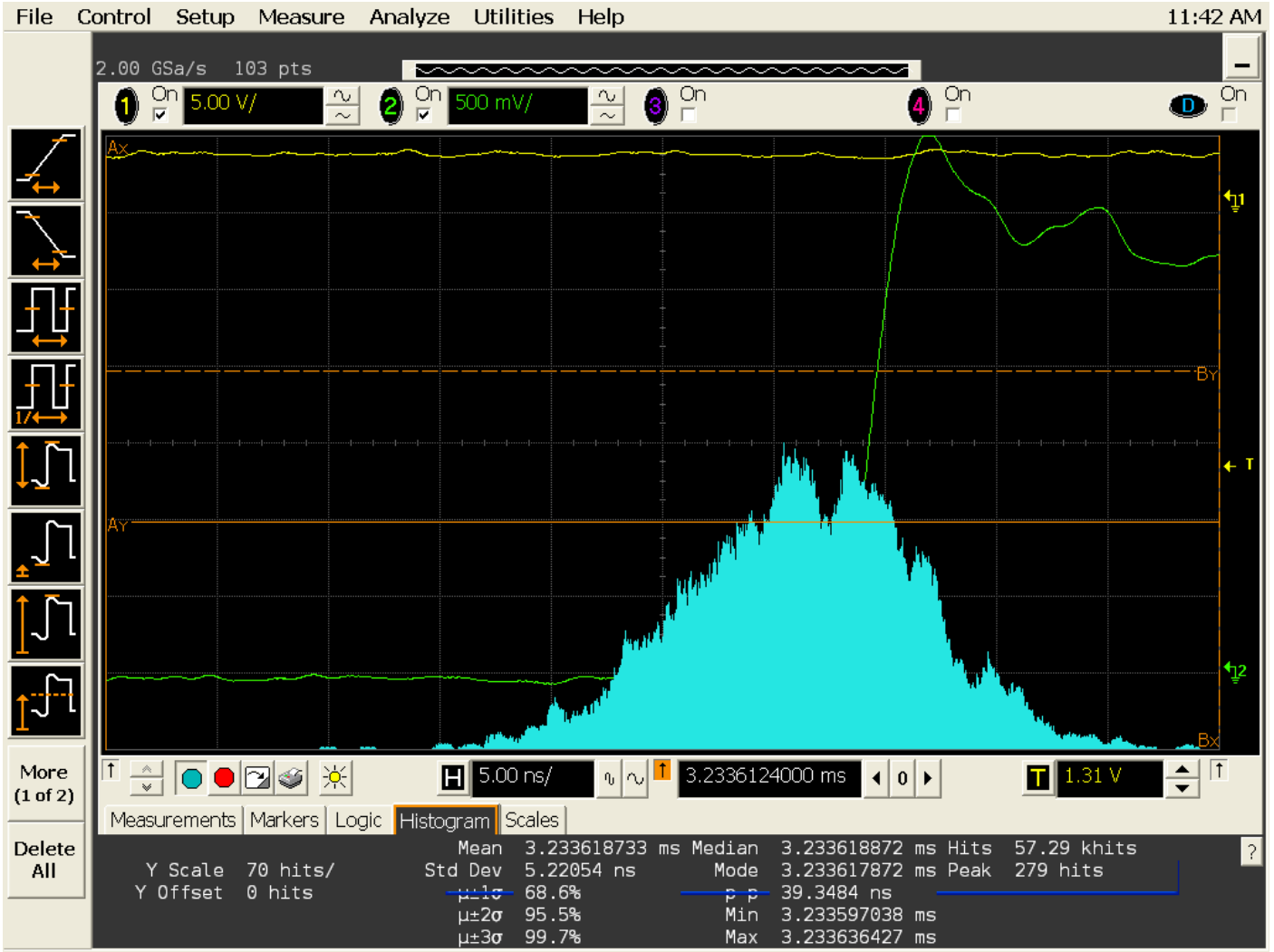
Storage Cell Linearity Test



Plotting the cell input voltage vs the time the comparator fires in relation to Vramp. Data taken from the scope.

Noise (RMS)

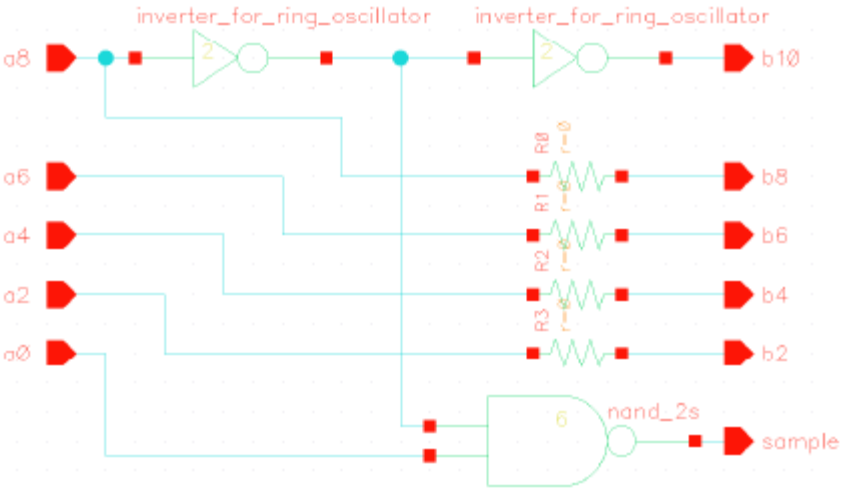
- Measured noise
  - ~1.0mV +/- 0.1mV variation between cells

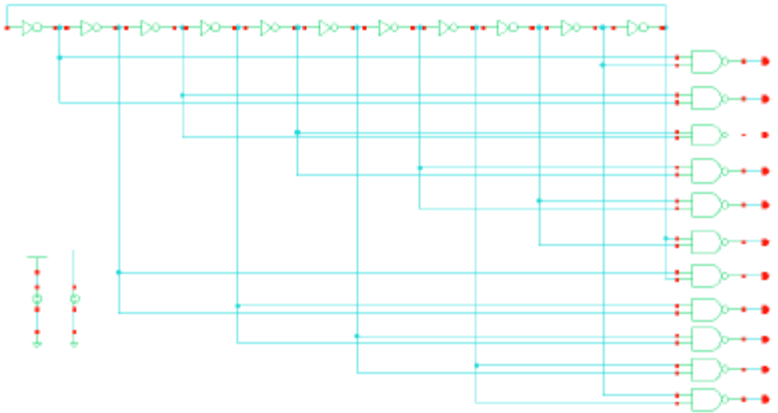


Jitter on comparator output edge, measuring noise (5.23ns)

Hawaii: Voltage Controlled Delay Lines

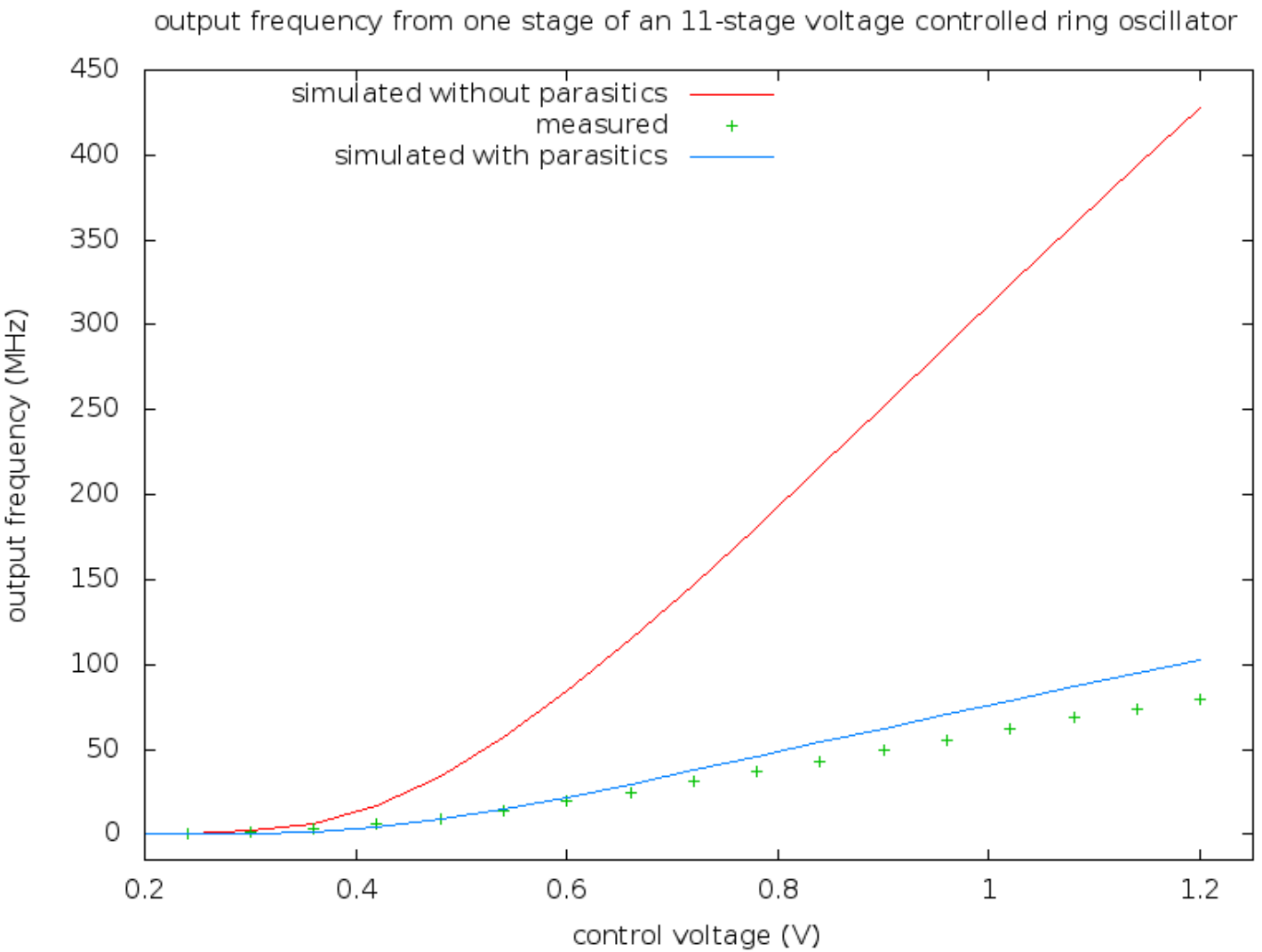
- Two delay lines
  - 64 stages with 9 stage delay
    - One delay line uses normal voltage FETs
    - One delay line uses low voltage FETs
- One ring oscillator
  - 11 stages with 9 stage delay
  - Several GHz in simulation (No parasitics)





Control logic for VCDL

VCRO: Result



Simulations are almost useless for quantitative predictions without parasitics.

Waveform Sampling Arrays

Four sampling arrays to explore high analog bandwidth sampling, compare simulated / measured bandwidth.

Simulated bandwidths (approximate): **1.8, 2.2, 2.6, 4.2 GHz**

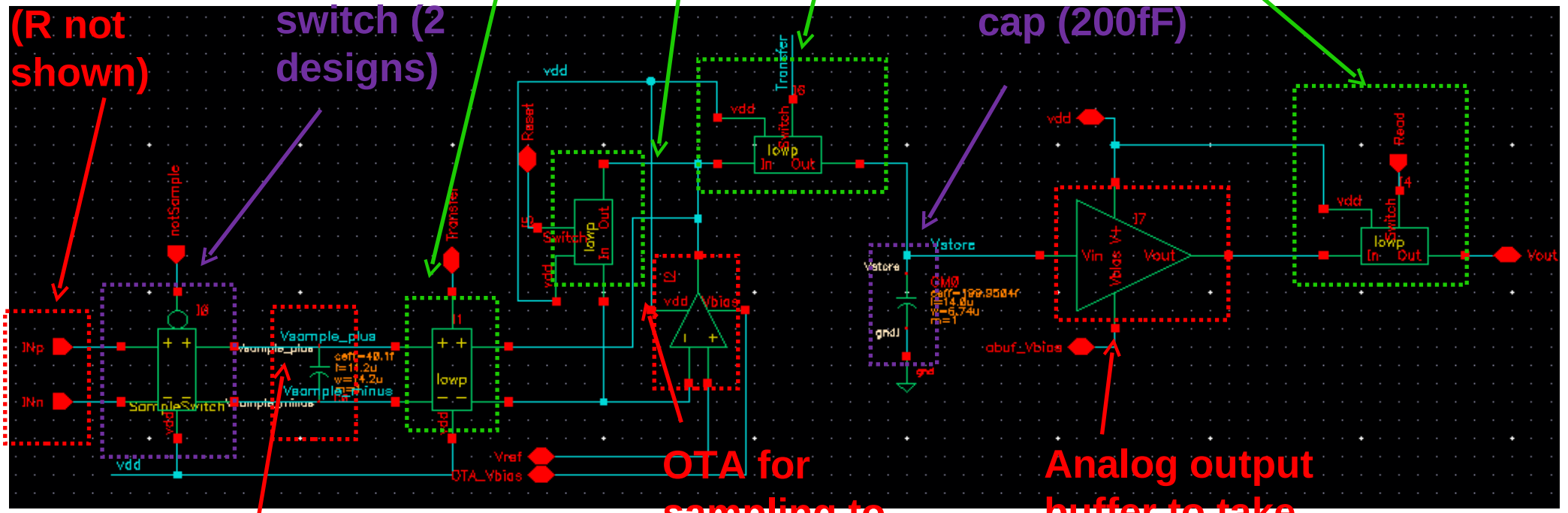
Each sampling cell consists of 64 of the following basic cell:

Inputs, 50 Ω terminated (R not shown)

Differential sampling switch (2 designs)

Transfer / reset / read switches (low power)

Storage cap (200fF)

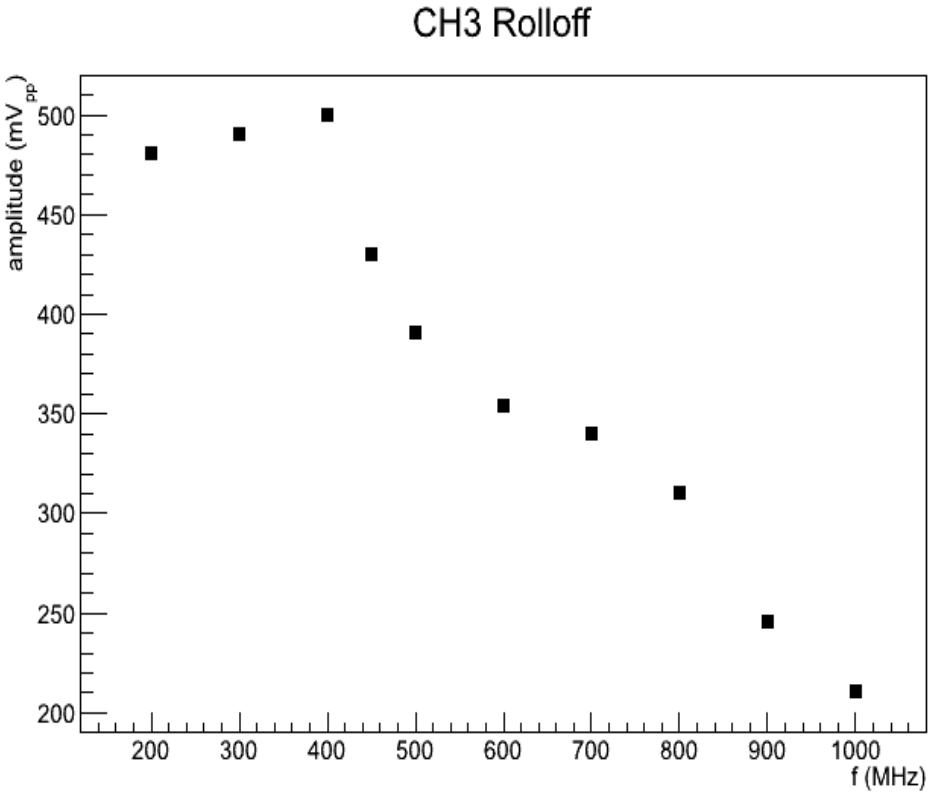


Sample cap (20,30,40 fF)

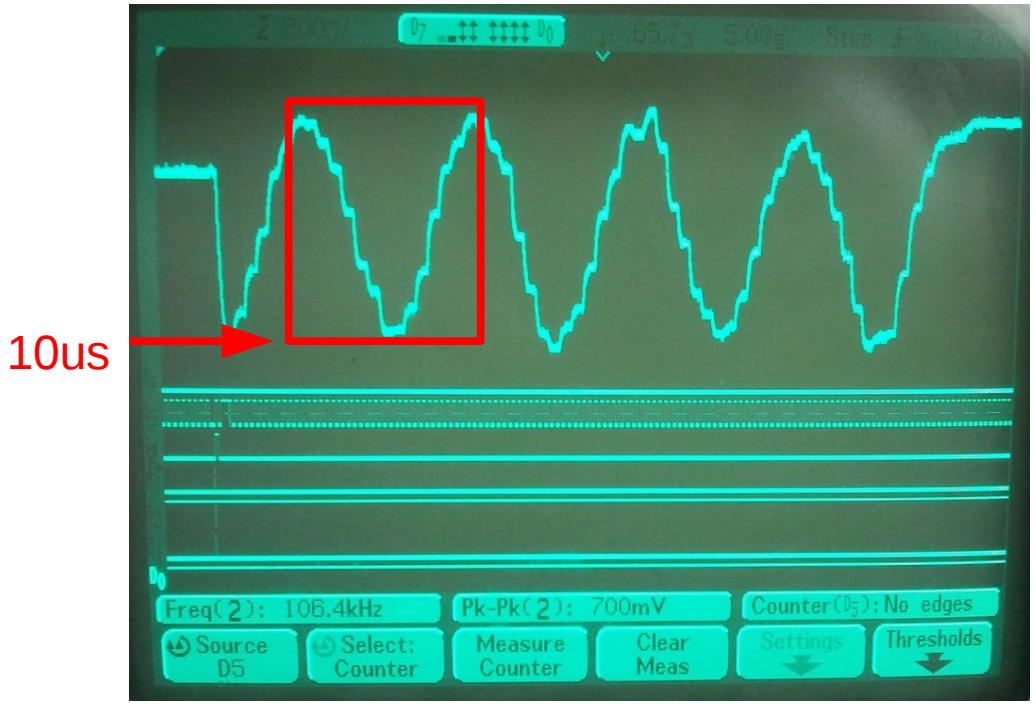
OTA for sampling to storage transfer

Analog output buffer to take stored V off-chip for reading

Waveform Sampler: Results



Measured rolloff response of channel 3 of the sampling array.



Analog voltage output with 100MHz sine wave input. The input and output are analog voltages, so each step is quantized in time, hence the apparent steps.

- Initial results indicate bandwidth is comparable to PSEC3. Testing is ongoing.

Conclusion

- CHAMP submission in IBM 130nm lays groundwork for future designs
  - Sampling capability
  - Trim DACs for bias control
    - Used in two other ASIC designs already
- Confirm independent versions of structures that were similar or identical to PSEC3
  - Useful for characterization and independent debugging
- First ASIC design experience for 4 Hawaii students
  - More student involvement for future designs