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Multipurpose Test Structures and Process Characterization using 0.13µm CMOS: The CHAMP ASIC.

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As fabrication processes continue to shrink, more and more electronics are able to be integrated on die for various physics experiments. Due to the increasing number of readout channels and required sensitivity of sensors, more dense and fast ASIC elements are required and the fabrication processes must be well understood. To this end, the University of Hawaii in collaboration with the University of Chicago submitted a test ASIC, the CHAMP, composed of a number of discrete test elements on a 0.13µm CMOS process via CERN. This paper describes the structures submitted by UH and UC. Hawaii designs include high speed flip-flops, voltage controlled ring oscillators, an LVDS receiver, a charge sensitive amplifier, a set of four 64-cell waveform samplers with shared input, an analog storage and comparator structure, as well as a 12-bit DAC. The Chicago designs include voltage controlled delay lines, delay locked loops, voltage controlled ring oscillators, transmission lines, and resistors. Each of the structures will be described, with simulation and test results presented. Each of the structures has important applications in future designs as well as helping to characterize the overall fabrication process.

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