A 4-Channel Fast Waveform Sampling ASIC in 130 nm CMOS

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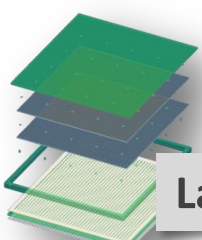
University of Hawai'I

TIPP 2011



Large-Area Picosecond Photo-Detectors (LAPPD) Collaboration

Outline

- LAPPD Detector & electronics integration overview
- Waveform sampling ASIC specs & design
- Results

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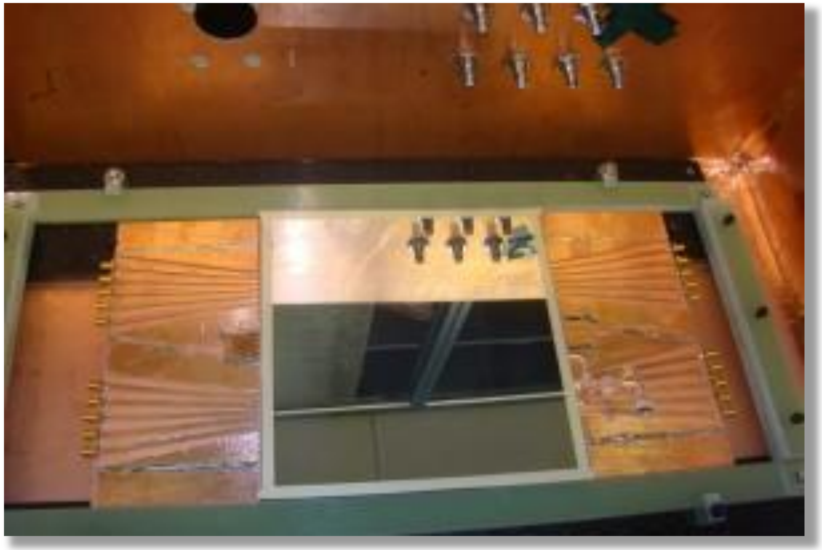
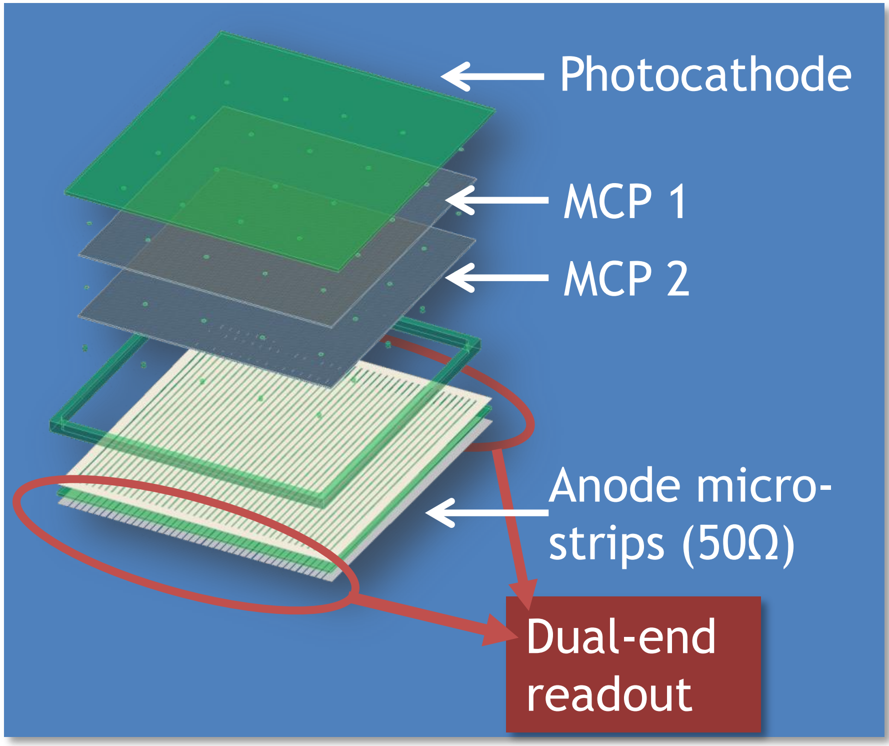


The LAPPD project

- Development of large-area, relatively inexpensive Micro-Channel Plate (MCP) photo-detectors
  - 8” x 8” phototubes = ‘tile’
  - Gain >= 10^6 with two MCP plates
  - Transmission line readout – no pins!
  - Fast pulses + low TTS ~30ps
  - Large active area



The LAPPD project

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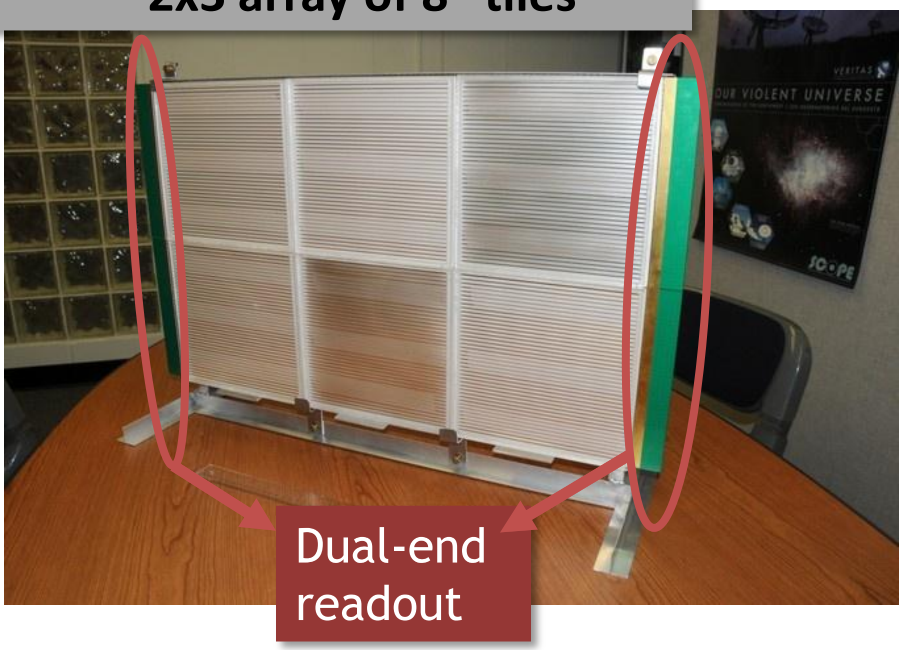
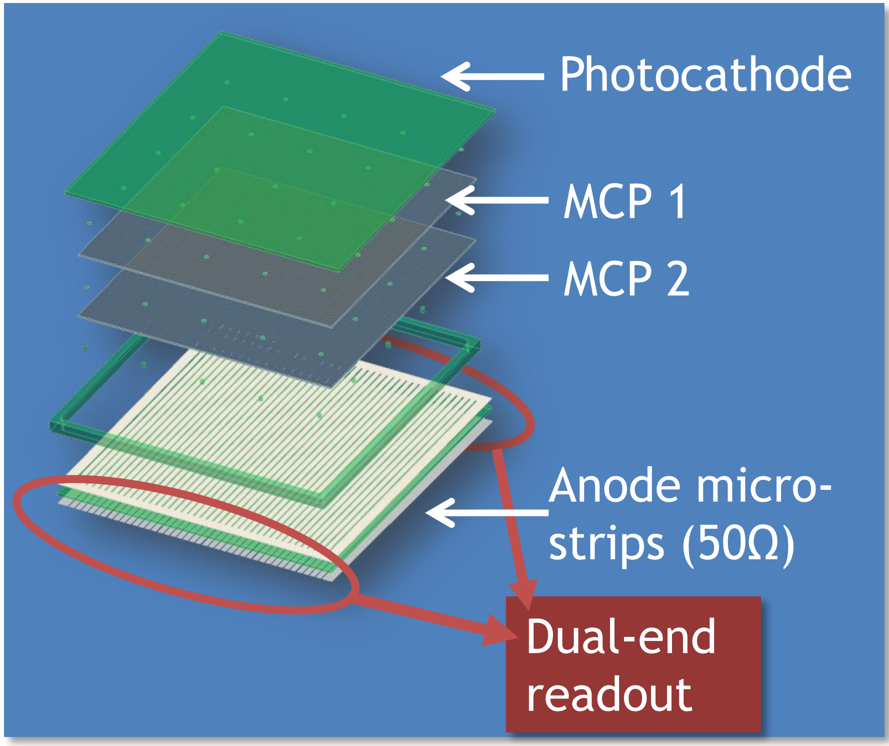
***Much* more: Saturday 4-6pm, Ballroom 9**

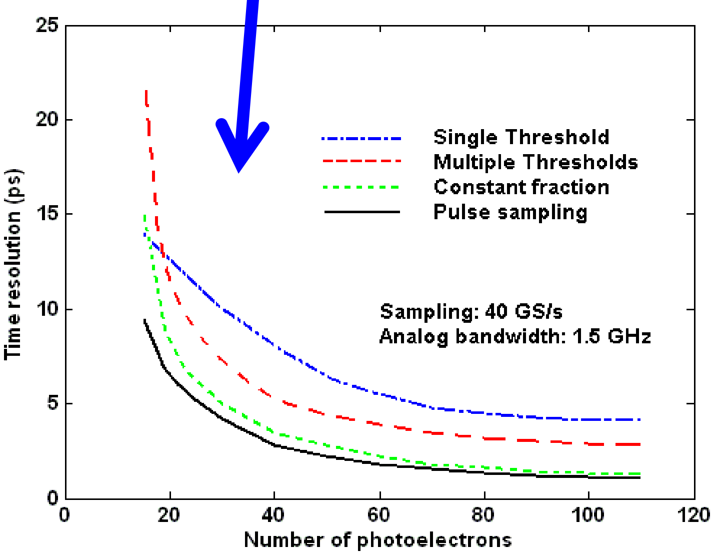
- **“Super Module”:**
  - **2x3 array of 8” tiles**

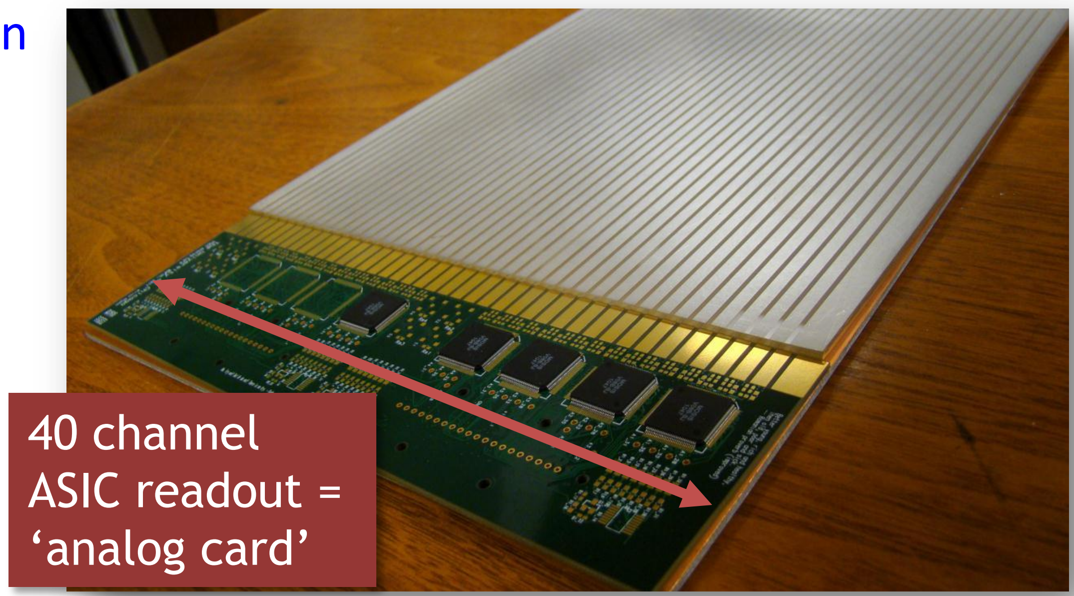




Detector -> Readout integration

- Dual-end 50 Ω Transmission line readout – up to 2 GHz bandwidth
- Waveform sampling ASICs readout both ends
  - → High channel density
  - → Low power
  - → Preserve timing information





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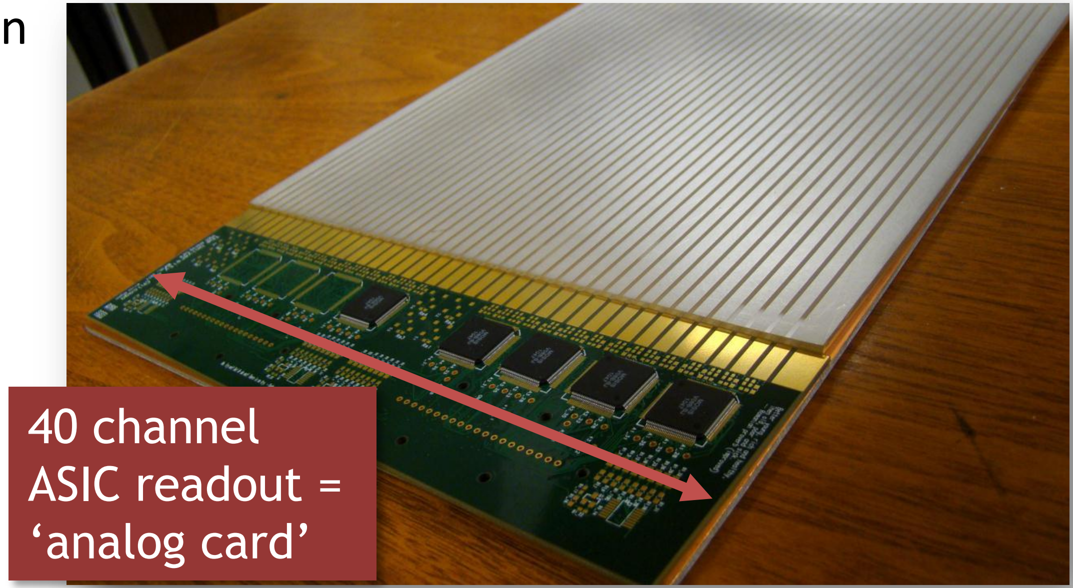
Can we push certain limitations on current waveform sampling ASICs? *(i.e. sampling rate)*

→ ***130 nm CMOS***



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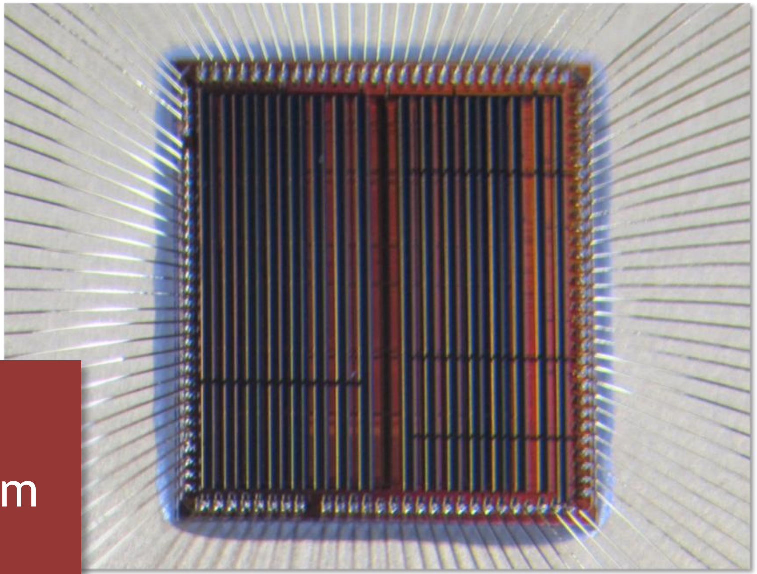
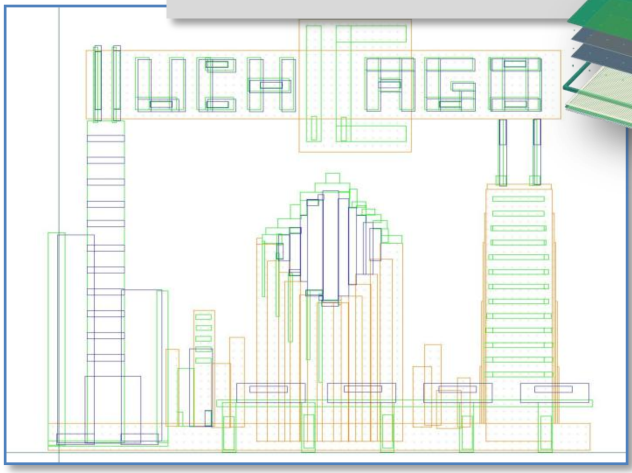


PSEC-3 :
4 channel waveform sampling ASIC

PSEC-3 ASIC

LAPPD Collaboration



Designed to sample & digitize fast pulses (MCPs):

- Sampling rate capability > 10GSa/s
- Analog bandwidth > 1 GHz (challenge!)
- Relatively short buffer size
- Medium event-rate capability (~100 KHz)

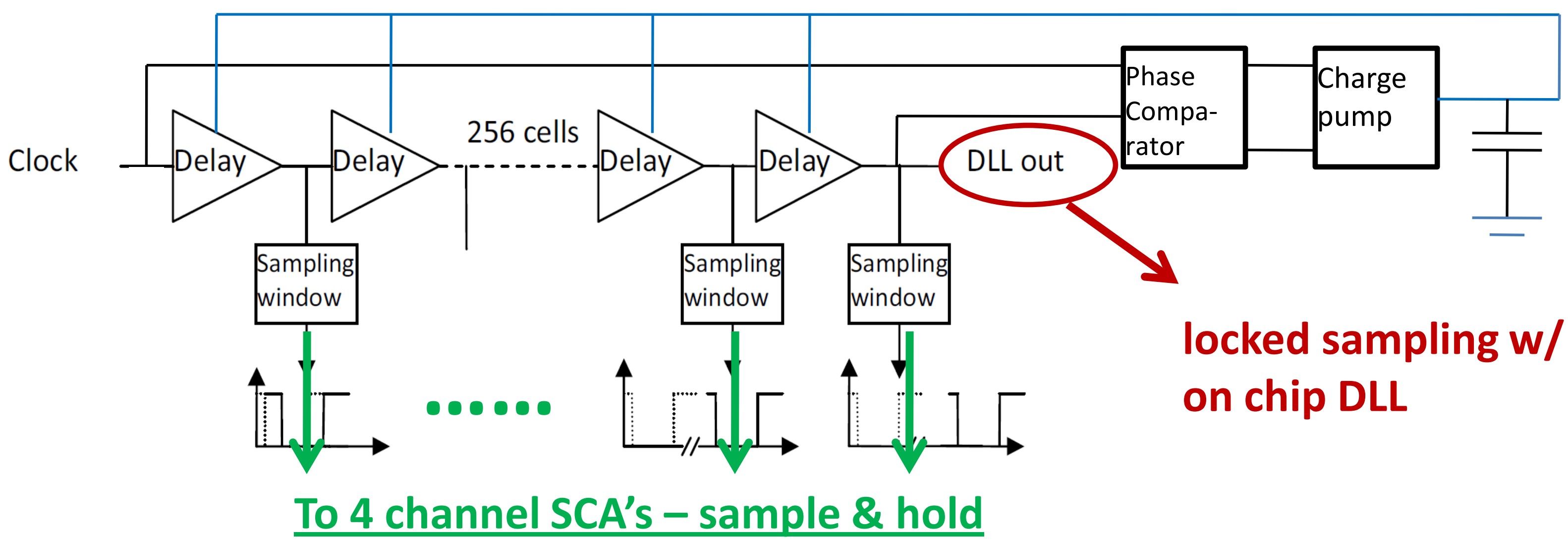
→ ***130 nm CMOS***

	SPECIFICATION
Sampling Rate	500 MS/s-15GS/s
# Channels	4
Sampling Depth	256 cells
Sampling Window	256*(Sampling Rate)$^{-1}$
Input Noise	1 mV RMS
Analog Bandwidth	1.5 GHz
ADC conversion	Up to 12 bit @ 2GHz
Latency	2 µs (min) – 16 µs (max)
Internal Trigger	yes

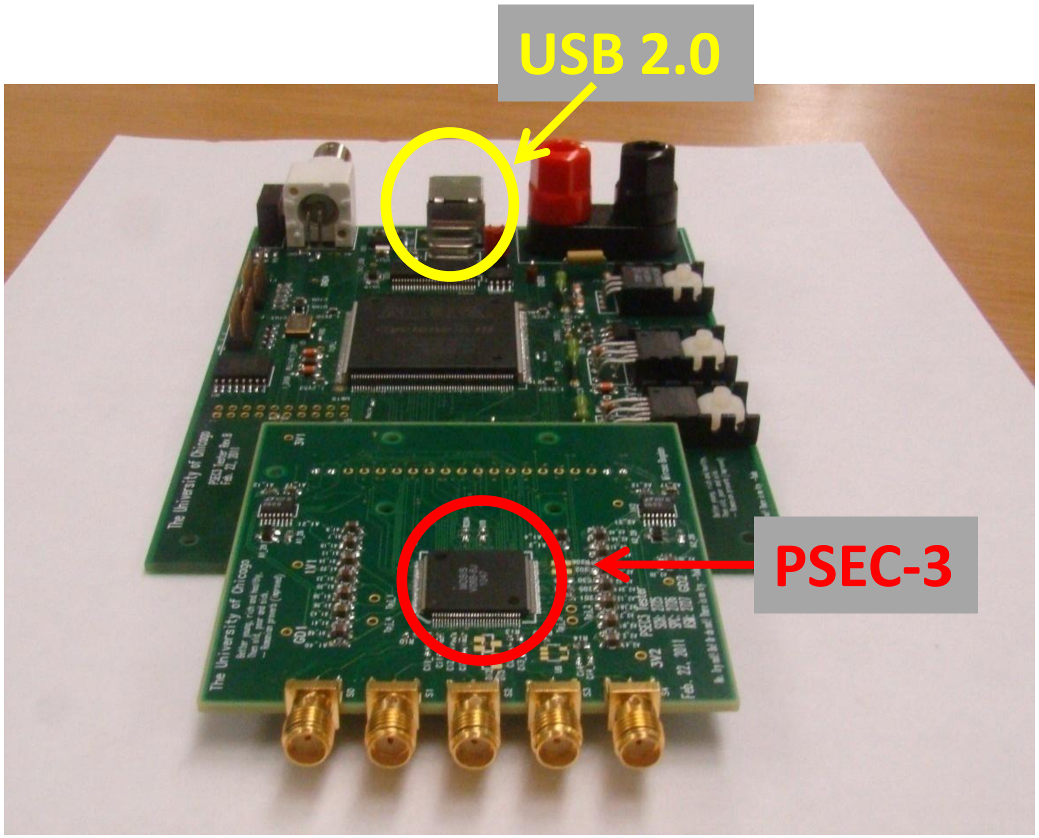
PSEC-3 architecture

- Waveform sampling using Switched Capacitor Array (SCA)
  - 256 points/waveform
- On-chip Wilkinson digitization up to 12 bits
- Serial data readout @ 40 MHz
  - Region of interest readout capability
- Self-triggering option

5-15 GSa/s Timing Generation:



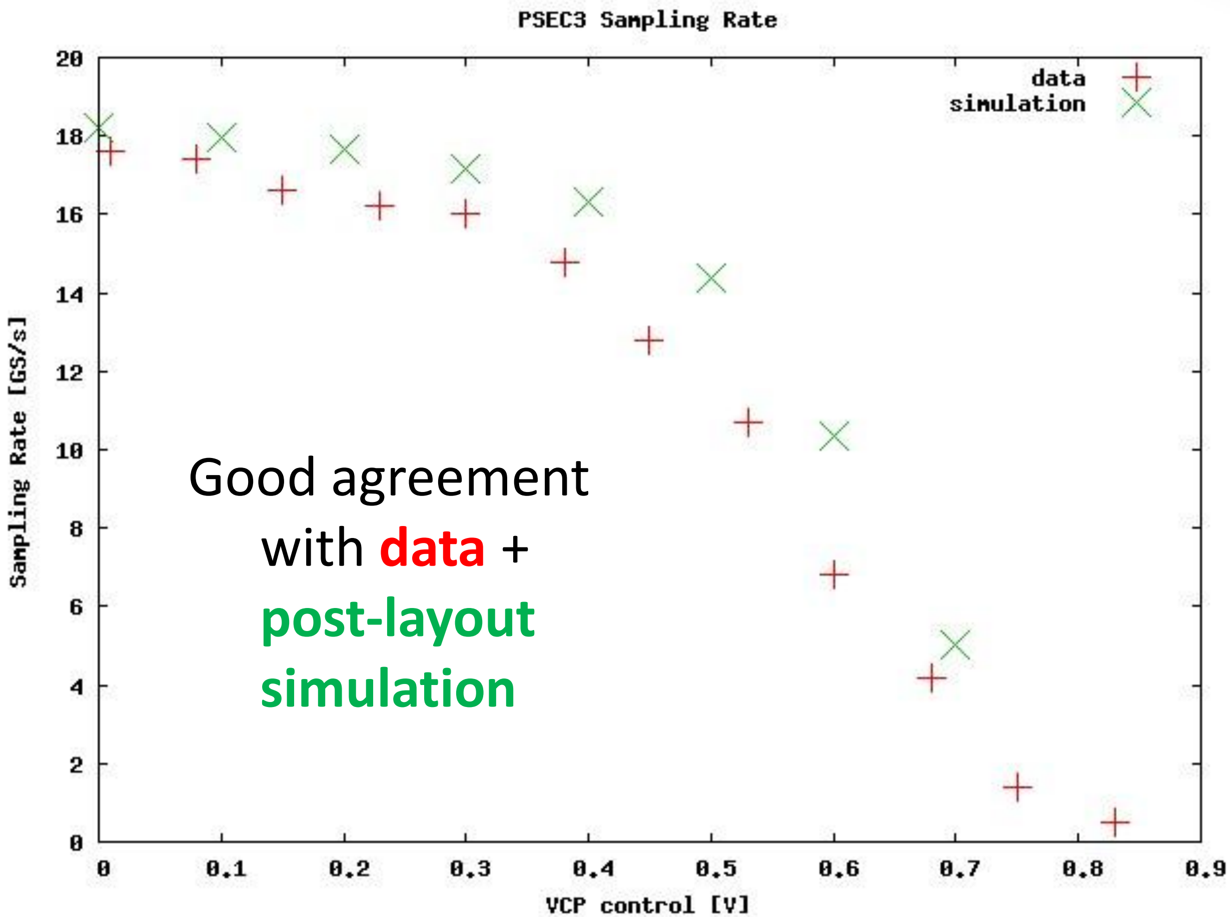
PSEC-3 Evaluation Board



- 4 channel, 5-15 GSa/s “oscilloscope”
- 5V power
- Hardware trigger capability
- Accompanying USB DAQ software

Sampling Rate

- Sampling rates adjustable 2.5 – 17 GSa/s
- Default setting of 10 GS/s, sampling lock with on-chip Delay-Locked Loop (DLL)



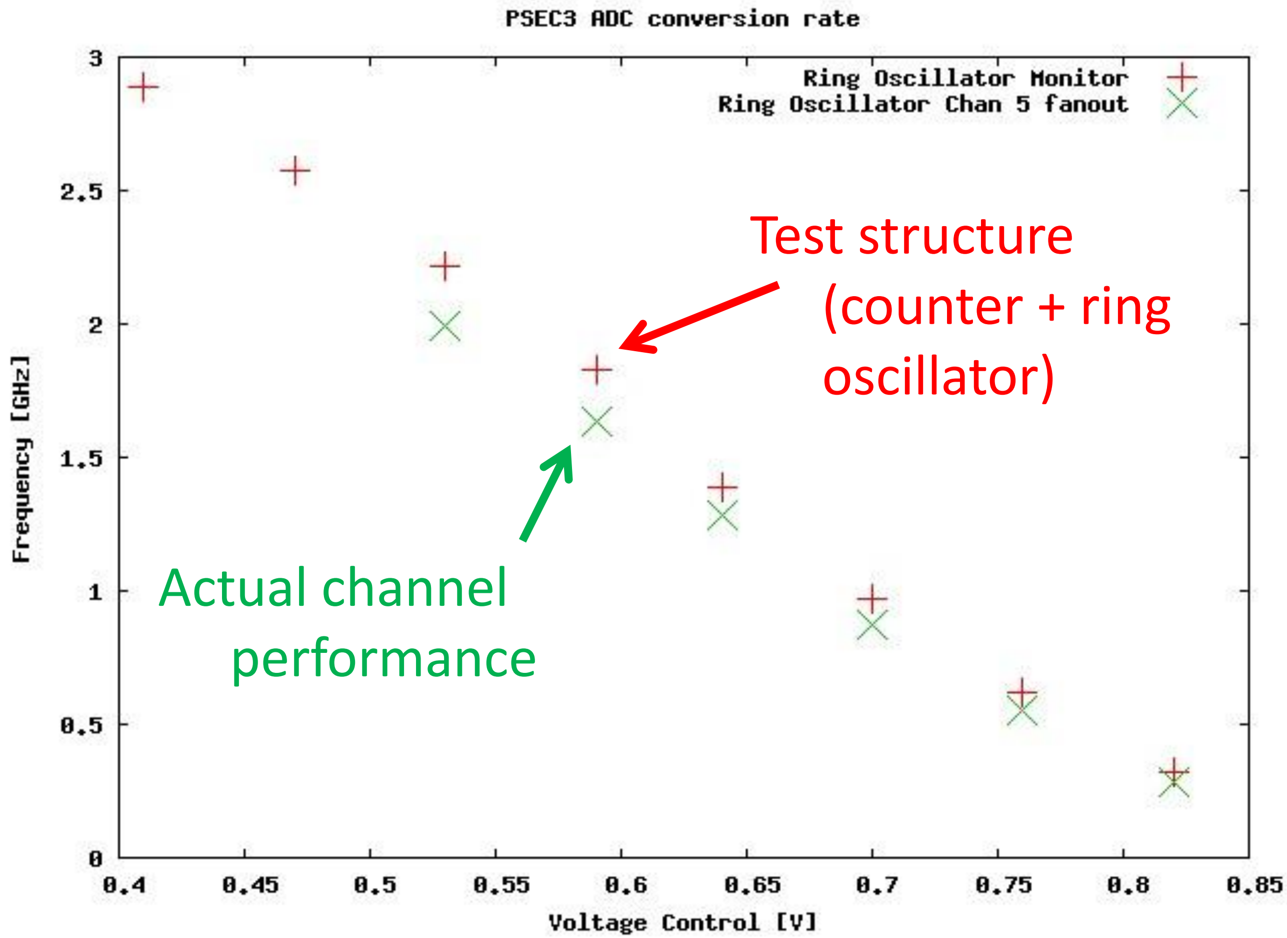
ADC performance

- Wilkinson ADC runs successfully to 2GHz (registers can be clocked to 3GHz)
- Running in 10 bit mode:

  <u>700 ns conversion time</u> (ramp ->0-1V) @ 1.6 GHz

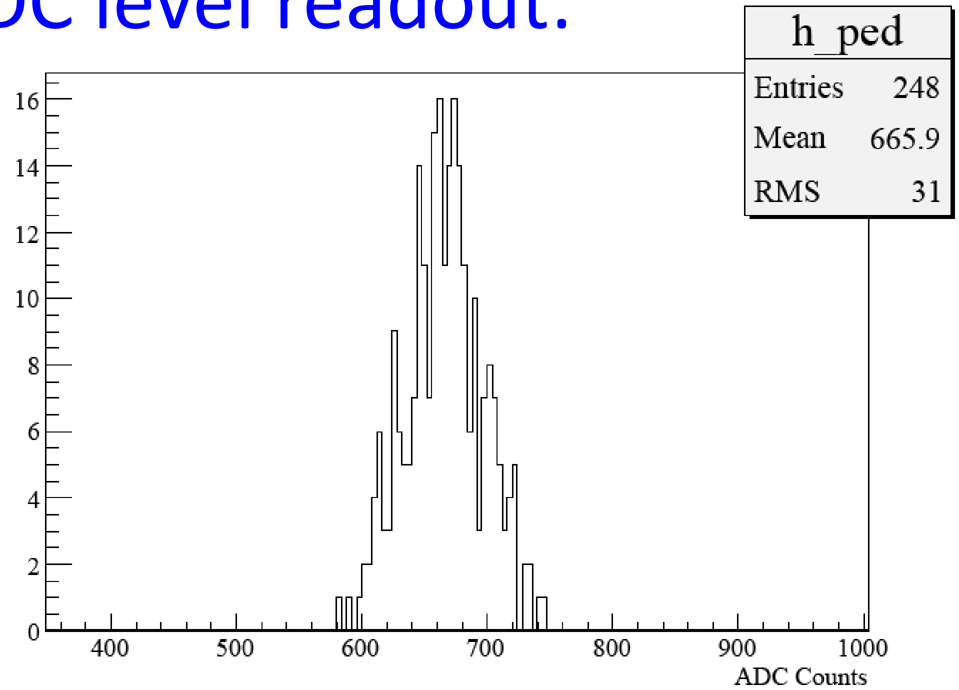
A/D conversion main power consumer in PSEC-3 – **~15 mW per channel**

(only ON during 700 ns digitization period)



PSEC-3 noise

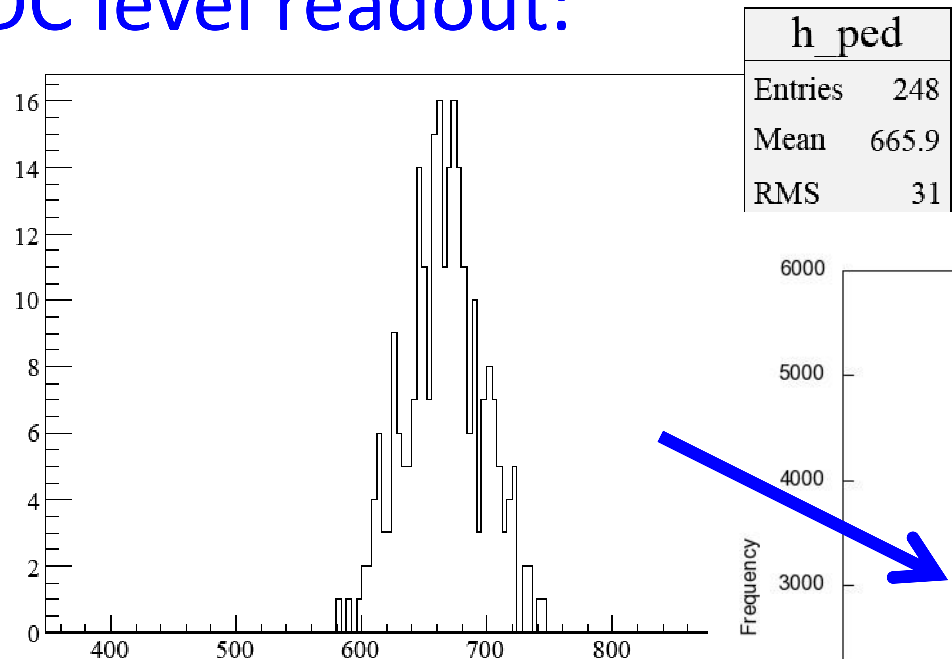
DC level readout:



Fixed pattern noise dominates -- due to cell-to-cell process variations

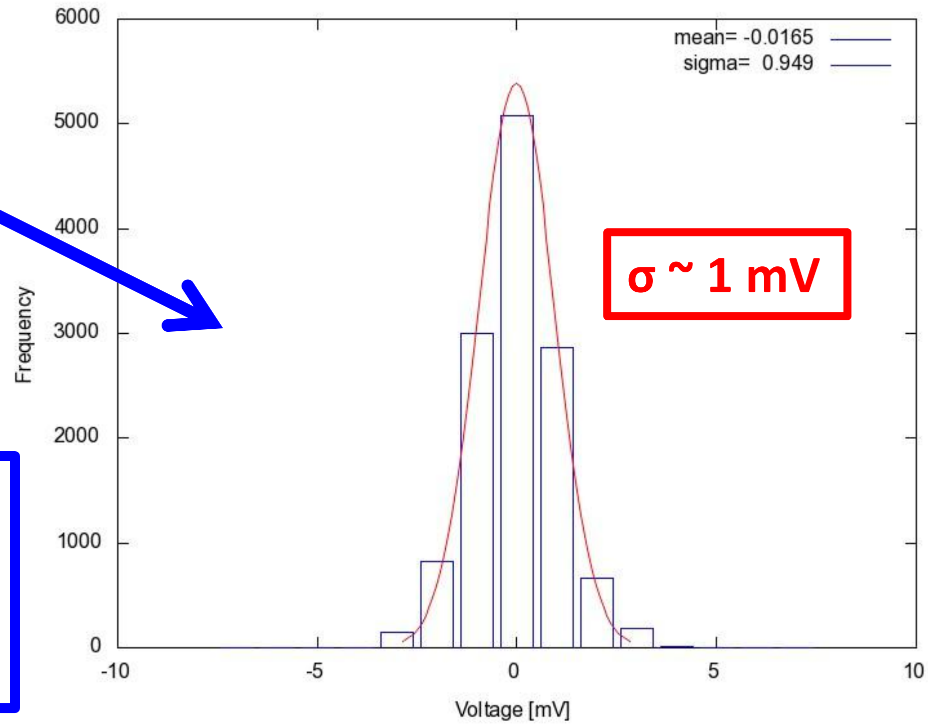
PSEC-3 noise

DC level readout:



Count-voltage conversion & pedestal subtraction

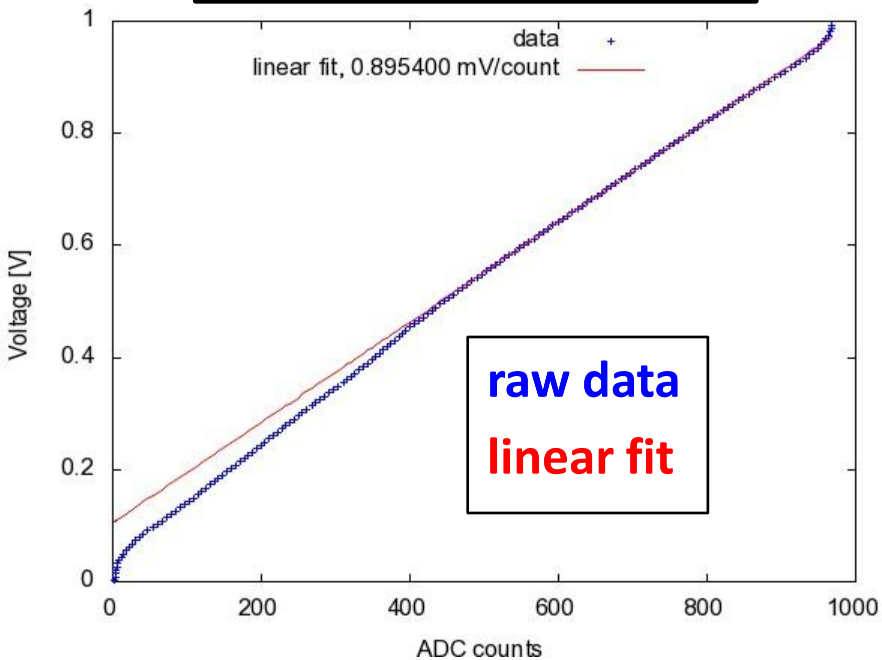
Sample noise



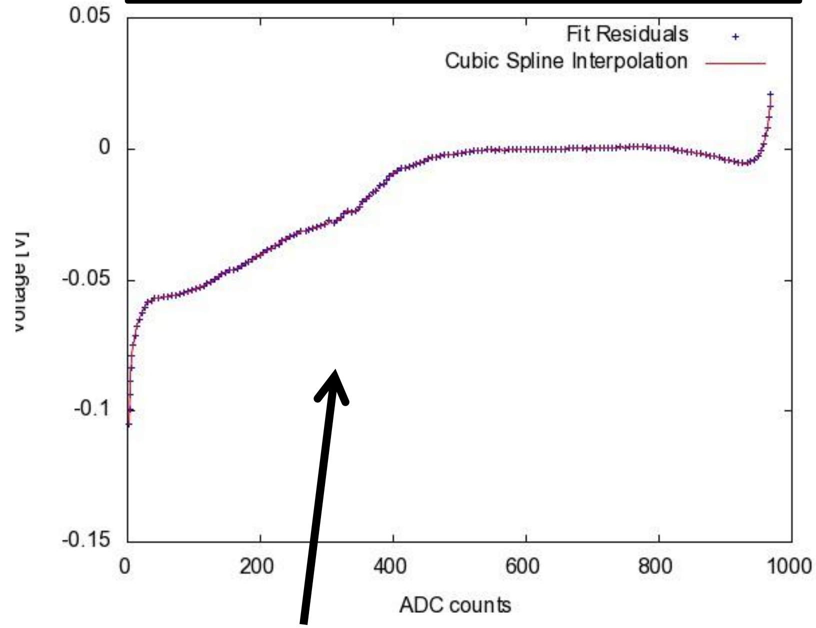
Linearity & Dynamic Range

- Dynamic range limited to ~ 1V in 130nm CMOS (rail voltage = 1.2V)
- Good linearity observed

Linear DC voltage scan



Fit residuals + interpolation

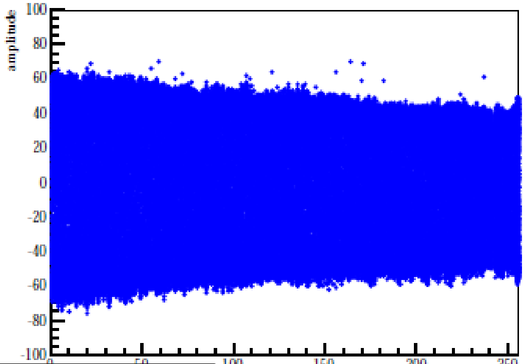


Implemented in software LUT for diff. non-linearity correction

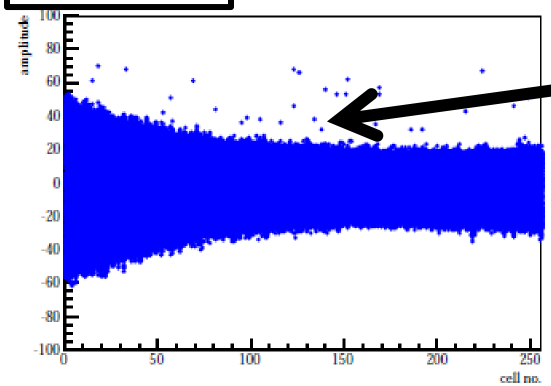
Analog Bandwidth

- Sine wave data – overlay 100's of readouts:

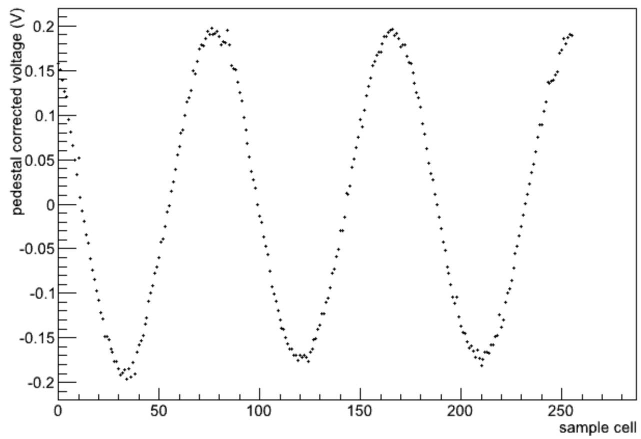
100 MHz



600 MHz



Sample 1 **256**



Visible attenuation along chip input at higher frequencies

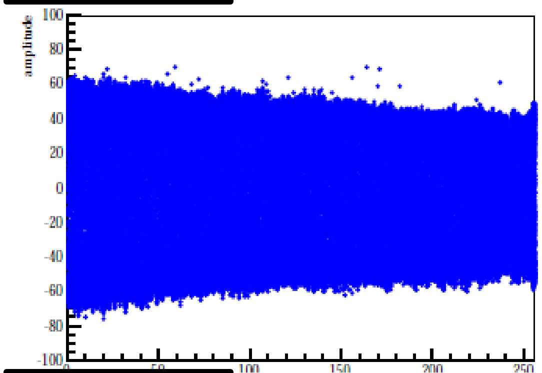
→ input **much** too resistive (R_{in}~160 Ω)

→ fall-off due to $R_{in}\ C_{parasitic}$

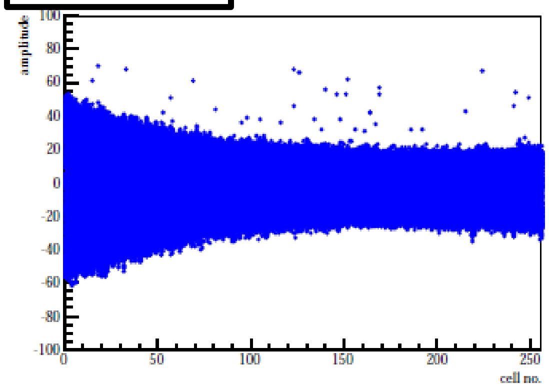
Analog Bandwidth

- Sine wave data – overlay 100’s of readouts:

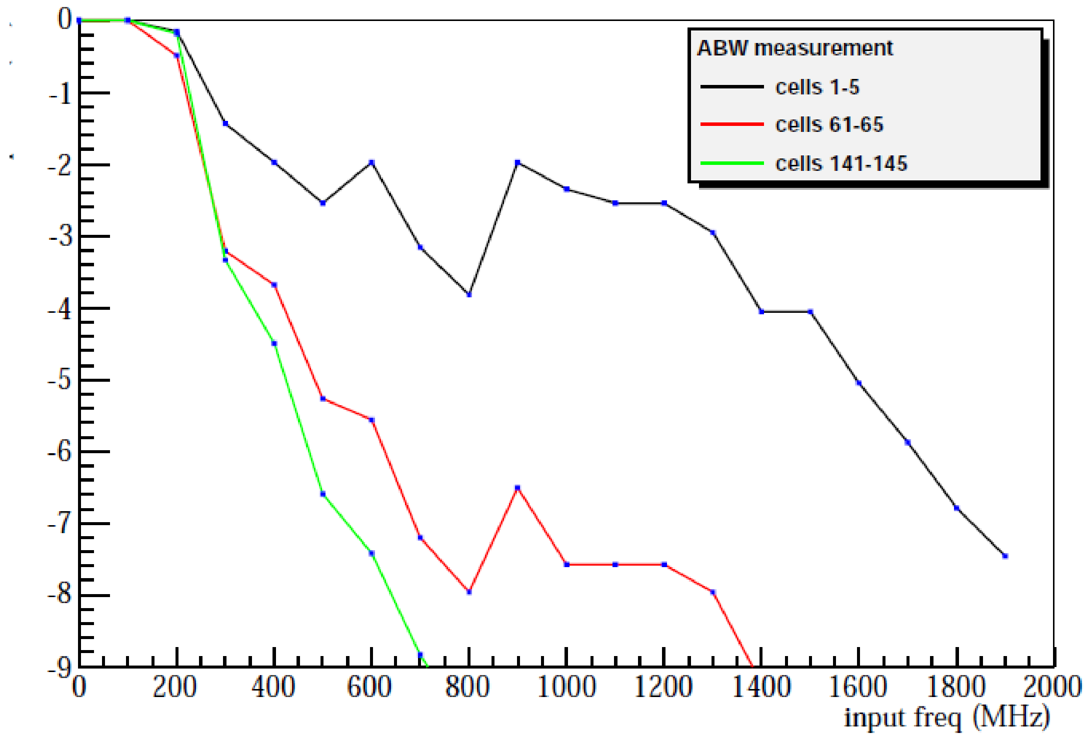
100 MHz



600 MHz



Sample 1 **256**



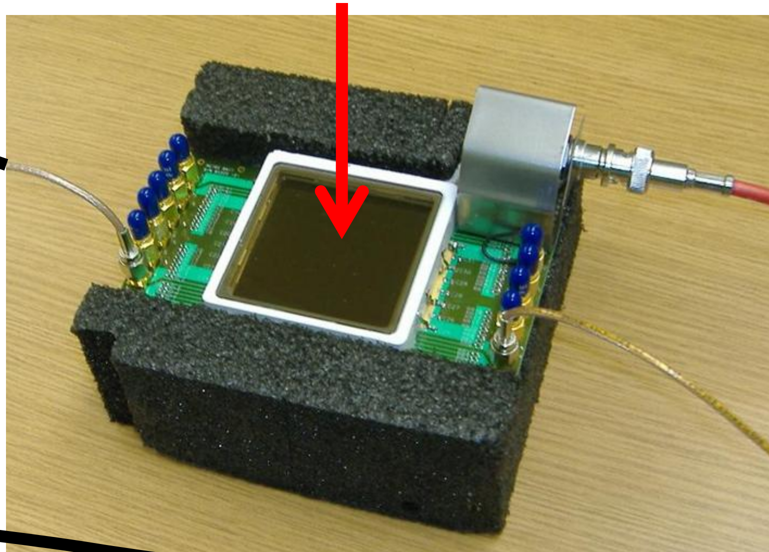
-3dB Bandwidth ~ 1.4 GHz for first cells (but only ~ 300 MHz for later cells)

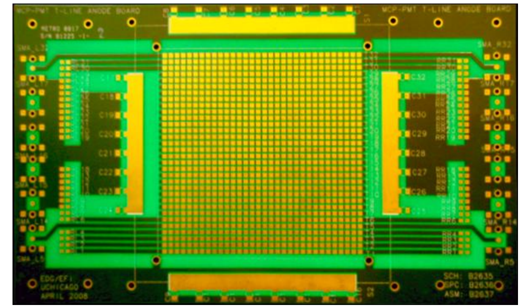
→ **corrected in PSEC-4 design**

Transmission Line-MCP readout with PSEC-3

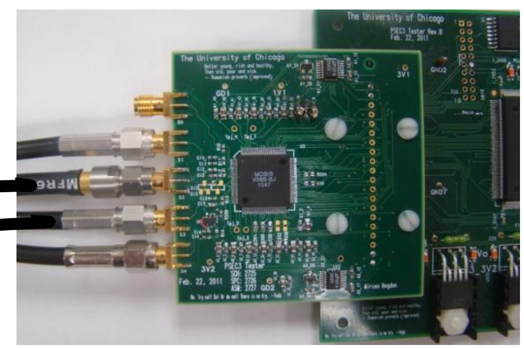
2” x 2” Burle Planacon w/ custom PCB T-Line board

laser





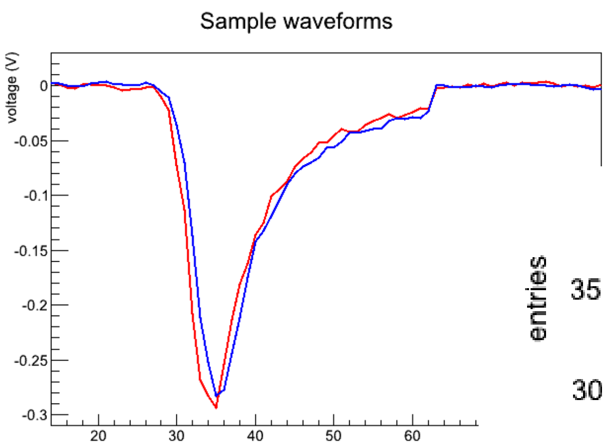
F. Tang

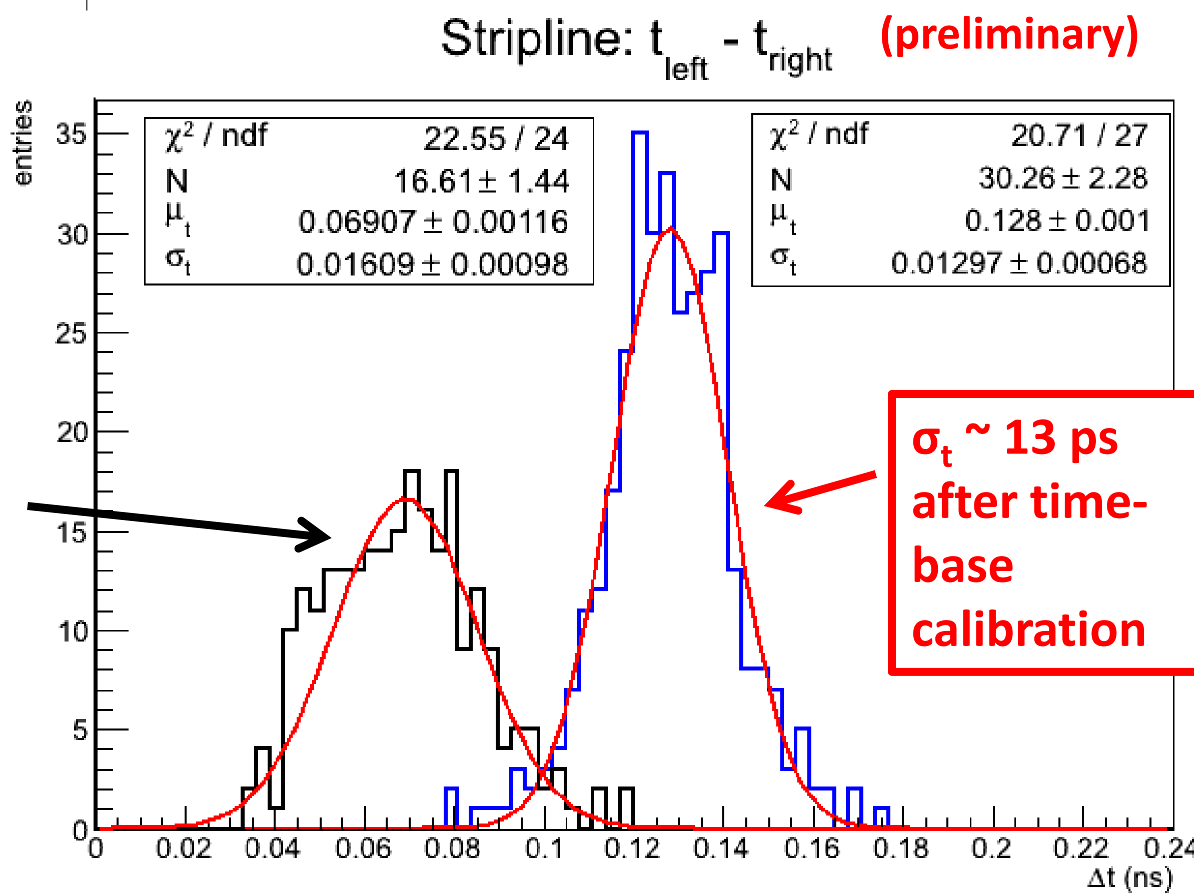


PSEC-3 sampling @ 10 Gsa/s

Transmission Line-MCP readout with PSEC-3

LAPPD Collaboration





σ_t ~ 17 ps
assuming nominal 100ps per cell

σ_t ~ 13 ps after time-base calibration

K. Nishimura's talk (4:30)- novel timing calibration technique

PSEC-3 + (upcoming) PSEC-4

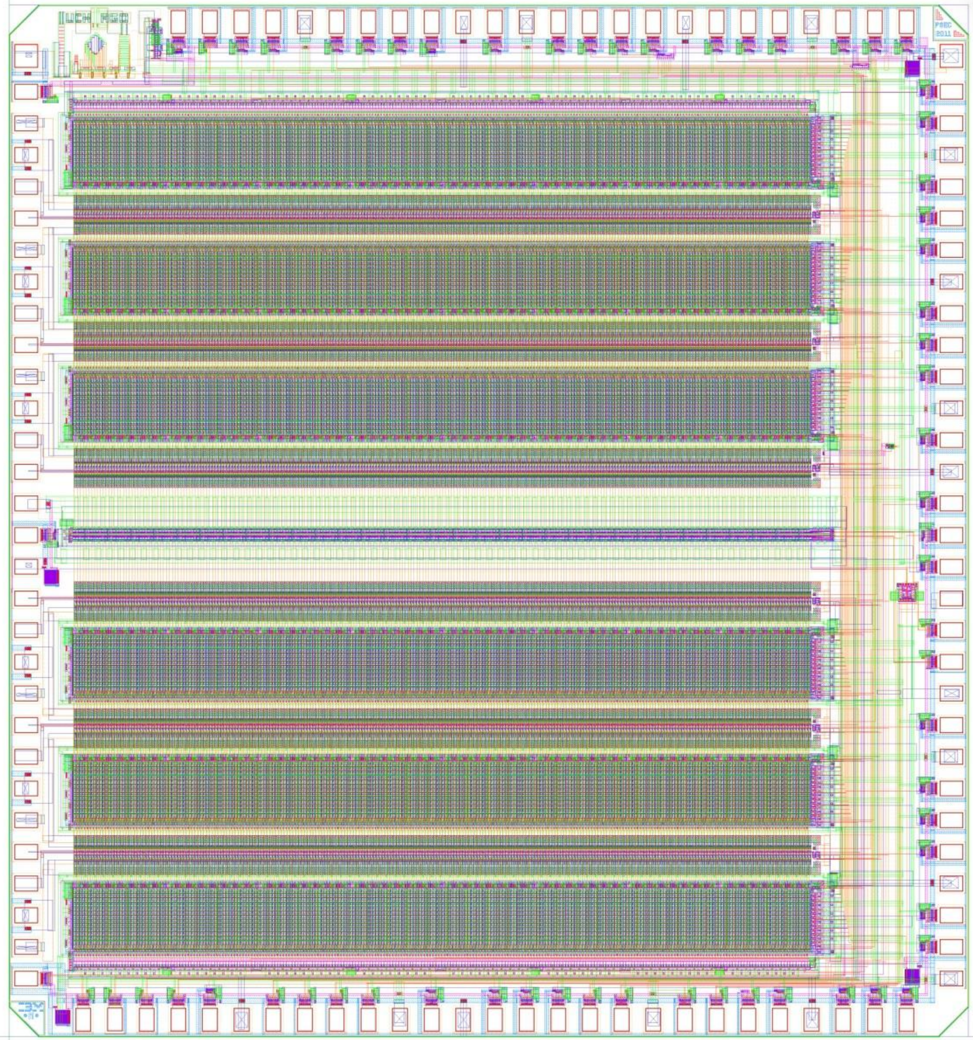
	PSEC-3		PSEC-4
	SPECIFICATION	**ACTUAL**	**SPEC**
Sampling Rate	500 MS/s-17GS/s	2.5 GSa/s-17GS/s	2.5 GSa/s-17GS/s
# Channels	4	4	6 (or 2)
Sampling Depth	256 cells	256 Cells	256 (or 768) points
Sampling Window	256*(Sampling Rate)$^{-1}$	256*(Sampling Rate)$^{-1}$	Depth*(Sampling Rate)$^{-1}$
Input Noise	1 mV RMS	1-1.5 mV RMS	<1 mV RMS
Dynamic Range	0-1V	0-1V	0-1V
Analog Bandwidth	1.5 GHz	Average 600 MHz	1.5 GHz
ADC conversion	Up to 12 bit @ 2GHz	Up to ~10 bit @ 2GHz	Up to 12 bit @ 2GHz
Latency	2 μs (min) – 16 μs (max)	3 μs (min) – 30 μs (max)	2 μs (min) – 16 μs (max)
Internal Trigger	yes	yes	yes

Red= issues addressed from PSEC-3

PSEC-4 – 5-15 GSa/s, 1.5 GHz

LAPPD Collaboration

- Design targeted to fix issues with PSEC-3
- 6 identical channels
  - each 256 samples deep
- Submitted to MOSIS 9-May 2011
  - 40 parts
  - May get a larger run via CERN MPW if necessary



LAPPD Collaboration

Summary

- PSEC-3 (soon PSEC-4) baseline ASIC for LAPPD MCP photodetectors
  - 80 channel DAQ system based on PSEC-3 & 4 under development
  - Experience with IBM 130 nm CMOS
  - Other applications?

M. Bogdan poster

- Sampling rates 10-15 GSa/s achieved
  - analog bandwidth fixed in PSEC-4 (back from foundry ~ 8/2011)
- Robust timing calibrations/measurements underway

LAPPD Collaboration

The Development of Large-Area Fast Photo-detectors

April 15, 2009

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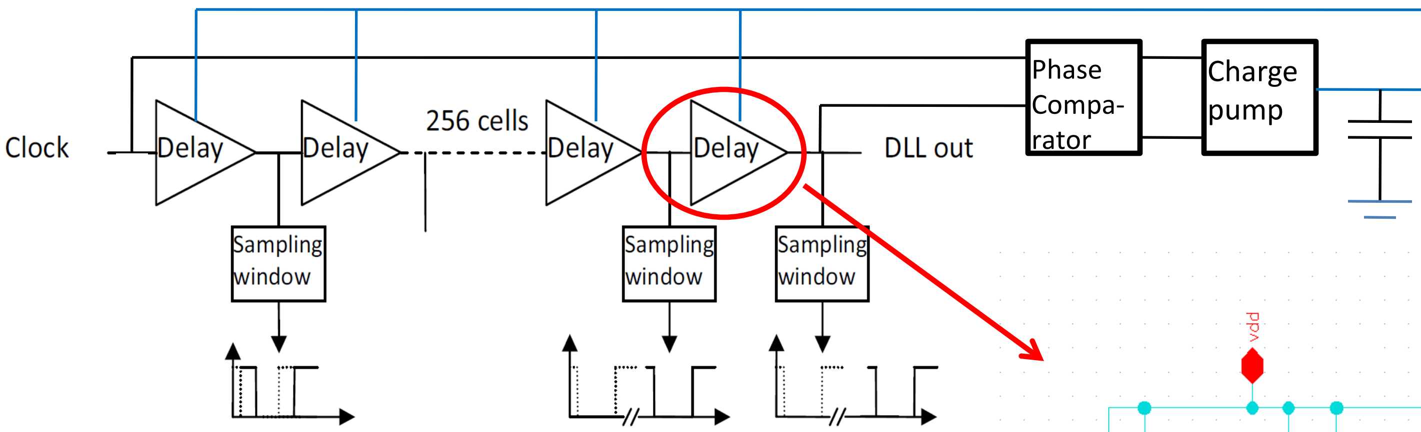
[1] Joint appointment Argonne National Laboratory and Enrico Fermi Institute, University of Chicago

3 National Labs +SSL, 6 Divisions at Argonne, 3 US small companies; electronics expertise at Universities of Chicago and Hawaii

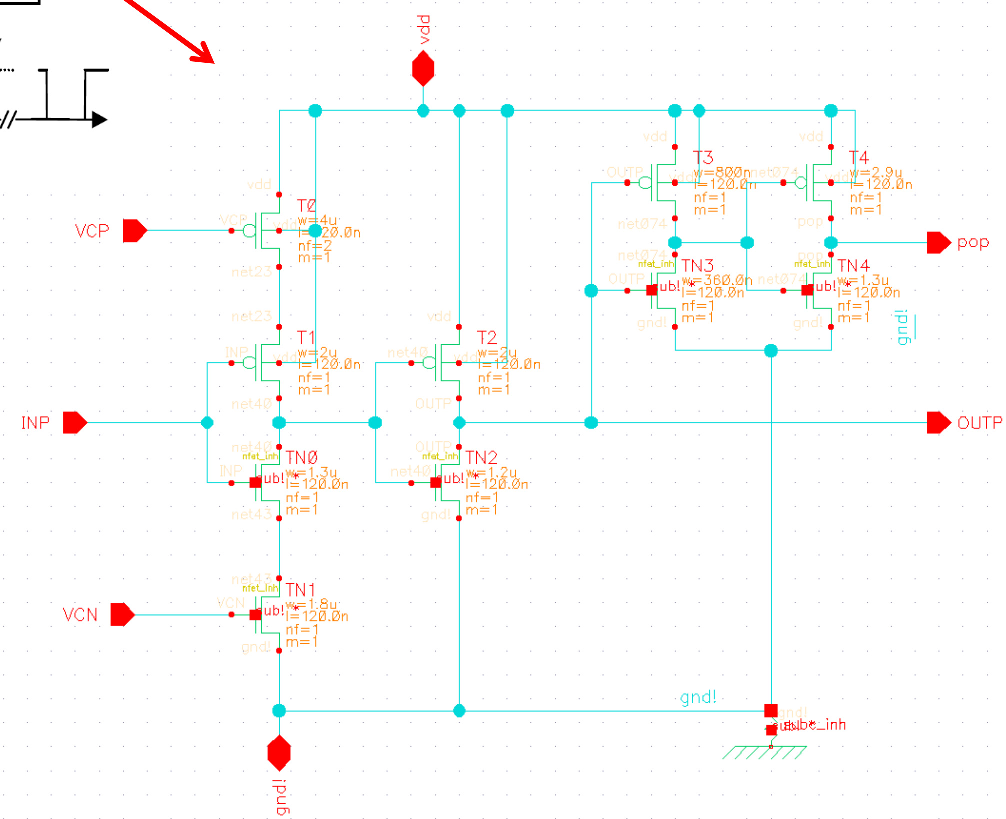
Goal of 3-year R&D- commercializable modules.

Backup

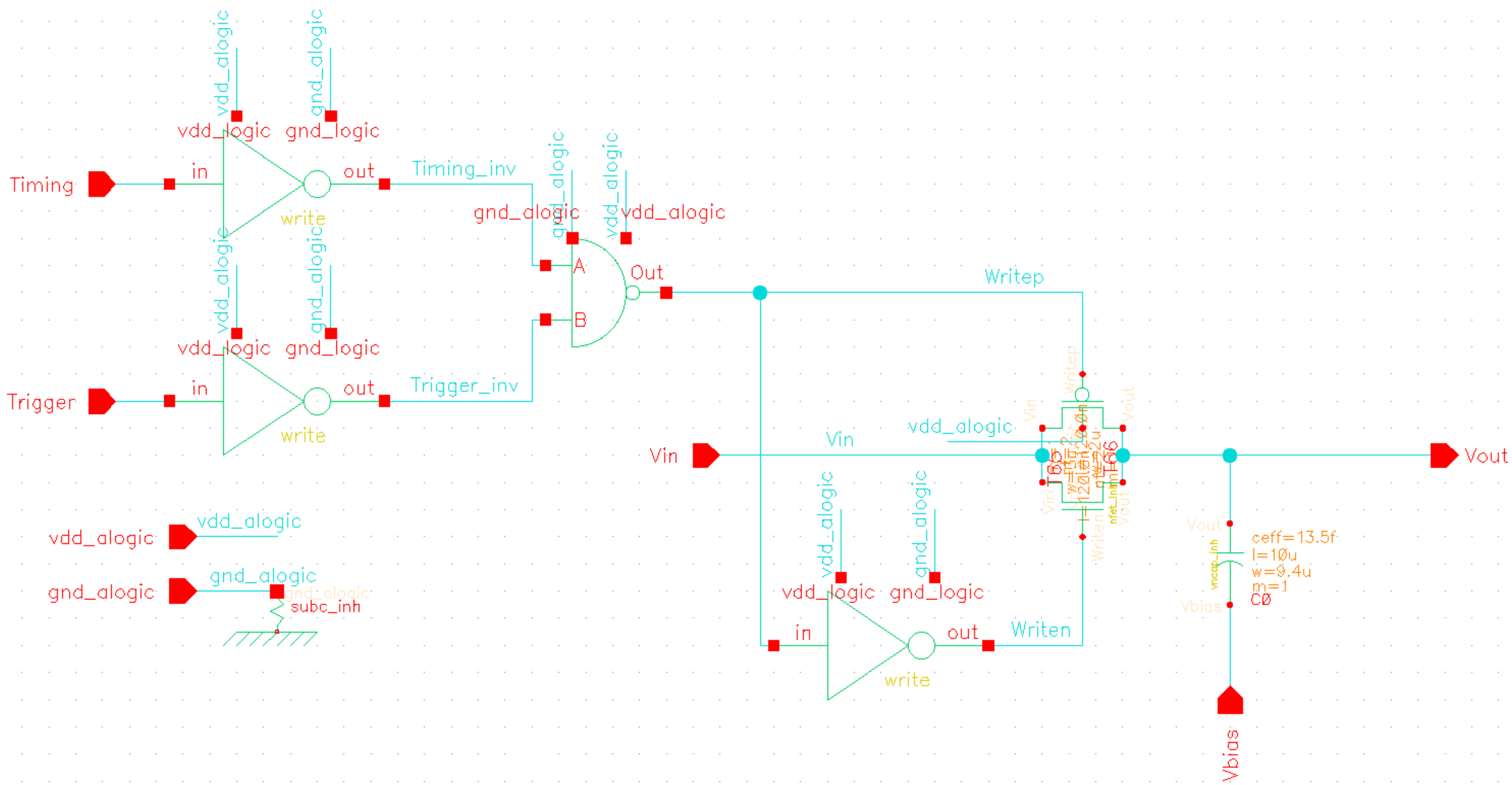
PSEC architecture – **timing generation**



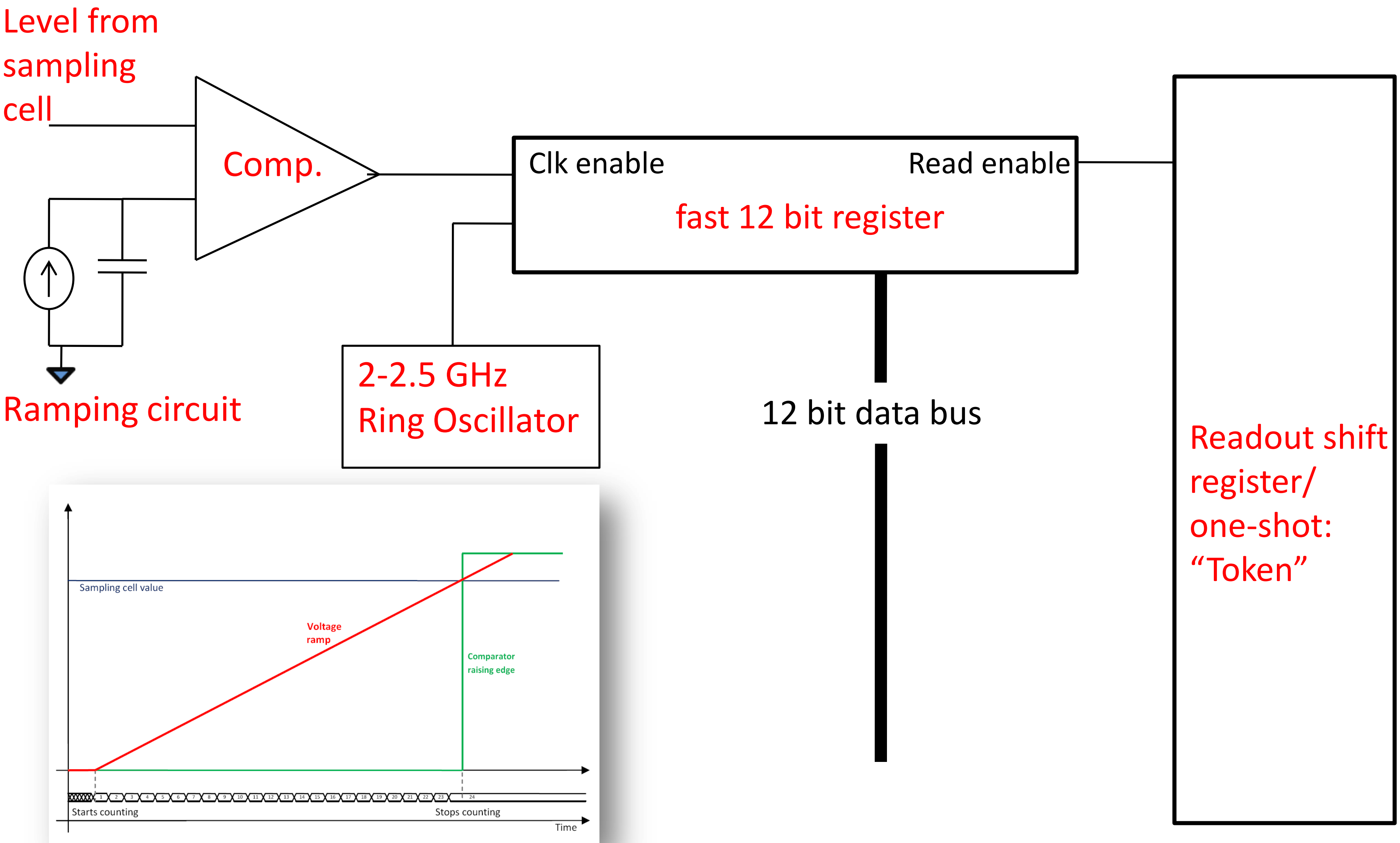
- 256 Delay units – starved current inverter chain ----------->
- Sampling window strobe (8x delay) sent to each channel's SCA
- On chip phase comparator + charge pump for sample lock



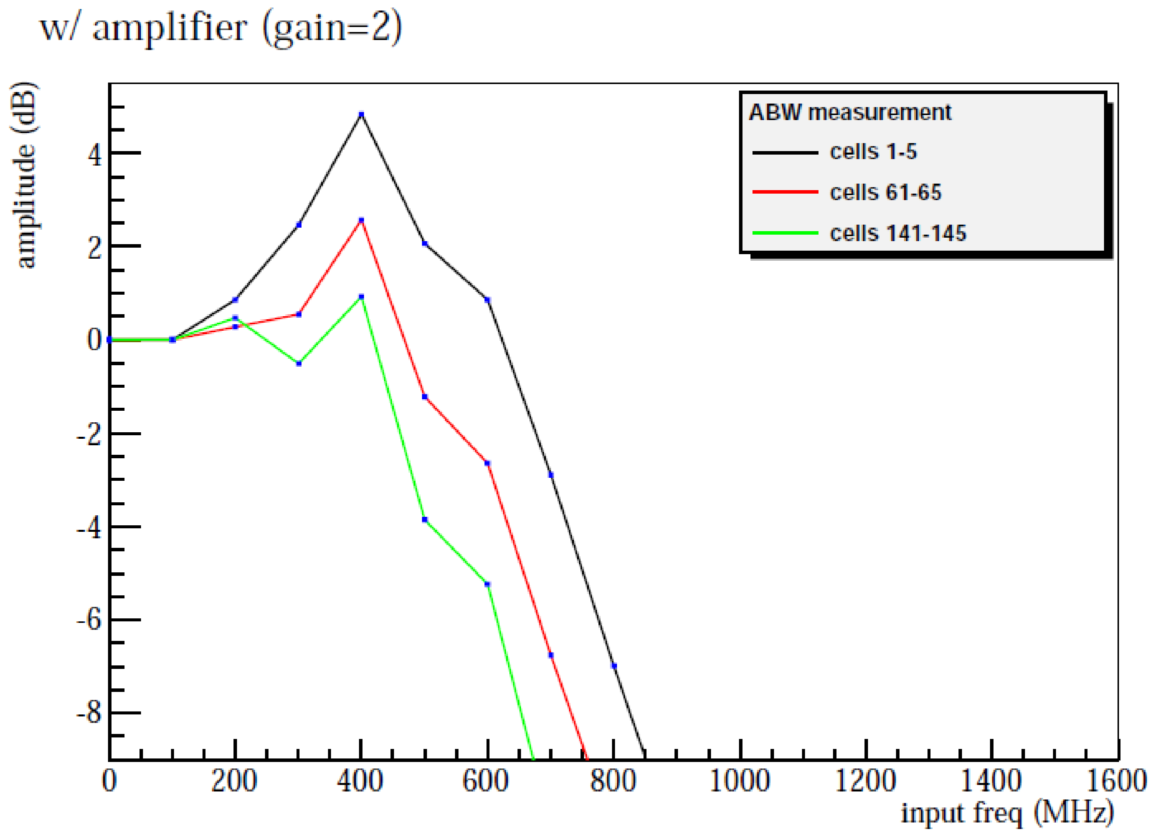
PSEC architecture -- **sampling**



PSEC architecture – **ADC + readout**



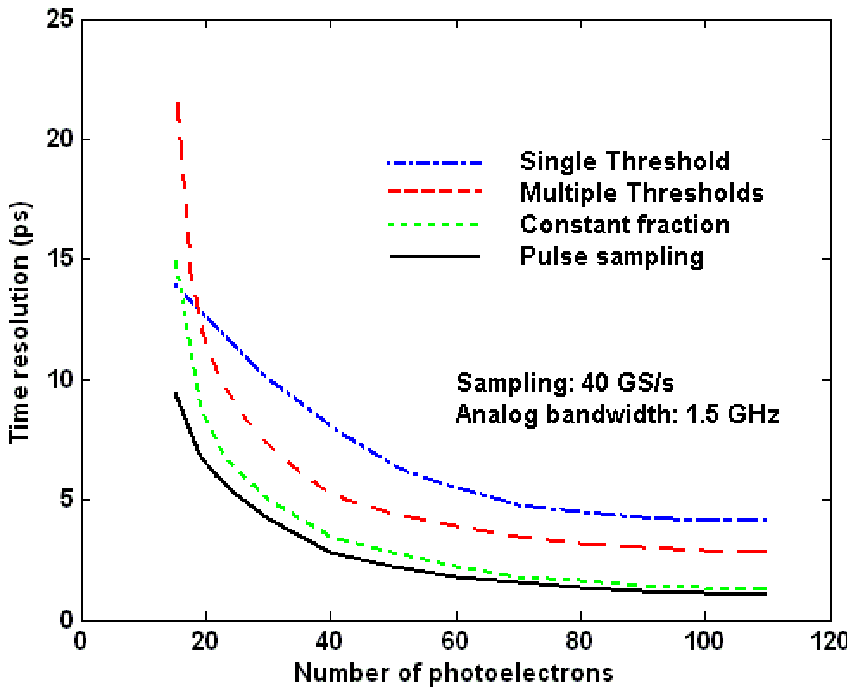
Bandwidth with gain=2 amplifier

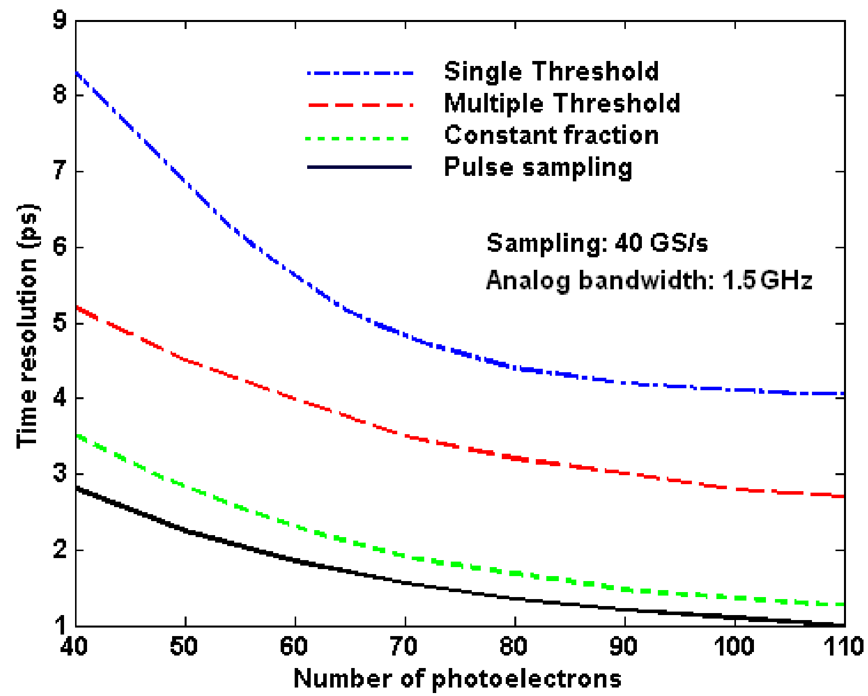


Comments:

- On-board amplifier (channel 4) unstable with unity gain – works with gain=2
- -3dB BW ~700 MHz for first cells
- Amplifier = THS4304

Electronics: Methods compared (simulation)





zoom

Time resolution vs Number of photo-electrons
Jean-Francois Genat