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A 4-Channel Waveform Sampling ASIC using 130nm CMOS technology

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We describe here the development and characterization of PSEC-3, a custom analog and digital integrated circuit designed in the IBM8RF 130 nm process, intended for fast, low-power waveform sampling. As part of the Large-Area Picosecond Photo-Detector (LAPPD) collaboration, this ASIC has been designed for the front-end transmission line readout of large area micro-channel plates (MCP), among other potential applications. With 4 analog input channels, PSEC-3 has achieved sampling rates of 1-17 GSa/s. Analog sampling is performed with a 256-sample switched-capacitor array architecture in which the stored analog values are digitized with an on-chip 2 GHz Wilkinson ADC. Sampling lock is possible with an on-chip delay locked loop (DLL). Readout latency varies from 1.5 us to 17 us depending on the trigger event and number of channels read. The input noise has been measured at 1mV RMS, and power
consumption is less than 20mW per channel. The intrinsic analog bandwidth is presently under evaluation.

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