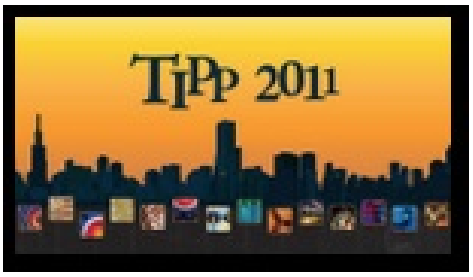


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# ADC System with On-board Demodulation for QUIET-II Experiment

The Q/U Imaging ExperimenT (QUIET) is designed to measure the
B-mode in cosmic microwave background (CMB) polarization, which is
smoking-gun evidence for the inflationary universe.
Since the B-mode signal is so faint (nK orders),
a large detector array is required.
Using a 500-element HEMT-based polarimeter array,
QUIET-II plans to search for the B-mode at the Atacama desert in Chile,
about 5,000 m above sea level.
To handle the large number of analog signals from the polarimeters
(500-elements x 4ch = 2,000 signals) on the telescope mount
where space is quite limited,
ADC system composed of high density and scalable electronics is a key issue.
We developed 64ch VME-6U-size Analog-to-Digital Converter (ADC)
boards with a high resolution (18 bits), sufficient sampling speed
(800 kS/s) and digital demodulation functionality.
The demodulation of the amplitude-modulated signals from the
polarimeters provides Stokes Q and U parameters, simultaneously.
All demodulated signals are averaged with a frequency of 50 Hz to reduce the data size.
The demodulation and averaging algorithms are implemented in a
FPGA on the ADC board.
To obtain the high scalability,
data are transferred via not the VME protocol, but the TCP protocol implemented in the same FPGA.
In this talk we will present the design and test results of the ADC system.

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