# Radiation-Hard ASICS for Optical Data Transmission in the First Phase of the LHC Upgrade

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# Outline

- Introduction
- Result on VCSEL Driver Chip
- Result on PIN Receiver/Decoder Chip
- Summary

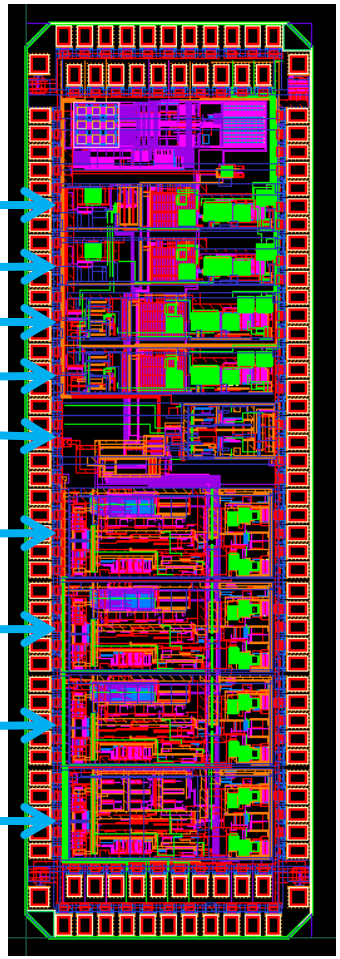
# IBL

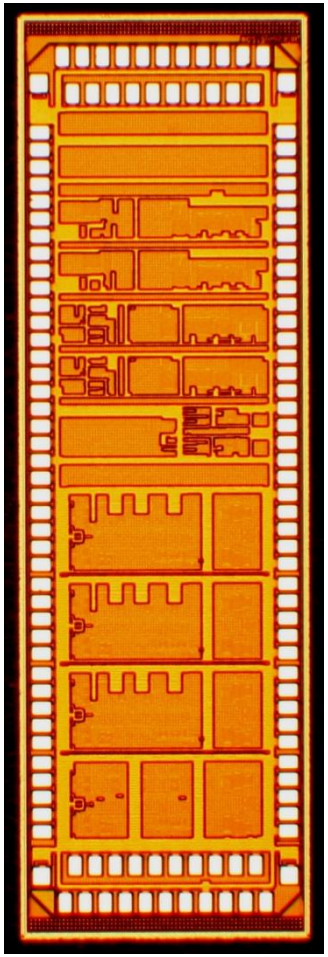
- ATLAS proposed to add one more layer to the current pixel detector
  - “Insertable B-Layer” or IBL
  - Installation ~2013
  - Optical links will use VCSEL/PIN array as in current pixel detector
  - An updated version of the current driver (VDC) and receiver (DORIC) with redundancy and individual VCSEL current control would be a logical improvement
    - Experience gained from the development/test of such new chips would help in the development of on-detector array-based opto-links for the SLHC
      - → Submission of 1st prototype chip (130 nm) on 2/2010
        - » Irradiated for studies
      - → Submission of 2nd prototype chip (130 nm) on 5/2011

# Chip Content

Design

Photo





VCSEL Driver (spare)

VCSEL Driver

VCSEL Driver with pre-emphasis

VCSEL Driver with pre-emphasis

CML Driver with pre-emphasis

Decoder (40Mb/s)

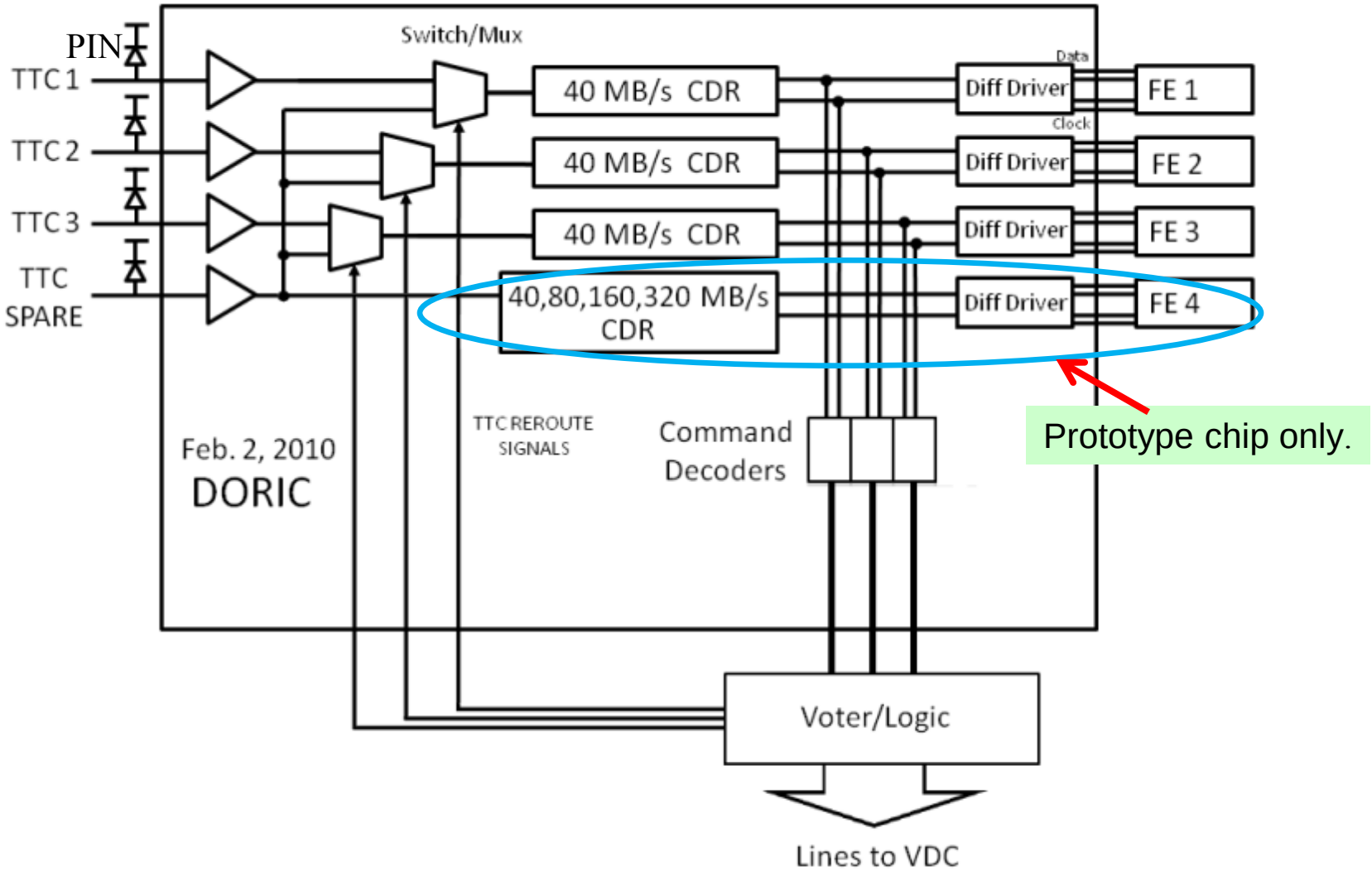
Decoder (40Mb/s)

Decoder (40Mb/s)

Decoder (40/80/160/320 Mb/s, spare)

1.5 mm

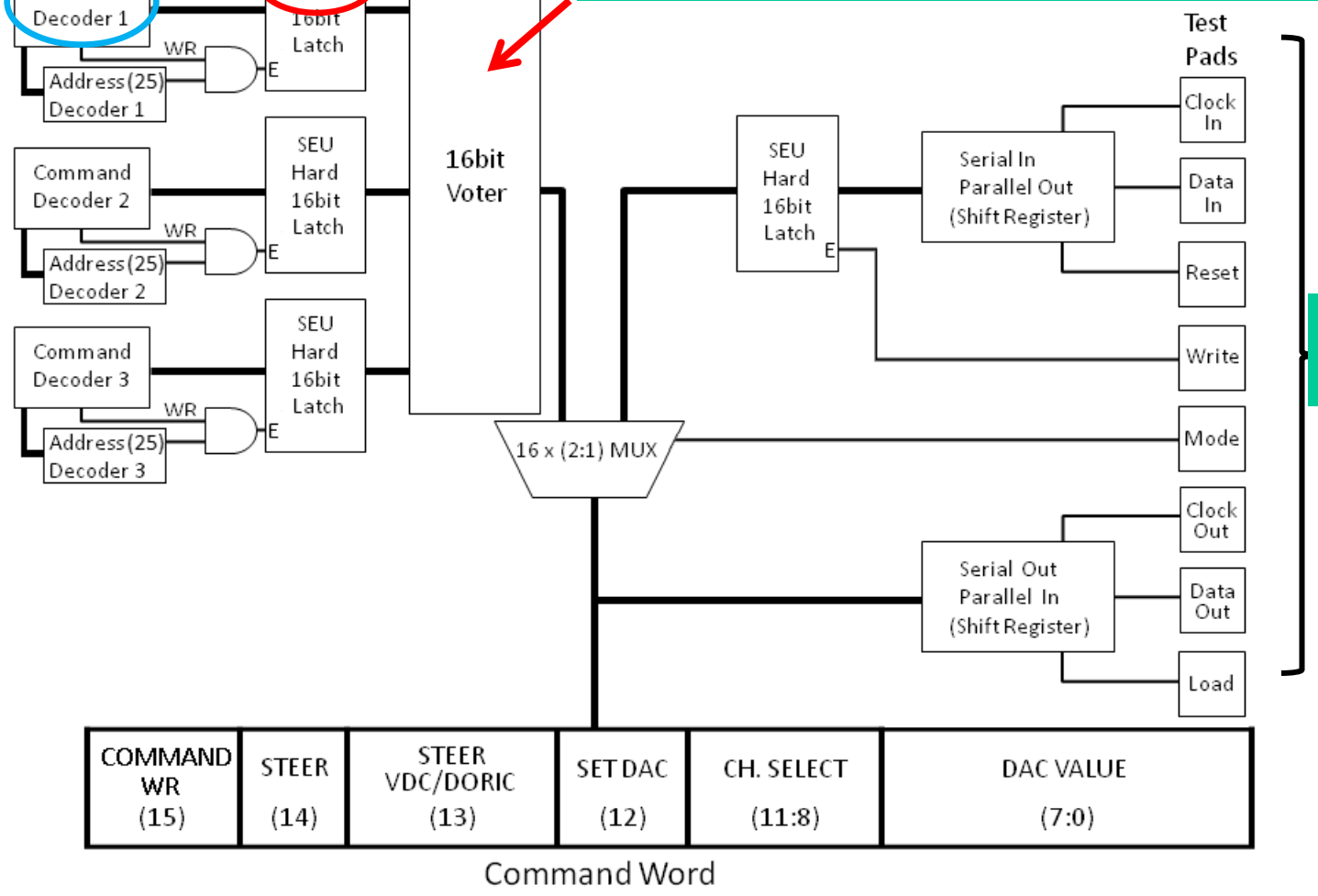
# PIN Reciever/Decoder



# Command Decoder Interface

Courtesy of FE-I4 of IBL

Prototype: majority voting from 3 command decoders
Production: majority voting from up to 11 command decoders



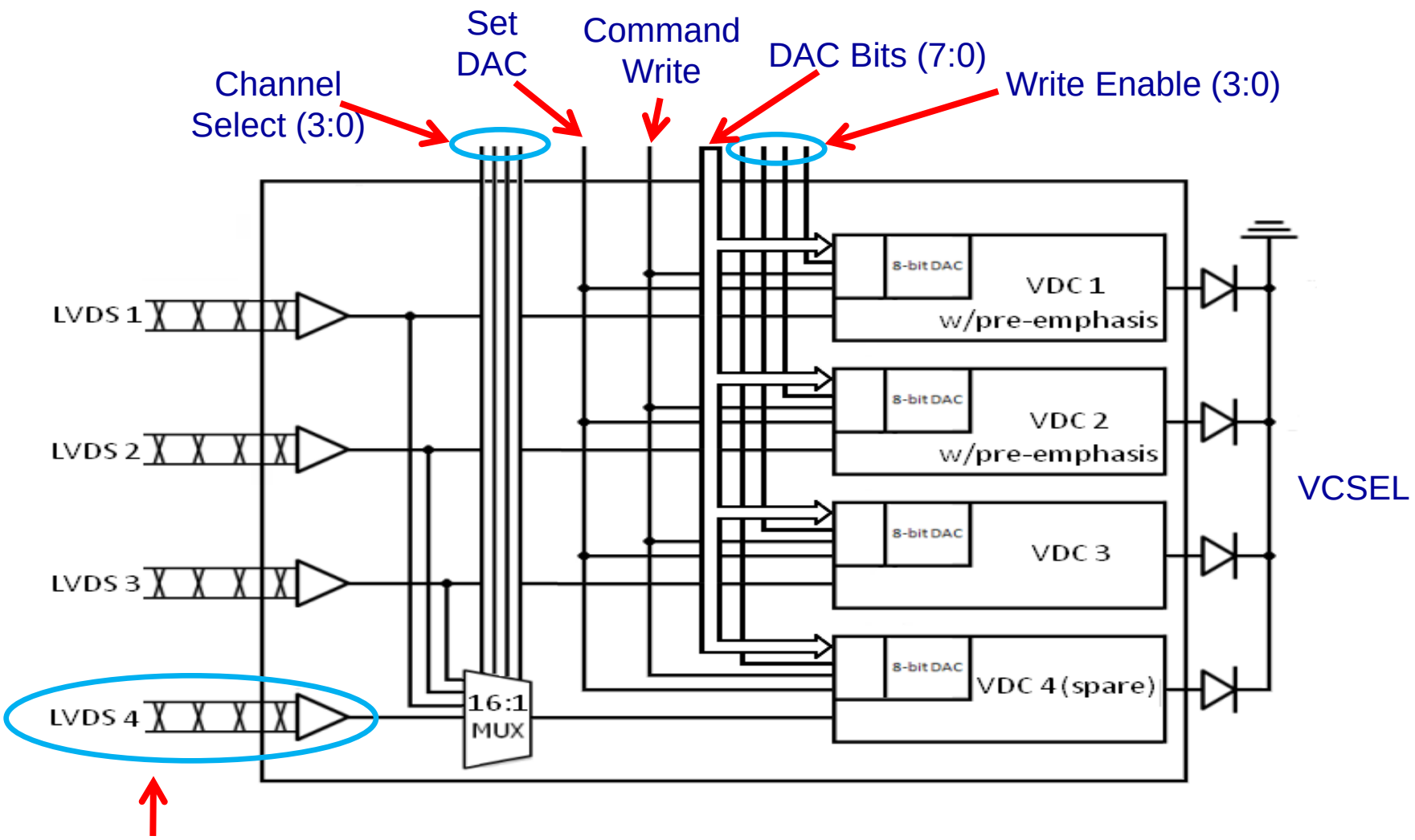
# Jitters/Thresholds

- Peak-to-peak clock jitter:
  - 40 Mb/s: 132 ps (normal), 1420 ps (multi speed)
  - 80 Mb/s: 750 ps
  - 160 Mb/s: 193 ps
  - 320 Mb/s: 103 ps
- Threshold for no bit errors
  - 40 Mb/s:
    - Multi speed: 40 μA
    - Ch 1: 10 μA
    - Ch 2: 22 μA
    - Ch 3: 20 μA
  - 80 Mb/s: 58 μA
  - 160 Mb/s: 74 μA
  - 320 Mb/s: 110 μA

# PIN Receiver/Decoder

- All channels work at 40 Mb/s
- Multi Speed version works at 40 Mb/s, 80 Mb/s, 160 Mb/s and 320 Mb/s
  - 160 and 320 Mb/s need external bias tuning for proper operation
- Steering signal to spare channel works

# VCSEL Driver Chip




LVDS input added for prototype chip only.

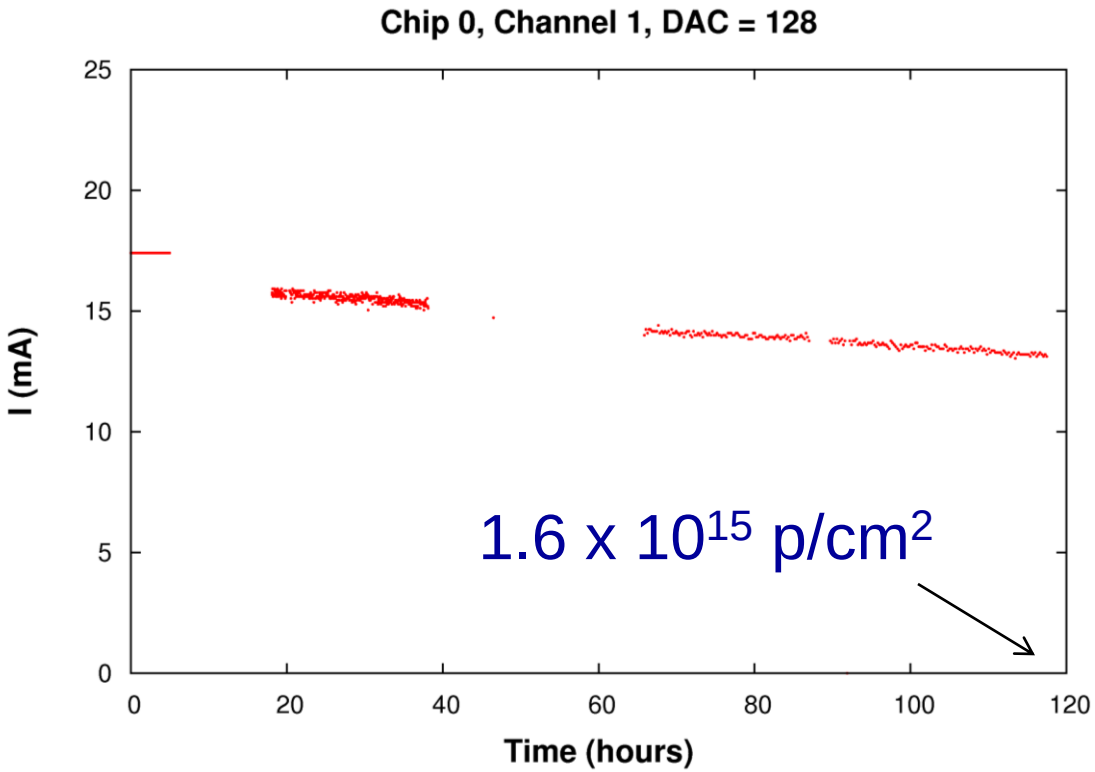
# VDC Results

- Power-on reset circuit
  - An open control line disables 6 opto-links in current pixel detector
    - Implemented power-on reset circuit in prototype chip
    - Chips power up with several mA of VCSEL current
- Test port
  - Can steer signal received to spare VDC/VCSEL
  - Can set DAC to control individual VCSEL currents
- All four channels run error free at 5 Gb/s
  - Includes the spare with signal routed from the other LVDS inputs

# Irradiation

- Two chips were packaged for irradiation with 24 GeV/c protons at CERN in August 2010
  - Each chip contains four channels of drivers and recievers
  - Total dose: 1.6 x $10^{15}$ protons/$cm^2$
  - All tests are electrical to avoid complications from degradation of optical components
    - Long cables limited testing to low speed
  - Observe little degradation of devices

# VDC Irradiation 2010




- VDC drives 25 Ω with constant control current
- Decrease in drive current is small

# Single Event Upset

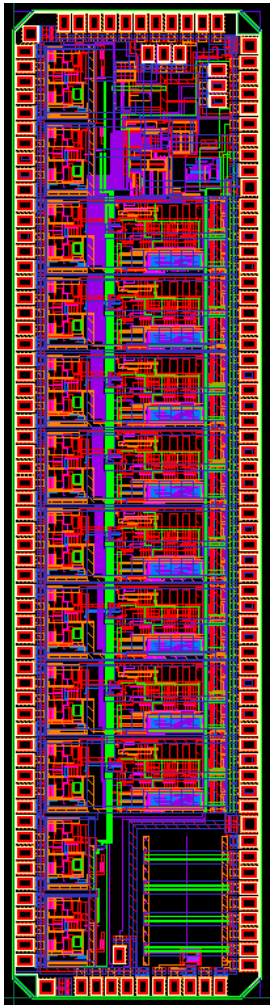
- SEU hardened latches or DAC could be upset by traversing particles
  - 40 latches per 4-channel chip
  - SEU tracked by monitoring the amplitude of VDC drive current
  - 13 instances (errors) of a channel steered to a wrong channel in 71 hours for chip #1
    - Similar upset rate in chip #2
    - $\sigma = 3 \times 10^{-16}$ cm$^2$
    - Particle flux ~$3 \times 10^9$ cm$^{-2}$/year at opto-link location
    - SEU rate ~$10^{-6}$/year/link

# 12 Channel PIN Reciever/Decoder

- Submitted May 9 – 6.5mm X 1.6mm
- Decodes 40 Mb/s bi-phase mark (BPM) signal
- Designed for 8 channel operation

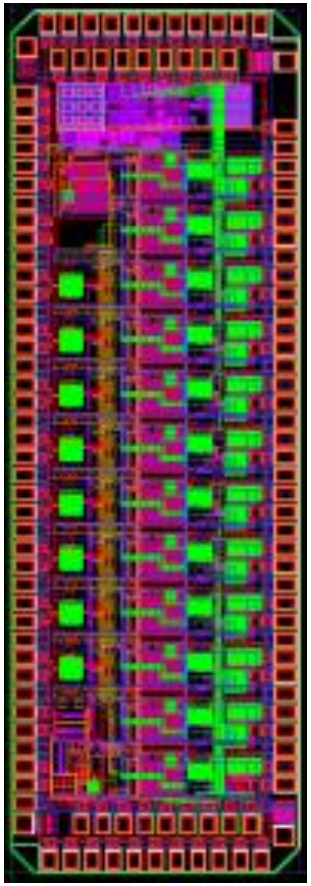
- Includes 4 spare PIN receivers for redundancy
  - If one of the 8 inner PIN diodes fail, a signal from one of the 4 redundant PIN receivers can be steered to the digital portion of the failed channel
  - Allows working control even if only 1 of the inner 8 PIN channels is alive

- Includes 8 FE-I4 command decoders
  - Allows remote control of opto-module via commands received by the command decoders



# 12 Channel VCSEL Driver

- Submitted May 9 – 1.5 mm X 4.5 mm
- Designed for 8 channel operation up to 5 Gb/s
- 4 spare VCSEL driver outputs
- Receives serial data from PIN receiver/decoder for configuration
- If one of the 8 inner VCSELs fail
  - the data signal from the detector can be steered to any of the spare VCSELs
- Per channel 8 bit DAC for remote VCSEL modulation current control



# Summary

- Prototyped opto-chip for 2nd generation ATLAS pixel opto-links incorporated experience gained from current links
  - Add redundancy to bypass broken PIN or VCSEL channels
  - Add individual VSCEL current control
  - Add power-on reset to set VCSEL current to several mA on power up
  - VCSEL driver can operate up to ~5 Gb/s with BER < $5 \times 10^{-13}$
  - PIN receiver/decoder properly decodes signal with low threshold
  - Little decrease in VCSEL driver output current
  - Very low SEU rate in latches/DAC
  - All added functionalities work

- Submitted updated version of chip with full design to be studied in radiation later this year