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RADIATION-HARD ASICS FOR OPTICAL DATA TRANSMISSION

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The LHC (CERN), the highest energy hadron collider in the world, will be upgraded in two phases to increase the design luminosity by a factor of five. The ATLAS experiment plans to add a new pixel layer to the current pixel detector during the first phase of the upgrade. The optical data transmission will also be upgraded to handle the high data transmission speed. Two ASICs have been prototyped for this new generation of optical links to incorporate the experience gained from the current system. The ASICs were designed using 130 nm CMOS process. One ASIC contains a 4-channel VCSEL driver array and the other a 4-channel PIN receiver/decoder array with one channel of each array designated as a spare to bypass a bad VCSEL or PIN channel.

Each of the receiver/decoder contains a pre-amplification, a bi-phase mark (BPM) clock/data recovery circuit, and low voltage differential signal (LVDS) outputs for both the clock and data. In order to allow remote control of the chip, the ASIC includes command decoders that have been designed to be single event upset (SEU) tolerance. The command word for configuring the chip is formed by a majority vote of the command decoders. To further improve the SEU tolerance, all latches are based on a dual interlocked storage cell (DICE) latch.

The driver ASIC is designed to operate at 5 Gb/s. Each channel has an LVDS receiver, an 8-bit DAC, and a VCSEL driver. One channel is designated as the spare channel and contains a 16:1 multiplexer. The multiplexer allows routing of the received signal from any of the three channels to the spare channel output. The 8-bit DAC is used to set the VCSEL modulation current. To enable operation in case of a failure in the communication link to the command decoder, we have included a power on reset circuit that will set the VCSEL modulation current to 10 mA upon power up.

We have extensively characterized the ASICs and then irradiated the ASICs to measure the radiation hardness and SEU tolerance. We will present the results of the study. In addition, the ASICs have been expended to 12 channels with improvements based from the prototype results. We will briefly discuss the new design that will be submitted in May.

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