Basic Electronics

Introductory Lecture Course for

Technology and Instrumentation in Particle Physics 2011

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Presented By

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Session 3

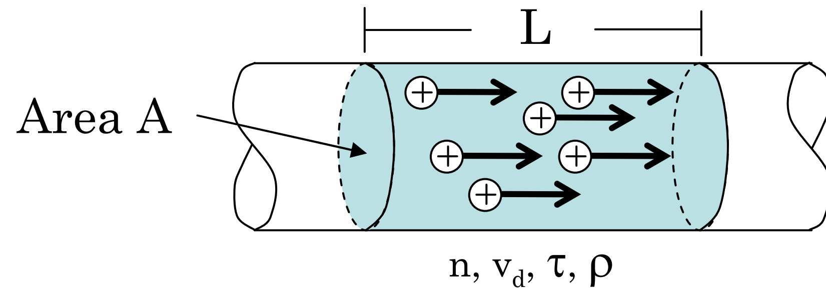
Session 3

Semiconductor Devices

Preliminary Concepts

- Resistivity Revisited

$R = \rho L / A$



$\rho = 1 / \sigma = 2\ m / (n\ q\ \tau)$ → Units: Kg-meter^3 / Coulomb-sec
= Ohm-meter
(or often, Ohm-cm)

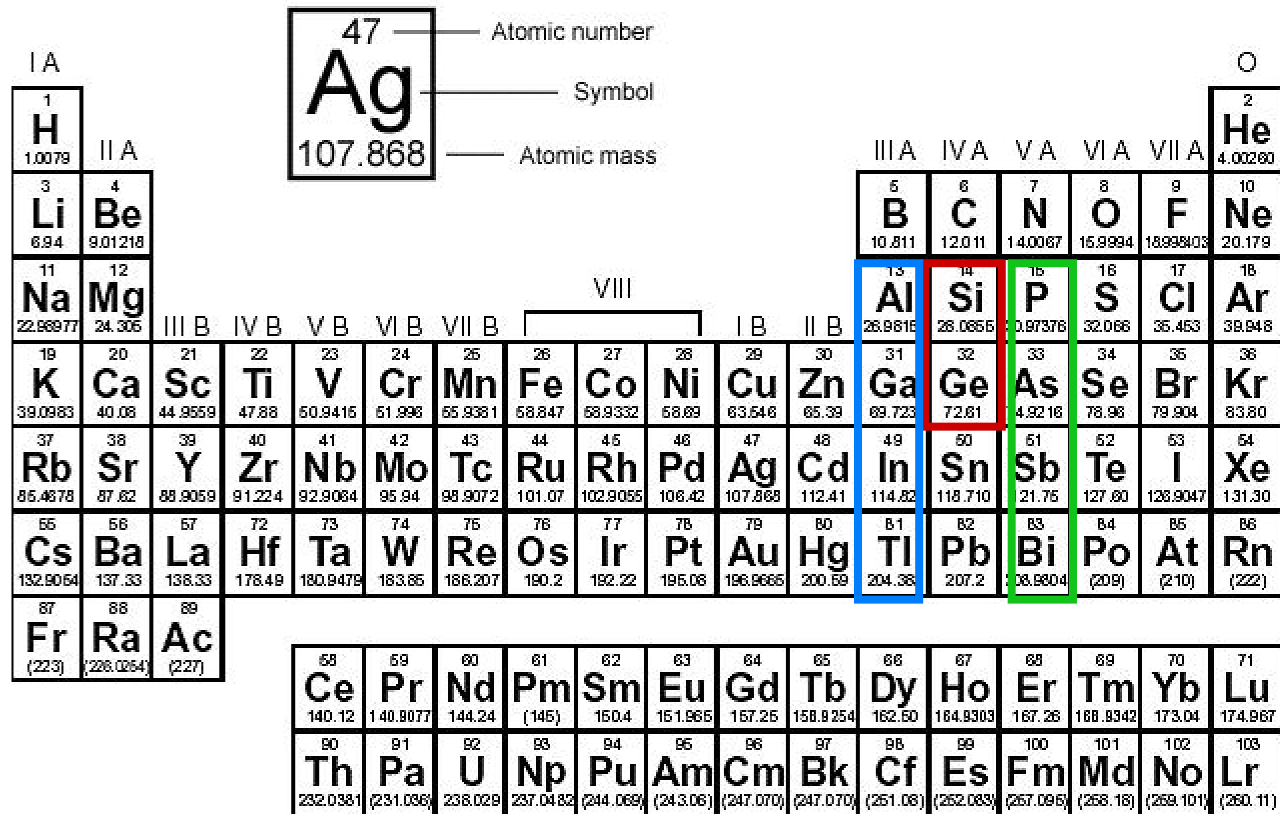
⇨ Only depends on physical properties

Resitivity of Materials

Metals	Semiconductors	Insulators
10^{-6} to 10^{-4} Ω-cm	10^{-3} to 10^{+8} Ω-cm	> 10^{+8} Ω-cm
– Upper electron shells nearly empty	– Partially filled shells – Bonds covalently to form weakly stable structures	– Completely filled shells

Preliminary Concepts

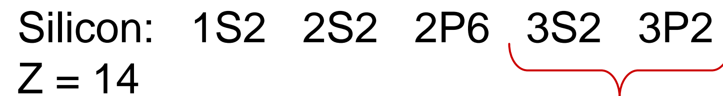
- Semiconductors on the Periodic Chart



Preliminary Concepts

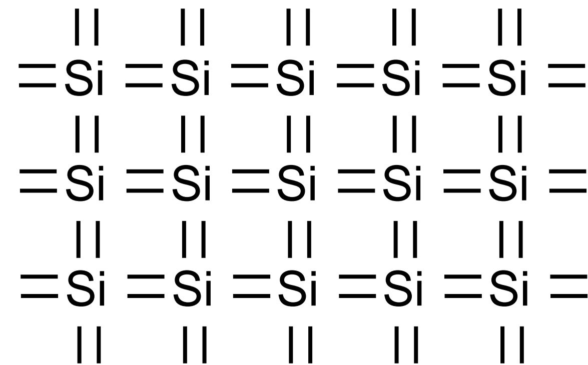
- Atomic Structure of Silicon – Group IVA
  - Electron structure

4 empty positions in the 3P shell



4 / 8 positions filled

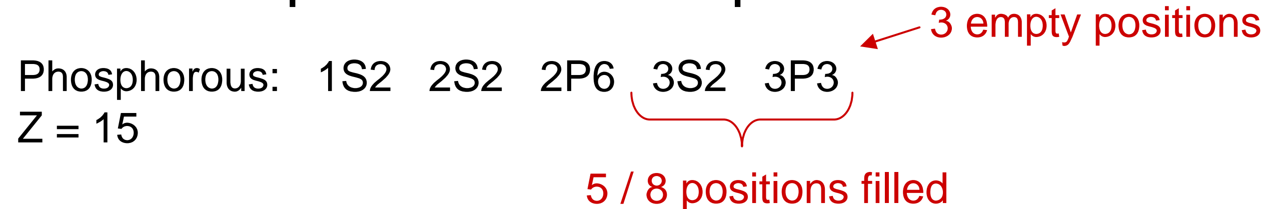
  - Represented as: –Si– ← Each line is an electron in the 3rd shell
  - Covalent Bonding
    - Intrinsic silicon bonds covalently in a crystalline structure, sharing electrons with neighbors to completely fill the 3P shell



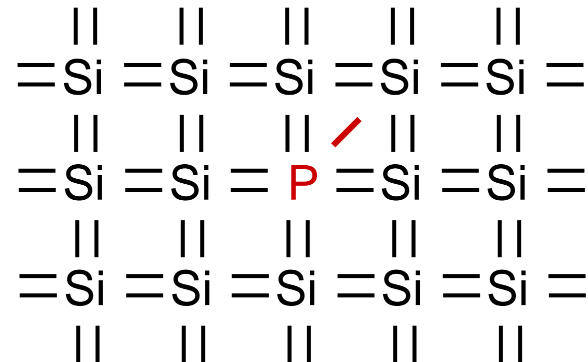
⇨ Bonds can break from thermal energy or E field to give mobile charge

Preliminary Concepts

- Adding Impurities into Silicon
  - Consider Phosphorous – Group VA

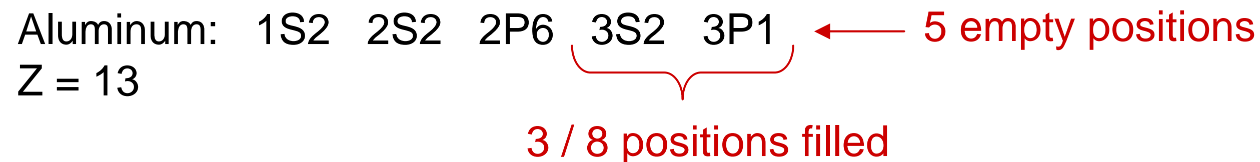


  - Represented as: — P — ← Each line is an electron in the 3rd shell
  - Introduction into Silicon Crystalline Structure
    - Extra electron is weakly bound, and easily removed
      → ***Donor Impurity***

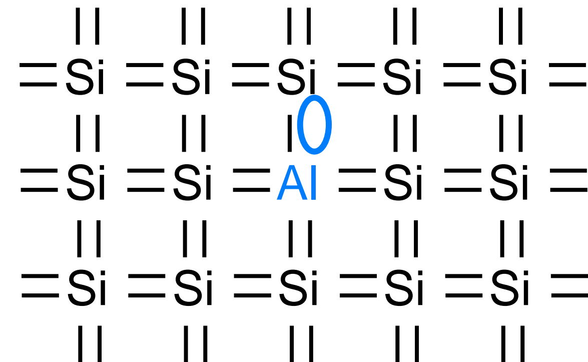


Preliminary Concepts

- Adding Impurities into Silicon (Continued)
  - Consider Aluminum = Group IIIA



  - Represented as: — Al — ← Each line is an electron in the 3rd shell
  - Introduction into Silicon Crystalline Structure
    - Missing electron is weakly accepted into lattice
      → ***Acceptor Impurity***
    - Concept of mobile ***"holes"***
      - When electron is captured, hole moves from location to location



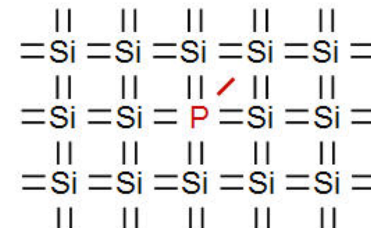
Preliminary Concepts

- Adding Impurities into Silicon (Continued)

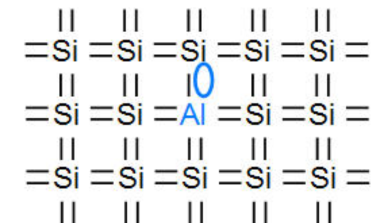
  - Introduction of impurities into intrinsic silicon is called ***"Doping"***

  - Amount of doping characterized by concentration of charge carriers
    - n_i = # intrinsic carriers in pure silicon / unit volume $\approx$ 1.4E10 / cm^3 @ 300° K
    - N_d = # donor atoms / unit volume
    - N_a = # acceptor atoms / unit volume

  - ***N-type Silicon***
    - $N_d - N_a >> n_i$
      - High concentration of donor atoms
      - Provides excess electrons to lattice as mobile charge carriers



  - ***P-type Silicon***
    - $N_a - N_d >> n_i$
      - High concentration of acceptor atoms
      - Provides excess holes to lattice as mobile charge carriers

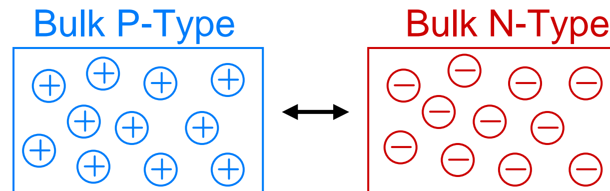


Preliminary Concepts

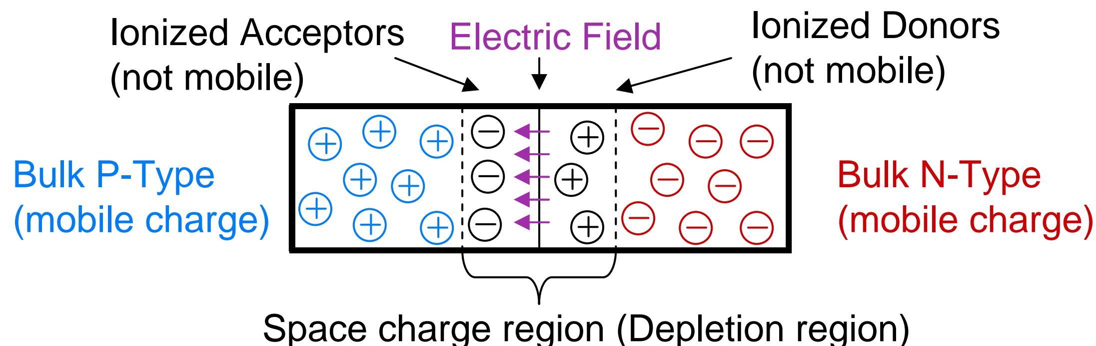
- Adding Impurities into Silicon (Continued)
  - How to make use of mobile charge carriers
    - Bonds can be broken by:
      - Application of an Electric Field
        - » Basic principle of how integrated circuits work
      - Application of Light → Photons impart energy
        - » Basic principle of how photo cells work
        - » Use reverse principle for light emitting diodes (LEDs)
      - Heat → Kinetic Energy
        - » Basic use for temperature sensors
        - » Generally a bad property for semiconductors…

PN Junctions

- Forming a PN Junction
  - Take P-type & N-type silicon, and butt them together



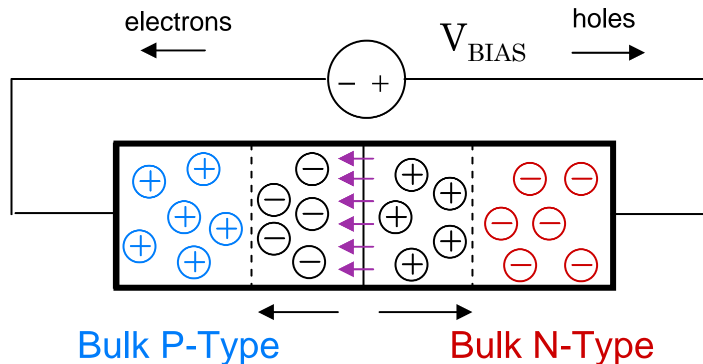
  - When butt together, opposite charges attract
    - Mobile electrons from N-type silicon attracted to vacancies in P-type
    - Mobile holes from P-type silicon attracted to vacancies in N-type
    - ⇨ ***Results in Acceptor & Donor atoms being ionized***
    - ⇨ ***Creates space charge regions***
    - ⇨ ***Results in the creation of a built-in Electric Field***



PN Junctions

- Biasing a PN Junction

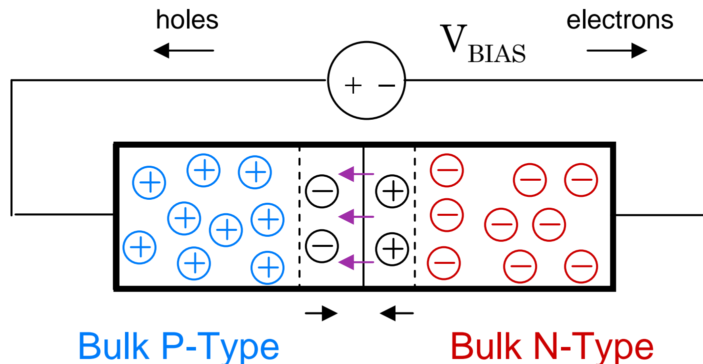
  - Suppose apply a voltage to the PN Junction



  - Positive terminal of V_{BIAS} attracts electrons
  - Negative terminal of V_{BIAS} attracts holes
  - Makes space charge region bigger
  - Increases E field across junction
  - Reduces ability of current to flow across junction

  ⇨ ***Reverse Bias***

  - Now suppose we reverse the polarity of V_{BIAS}



  - Positive terminal of V_{BIAS} adds holes to P region
  - Negative terminal of V_{BIAS} adds electrons to N
  - Makes space charge region smaller
  - Decreases E field across junction
  - Enhances ability of current to flow across junction

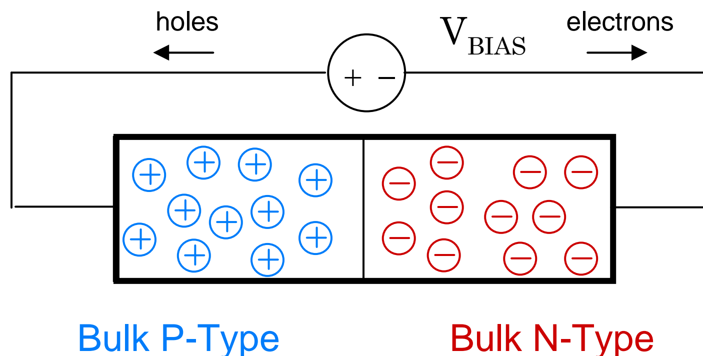
  ⇨ ***Majority Carrier:***

  Holes recombine with ionized acceptors
  Electrons recombine with ionized donors

PN Junctions

- Biasing a PN Junction (Continued)

  - At a critical bias, space charge region disappears



- Built-in E field across junction is gone
- Now charge carriers provided by V_{BIAS} can move across PN junction

⇨ ***Forward Bias → Conduction***

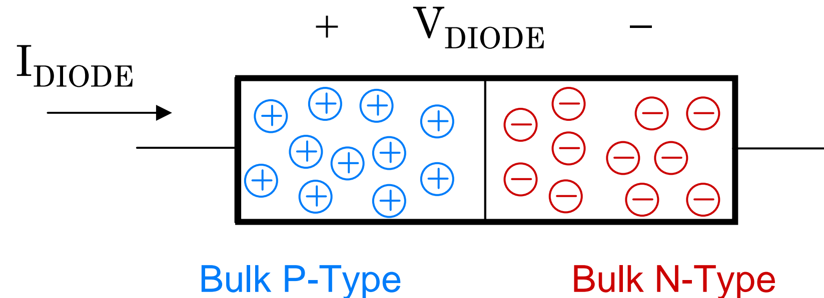
⇨ ***Each new electron/hole pair pushes existing pair out of bulk***

  - How much voltage is required to reach forward bias?
    - Answer: Related to how much energy is required to remove bound electrons (or holes) from their nuclei → Work Function
      - Depends on doping concentrations
      - Depends on intrinsic carrier concentration
      - Depends on temperature

$$\phi = kT/q \ \ln [N_d N_a / n_i^2]$$

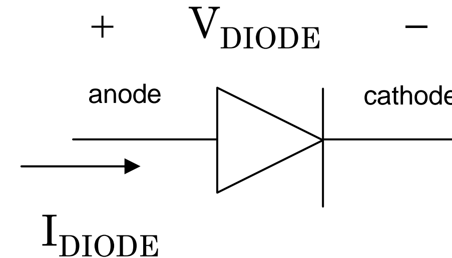
Diodes

- Physical Description
  - Essentially a simple PN Junction



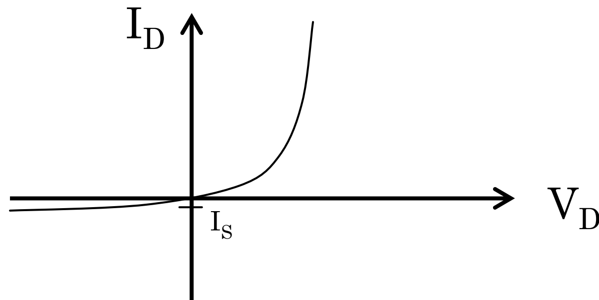
Bulk P-Type   Bulk N-Type

  - Symbol



- IV Characteristics
  - Shockley Diode Equation

$$I_D = I_S \left[e^{-[k V_D / (n q T)} - 1 \right]$$



⇨ Nonlinear IV relationship

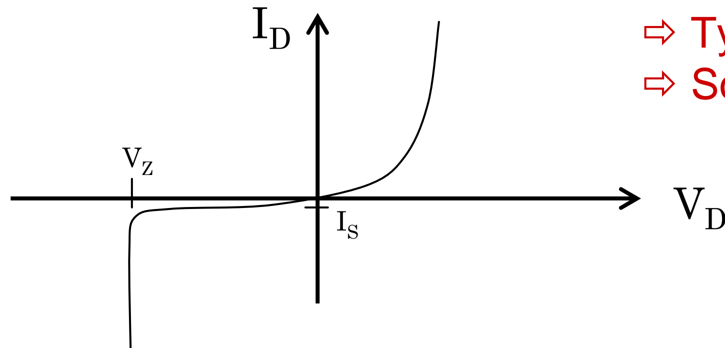
Where: I_S = Reverse Saturation Current
k = Boltzman Constant (1.38E-23 J/K)
T = Temperature (º Kelvin)
q = charge (1.6E–19 C/e⁻)
n = quality factor, $1 \geqq n \geqq 2$

V_T = k T / q = 25.8 mV @ room temp
= Thermal Voltage

⇨ In most diodes, I_S is very small

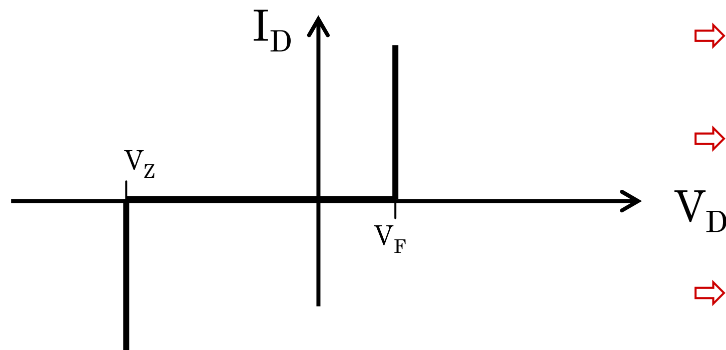
Diodes

- IV Characteristics (Cont.)
  - Many diodes exhibit reverse breakdown → Zener Effect



⇨ Typical values: V_Z ~ 5V – 15V
⇨ Sometimes used for voltage references

  - Ideal Characteristics
    - Sometimes, it is useful to use a linear approximation

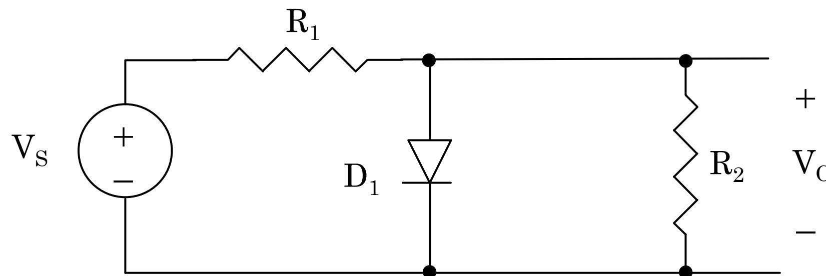


⇨ Typical values V_F ~ 0.6V – 0.7V for Si
→ Looks like Voltage Source!
⇨ Approximates current flow in one direction only

⇨ Looks like a switch!

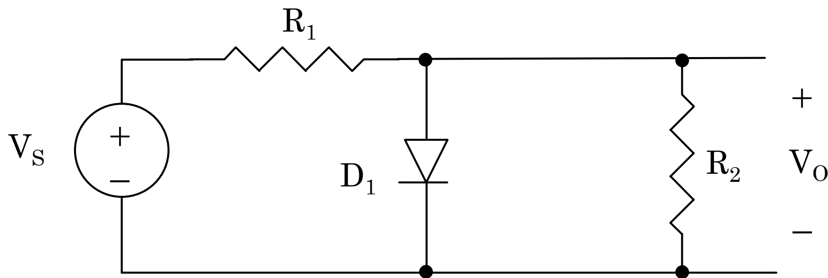
Diodes

- Circuits
  - Rarely use Shockley equation in hand calculations
  - SPICE uses Shockley equation or behavioral models
    - Gives accurate solution
  - For hand calculations – 2 methods:
    - Use linear approximation
    - Use graphical techniques

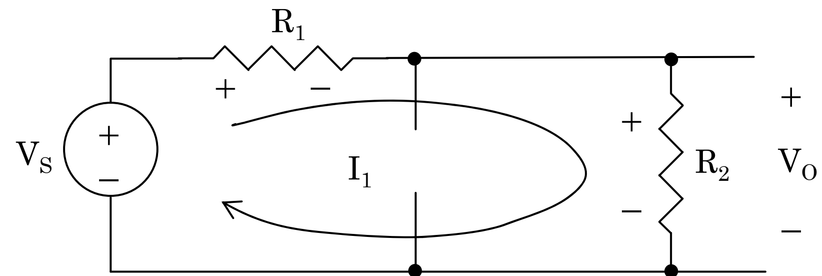


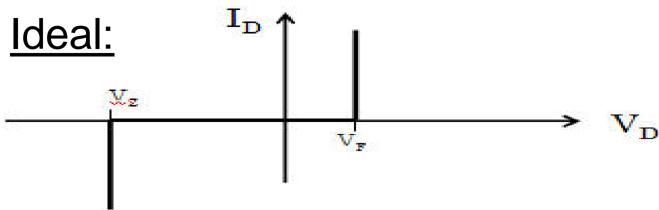
Diodes

- Circuits (Continued
  - Example – Use Linear Approximation:



If diode is OFF:



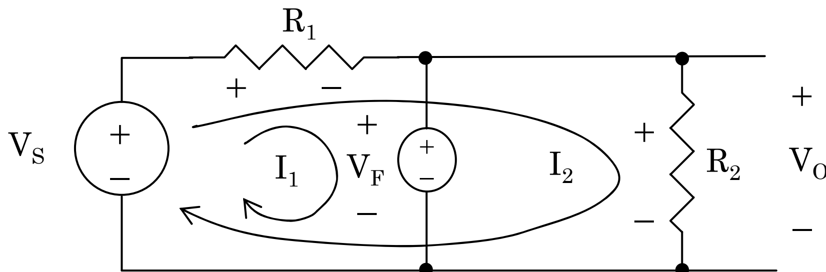


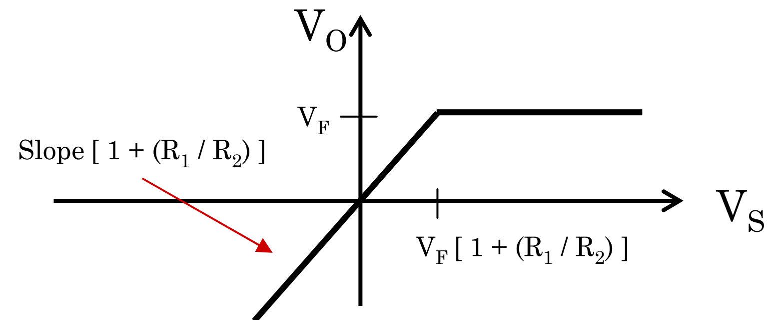
$V_O = V_S\, R_2 / (R_1 + R_2)$

Valid for: $V_O < V_F$

Or: $V_S < V_F\ [\, 1 + (\, R_1 / R_2)\,]$

If diode is ON:





$V_O = V_F$

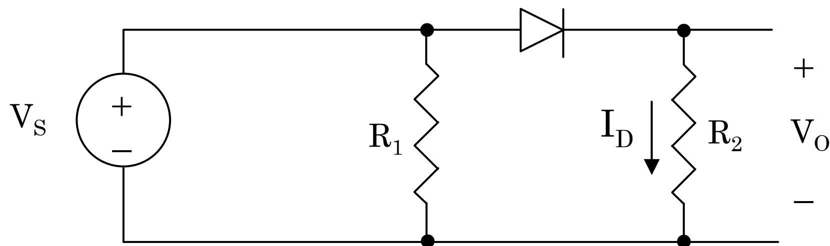
Valid for: $I_1 > 0$

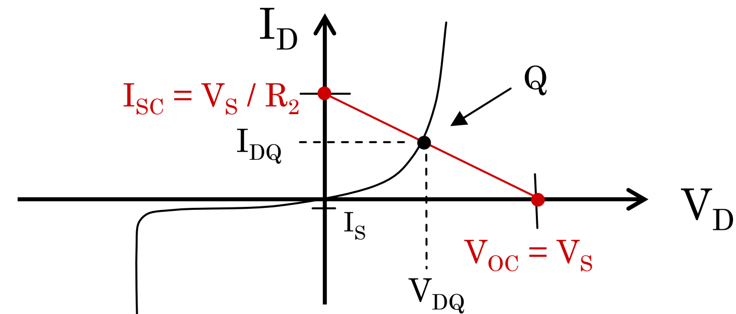
Or: $V_S > V_F\ [\, 1 + (R_1 / R_2)\,]$

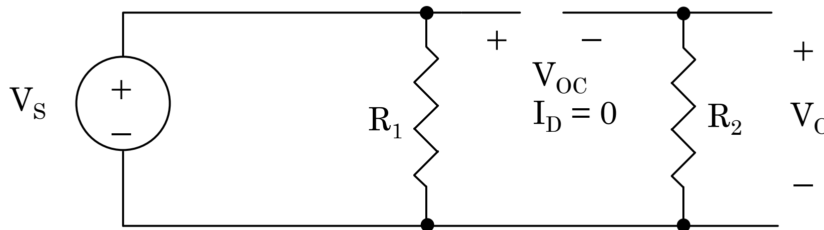
⇨ Called a Clamp Circuit

Diodes

- Circuits (Continued)
  - Example – Use Graphical Methods → Load Line Analysis:
    - Take Diode out – Calculate open-circuit voltage → $I_D = 0$
    - Then replace diode with short – Calculate short circuit current → $V_D = 0$
    - Plot on diode IV graph → Find Operating Point Q



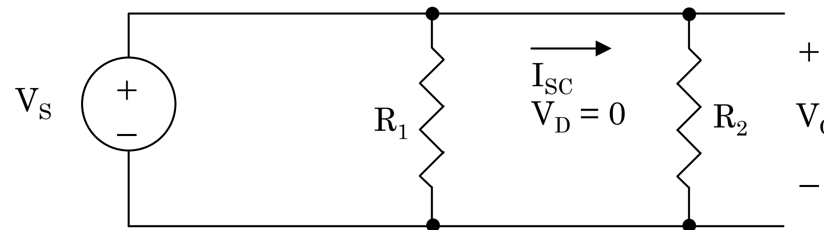




$V_{OC} = V_S$

Then:

$V_O = I_{DQ} R_2$



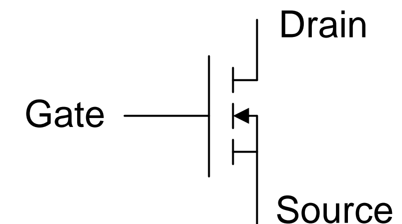
$I_{SC} = V_S / R2$

⇨ Don't always have the IV curves for particular diodes…

Field Effect Transistors

- Introduction

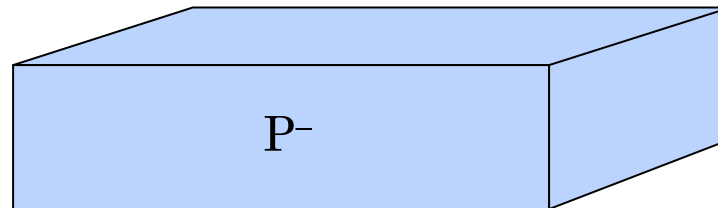
  - Field Effect Transistors (FETs) are 3-terminal devices, where the current flow between two of the terminals (Drain & Source) is controlled through the use of an electric field applied at the third terminal (Gate), which modulates a conduction channel between the two active terminals.
    - Current flow is achieved by drift currents through the channel
    - Charge carriers are majority carriers (p-type → holes, n-type → electrons)
    - Current flow is uni-directional



  - Several different kinds:
    - Metal Oxide Semiconductor FET (MOSFET) ← We will focus on this today
      - ⇨ Used extensively in HEP
      - ⇨ Custom ASIC design!
    - Junction FET (JFET)
    - Metal Oxide Semiconductor FET (MESFET)
    - High Electron Mobility Transistor (HEMT)
    - Depleted FET (DEPFET)
    - (Many other variations…)

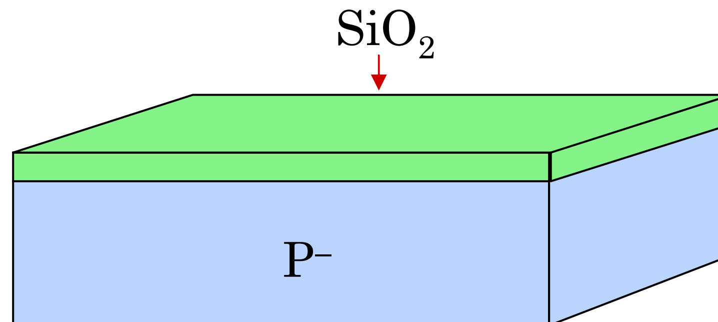
MOSFETs

- Basic Construction
  - Begin with lightly-doped P-type substrate (could be N-type as well…)



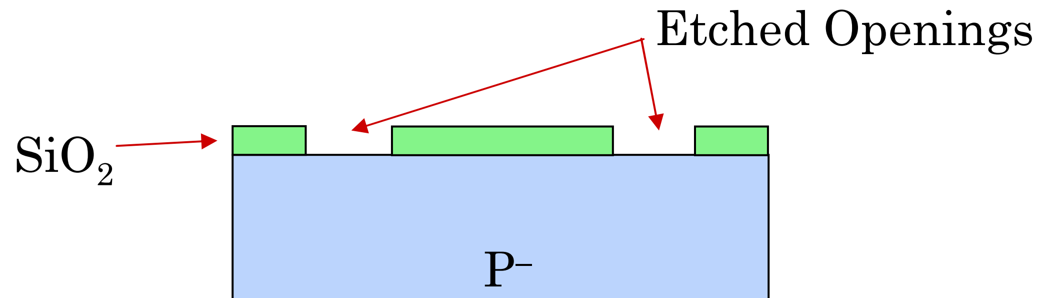
  - Cover surface with layer of silicon dioxide (SiO2)
    - Like glass
    - Insulator → Very high resistivity → ρ ~ 1E18 Ω-cm

⇨ Very Important Aspect!

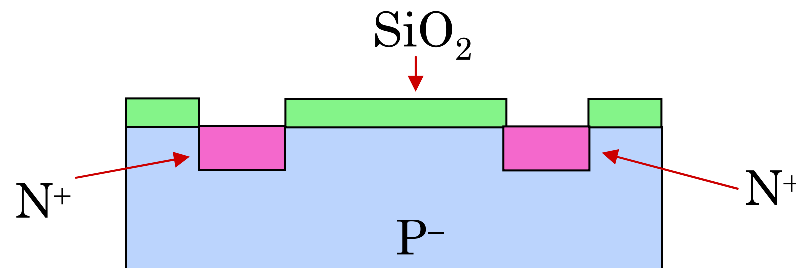


MOSFETs

- Basic Construction (Continued)
  - Etch openings into the SiO_2 using hydrofluoric acid (HF)
    - Dissolves SiO_2 but not the silicon underneath

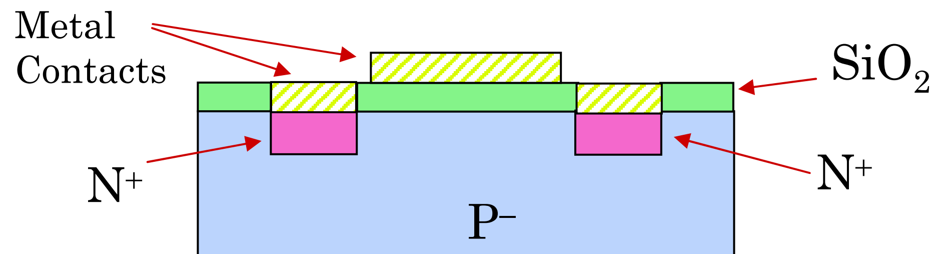


  - Diffuse donor impurities into substrate to make N-type implants
    - Heavy doping → N^+

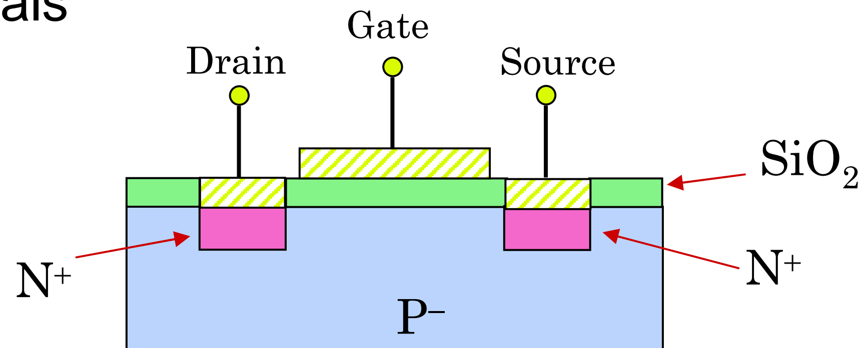


MOSFETs

- Basic Construction (Continued)
  - Add metal contacts
    - Applied using Sputtering or Evaporating Metal

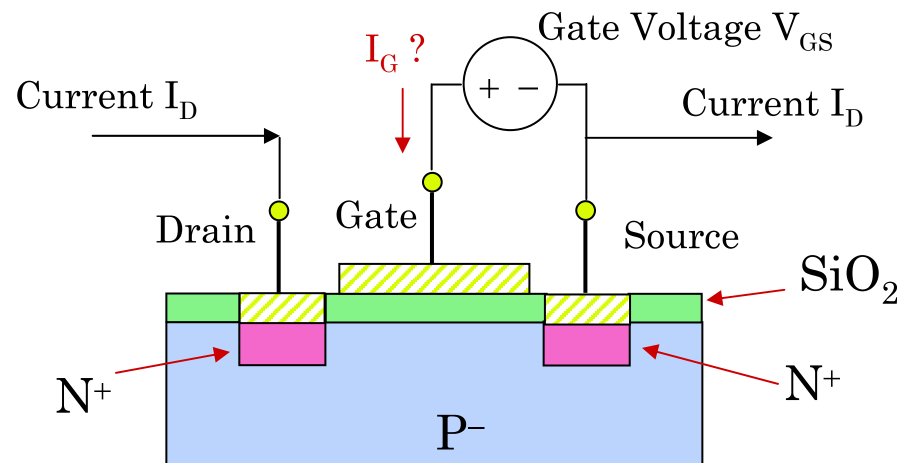


  - Basic construction done
    - All process steps done with masks → lithography
  - Define terminals



MOSFETs

- Basic Operation
  - Idea is to use the Drain and Source terminals for conduction, and to control the flow of current through these terminals by applying a voltage to the Gate

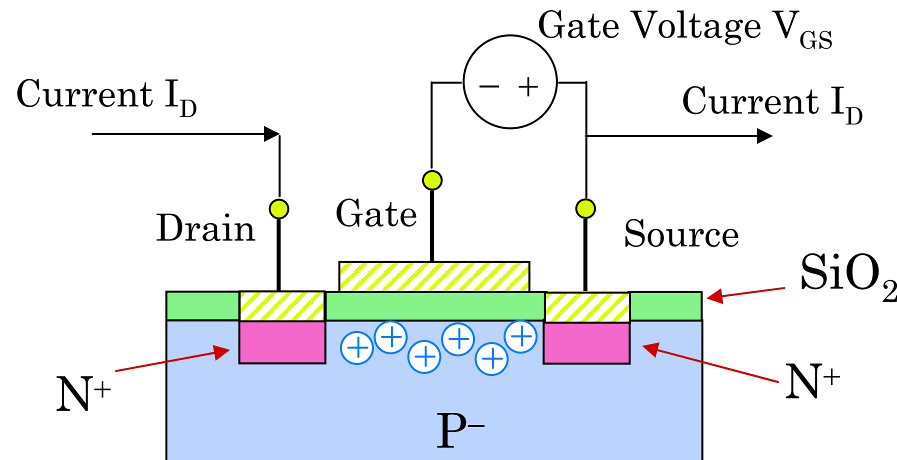


⇨ Current $I_G = 0$ due to SiO_2

  - There are three states of operation:
    - Accumulation
    - Depletion
    - Inversion

MOSFETs

- Basic Operation (Continued)
  - ***Accumulation***
    - Occurs when Gate voltage creates an electric field in the region between the N wells that attracts majority carriers → holes
    - To attract holes in a P-type substrate, use a negative gate voltage

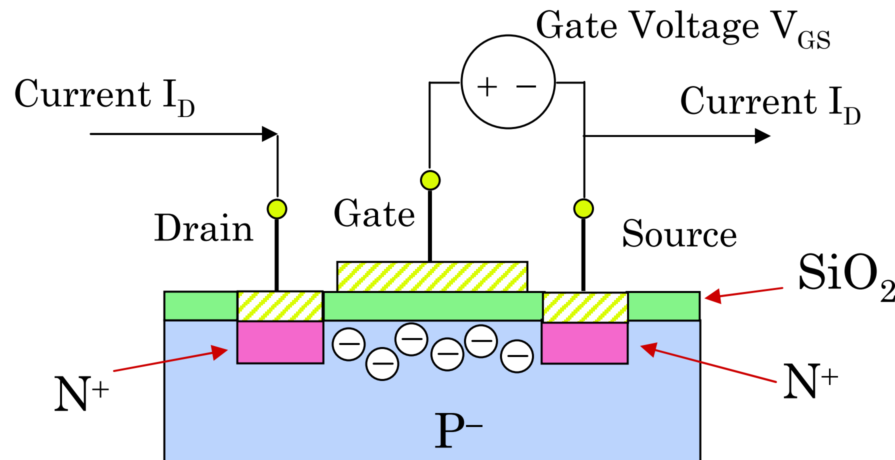


- The electric field lines from the Gate terminate on the accumulated holes, so that there is no attraction of electrons from the Drain and Source regions

  ⇨ Results in no current flow between Drain and Source

MOSFETs

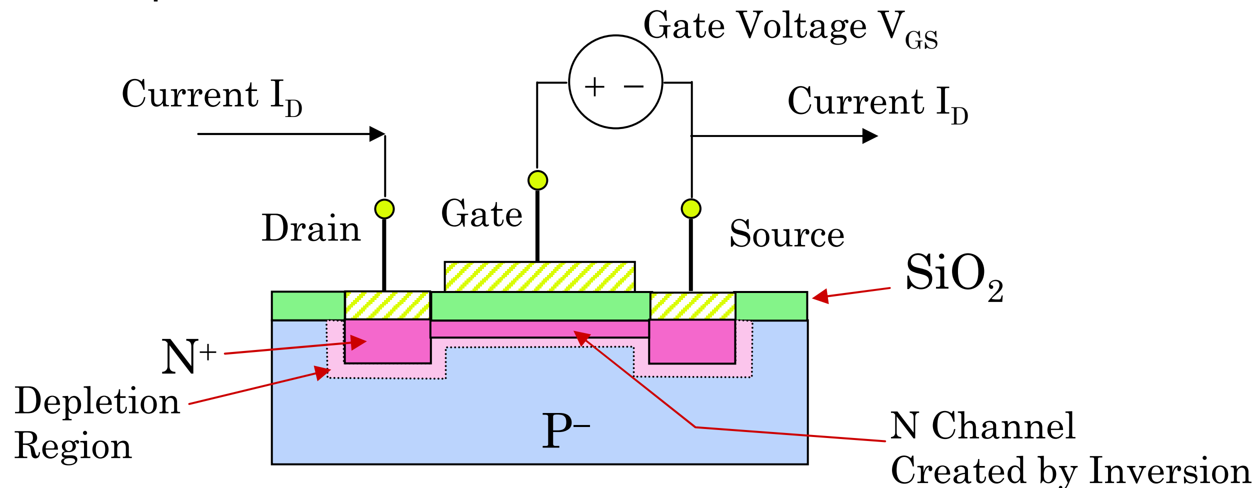
- Basic Operation (Continued)
  - ***Depletion***
    - Occurs when Gate voltage creates an electric field in the region between the N implants that <u>repels majority carriers</u> → holes
    - To repel holes in a P-type substrate, use a positive gate voltage



    - Note that charge under Gate region is fixed charge, created by removing holes from their acceptor atoms in the P substrate
    - The electric field lines from the Gate terminate on the depleted acceptor atoms
      - ⇨ Results in no current flow between Drain and Source

MOSFETs

- Basic Operation (Continued)
  - ***Inversion***
    - Occurs when Gate voltage reaches a critical point, where electrons begin to be attracted from N^+ Drain and Source regions
      - Forms an N-type channel between the Drain and Source
      - Density of electrons in the channel ~ density of donor atoms in the N^+ implants

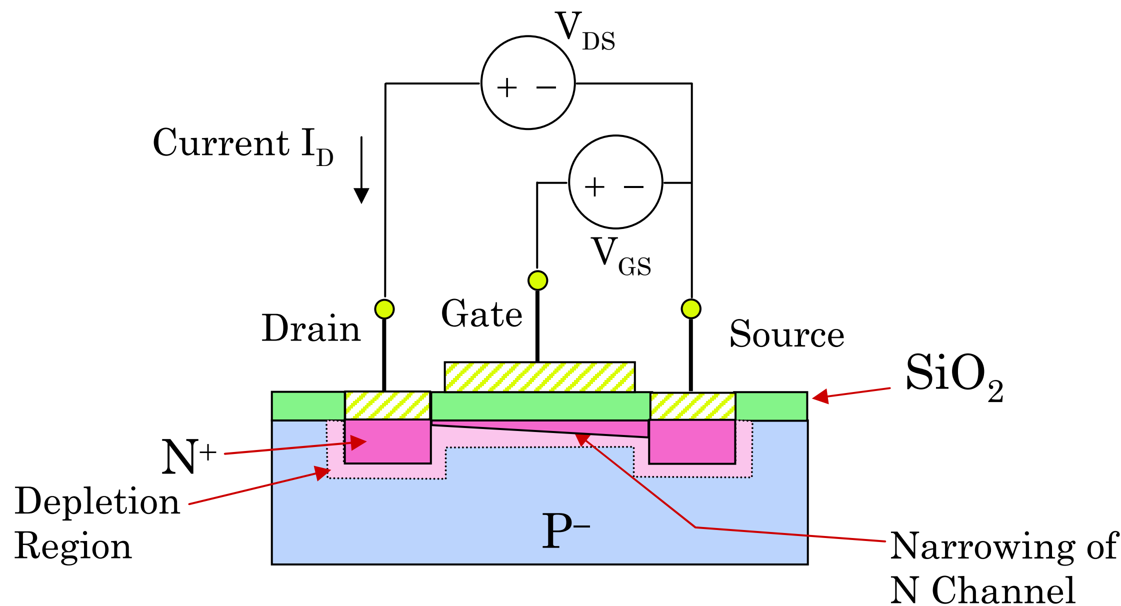


    - Now can have flow of electrons from Drain to Source
    - Current flow is controlled by the Gate Voltage
    - The point at which the Gate voltage creates a conductive channel under the Gate is called the Threshold Voltage V_{Th}

$$V_{GS} \geq V_{TH}$$

MOSFETs

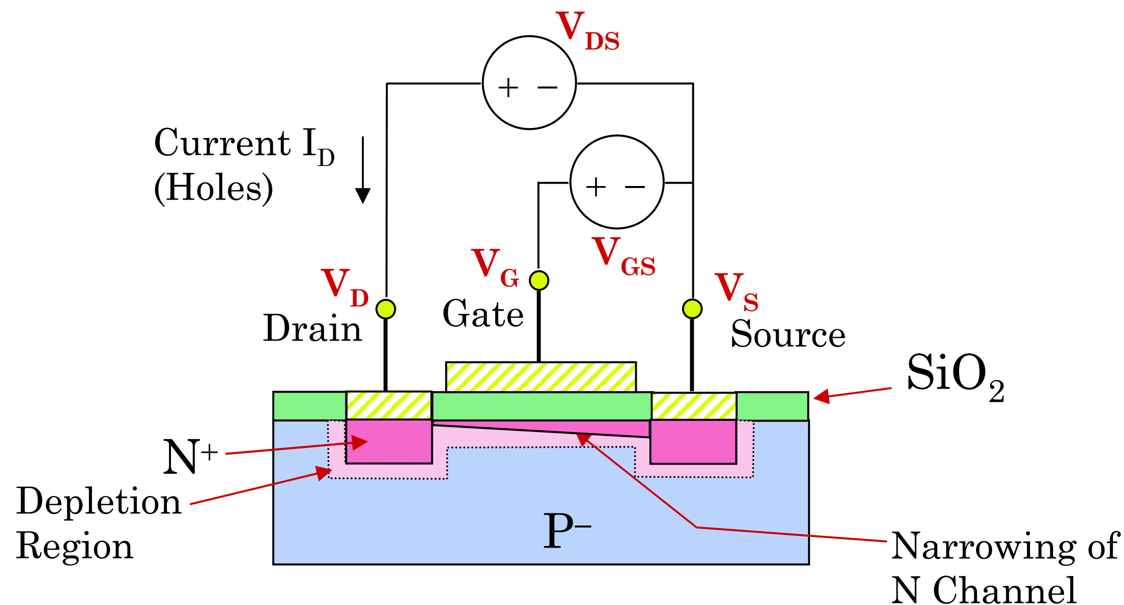
- Basic Operation (Continued)
  - ***Inversion*** (Continued)
    - Suppose now connect a voltage source between Drain and Source
      - Allows current to flow between Drain and Source
      - Results in voltage drop across channel
        → Channel begins to narrow at Drain end



      - Holes pumped into the Drain recombine with ionized acceptors in the channel near the Drain
      - Electric field from the Gate is not strong enough to sustain the full width of the channel at the Drain, resulting in a narrowing of the channel

MOSFETs

- Basic Operation (Continued)
  - ***Inversion*** (Continued)
    - If there is a voltage drop across the channel, then the voltage at the drain must be greater than at the source:



For the channel to exist:

$$V_{GS} > V_{TH}, \quad V_{GD} > V_{TH}$$

Then:

$$V_{GD} = V_{GS} + V_{SD} > V_{TH}$$

Or:

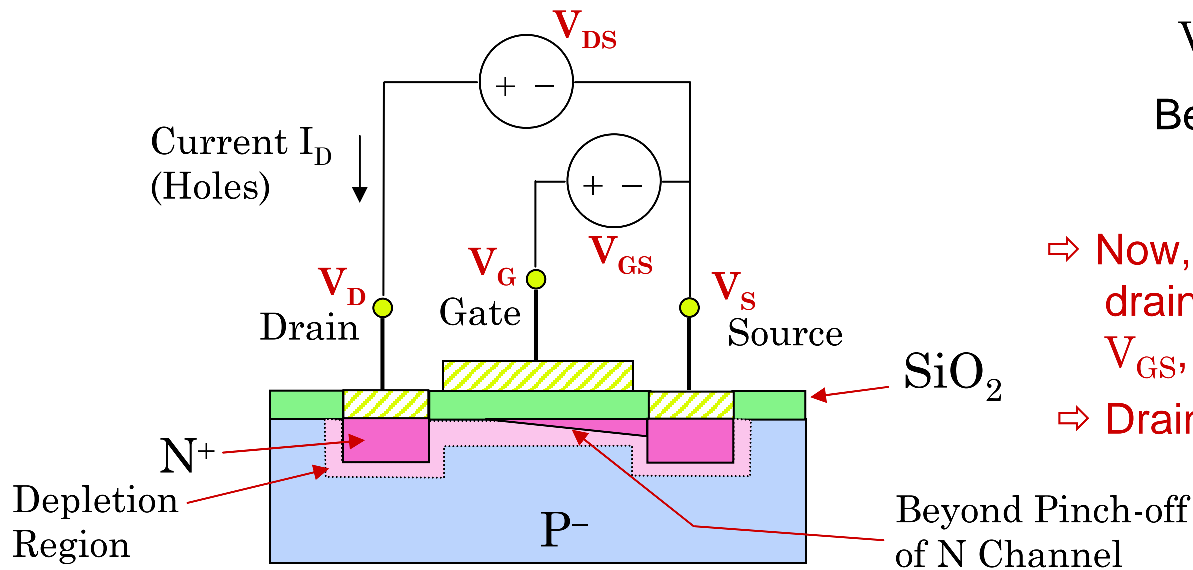
$$V_{DS} < V_{GS} - V_{TH}$$

– It can be shown that, for this mode of operation, <u>the voltage drop in the channel is resistive</u>, and that the current I_D is given by:

$$I_D \approx K\, V_{DS}\, [\, V_{GS} - V_{TH}\,], \text{ valid for } V_{DS} < V_{GS} - V_{TH}$$

MOSFETs

- Basic Operation (Continued)
  - ***Inversion*** (Continued)
    - As continue to increase V_{DS}, channel reaches a point where the width goes to 0 at the Drain ***→ Pinch-Off***
    - As continue to increase VDS, channel begins to recede at the Drain ***→ Beyond Pinch-Off***



At Pinch-off:

$$V_{DS} = V_{GS} - V_{TH}$$

Beyond Pinch-off:

$$V_{DS} > V_{GS} - V_{TH}$$

⇨ Now, current flow from drain to source depends only on V_{GS}, not on resistance in channel

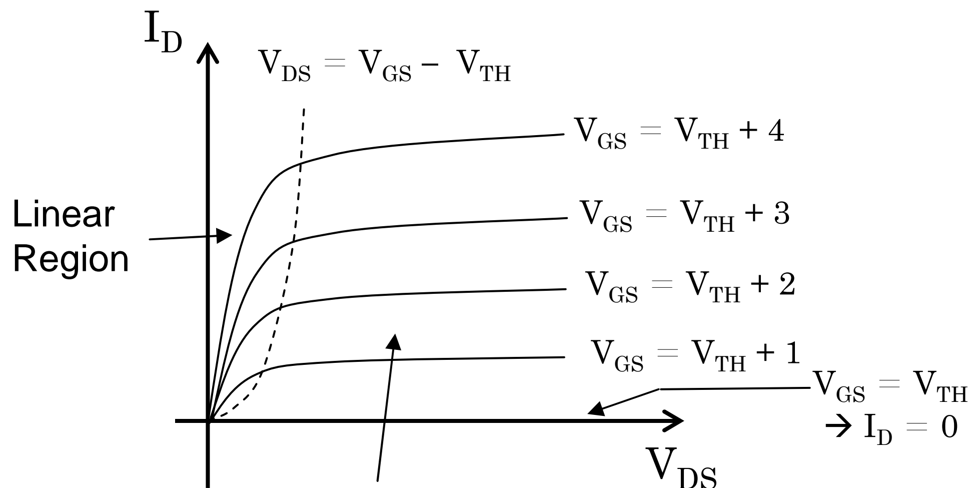
⇨ Drain looks like current source!

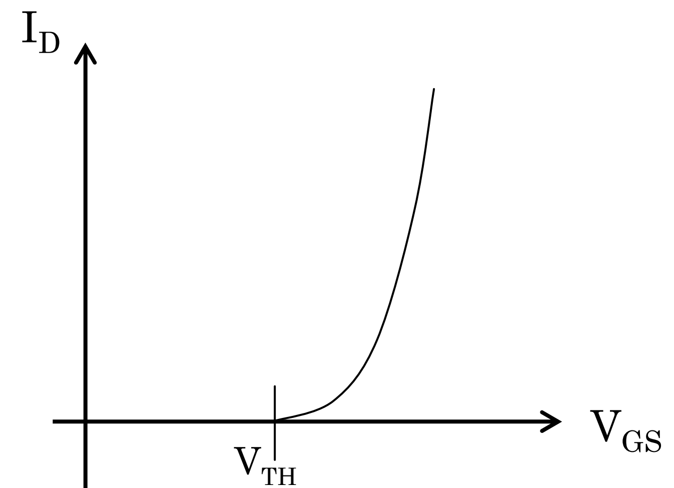
– It can be shown that for Beyond Pinch-off, <u>the Drain looks like a current source</u>, independent of V_{DS}, and that the current I_D is given by:

$$I_D \approx K/2 \; (V_{GS} - V_{TH})^2 \text{ , valid for } V_{DS} \geq V_{GS} - V_{TH}$$

MOSFETs

- IV Characteristics
  - Have defined 2 regions of operation
    - Linear region → IV characteristics look resistive → Voltage-controlled resistor
    - Beyond Pinch-off → IV characteristics look like a current source
  - Typically plot I_D versus V_{DS} as a function of V_{GS} ⇨ Family of curves





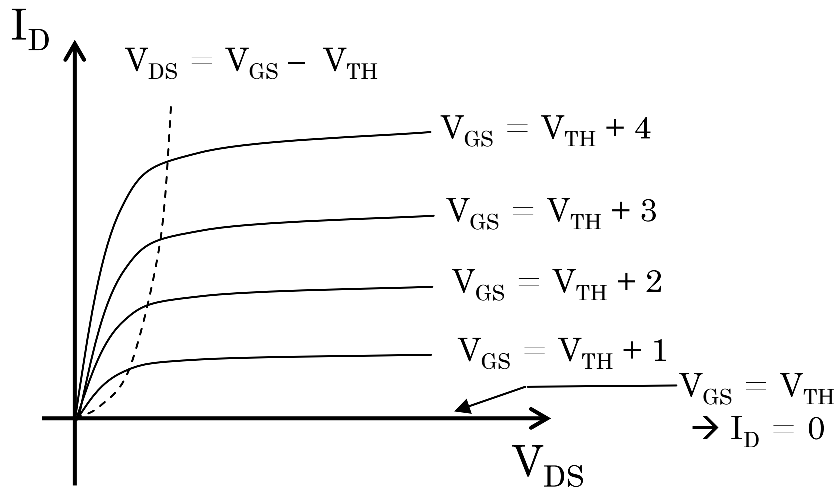
I_D vs V_{GS} in the Active Region

- Linear Region: $I_D = K\, V_{DS}\ [\, V_{GS} - V_{TH}\,]$, valid for $V_{DS} < V_{GS} - V_{TH}$

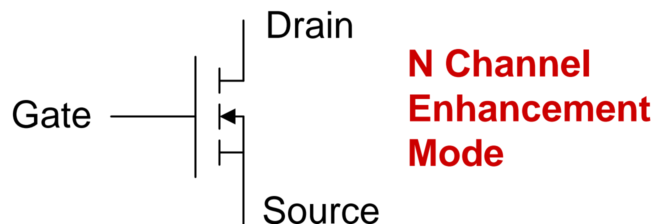
- Active Region: $I_D = K/2\ (V_{GS} - V_{TH})^2$, valid for $V_{DS} \geq V_{GS} - V_{TH}$

MOSFETs

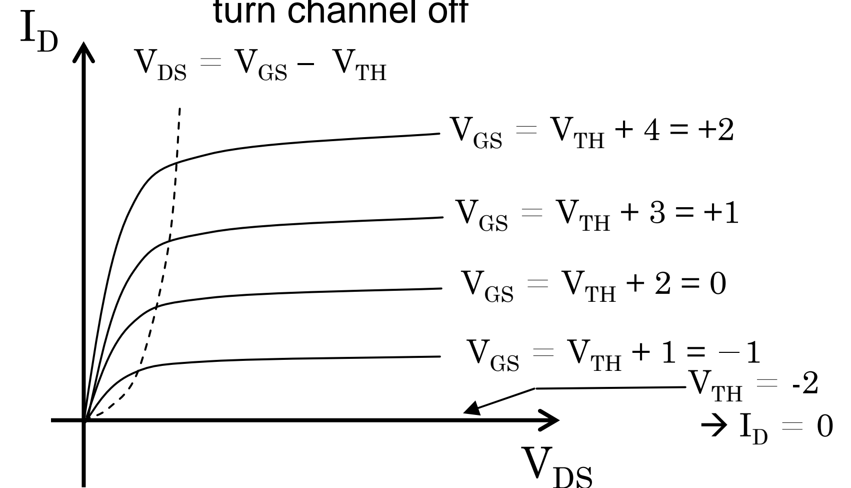
- Types of N-Channel MOSFETs
  - Enhancement Mode FETs
    - Channel does not exist at $V_{GS} = 0$
      - This is what has been described previously
      - Must provide bias V_{GS} to create channel



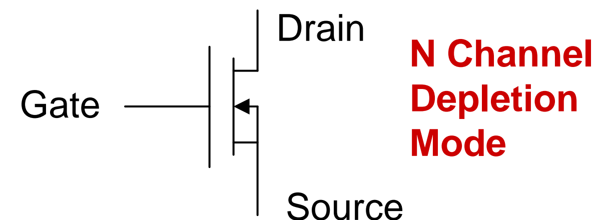
    - Electrical Symbol



  - Depletion Mode FETs
    - Channel does exist at $V_{GS} = 0$
      - These devices are made this way through doping the channel
      - Must provide negative bias V_{GS} to turn channel off



    - Electrical Symbol

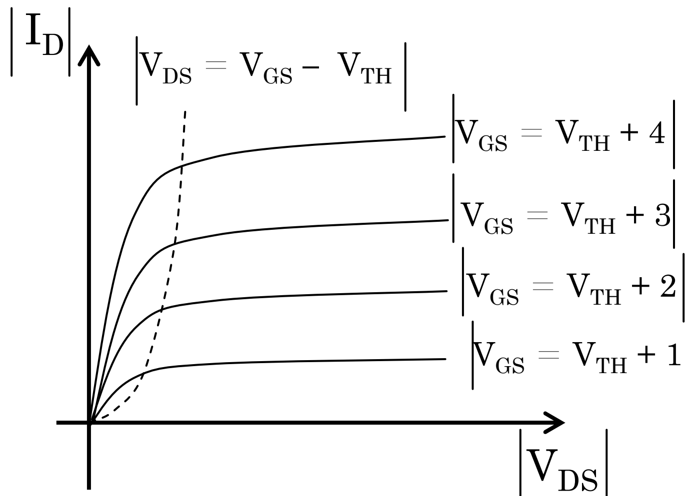


MOSFETs

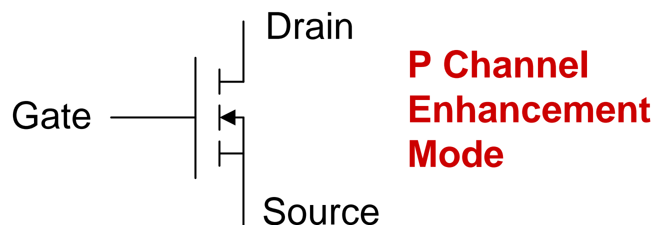
- Types of P Channel MOSFETs ⇨ Everything is reversed…

⇨ Same plots, just use absolute value signs…

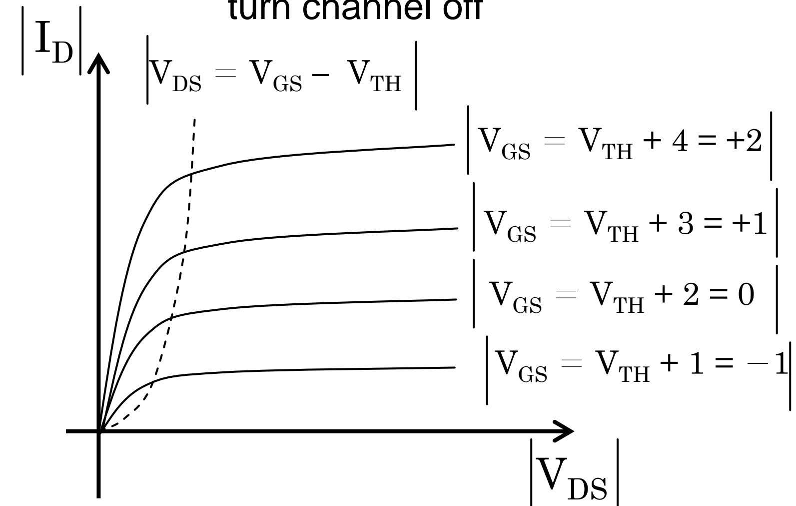
- Enhancement Mode FETs
  - Channel does not exist at $V_{GS} = 0$
    - Must provide bias V_{GS} to create channel



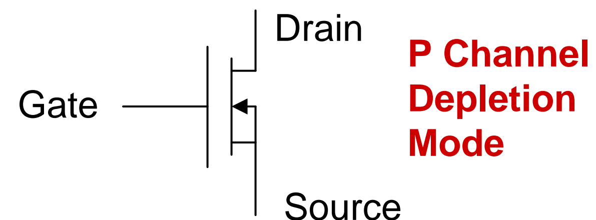
  - Electrical Symbol



- Depletion Mode FETs
  - Channel does exist at $V_{GS} = 0$
    - Must provide negative bias V_{GS} to turn channel off

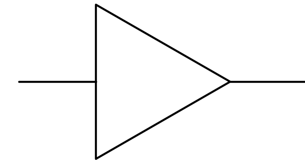


  - Electrical Symbol

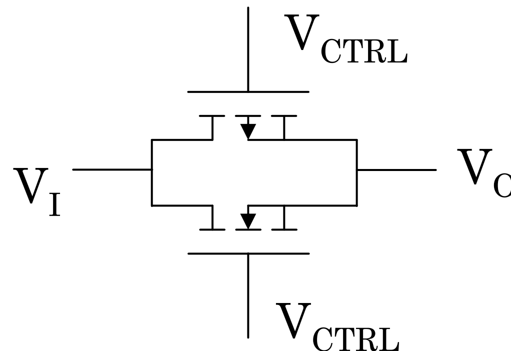


MOSFETS

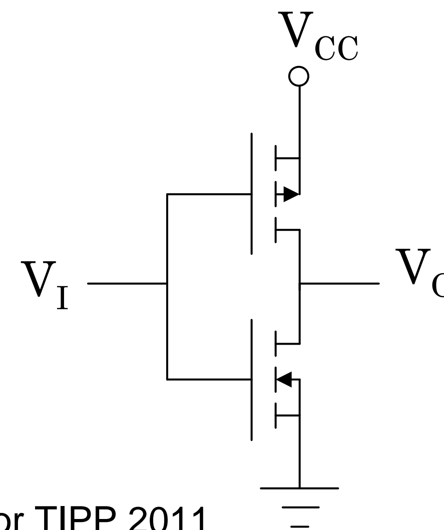
- Circuit Applications
  - Linear circuits → Amplifiers
    - Voltage-controlled current source with gain
    - Excellent when need high input impedance



  - Analog Switches

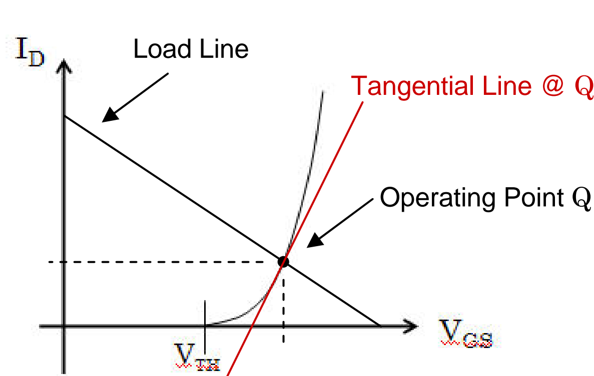


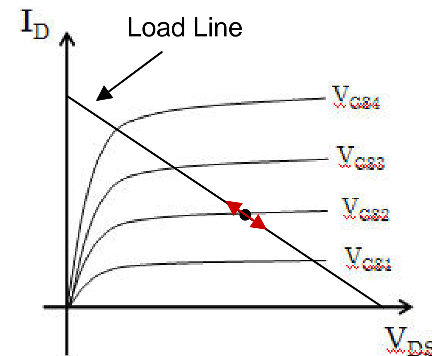
  - Digital Logic → CMOS



MOSFETs

- Linear Circuit Models (N channel Enhancement Mode)
  - Properties:
    - High impedance between Gate and Source
    - In Active Region, Drain-Source looks like a voltage-controlled current source
    - Generally, there are two types of models:
      - DC biasing
      - AC performance
  - General Approach
    - Find DC operating point
    - AC parameters found from small excursions around operating point





AC Transconductance: $g_m = \partial I_D / \partial V_{GS} \Big|_Q$

Found at Operating Point Q

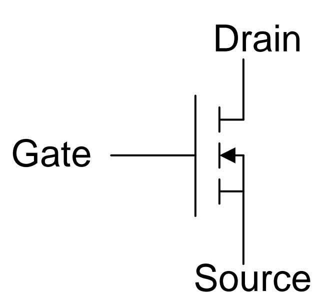
Generally, AC response occurs at small deviations around Operating Point

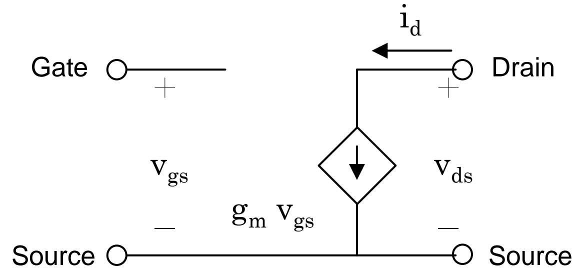
⇨ **Output will be the sum of the DC operating point + the AC response**

MOSFETs

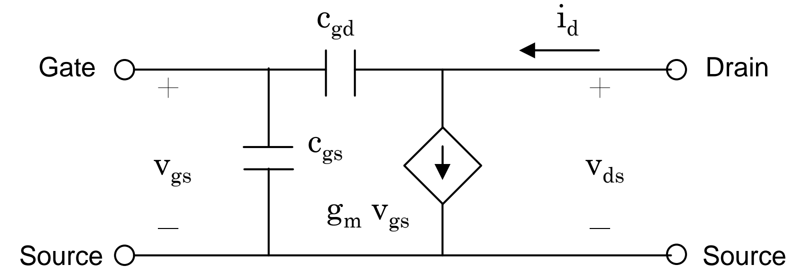
- Linear Circuit Models (N channel Enhancement Mode) (Continued)
  - AC Model (assumes operation in active region)
    - Includes voltage-dependent current source with transconductance g_m
    - Sometimes includes parasiitic capacitances between Gate and Drain c_{gd}, and between Gate and Source c_{gs}

    ⇨ Usually, FET parameters are supplied by the manufacturer





Mid-Frequency AC Model

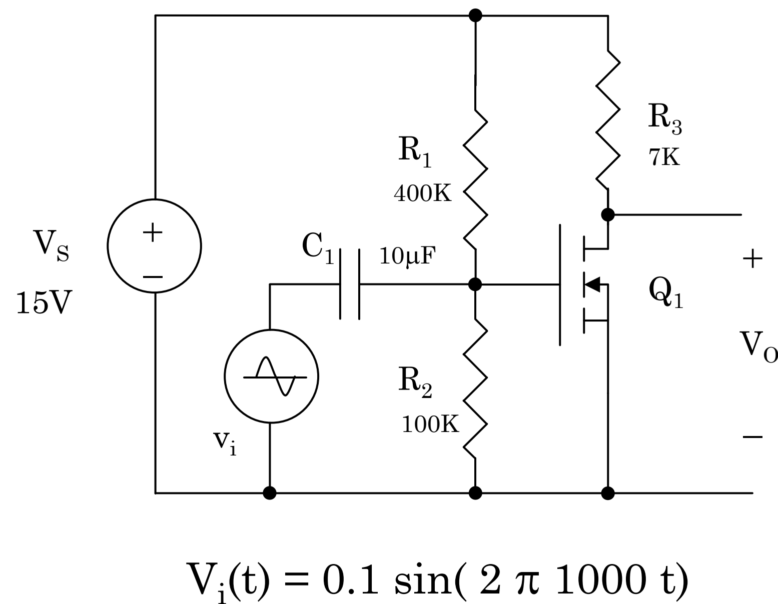


High Frequency AC Model

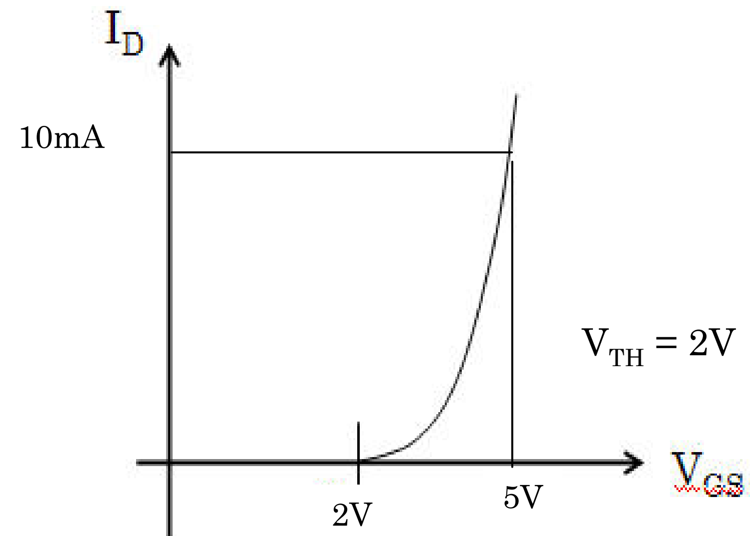
  - Spice Models
    - Level 2: Use equations
    - BSIM: Behavorial
      - Much more accurate
      - Takes advantage of knowing process parameters
      - Used extensively for ASIC design

MOSFETs

- Linear Circuits
  - Example – Common Source Amplifier – N-channel, Enhancement Mode



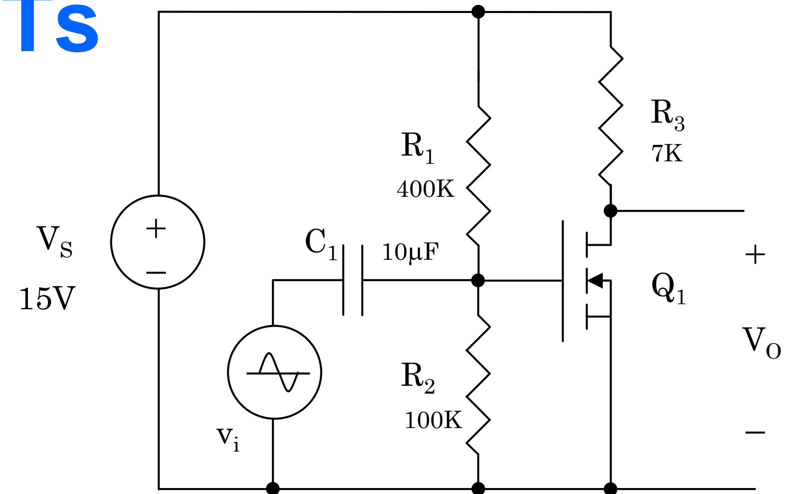
Data from Manufacturer



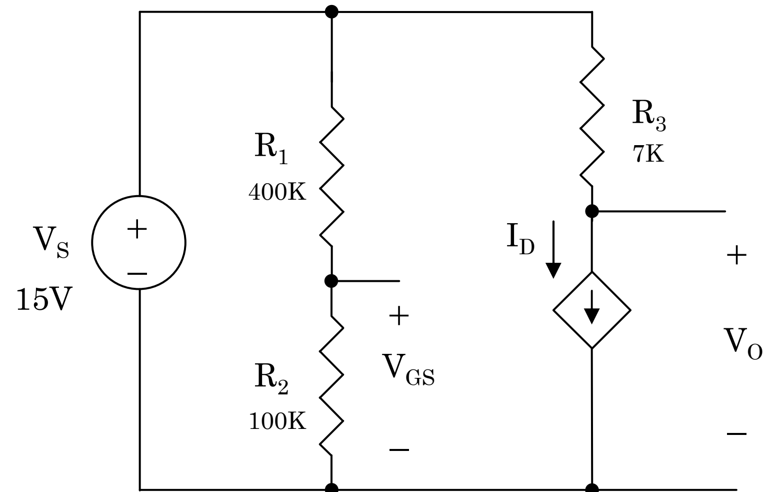
MOSFETs

- Linear Circuits
  - Example – Amplifier
    - DC Analysis – Find Q Point
      - Remove all L's & C's
        - Capacitors open
        - Inductors short
      - Remove all time-dependent sources
        - Voltage sources shorted
        - Current sources open
      - Insert DC model
      - Analyze circuit
      - Find operating point
    - In general, there is not a DC Model
      - In Beyond Pinch-off, operating point is nonlinear
        - Must find operating point using info from manufacturer

$$I_D = K/2\ (V_{GS} - V_{TH})^2, \text{ valid for } V_{DS} \geqq V_{GS} - V_{TH}$$

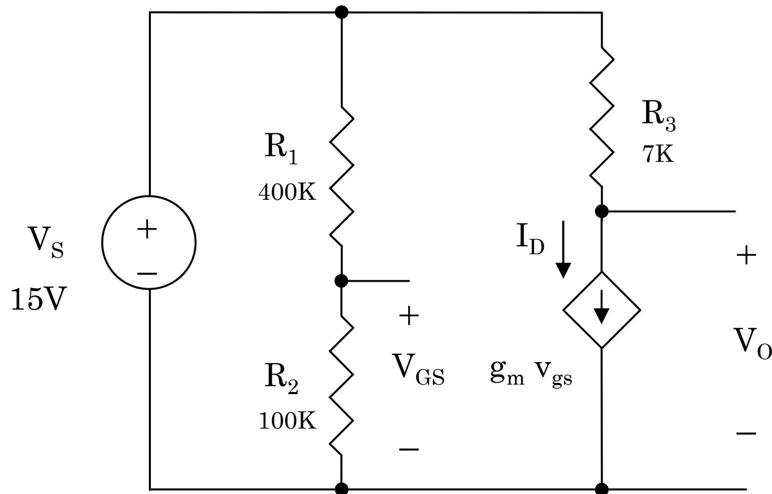


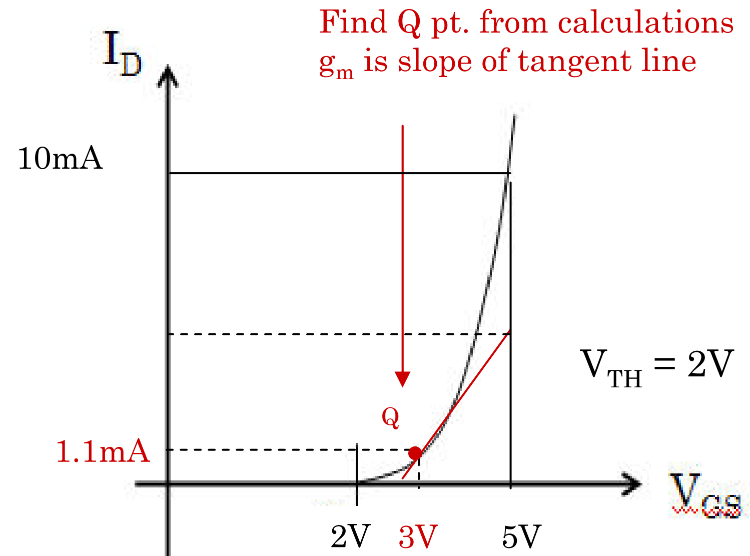
$V_i = 0.1 \sin(2\pi\, 1000\, t)$



MOSFETs

- Linear Circuits
  - Example – Amplifier
    - DC Analysis – Find Q Point (Cont.)





Find V_{GS} → Simple voltage divider:

$V_{GS} = V_S\ R_2 / (R_1 + R_2) = (15)\ (100K) / (500K)$

$= 3V > V_{TH}$ → Operating in Active Region

$I_D = K/2\ (V_{GS} - V_{TH})^2$

From curve, find:

$10mA = K/2\ (5 - 2)^2$ → $K = 2.2E\text{-}3$

Plug in K, V_{GS}, & V_{TH} to find I_D at Q:

$I_D = (2.2E\text{-}3)/2\ (3 - 2)^2 = 1.1mA$

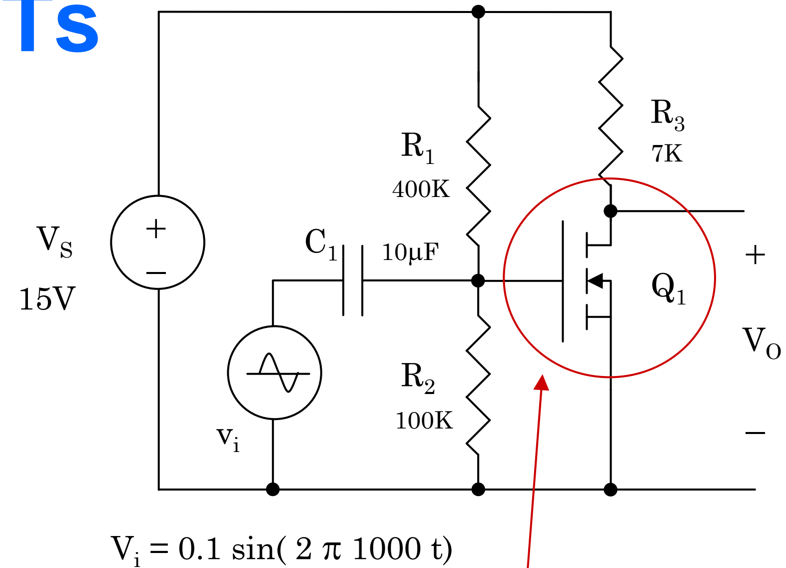
$V_O = V_S - (I_D\ R_3) = 15 - 7.7 = 7.3V$

Now find gm from curve at Q point:

$g_m = \partial I_D / \partial V_{GS} \big|_Q \approx 5\ mA / 2.5V = 2E\text{-}3$

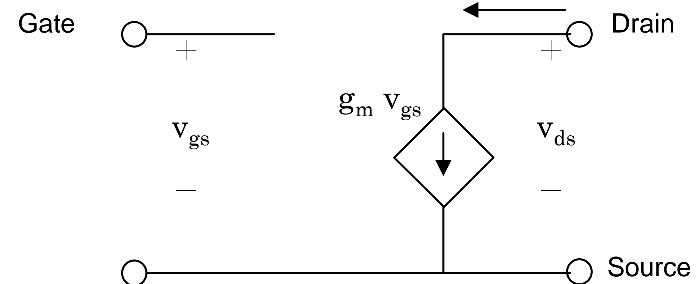
MOSFETs

- Linear Circuits (Continued)
  - Example – Amplifier (Cont.)
    - AC Analysis – Find the Gain
      - Remove all DC sources
        - Voltage sources → short
        - Current sources → open
      - Insert AC model
      - Analyze circuit
      - Find Gain



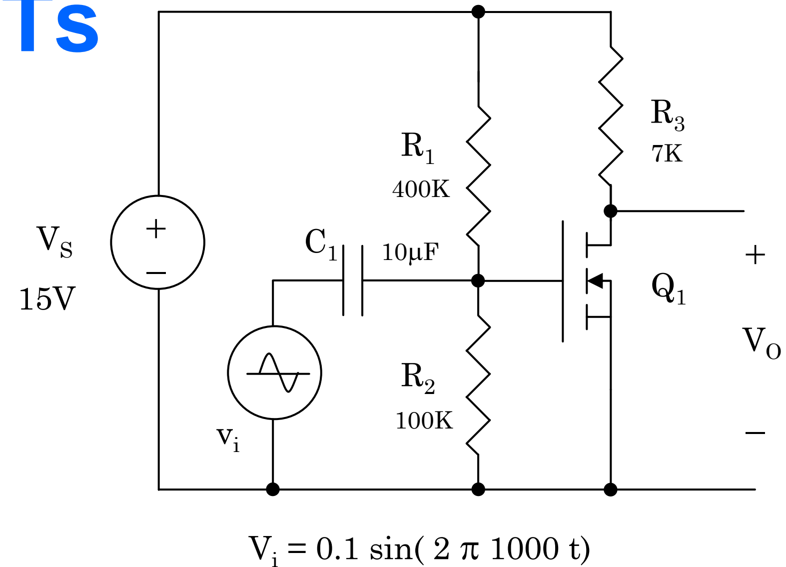
$V_i = 0.1 \sin(2 \pi 1000 t)$

Mid-Frequency AC Model



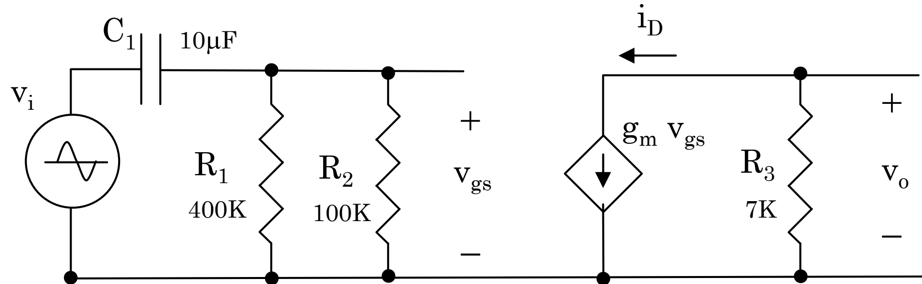
MOSFETs

- Linear Circuits (Continued)
  - Example – Amplifier (Cont.)
    - AC Analysis



$V_i = 0.1 \sin(2\pi\, 1000\, t)$

Equivalent Circuit at Mid-Frequency with Transistor Model



Find v_{gs} → Node Equation:

$[\, v_{gs} / R_1\,] + [\, v_{gs} / R_2\,] + [\, (v_{gs} - v_i) / (Z_{C1})\,] = 0$

$Z_{C1} = 1 / (j\, \omega\, C_1)$

$vgs\, [\, 1/R1 + 1/R2 + (j\, w\, C1)\,] = Vi\, (j\, w\, C1)$

$$v_{gs} = \frac{v_i\, (j\, w\, C_1)\, (R_1\, R_2)}{R_1 + R_2 + (j\, w\, C_1\, R_1\, R_2)}$$

$v_{gs} \approx v_i$

Find v_o → Node Equation:

$[\, v_o / R_3\,] + i_d = 0$

$[\, v_o / R_3\,] + g_m\, v_{gs} = 0$

$v_{gs} = v_i\,,\ g_m = 2E\text{-}3$ (from DC analysis)

$v_o = -\, g_m\, v_i\, R_3 = -(0.1)\,(2E{-}3) = -1.4$

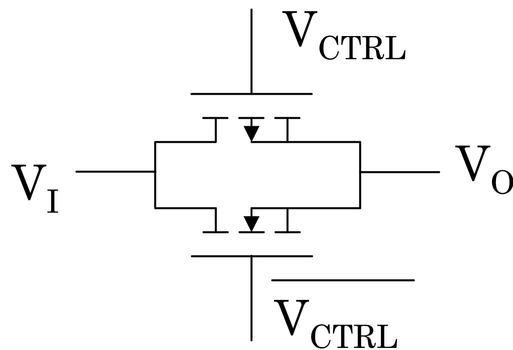
$$\frac{v_O}{v_i} = -\, g_m\, R_3 = -14$$

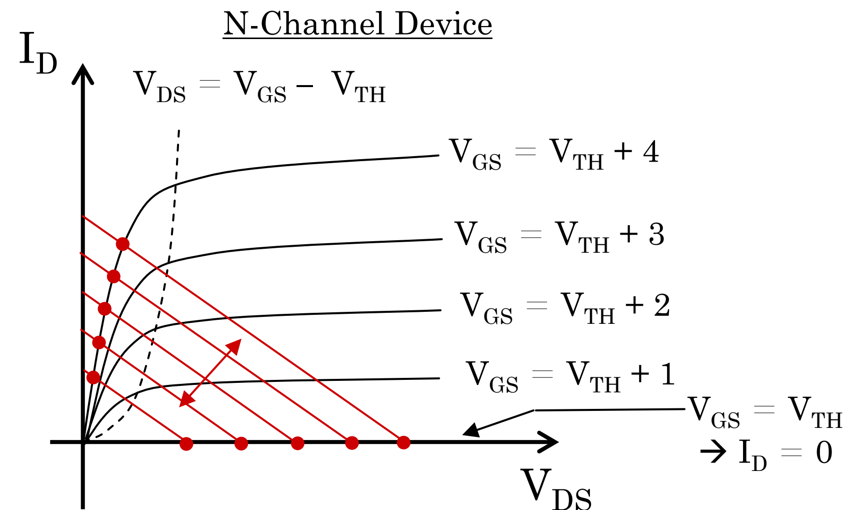
$v_o(t) = 7.3 - 1.4 \sin(2\pi\, 1000\, t)$

⇨ **Output is sum of DC + AC parts**

MOSFETS

- Analog Switches
  - Principle: Operate either in ohmic region, or at ID = 0

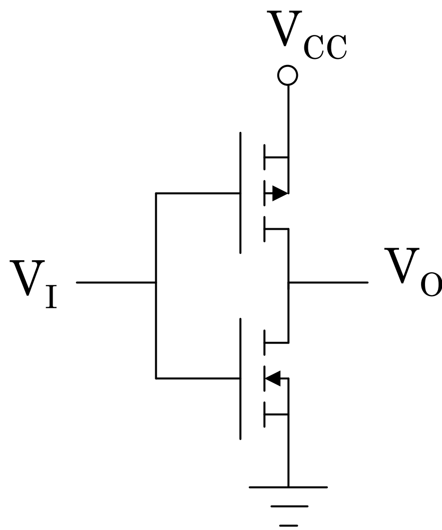


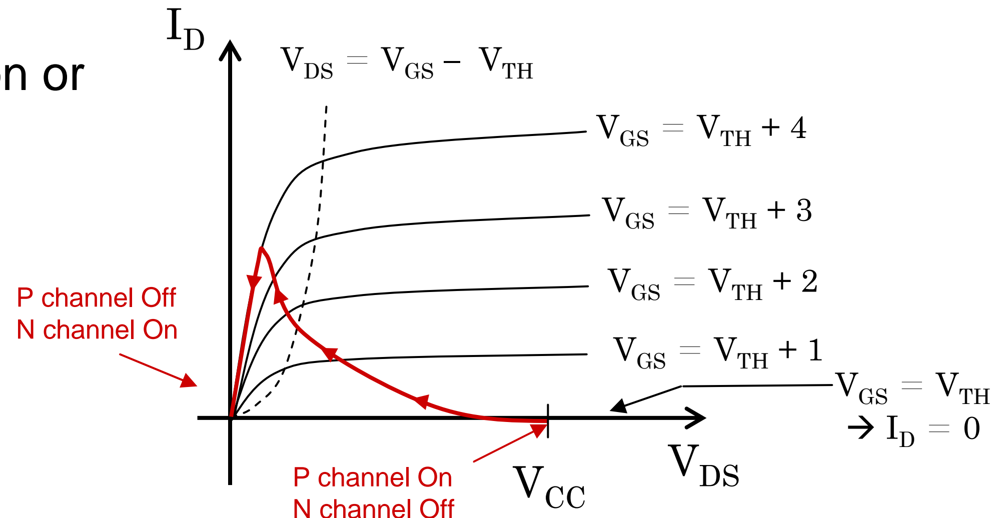


- Load line moves, depending on V_{DS}
- But operate either on $V_{GS} = V_{GS,MAX}$ or on $V_{GS}=V_{TH}$

MOSFETS

- Digital Logic → CMOS
  - Also operating either full on or full off, not in between
  - Consider an inverter





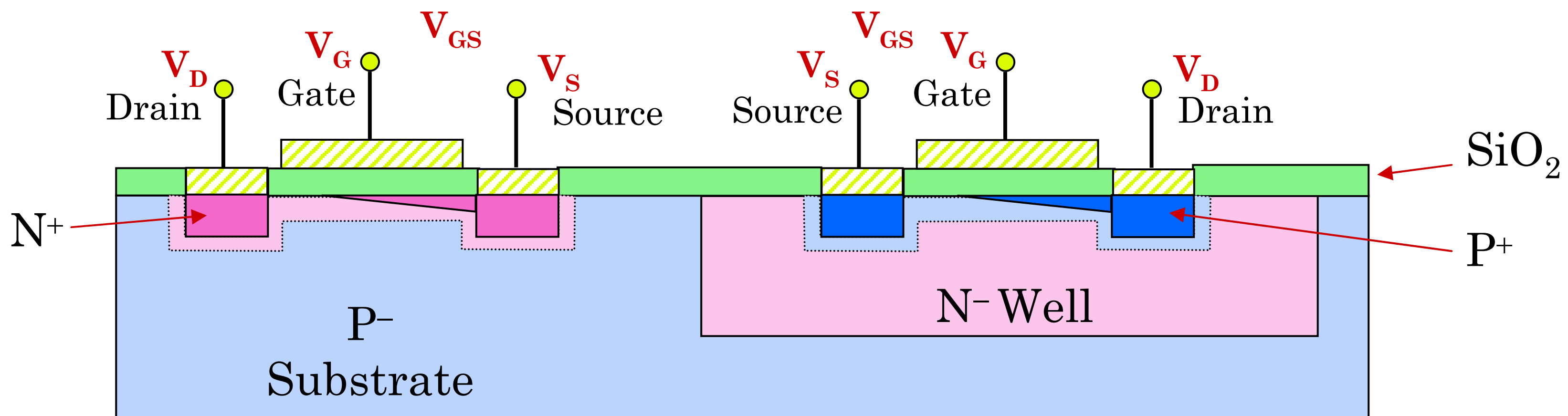
Only have current flow during switching
(Approximate Off-to-On transition showing)
Switching times: ~nSec → pSec
When not switching → No current → Low power

- When $V_I = V_{CC}$, Q_2 ON, Q_1 OFF → $V_O = 0V$
- When $V_I = 0V$, Q_2 OFF, Q_1 ON → $V_O = V_{CC}$

V_{IN}	V_{OUT}
L	H
H	L

CMOS

- Motivation
  - For many circuits (amplifiers, switches, digital logic), it is useful to have both N-channel and P-channel devices on the same substrate
    - How is this done? → P wells & N wells
- Basic Construction

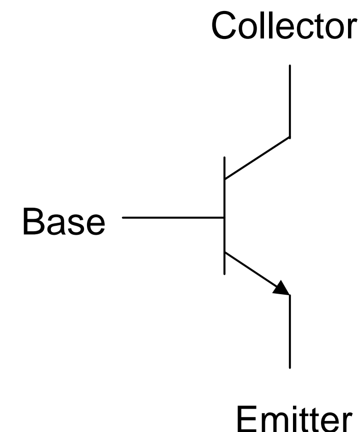


⇨ **Basis for modern IC fabrication technologies**

Bipolar Transistors

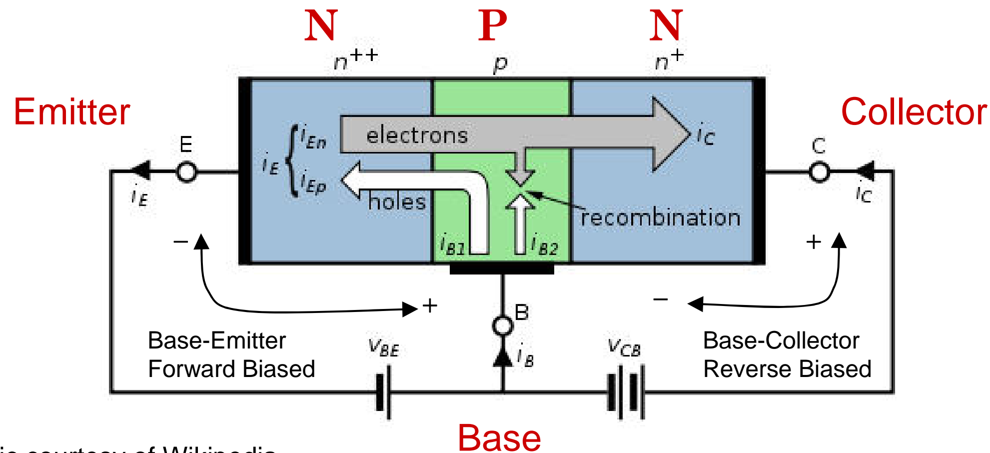
- Introduction

  - Bipolar Junction Transistors (BJTs) are 3-terminal devices, where the current flow between two of the terminals (Collector & Emitter) is controlled by injecting charge into the third terminal (Base), which creates diffusion currents between the two active terminals.
    - Current flow is achieved by diffusion currents between the two highly-doped active terminals (Collector & Emitter)
    - Charge carriers are minority carriers (p-type → electrons, n-type → holes)
    - Current flow is bi-directional (both electrons and holes participate)



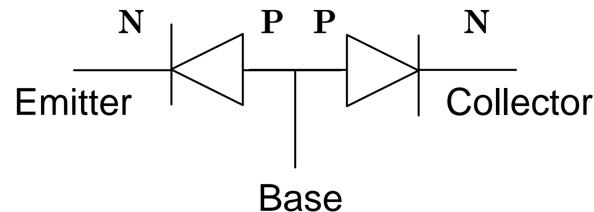
Bipolar Transistors

- Basic Construction – NPN Transistor
  - Conceptual construction



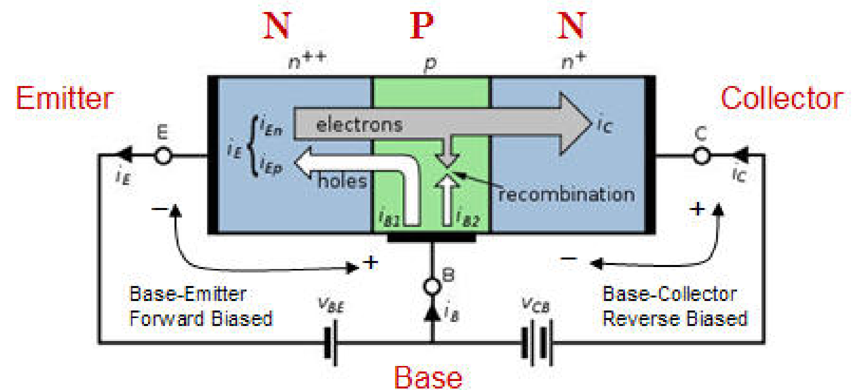
Graphic courtesy of Wikipedia

⇨ **Looks like two back-to-back diodes**
⇨ **Base-Emitter junction is forward-biased**
⇨ **Base-Collector junction is reverse biased**



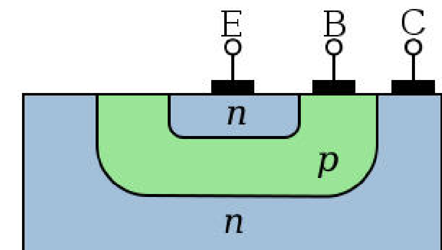
Bipolar Transistors

- Basic Construction – NPN Transistor
  - How does it work?
    - Start by injecting a hole into the Base from external source
    - Extra hole in Base attracts electrons from the Emitter
    - As electrons enter Base from Emitter, they are swept through the base by the strong electric field seen by the reverse-biased Base-Collector junction
    - Generally, N electrons are swept through from Emitter to Collector before hole in Base can migrate to Emitter
      - Gives Current Gain $\beta = I_C / I_B$
    - Some holes in Base recombine in Base with electrons from Emitter
    - Most holes make it to the Emitter



Graphic courtesy of Wikipedia

Typical Construction



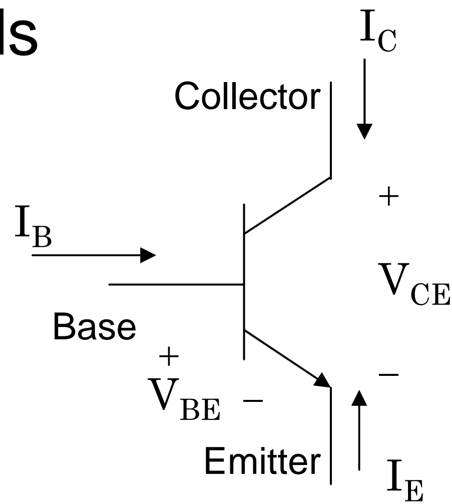
Graphic courtesy of Wikipedia

⇨ The unique construction of the junctions, along with the special doping levels, make this work

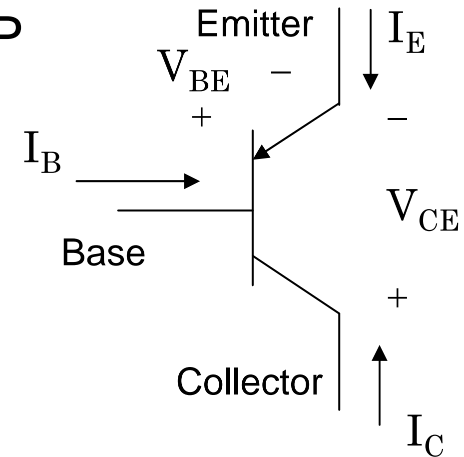
⇨ Can have NPN, or PNP Transistors

Bipolar Transistors

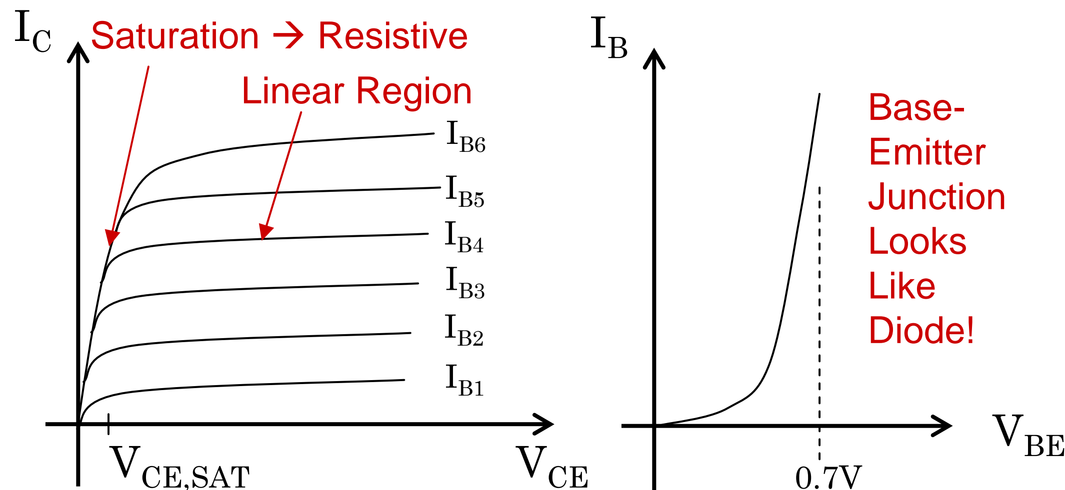
- Symbols
  - NPN



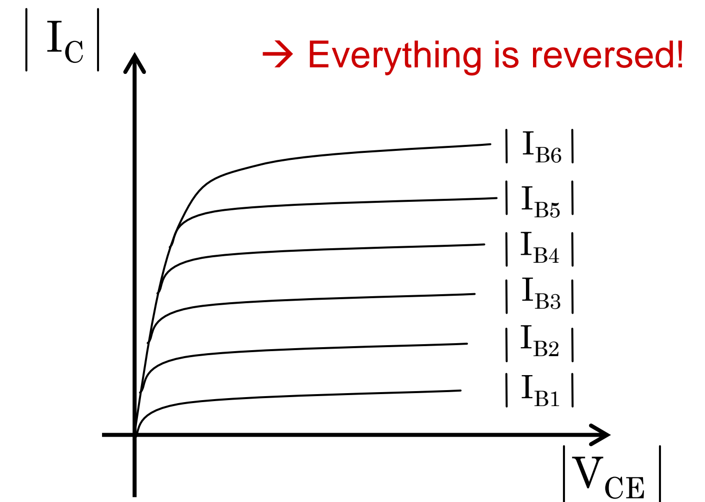
  - PNP



- IV Characteristics
  - NPN



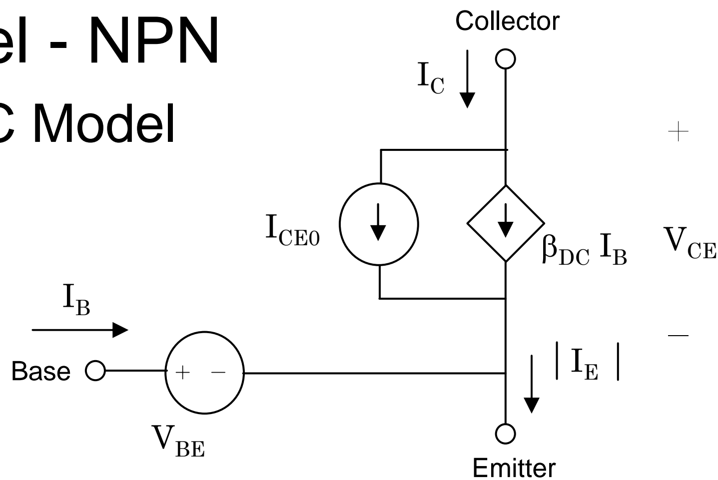
  - PNP

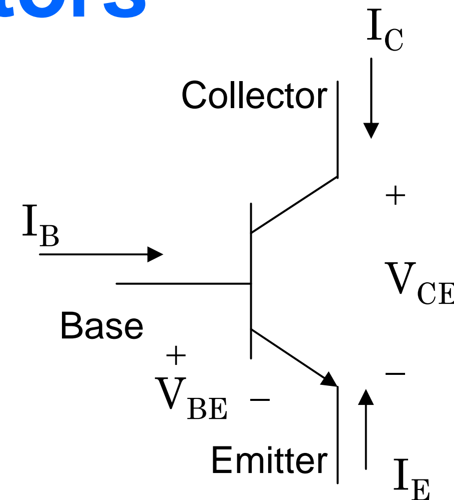


Bipolar Transistors

- Model - NPN
  - DC Model

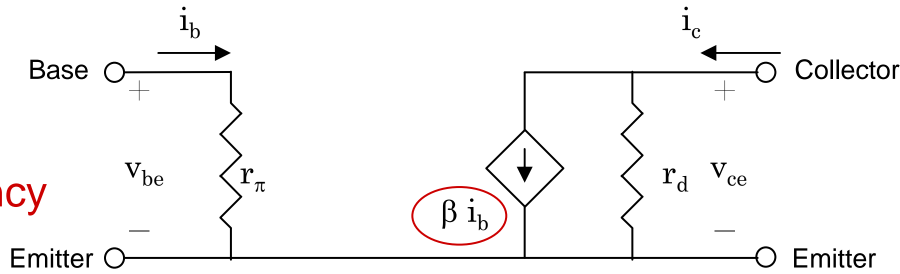
Model For Linear Region



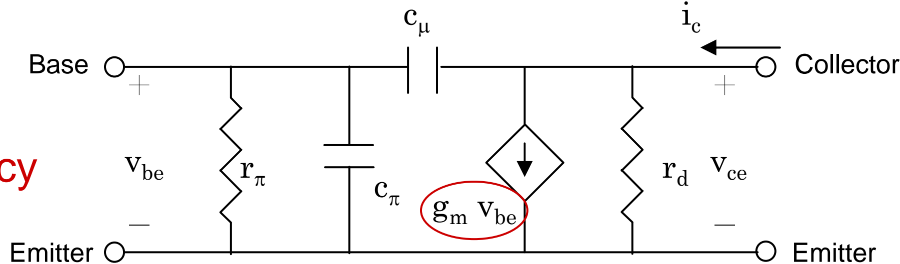


- AC Models – Hybrid Pi

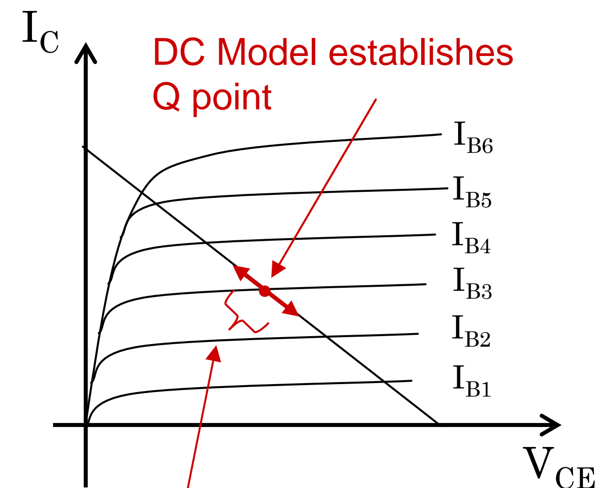
Mid Frequency



High Frequency



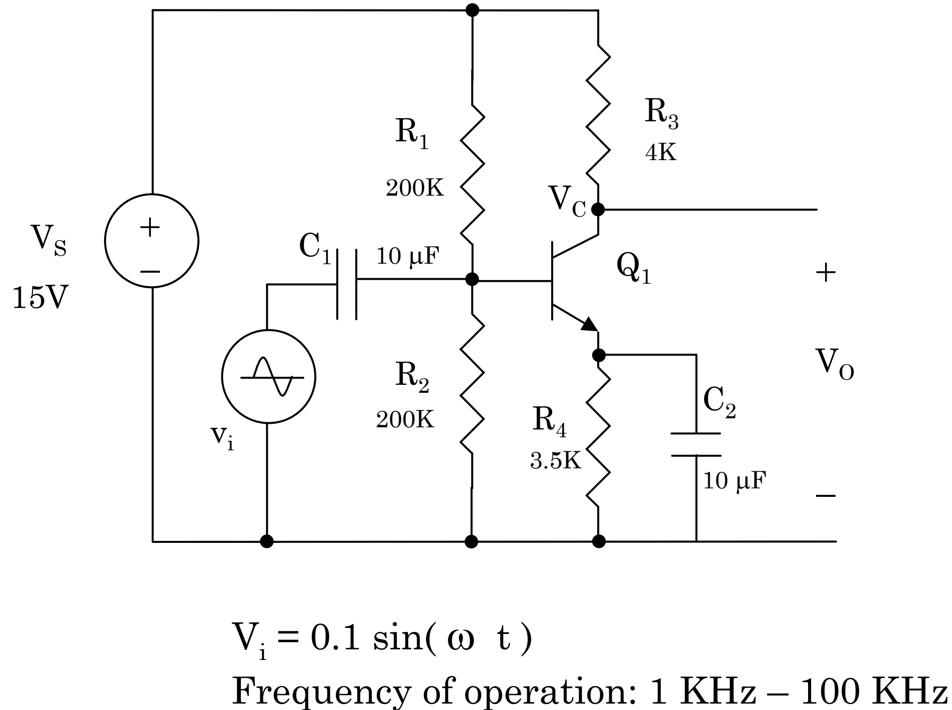
Generally have a "Load Line":



$$g_m\ v_{be} = \beta\ i_b$$

Bipolar Transistors

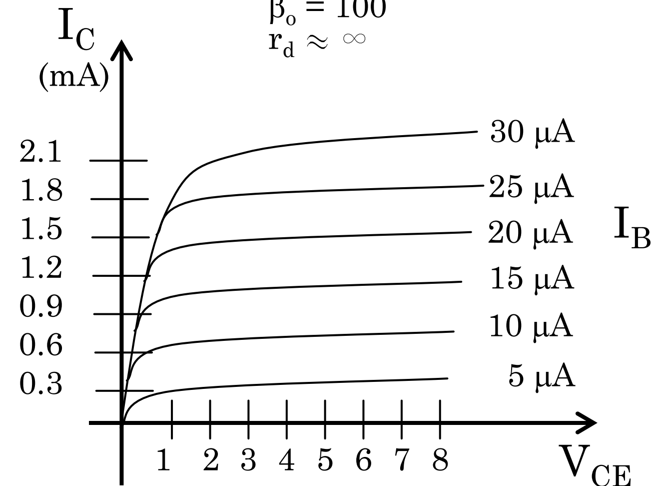
- Linear Circuits
  - Example: NPN Common Emitter Amplifier



$V_i = 0.1 \sin(\omega\ t)$

Frequency of operation: 1 KHz – 100 KHz

Data from Manufacturer

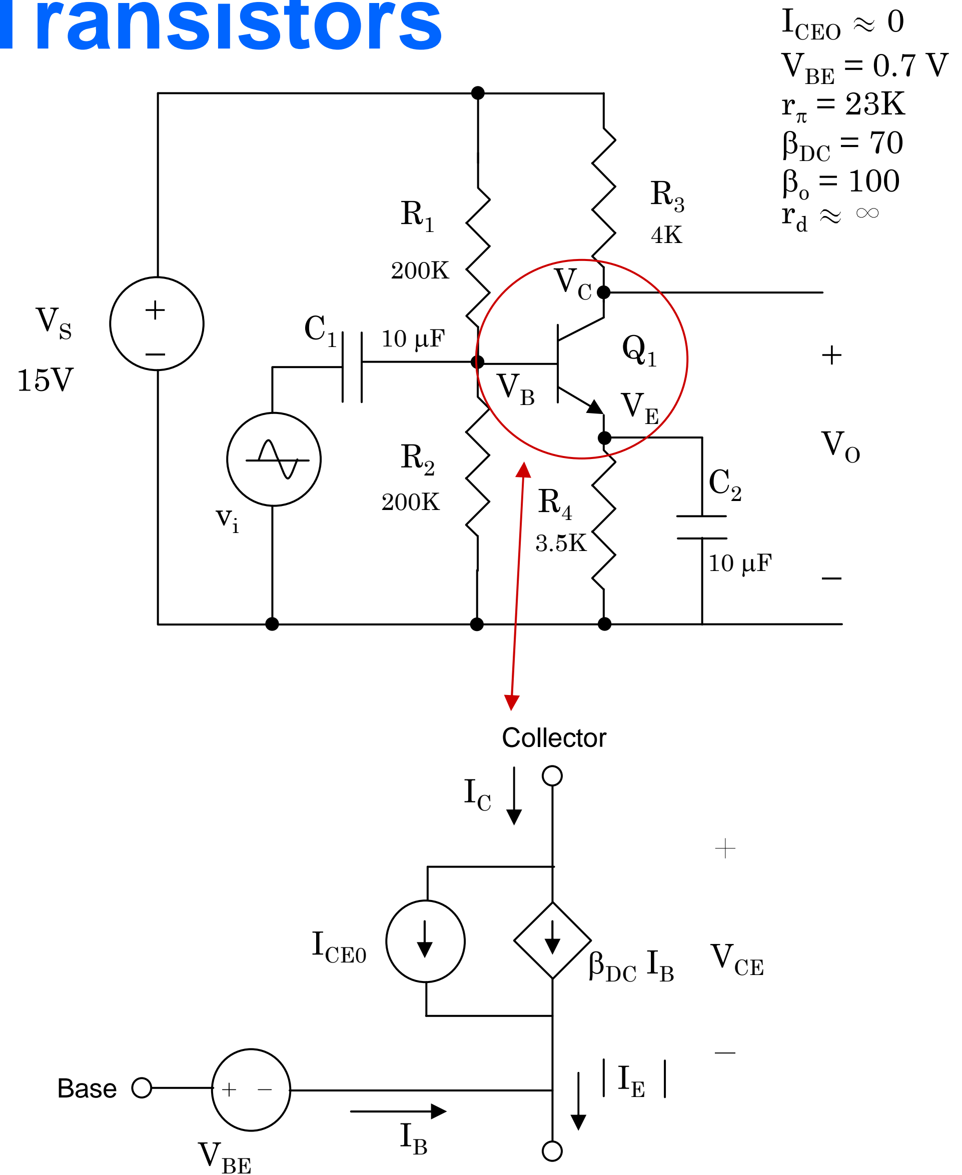


Bipolar Transistors

- Linear Circuits (Cont.)
  - Example (Cont.):

    NPN Common Emitter Amplifier

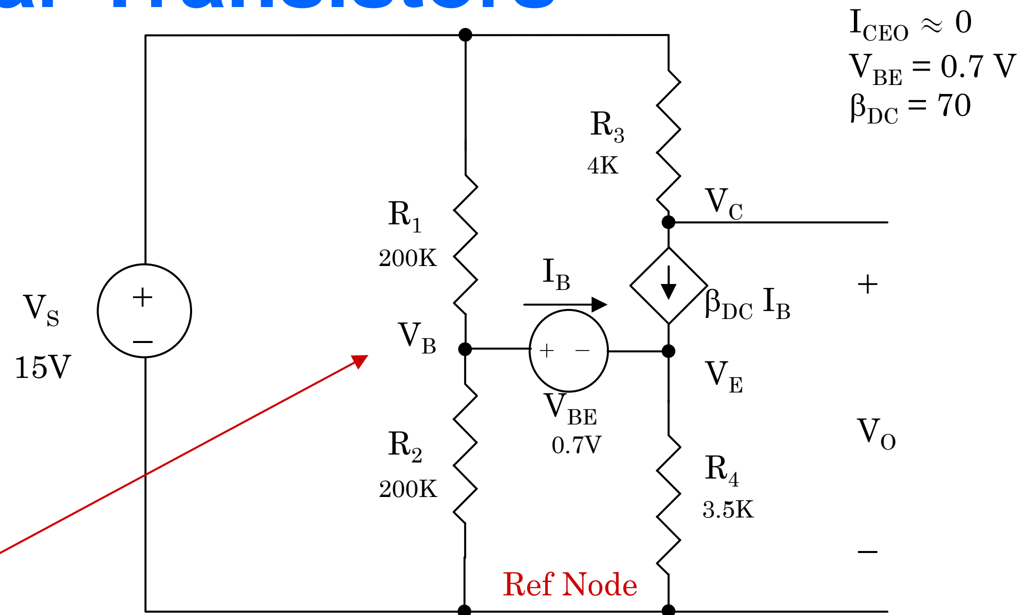
    - DC Analysis – Find Q Point
      - Remove all L's & C's
        - Capacitors open
        - Inductors short
      - Remove all time-dependent sources
        - Voltage sources shorted
        - Current sources open
      - Insert DC model
      - Analyze circuit
      - Find operating point



<u>DC Model for the NPN Transistor</u>

Bipolar Transistors

- Linear Circuits
  - Example (Cont.):
    - DC Analysis
      – Find Q Point



Write node equation at V_B:

$[\ (V_B - V_S\ ) / R_1\ ]\ + [\ V_B / (\ R_2)\ ] + I_B = 0$

At node V_E:

$V_E = (I_B + \beta_{DC}\ I_B)\ R_4 = I_B\ (1 + \beta_{DC})\ R_4$

Then, noting that V_B and V_E are related:

$V_E = V_B - V_{BE} = V_B - 0.7$
$= I_B\ (1 + \beta_{DC})\ R_4$

$I_B = (V_B - 0.7) / [\ (1 + \beta_{DC})\ R_4\ ]$

Solving:

$V_B\ [\ 1/R1\ + 1/\ R_2\ + 1/[(1 + \beta_{DC})\ R_4] = V_S/R_1 + 0.7 / [(1+\beta_{DC})R_4]$

Plugging in values, find:

$V_B = 5.56V$

$V_E = V_B - 0.7 = 4.86V$

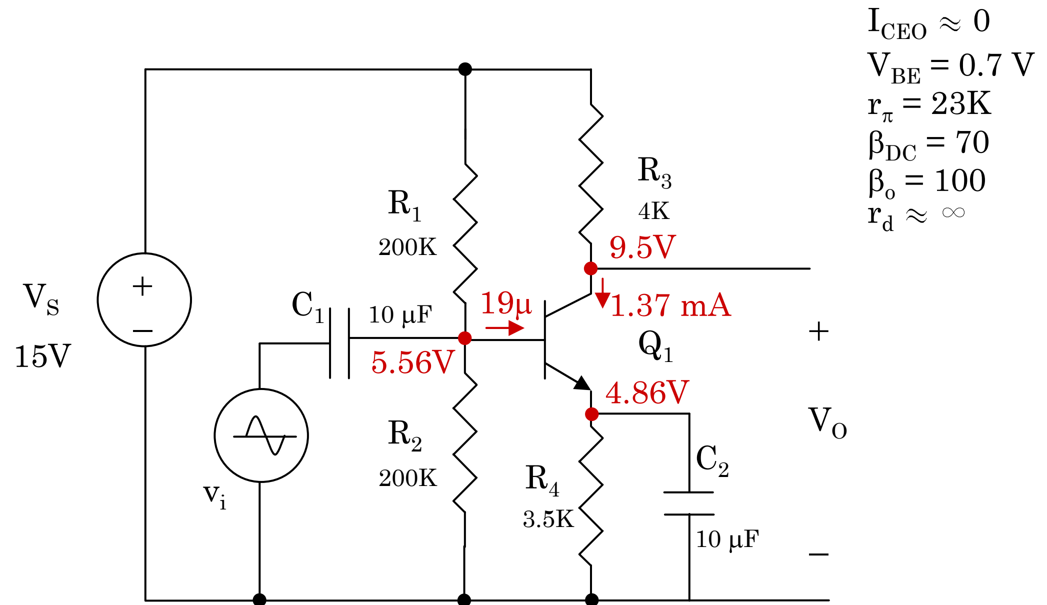
$I_B = = (V_B - 0.7) / [(1+\beta_{DC})\ R_4] = 19.6\ \mu A$

$V_C = V_S - [\beta_{DC}\ \ I_B\ R_3] = 9.5V$

$V_{CE} = V_C - V_E = 4.64V$, $\quad I_C = \beta_{DC}\ I_B\ = 1.37$ mA

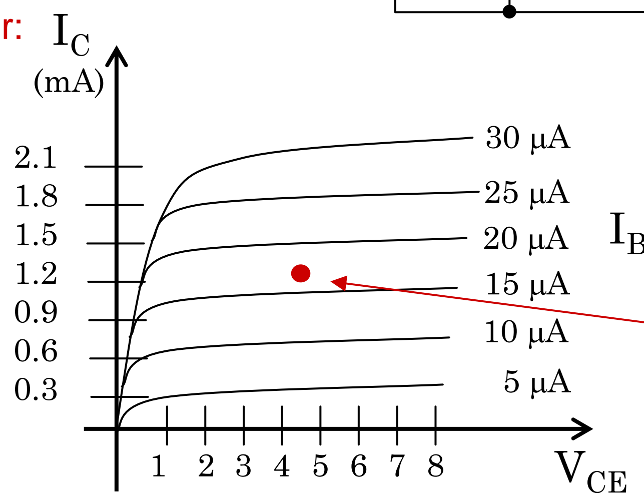
Bipolar Transistors

- Linear Circuits
  - Example (Cont.)
    - DC Analysis (Cont.)
      - Check results



$I_{CEO} \approx 0$
$V_{BE} = 0.7$ V
$r_\pi = 23$K
$\beta_{DC} = 70$
$\beta_o = 100$
$r_d \approx \infty$

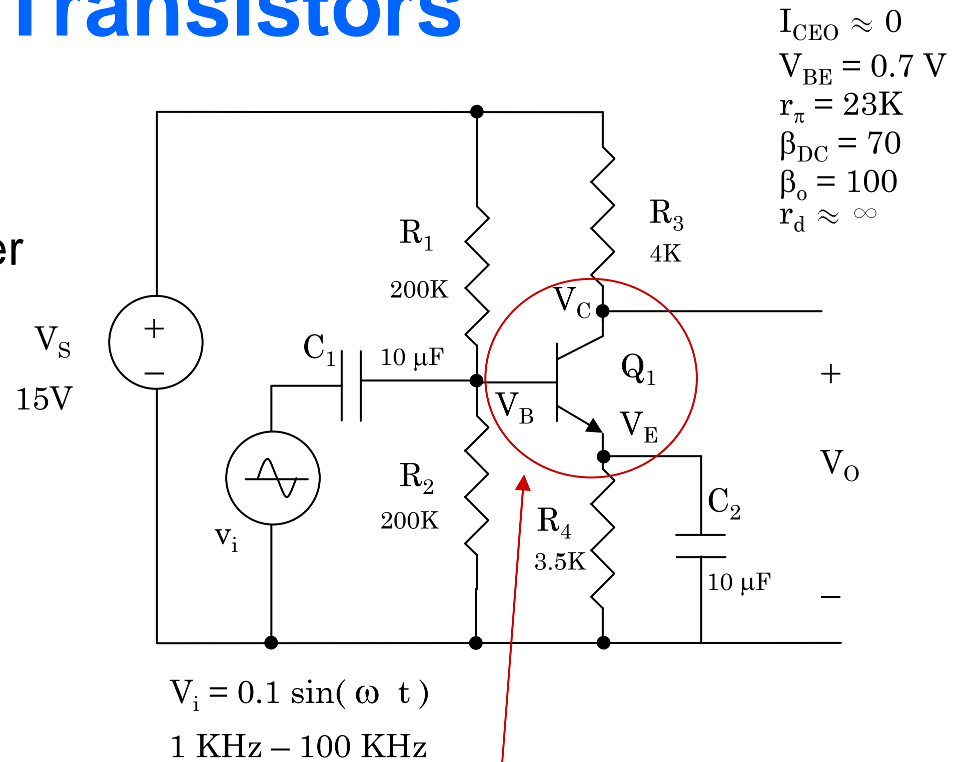
Curve from Mfgr:



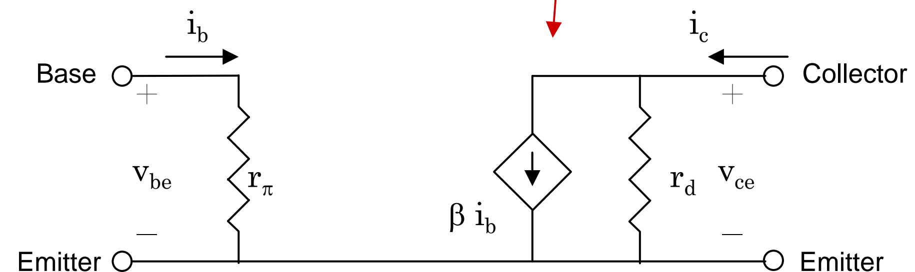
Approximate operating point
→ Good place to operate for a linear amplifier

Bipolar Transistors

- Linear Circuits
  - Example (Cont.):
    NPN Common Emitter Amplifier
    - AC Analysis – Find the Gain
      - Remove all DC sources
        - Voltage sources → short
        - Current sources → open
      - Insert AC model
      - Analyze circuit
      - Find Gain

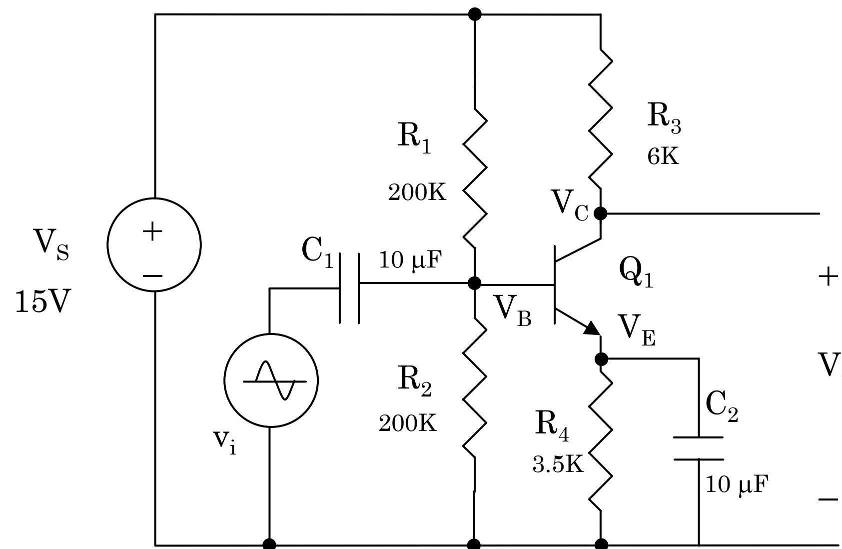


Mid-Frequency AC Model for the NPN Transistor



Bipolar Transistors

- Linear Circuits
  - Example (Cont.):
    - AC Analysis (Continued)



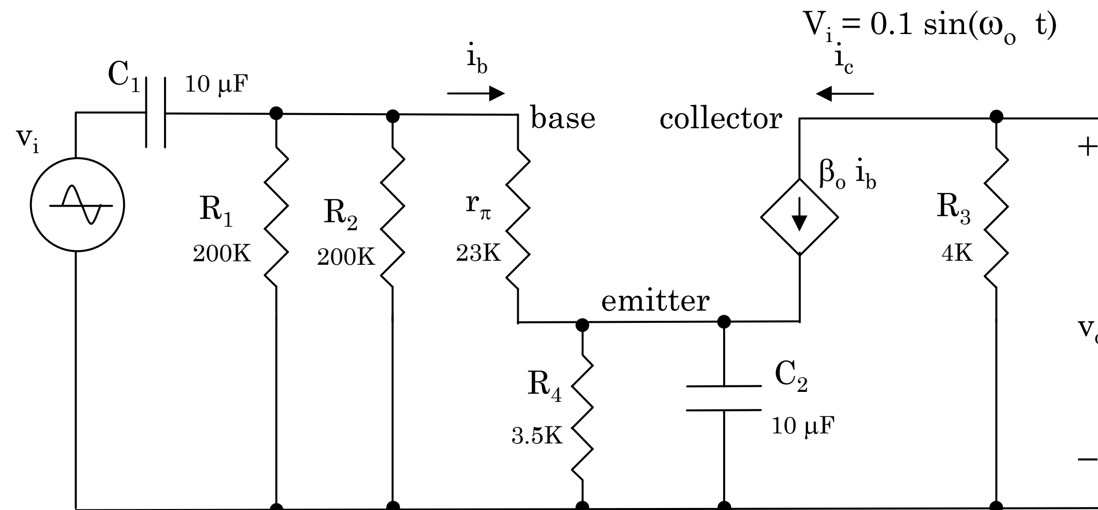
More complicated…

But, for mid frequencies, it turns out that can treat C_1 & C_2 as short circuits

Why?...

Impedances are small compared to $R_1, \ldots R_4$ at frequencies > 1000 Hz

⇨ Can Simplify…

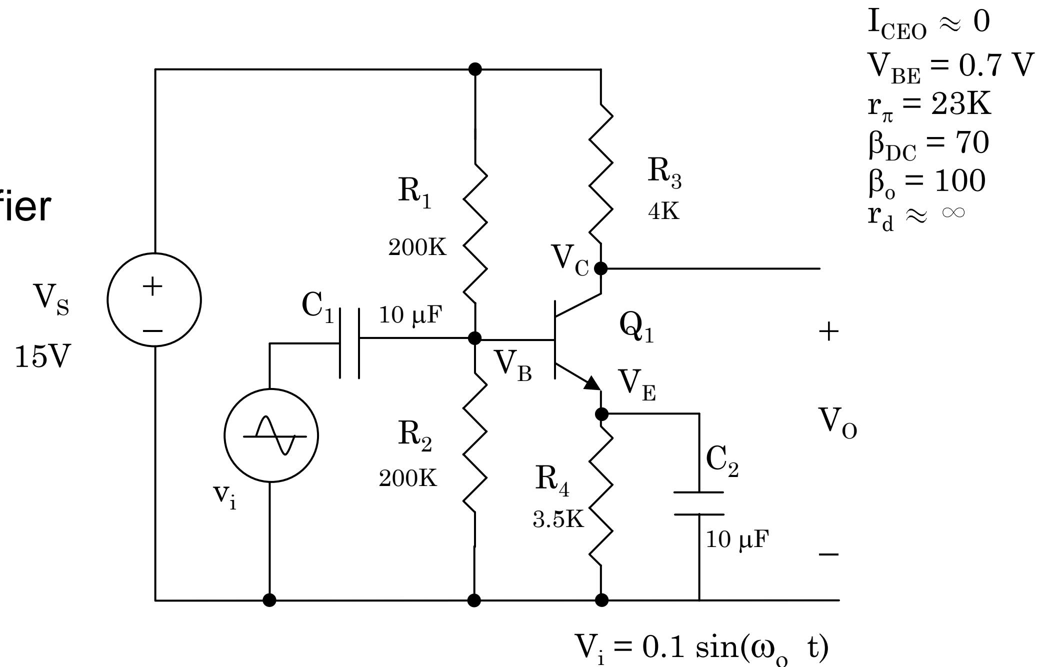


Bipolar Transistors

- Linear Circuits
  - Example (Cont.):

    NPN Common Emitter Amplifier

    - AC Analysis (Continued)

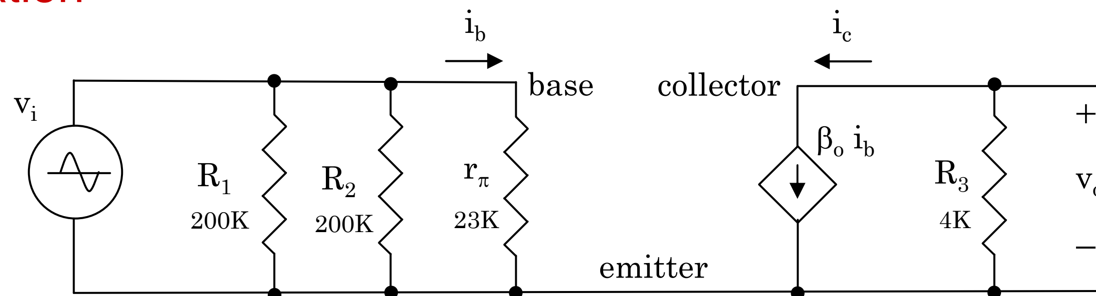


Treating C_1 & C_2 as short circuits:

⇨ Much simpler

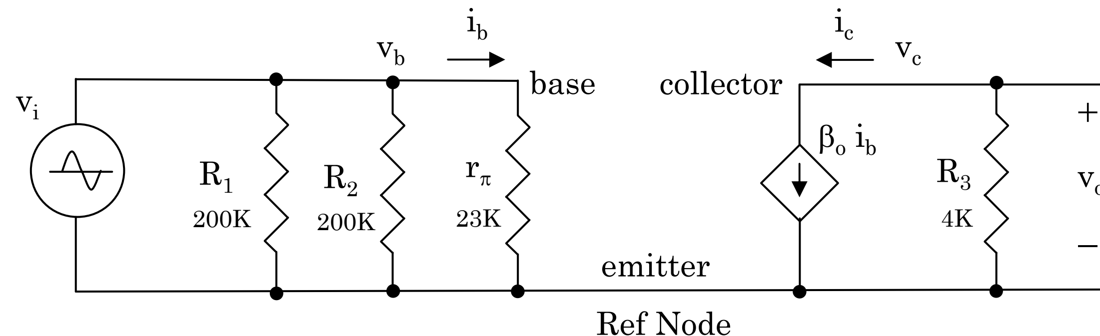
⇨ Need only 1 node equation to solve!

Equivalent Circuit at Mid-Frequency with Transistor Model



Bipolar Transistors

- Linear Circuits
  - Example (Cont.): NPN Common Emitter Amplifier
    - AC Analysis (Continued)



$I_{CEO} \approx 0$
$V_{BE} = 0.7\ V$
$r_\pi = 23K$
$\beta_{DC} = 70$
$\beta_o = 100$
$r_d \approx \infty$

$i_b = v_i / r_p$

$v_o = -\beta_o\, i_b\, R_3$

$= -\beta_o\, R_3\, v_i / r_p$

$$\frac{v_O}{v_i} = -\beta_o\, R_3 / r_\pi \quad = -\beta_o\, R_3 / r_\pi \; = \; -17.4$$

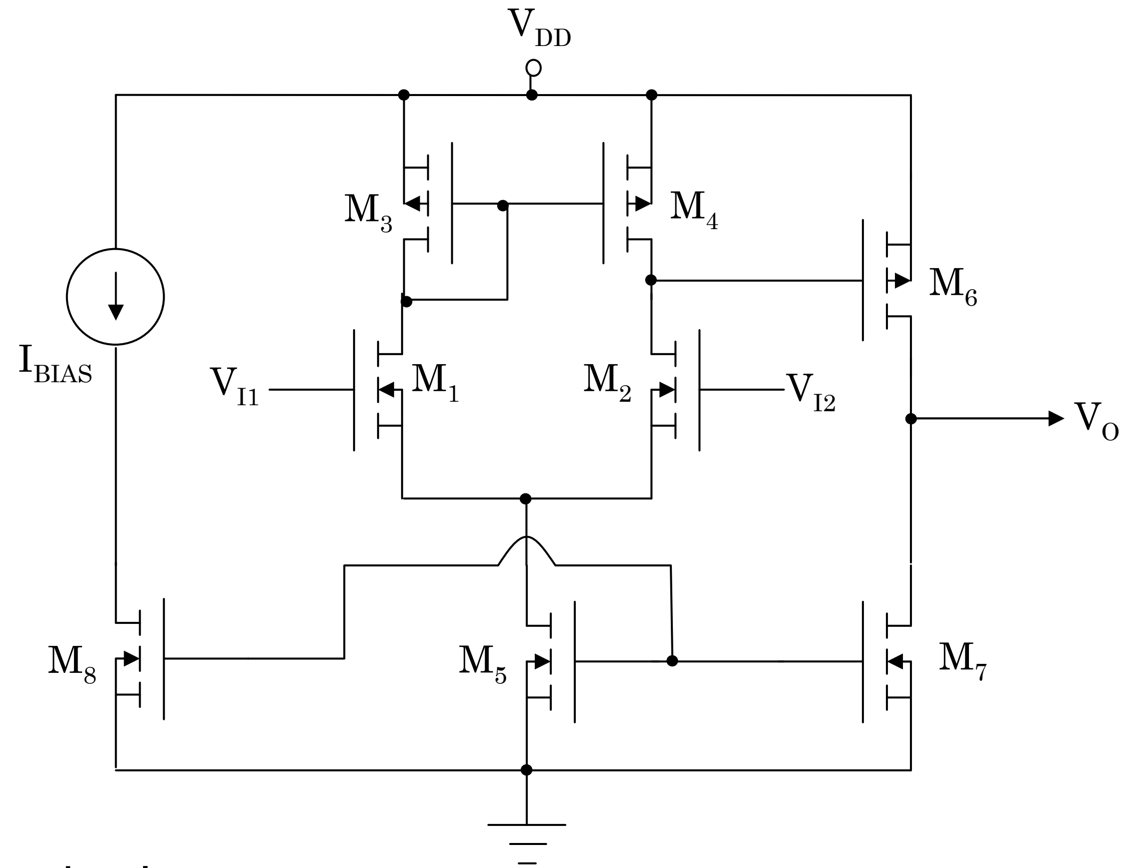
⇨ Valid over mid-frequencies ~1 KHz – 100 KHz

For: $v_i(t) = 0.1 \sin(2\pi\, 10{,}000\, t) \rightarrow v_o(t) = 9.5 - 1.74 \sin(2\pi\, 10{,}000\, t)$

⇨ **Output is sum of DC + AC parts**

CMOS Analog Circuits

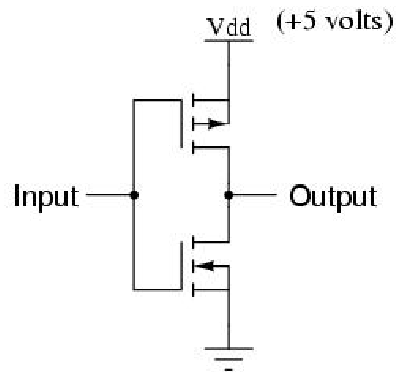
- A Basic CMOS, Differential, 1-Stage Amplifier
  - Uses P channel and N channel devices
  - No resistors!
  - Simple circuit can have gains ~1000
  - → ***ASICS***
    - Designer chooses transistor width and length of channel
  - Uses same principles introduced in this lecture
  - Each transistor has a role…
  - Generally use SPICE to simulate, but first design pass uses hand calculations



CMOS Digital Circuits

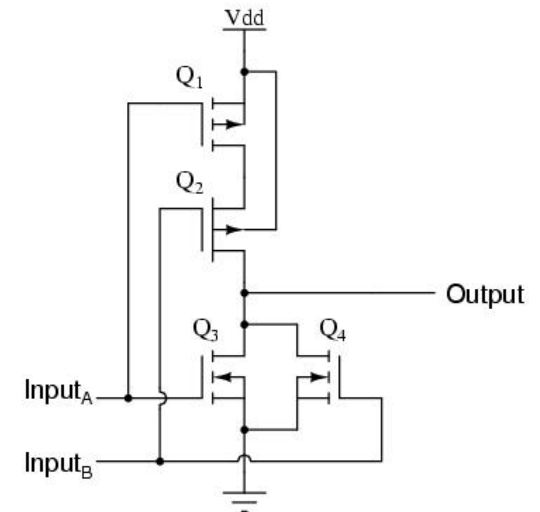
- Inverter

INPUT	OUTPUT
A	NOT A
0	1
1	0



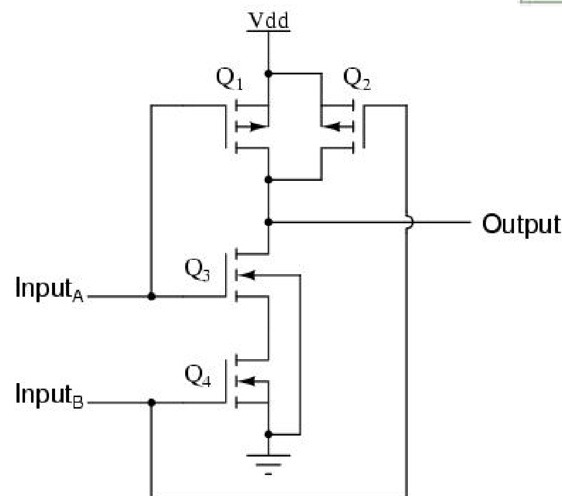
- NOR

INPUT		OUTPUT
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0



- NAND

INPUT		OUTPUT
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0



⇨**These are the basic building blocks for flip-flops, counters, registers Programmable Logic, Microprocessors, ….**

Images from allaboutcircuits.com

Thank You for your Attention!

I hope that you enjoyed the course and found it useful!