Omega

EASIROC, an easy & versatile ReadOut device for SiPM

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Orsay MicroElectronics Group Associated

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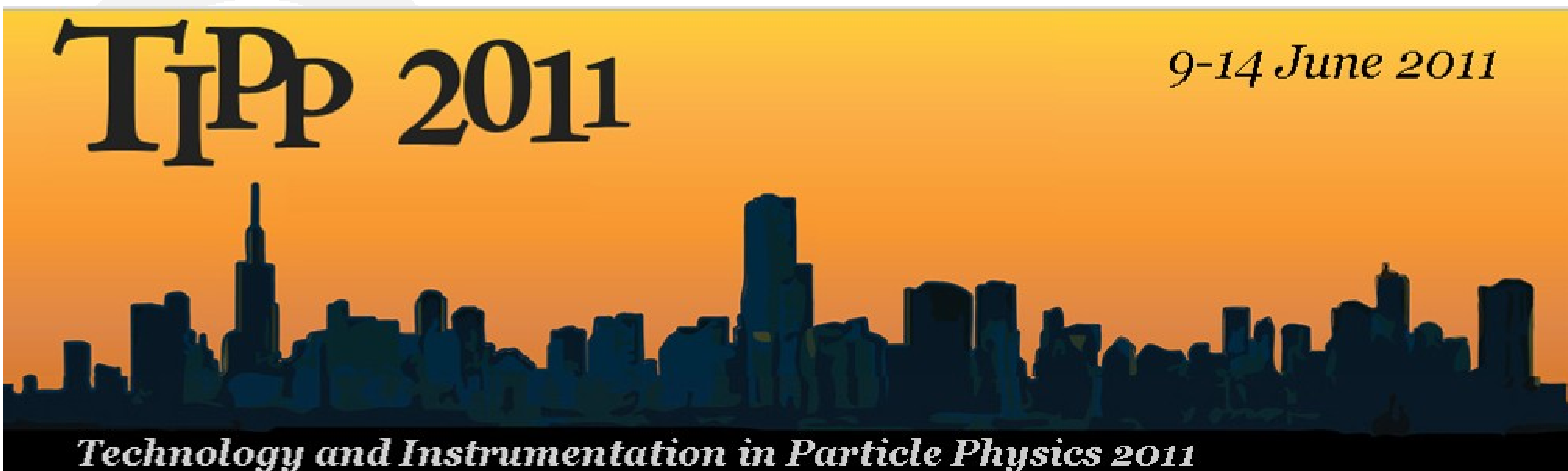
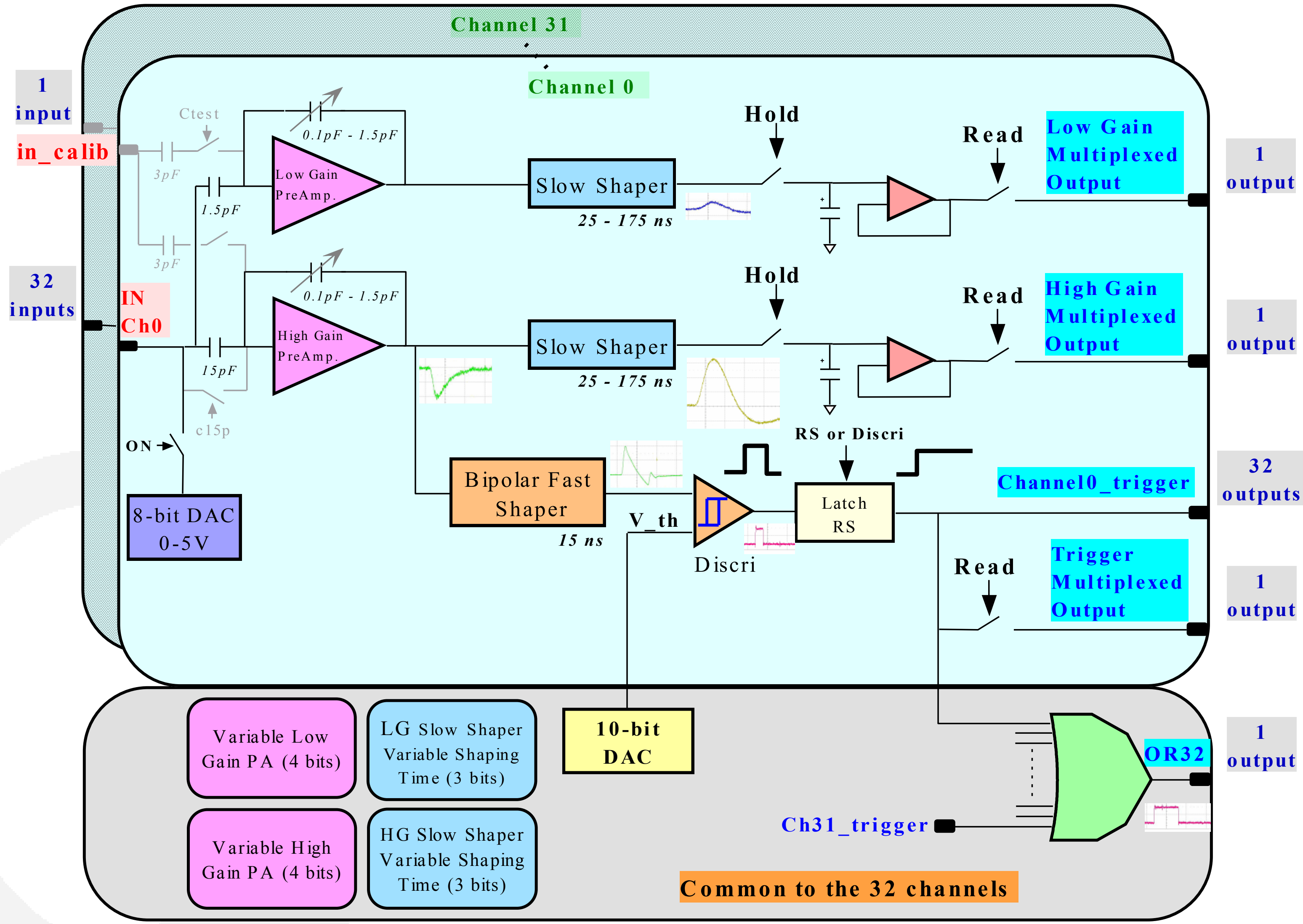


EASIROC FEATURES (BASED ON SPIROC CHIP)

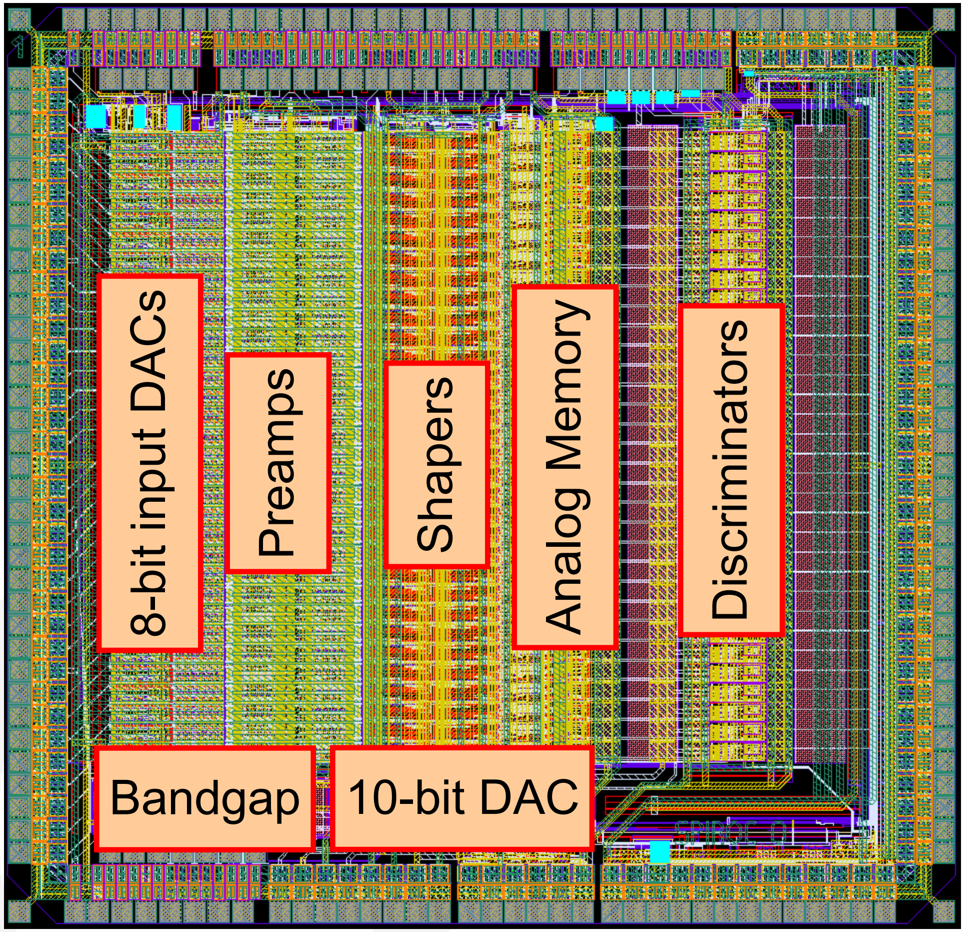
- 32-channel front-end readout
- Individual 8-bit DAC for SiPM Gain adjustment
- Energy measurement from 160fC to 320pC (1pe to 2000pe @ SiPM gain = 10^6)
  - 1 pe/noise ratio ~11
  - Variable gain preamplifier
  - Variable time constant CRRC² shaper (25 to 175ns)
  - Common 10-bit DAC for threshold adjustment
  - 2 multiplexed analog outputs (high gain, low gain) [tri state outputs]
- Trigger output
  - 1 pe/noise ratio ~24
  - Trigger on 1/3 pe (50fC)
  - 32 Trigger outputs
  - OR32 output
  - Trigger multiplexed output (latch included) [Tri state output]
- Individually addressable calibration capacitance
- Low power : 4.84mW/channel, 155mW/chip
  - Unused feature can be disabled to reduce power consumption
  - Power pulsing facility (idle mode with external signal)

EASIROC ANALOGUE CORE



EASIROC LAYOUT

32 SiPM inputs



32 trigger outputs

2 MUX charge outputs (LG + HG)

OR32 output

1 MUX trigger output

Technology :
AMS 0,35µm SiGe

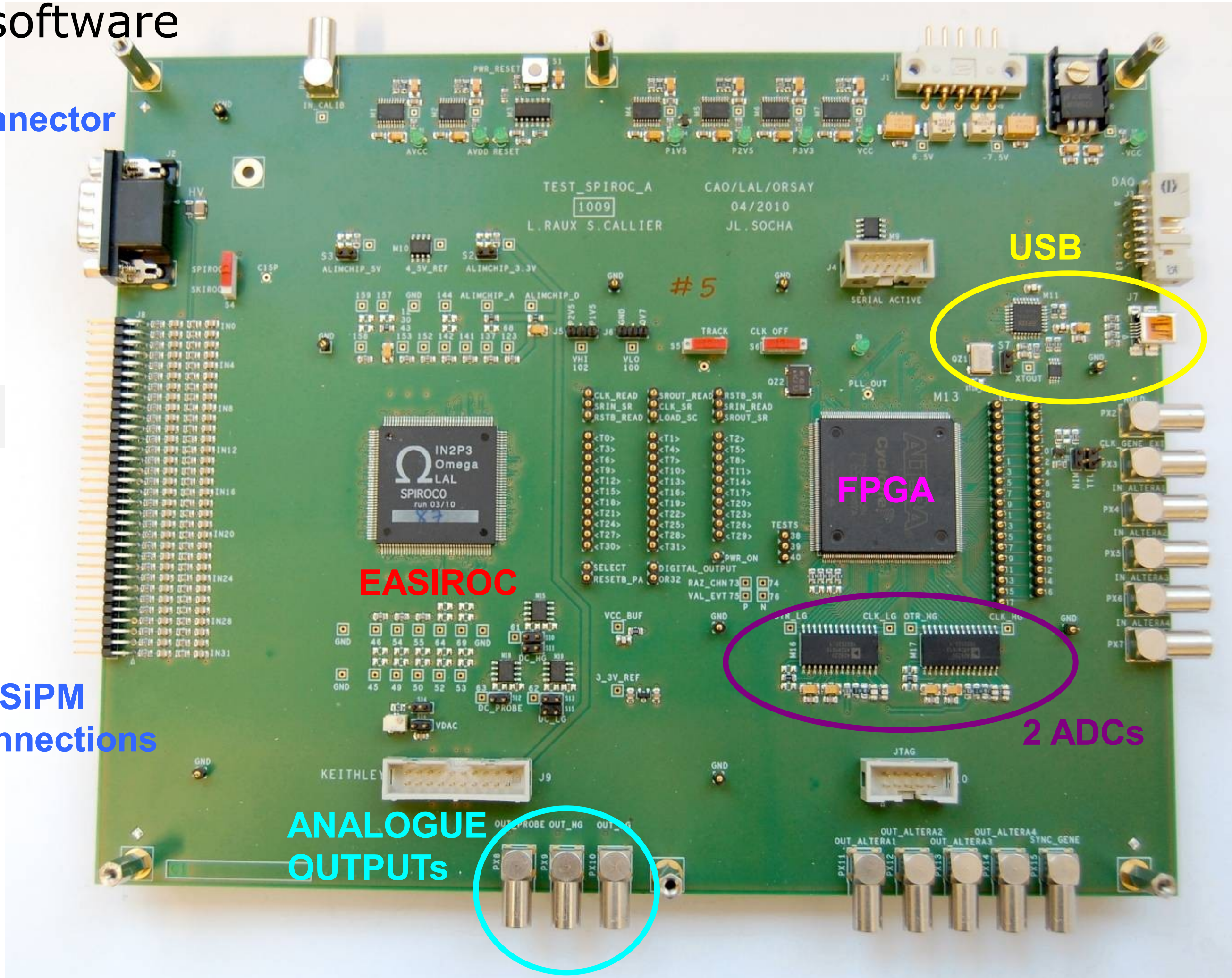
Die size : 16.6mm²
4.157 x 4.013 mm²

Package :
- Naked (PEBS)
- TQFP160

TQFP: heigth=1.4 mm

TEST BOARD

- Testboard allow easy acces to each EASIROC pin
- Testboard layout & cabling @ LAL
- Firmware using LAL USB interface
- Labview software

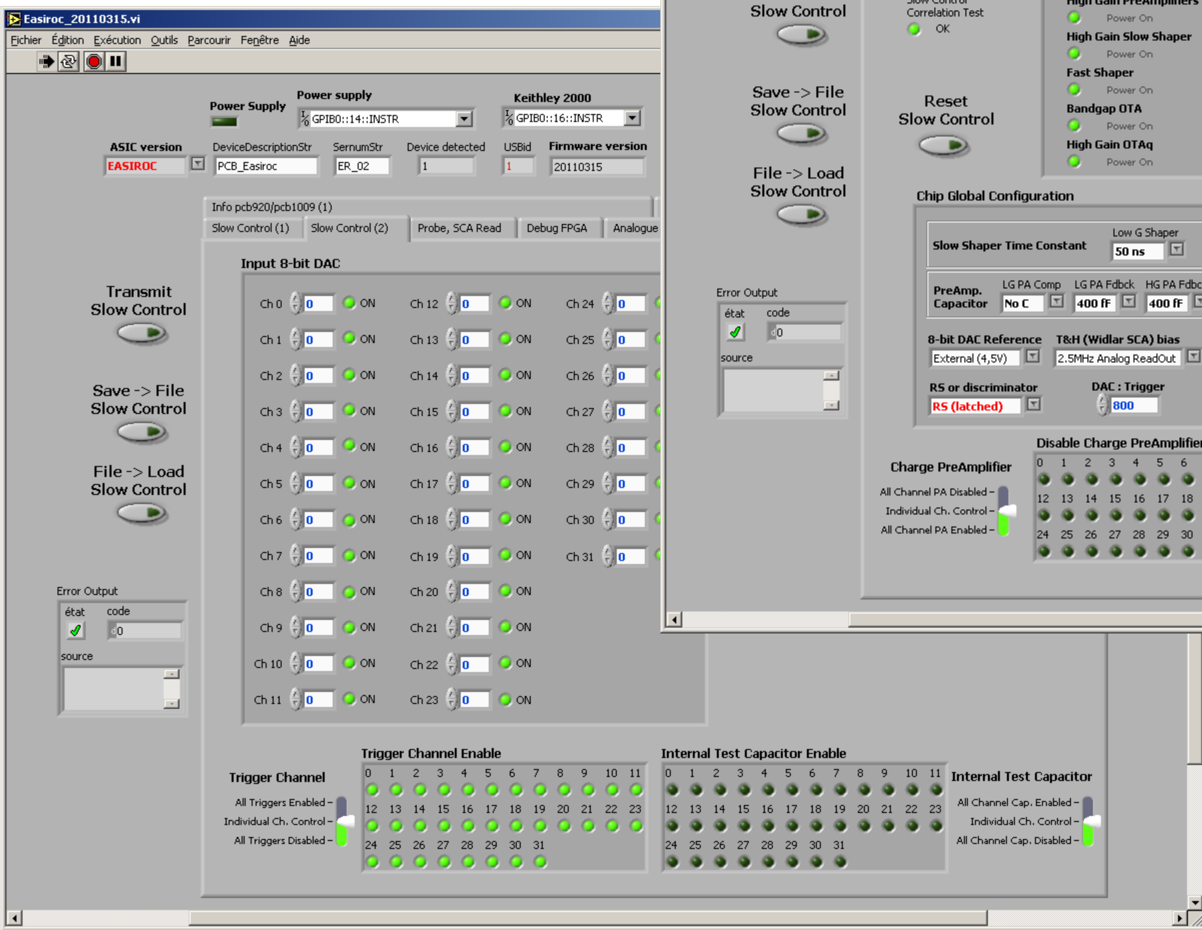


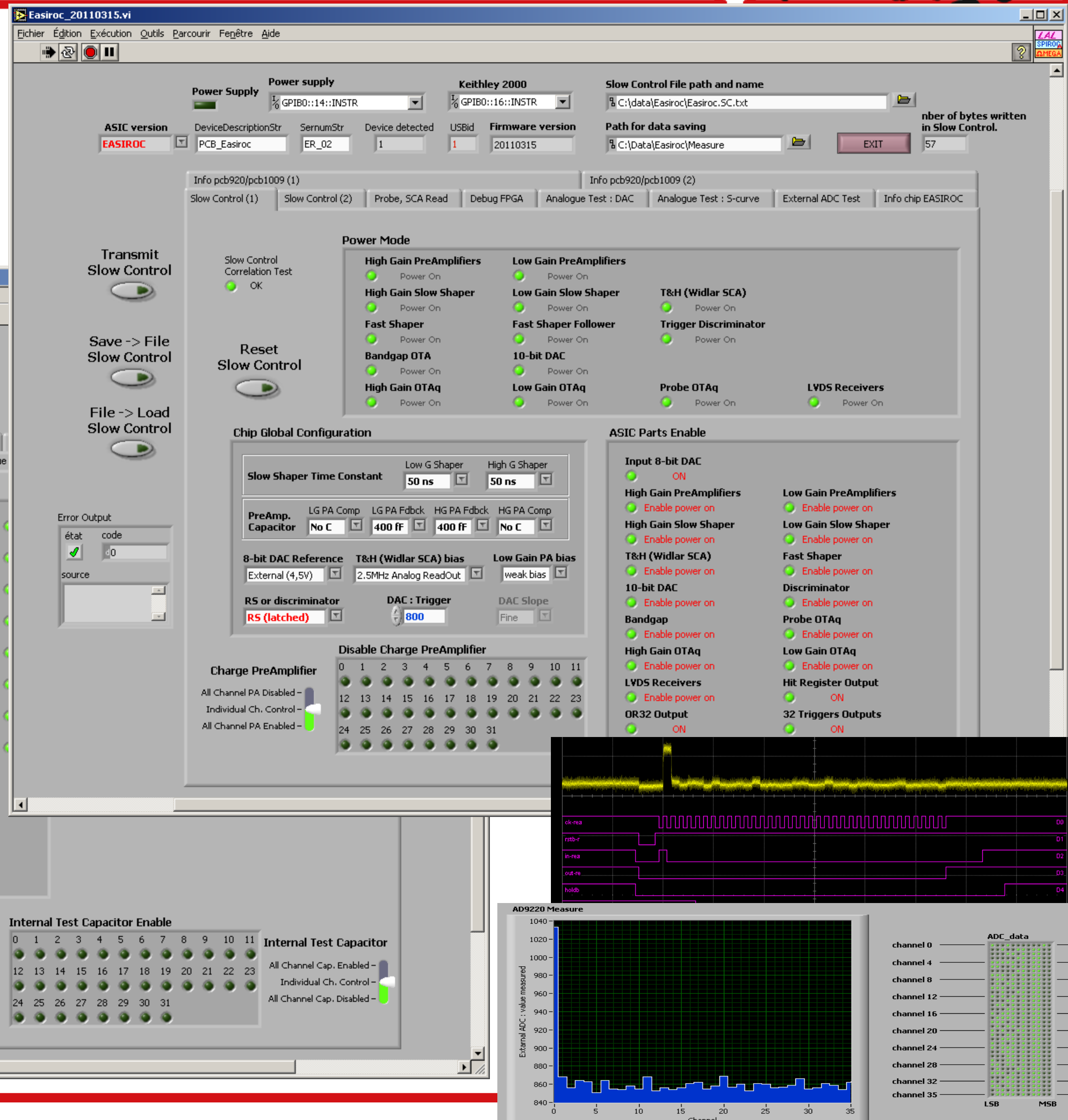
SOFTWARE

- ASIC versatility :

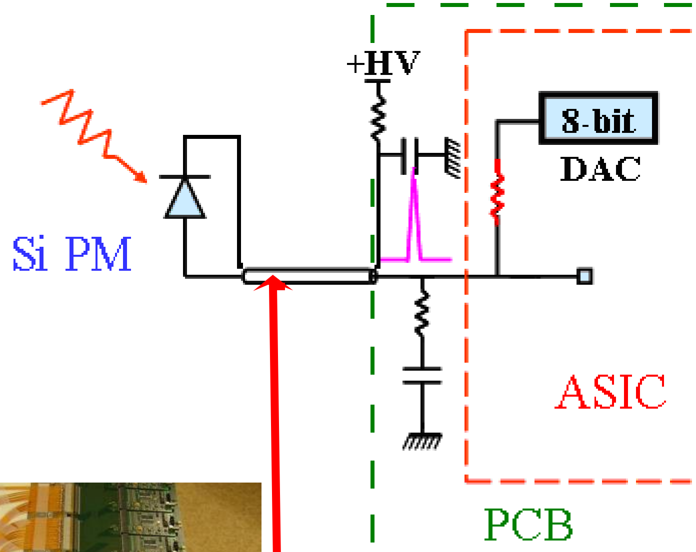
456 slow control bits

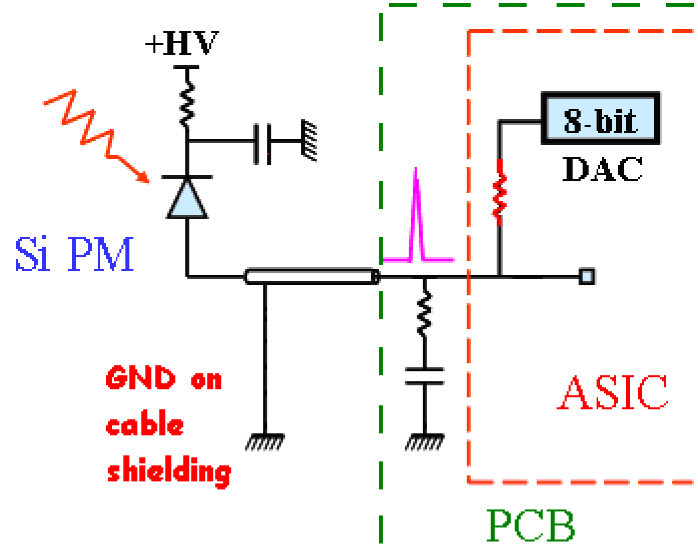
- Acquisition system

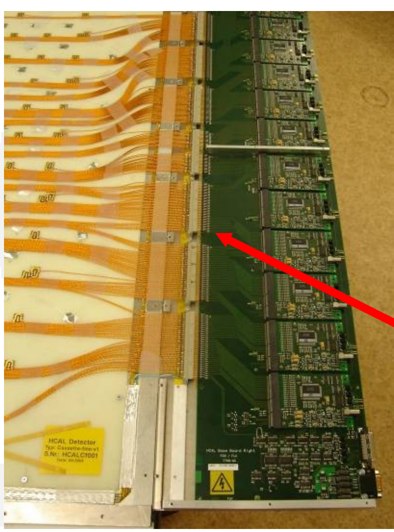




The input DACs allow to adjust HV channel by channel by slow control on each SiPM of the detector

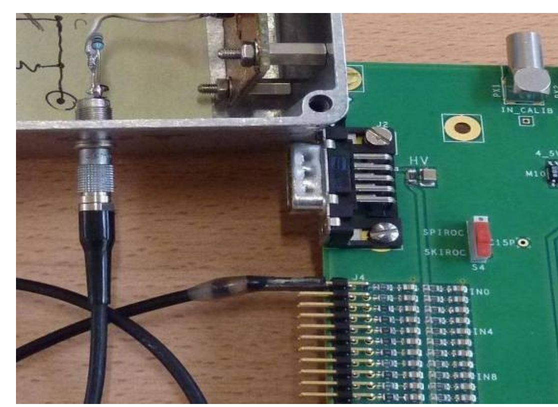






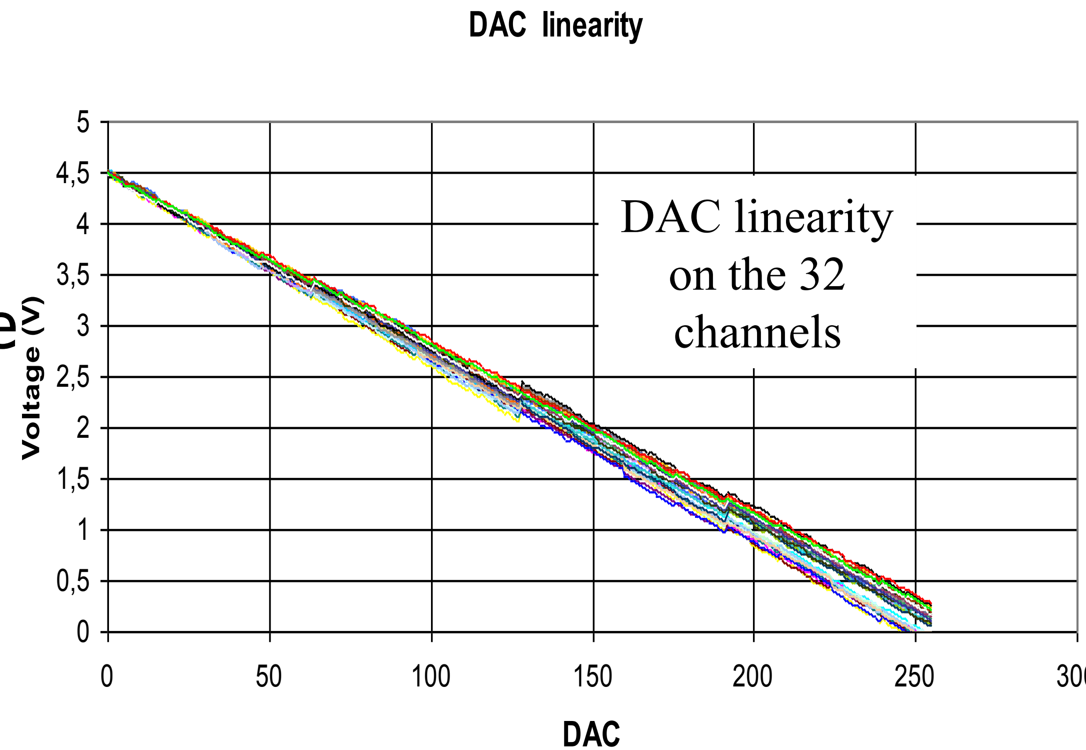
2 examples for SiPM connection allowing input DAC use

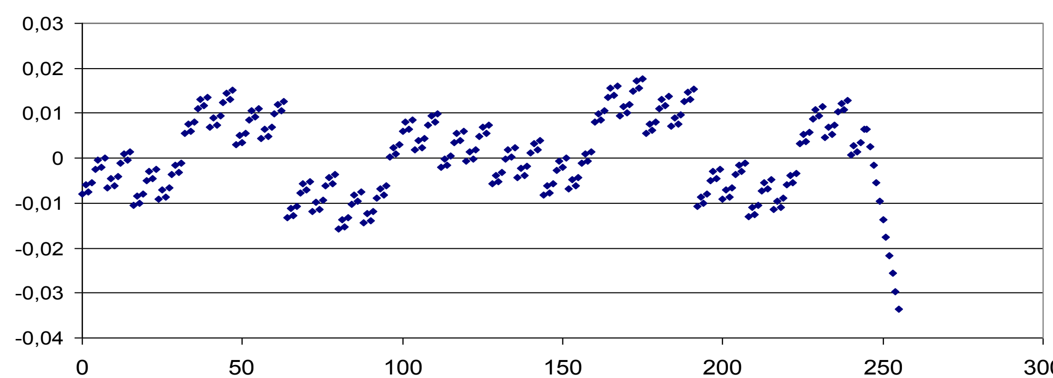
High voltage on the cable shielding



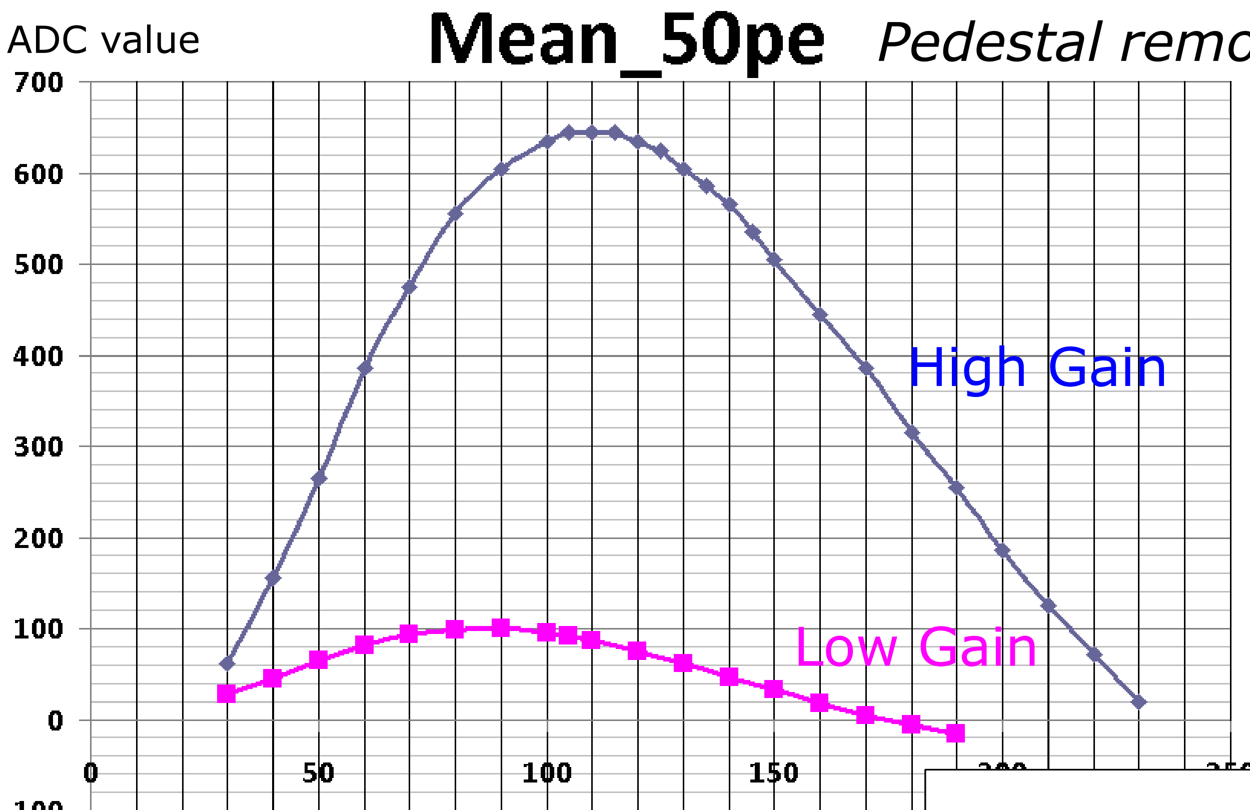
INPUT DACs

- Input DAC to optimize SiPM bias voltage (SiPM gain)
- 8 bits on 4,5V range => LSB : **20mV**
- **10µA** sink capability
- Ultra low power (**<1µW**)
- Linearity **±2%**
- DAC uniformity between the 32 channels : **~3%**





ANALOG OUTPUT (CHARGE)



ssh/ HG
G=200fF
Tau=50
C comp maxi
Cinj = 100pF

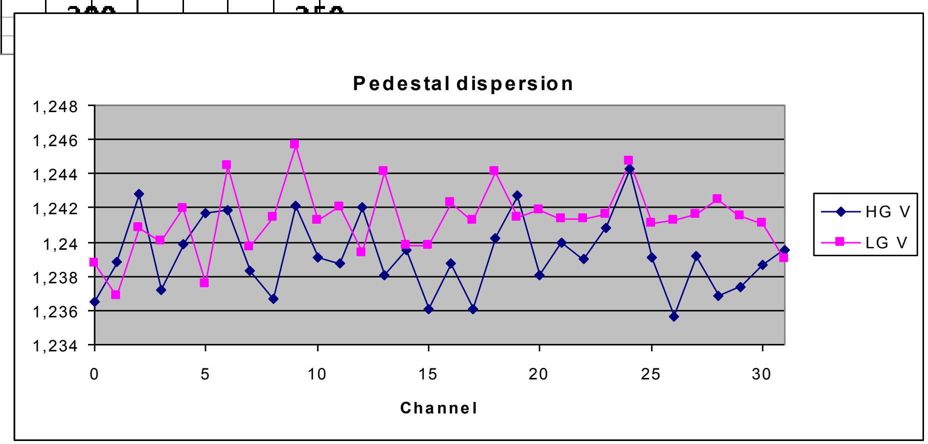
In= 50 pe -

F= 10kHz

100hit /point

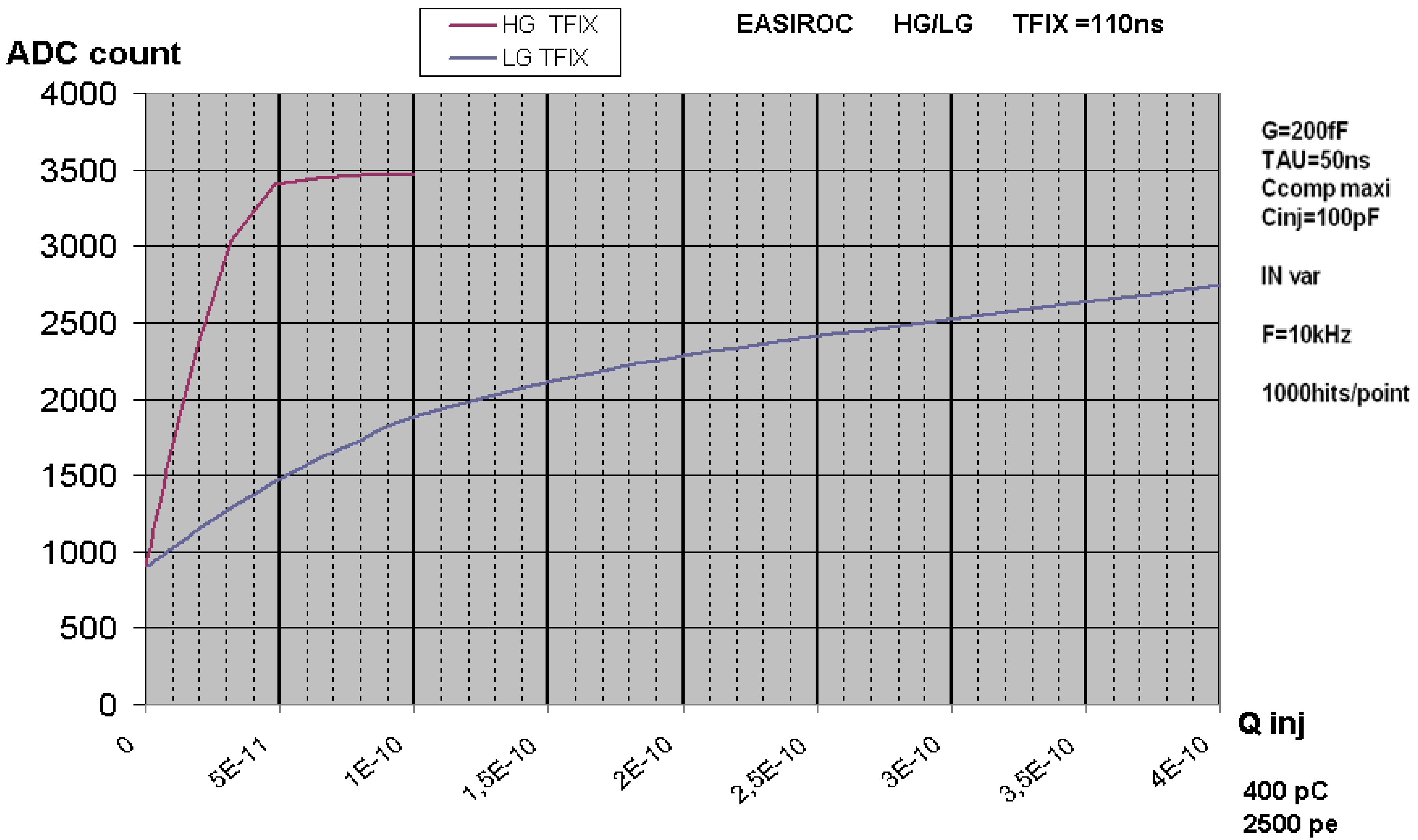
Hold scan performed on analogue data

[using external ADC]



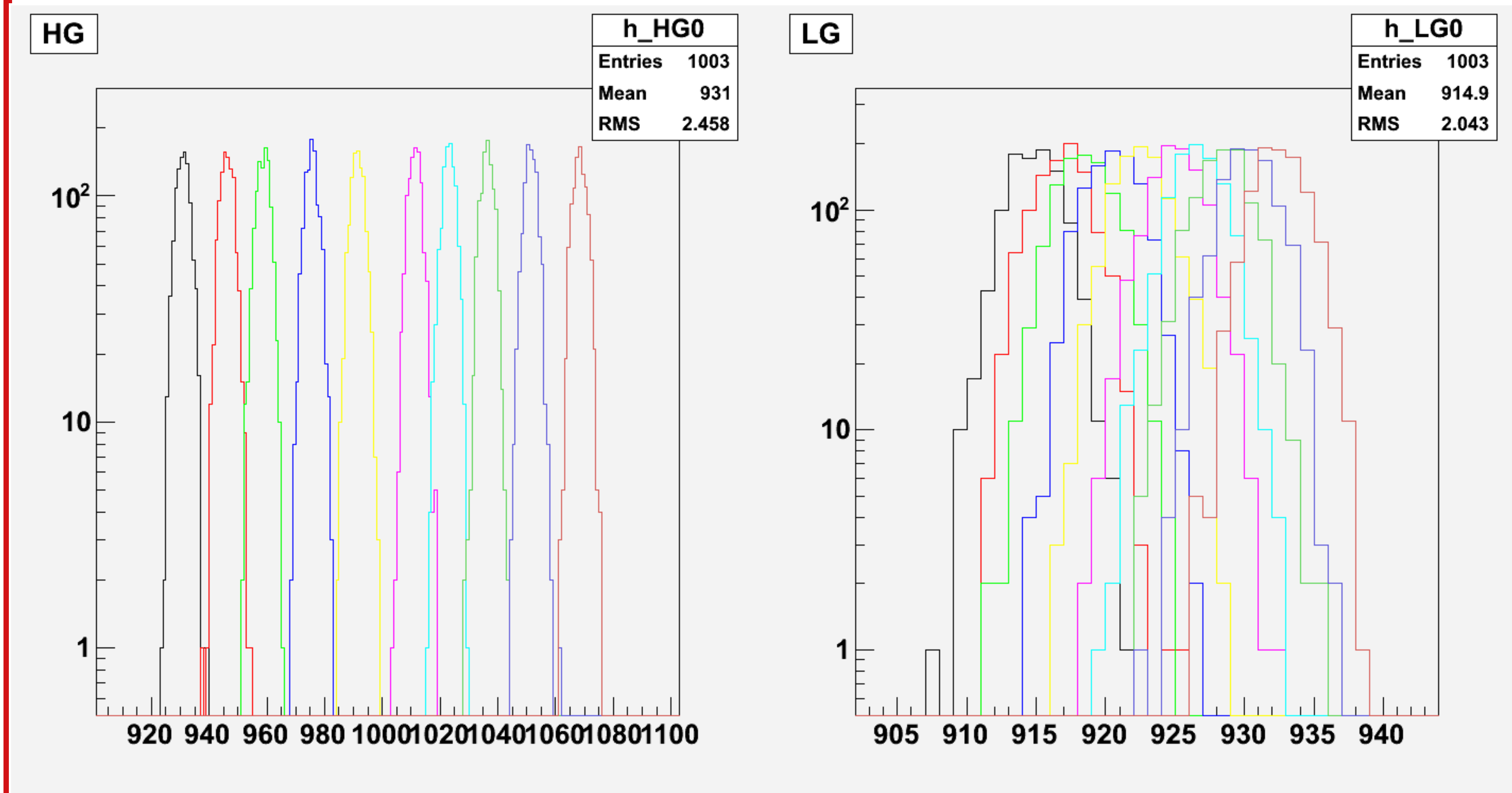
Pedestal uniformity for each Gain output <0.7%

CHARGE MEASUREMENT



ANALOG OUTPUT

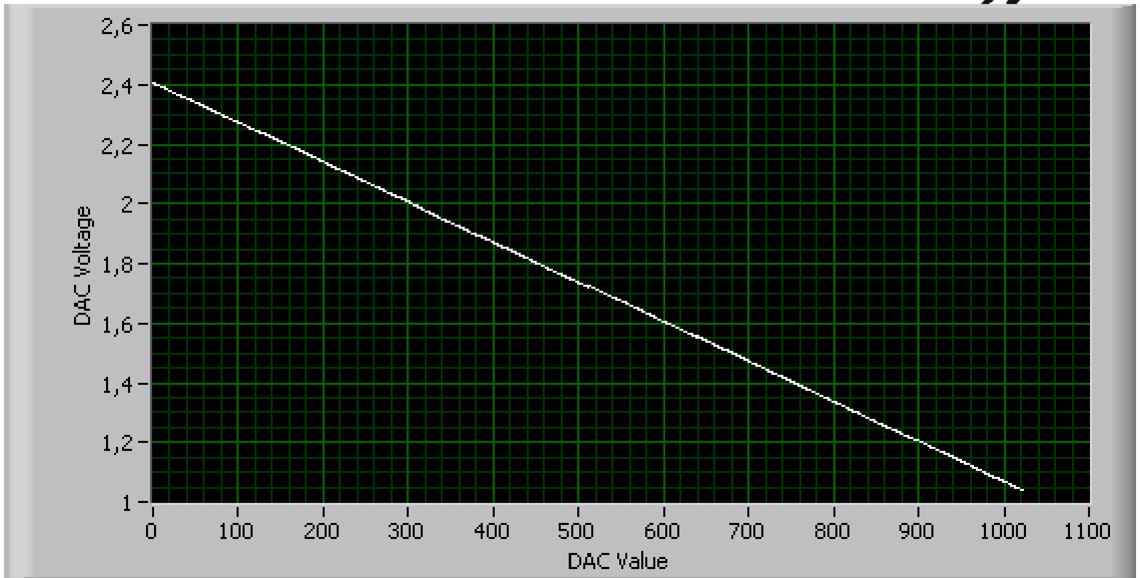
- Histogram for 1 to 10 pe- on both gains

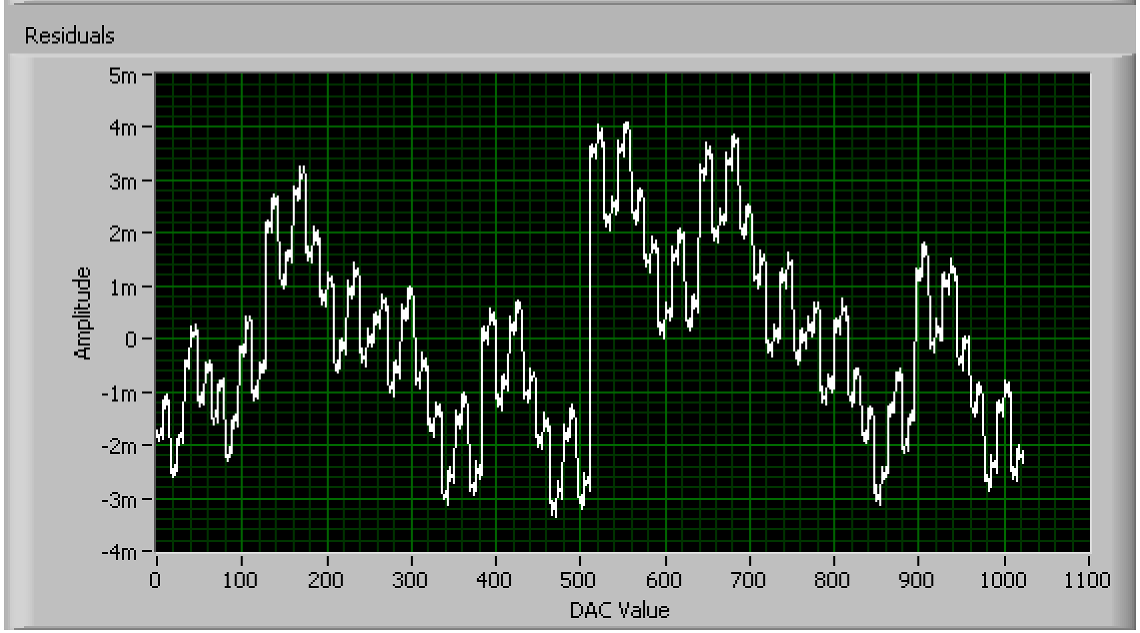


Courtesy : Ryotaro HONDA

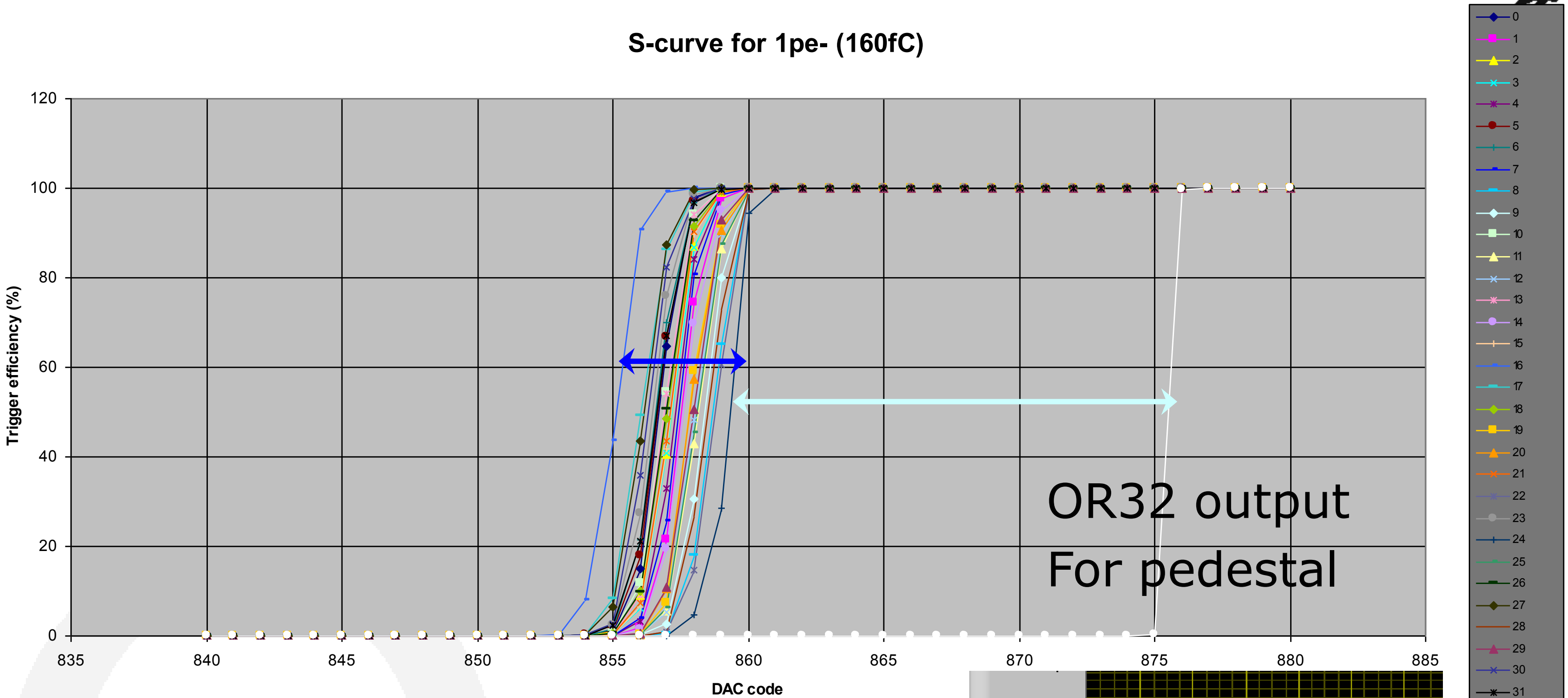
THRESHOLD DAC

- 10-bit DAC for Threshold adjustment (trigger)
- 10 bits on 1.3V range => LSB : **1.3mV**
- Linearity ±0.3%

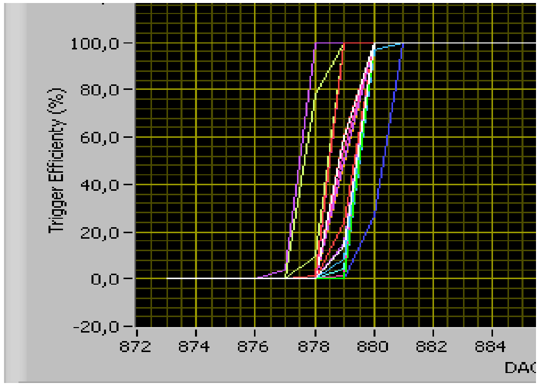




S-CURVES (TRIGGER EFFICIENCY)



OR32 output for 1pe on each channel



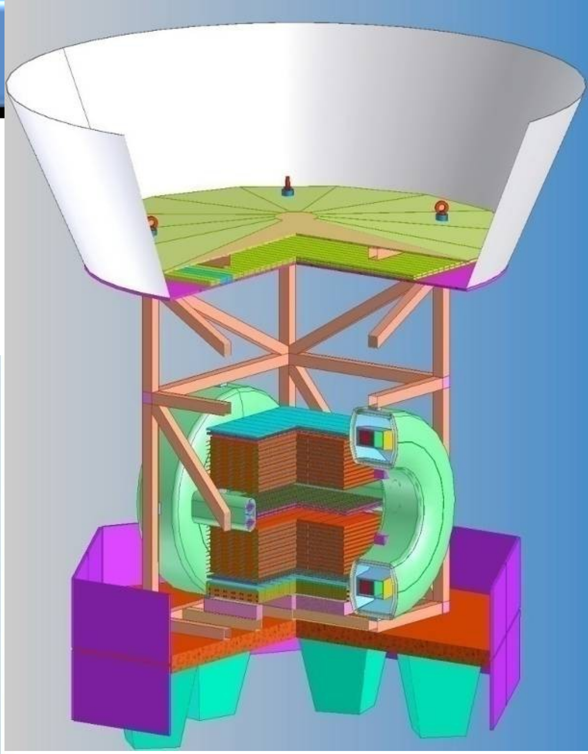
Individual pedestal

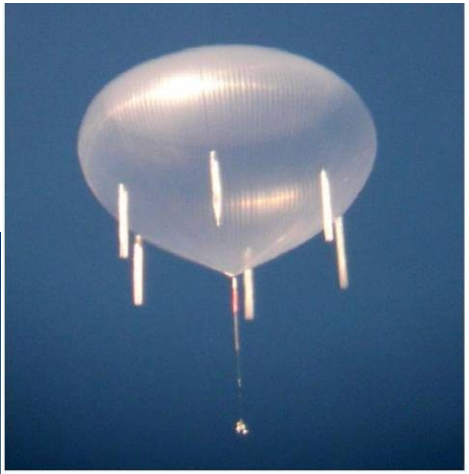
Dispersion : <5 DAC unit for 1pe

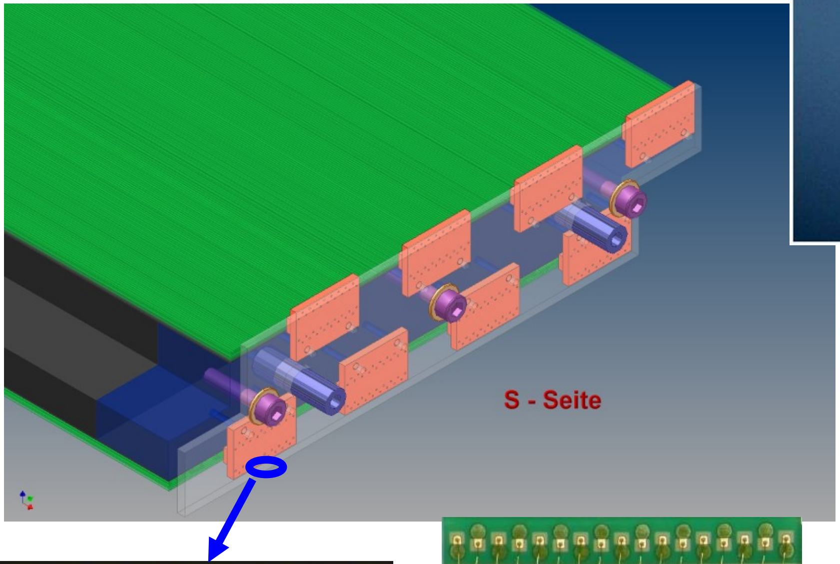
(8fC/DAC unit) *[Cf=200fF]*

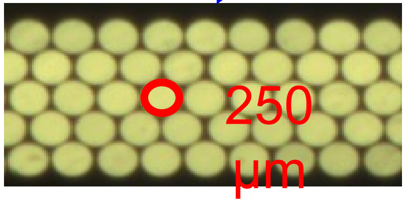
PEBS

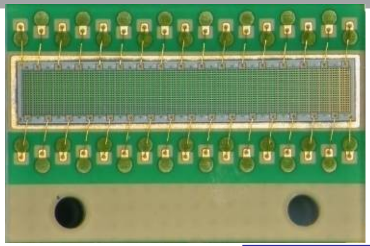
- **PEBS is a project in Research & Development phase The purpose of the experiment is a precision measurement of the electron & positron cosmic ray flux in the energy range from 1 to 2000 GeV.**

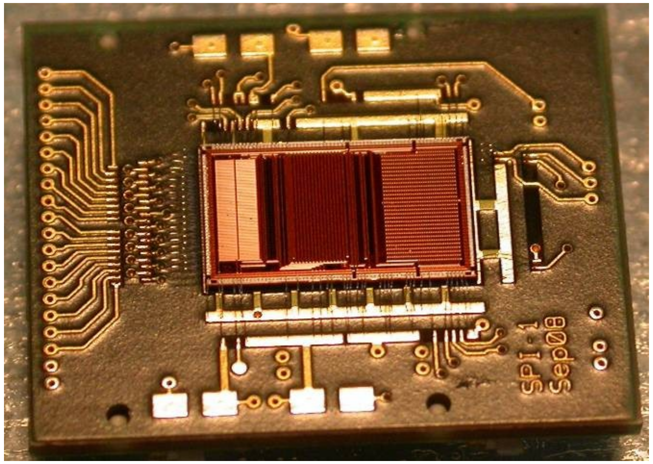












Courtesy: Waclaw KARPINSKI

RTWH Aachen

The MU-RAY project: high-resolution muon radiography with scintillators

Italy: Bologna,Firenze,Perugia,Napoli (INFN and Universities)
Istituto Nazionale Geofisica e Vulcanologia)
Japan: Tokyo University and Hearth Research Institute
USA: Fermilab

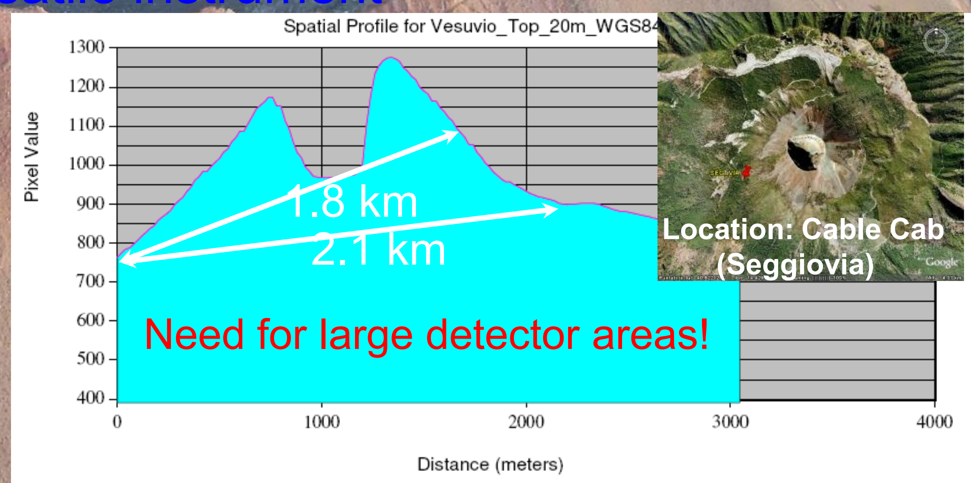
- International Collaboration of physicists, geologists and volcanologists to perform muon radiography of geological structures, Mt. Vesuvius first of all
- Design and build muon telescopes to be operated in difficult environments. Requirements:
  - modular, light, easy to transport and mount
  - little need for maintenance
  - very low power consumption
- Develop a methodology and a versatile instrument

INFN Napoli

Courtesy : Giulio Saracino

The challenge of Mt. Vesuvius

Given the mountain topology and the deep crater, there are ≈2 km of rock to cross!

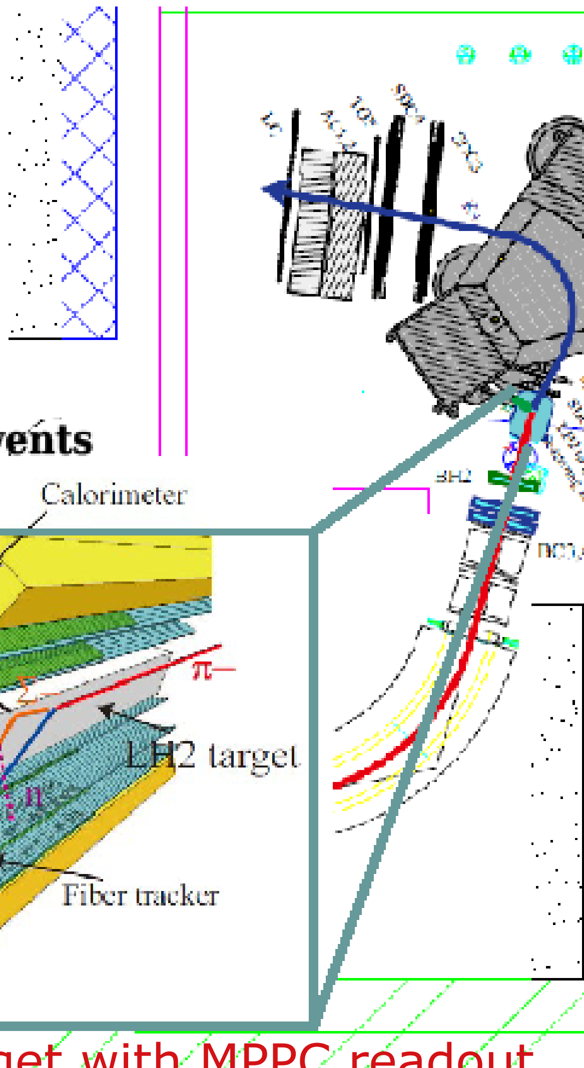


Experimental setup for YN scattering

Tohoku University + KEK

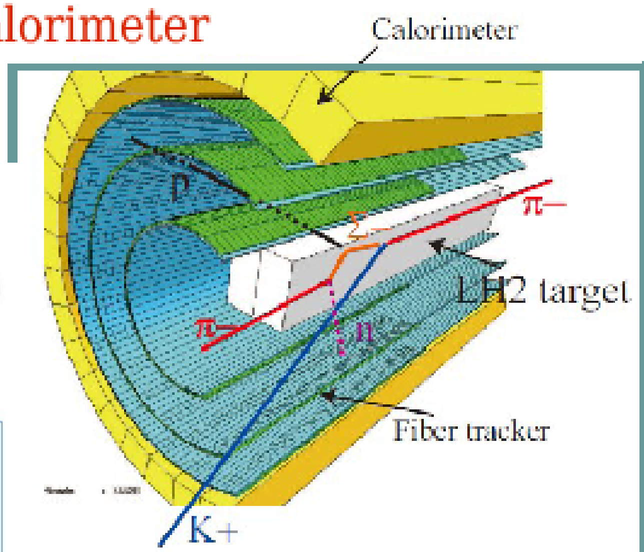
Courtesy: Ryotaro HONDA

- J-PARC K1.8 beam line
- Hyperon production
  - 1.3 GeV/c $\pi^- p \rightarrow K^+ \Sigma^-$ reaction
  - LH2 target
- Basic spectrometer
  - K1.8 beam line spectrometer
  - SKS spectrometer



New detector system for scattering events

Fiber tracker and calorimeter

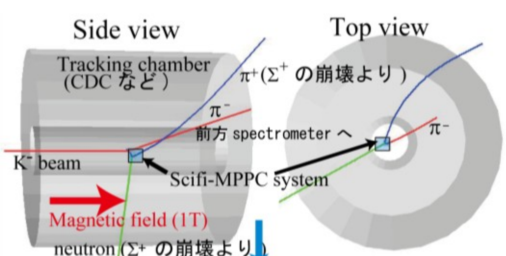


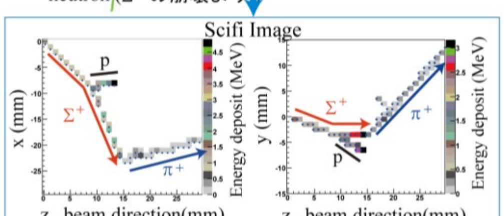
Fast time response
- Work in a high beam intensity

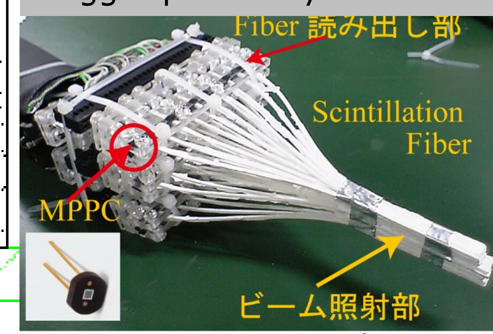
Large gain (10^5~10^6)
- Possible to detect 1 photon

Operation in the magnetic field
- Combination of Imaging and Spectrometer

Trigger possibility





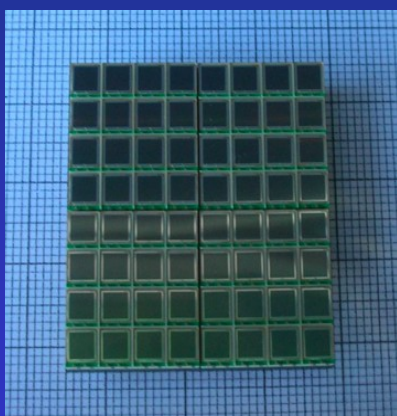


MPPC 50ch を用いた小型プロトタイプ

Active target with MPPC readout

SIPMED : SIlicium Photomultiplier for bioMEDical imaging

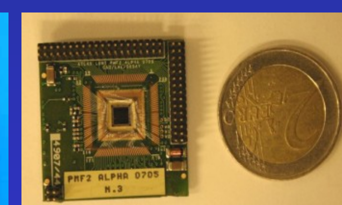
To develop a novel compact photodetection system with high energy and temporal measurement capabilities for radio-guided surgery



Task 1 : Characterization of single SiPMs and SiPMs matrixes performances (scintillation and fluorescent light measurements) under laboratory and real medical conditions (e.g. temperature up to 37 ° C)

Task 2 : Design and conception of a new optimized SiPM read-out electronics for both scintillation and fluorescent light measurement

Miniaturisation of the electronic board ->



Task 3 : Development and validation of new per-operative prototypes :

1) a compact positron probe

2) a mono-pixel fluorescent probe

3) a large field-of-view and ultra-compact intraoperative gamma-camera

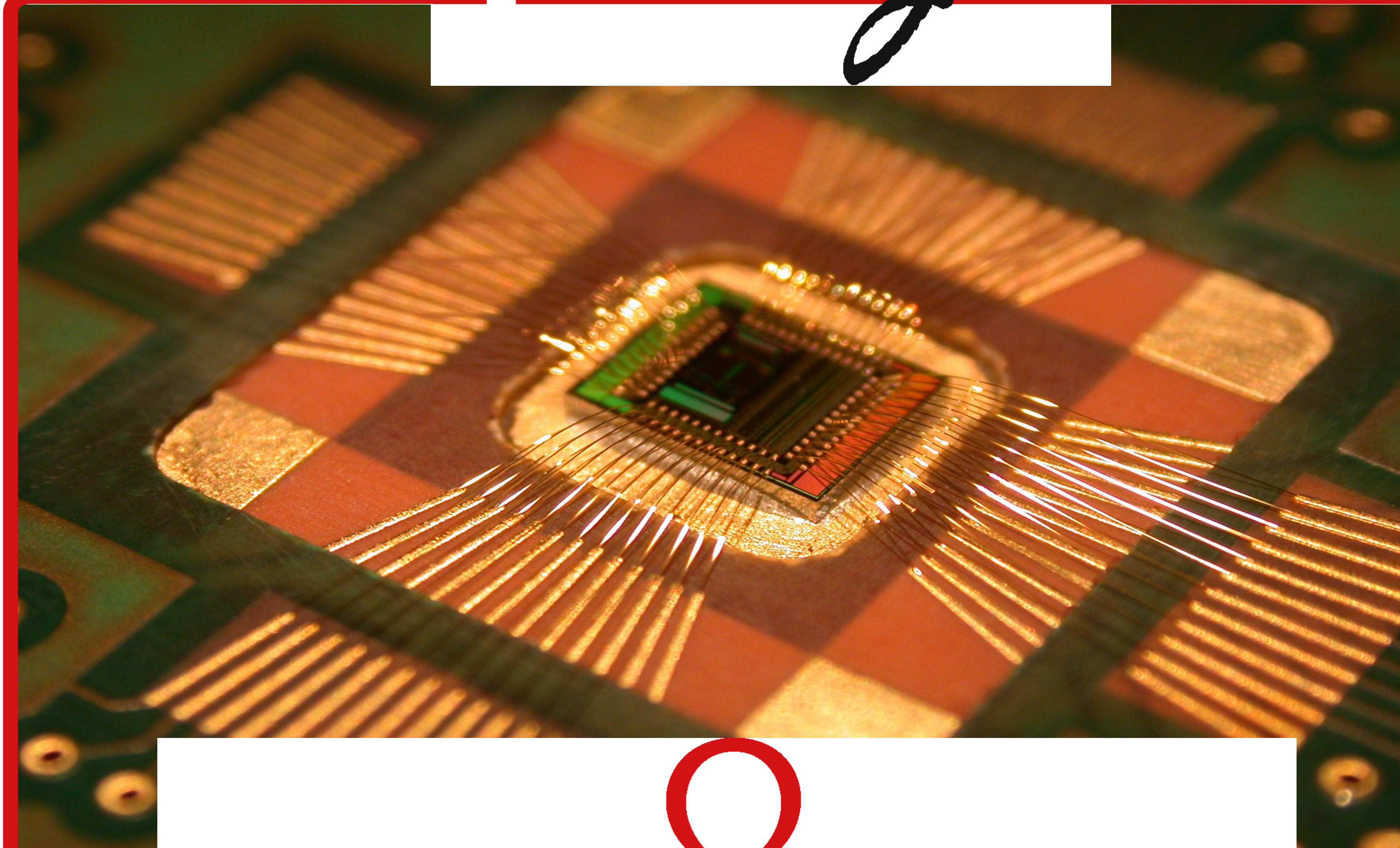
IMNC

Courtesy: Laurent MENARD

EASIROC SUMMARY

- 1pe$^-$ -> 2000pe$^-$ charge measurement
- 100% Trigger efficiency @ 1/3photo-electron
- Versatility & easy use
  - Testboard & Software ready to use, embedding acquisition system
- Very low power consumption
  - Full power pulsing capability
  - Unused stages can be shut down
- Large scale production in 2010
  - Already used in experiments (astrophysics, vulcanology, nuclear physics, medical imaging)
- Any extra information available on http://omega.in2p3.fr

Omega



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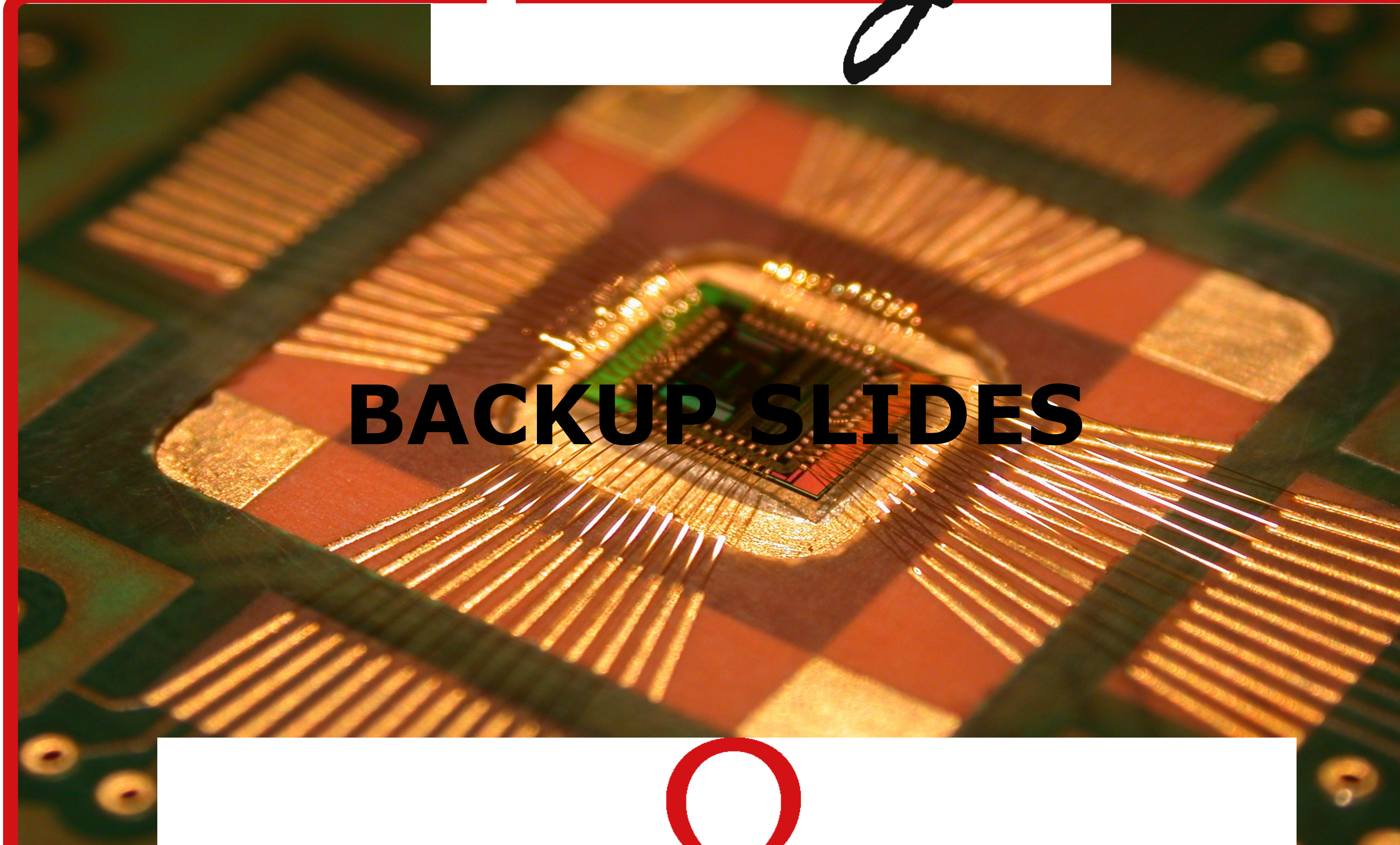
Omega



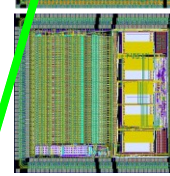
BACKUP SLIDES

Orsay MicroElectronics Group Associated

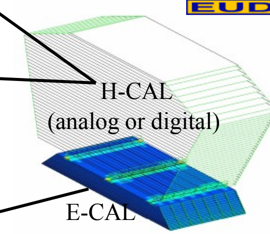
Engineering run (2010)

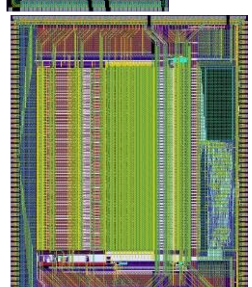
- **Reticle size : 18x25 mm2**
  - 50-55 reticles/Wafer
  - 25 wafers
- **Final arrangement:**
  - **« Calice » chips produced:**
- **7 Hardroc 2b** => ~9000 chips
  - **1 Spiroc 2a** => ~1250 chips
  - **1 Spiroc 2b** => ~1250 chips
  - **1 Skiroc 2** => ~1250 chips
  - **Additionnal chips produced:**
    - 1 Spaciroc : JEM EUSO experiement
      => ~1250 chips
    - 1 Maroc 3 : for PMT readout
      => ~1250 chips
    - 3 Easiroc : for PEBS experiment
      => ~3750 chips (5000 received)
- **Production run for CALICE chips**
  - => **cost reduction** for CALICE

SPIROC2B
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07 / June 08 / March 11



HARDROC2B
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06 / June 08 / Sept 09

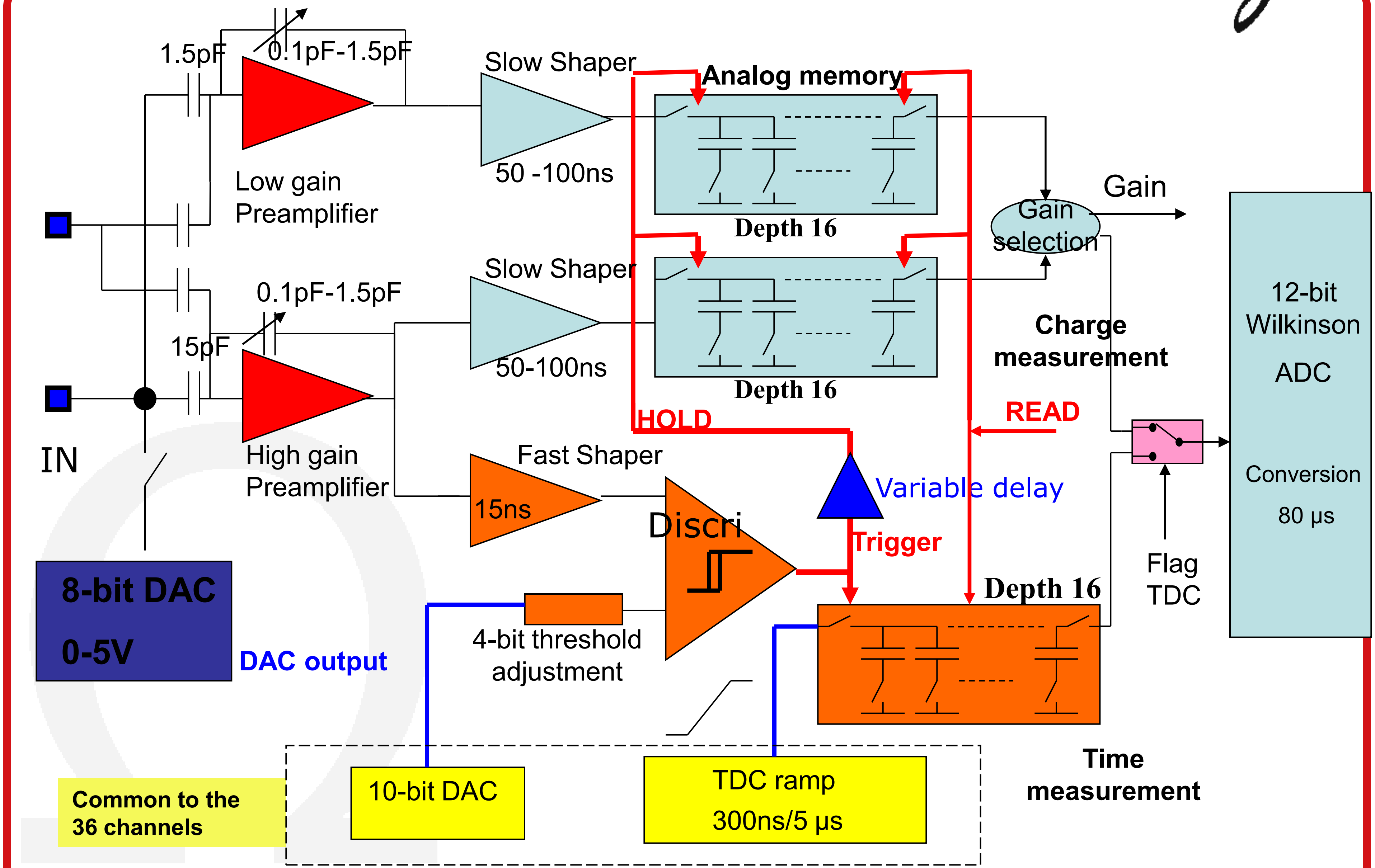


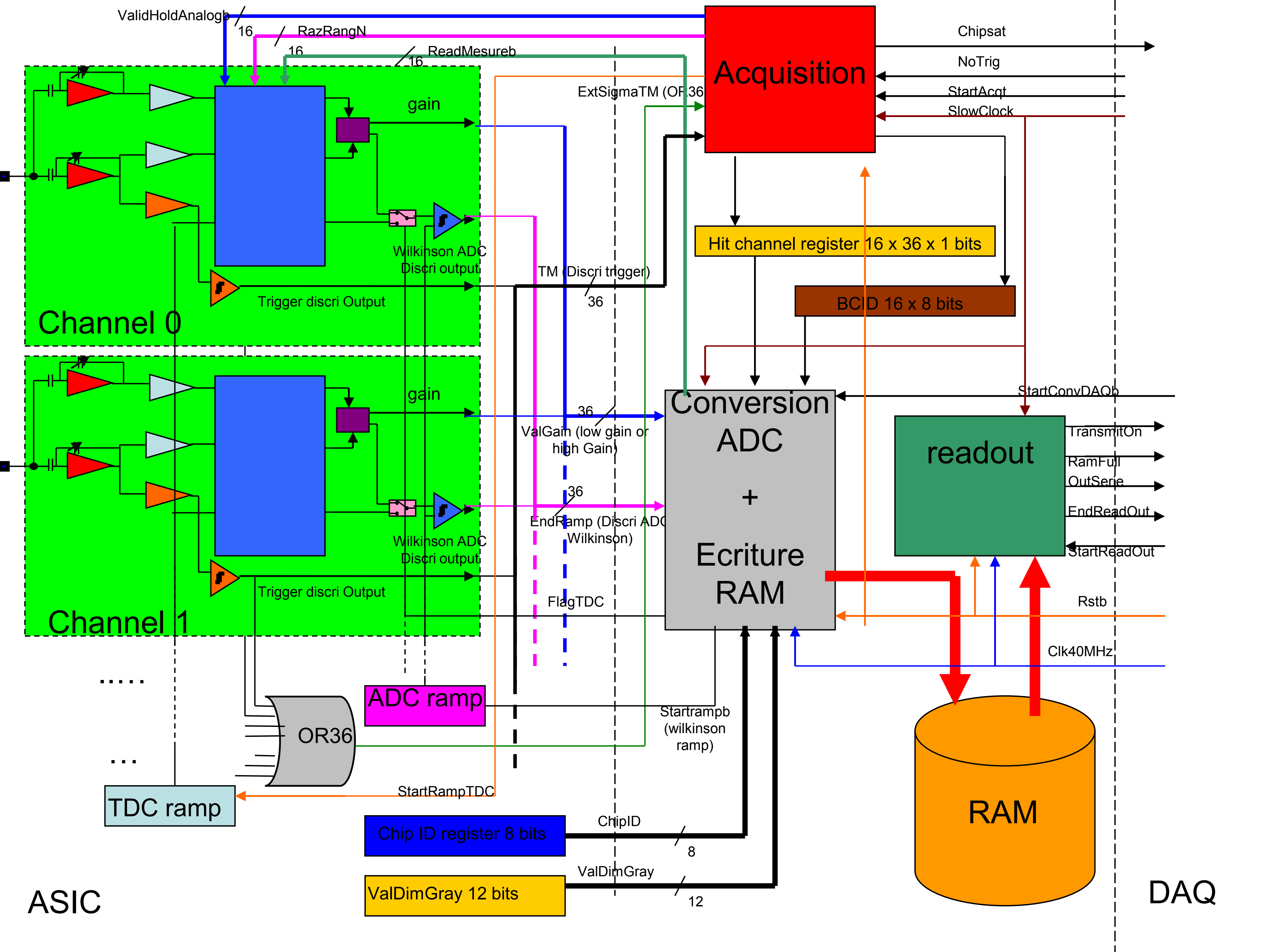


SKIROC2
ECAL
(Si PIN diode)
64 ch. 64mm²
March 11

Calorimeter for ILC

SPIROC : One channel schematic

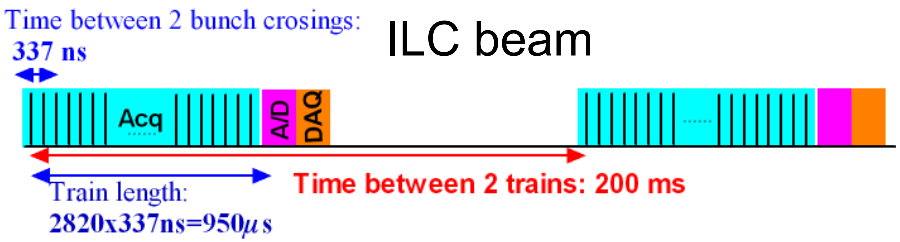


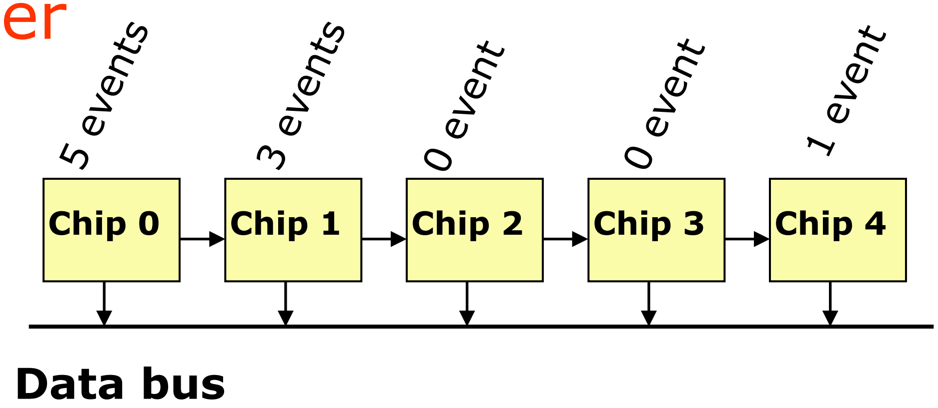


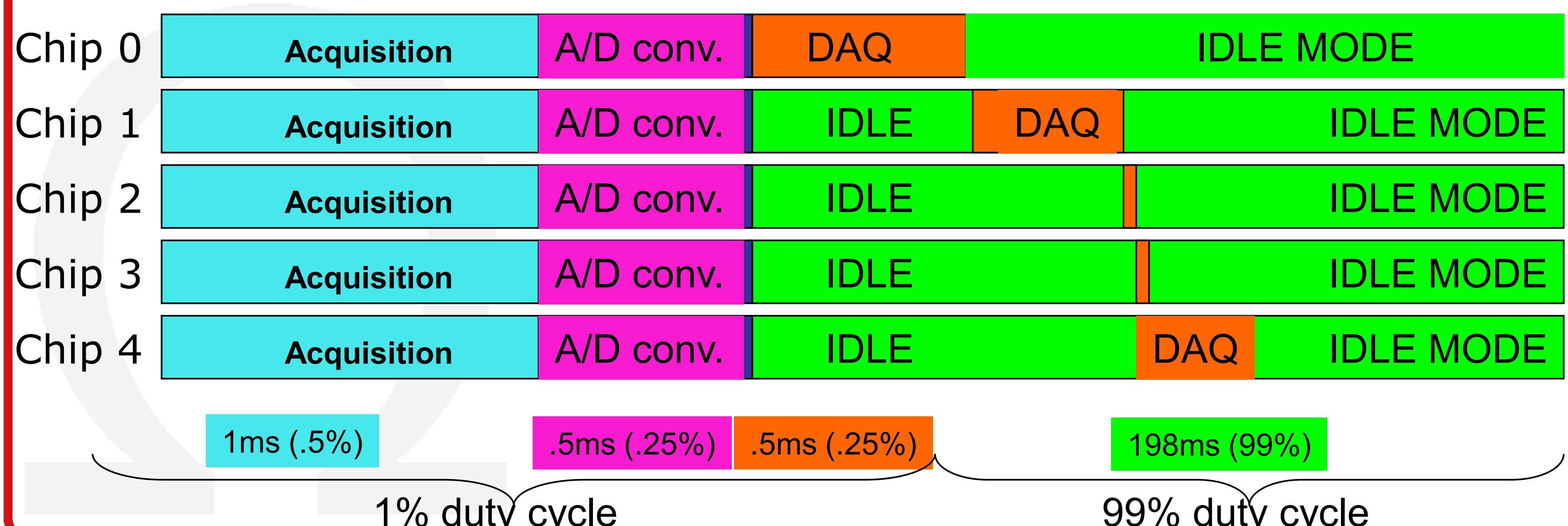
ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR36)
gain
Wilkinson ADC
Discri output
TM (Discri trigger)
36
Trigger discri Output
Channel 0
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
StartConvDAQb
Conversion
ADC
+
Ecriture
RAM
gain
36
ValGain (low gain or
high Gain)
36
EndRamp (Discri ADC
Wilkinson)
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
FlagTDC
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
ADC ramp
OR36
Startrampb
(wilkinson
ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray 12 bits
ValDimGray
12
RAM
ASIC
DAQ

SPIROC ReadOut: token ring

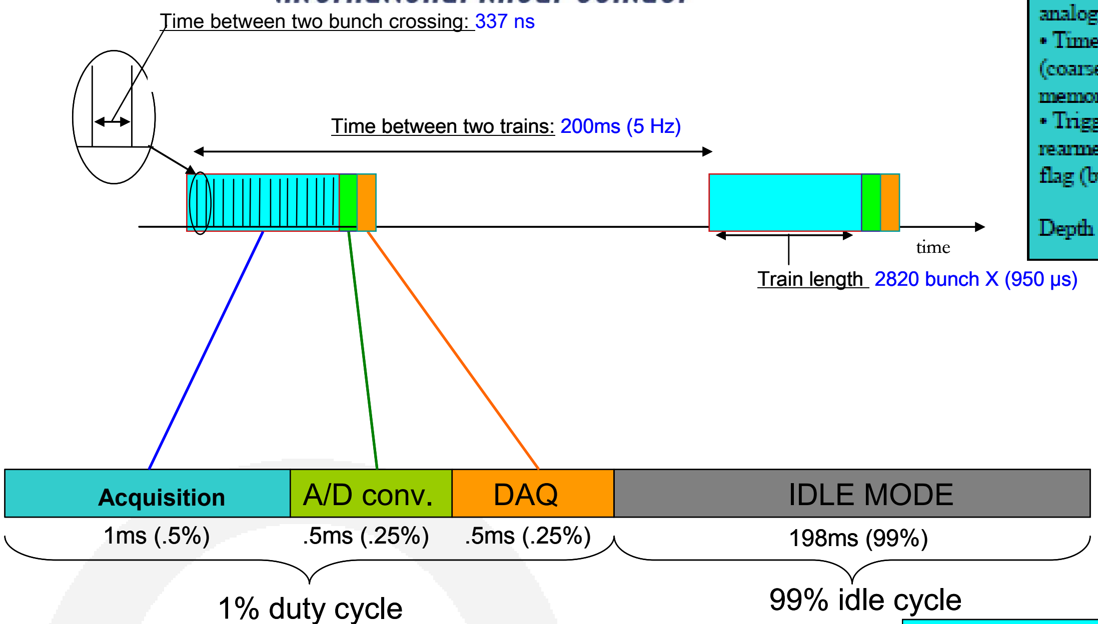
- Readout architecture common to all calorimeters
- Minimize data lines & power





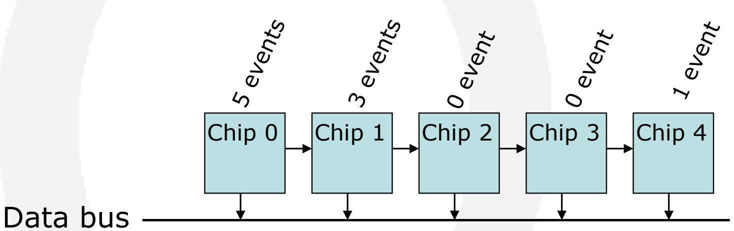


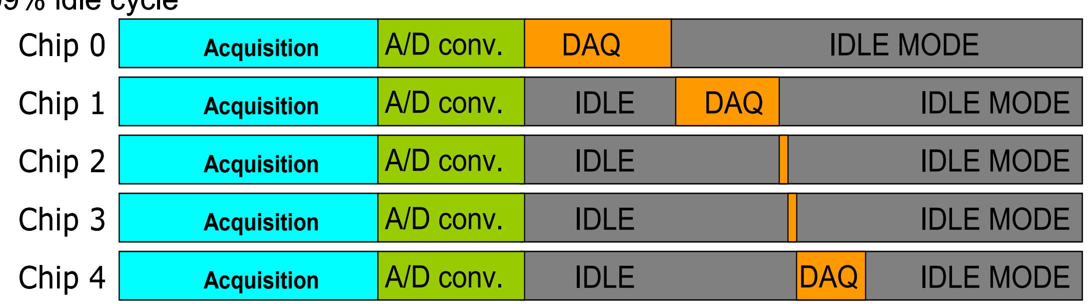
ILC beam structure and SPIROC running modes



Acquisition	A/D conversion	DAQ
When an event occurs : • Charge is stored in analogue memory • Time is stored in digital (coarse) and analogue (fine) memory • Trigger is automatically rearmed at next coarse time flag (bunch crossing ID) Depth of memory is 16	The data (charge and time) stored in the analogue memory are sequentially converted into digital data and stored in a SRAM.	The events stored in the RAM are readout through a serial link when the chip gets the token allowing the data transmission. When the transmission is done, the token is transferred to the next chip. 256 chips can be read out through one serial link

- **Readout based on token ring mechanism initiated by DAQ**
- **One data line activated by each chip sequentially**
- **Readout rate few MHz to minimize power dissipation**



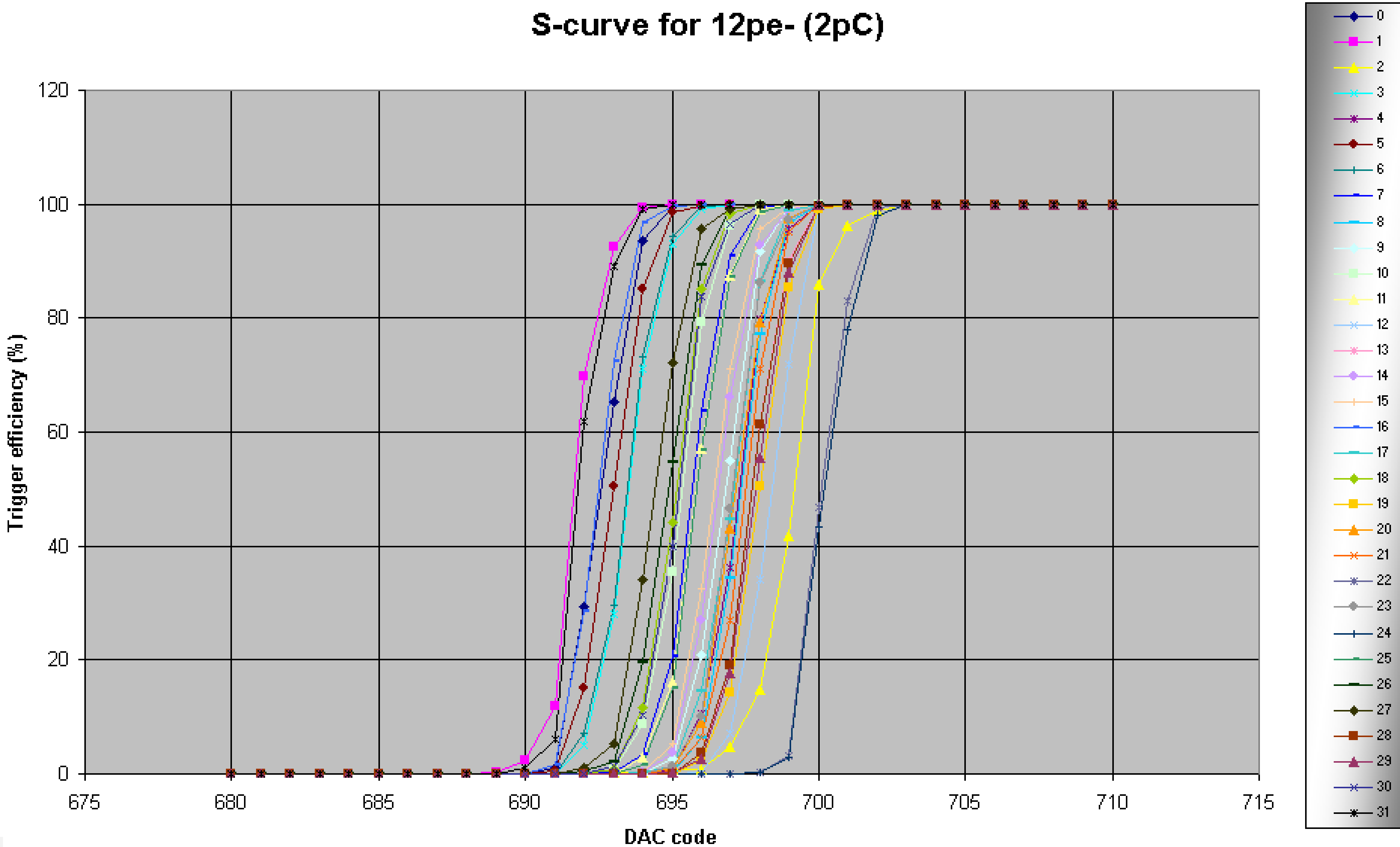


Two orders of magnitude saved on the consumption by using the ILC beam structure and the power pulsing

- Default value for Slow Control
  - Chip ready to use after a simple SC reset (except Threshold DAC)

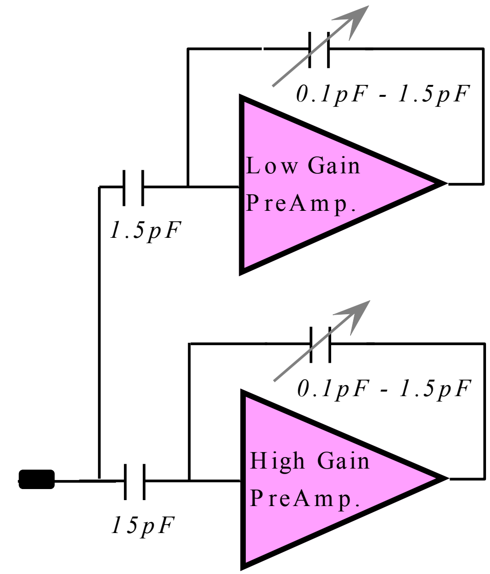
- Debug embedded feature :
  - Analog Probe system allow to monitor each critical point in the chip
    - 32 PreAmplifiers High Gain output
    - 32 PreAmplifiers Low Gain output
    - 32 Slow Shapers High Gain output
    - 32 Slow Shapers Low Gain output
    - 32 Fast Shapers output

S-CURVES (TRIGGER EFFICIENCY)



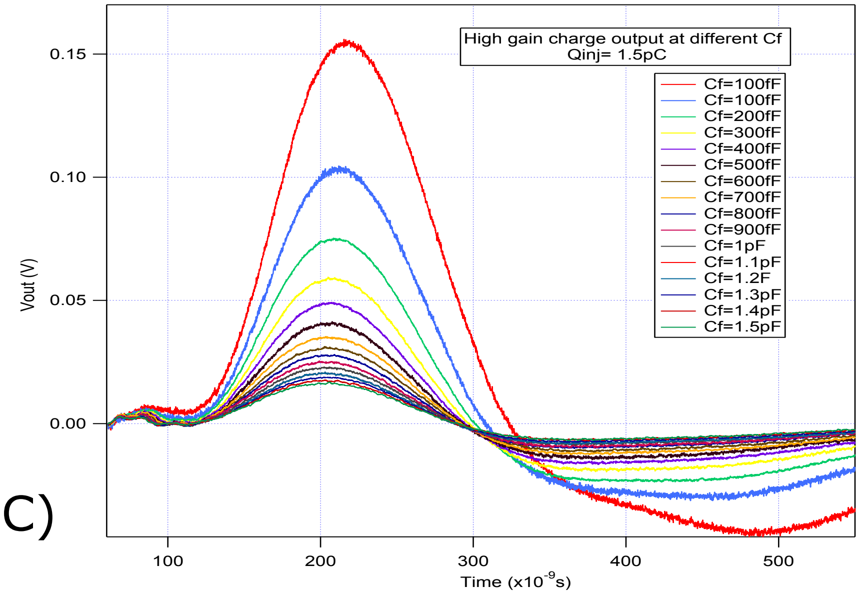
INPUT PREAMPLIFIERS

- Bi-gain low noise preamp
  - Low noise charge preamplifier capacitively coupled = voltage preamplifier
  - Gain adjustable with 4 bits common to all preamps : Cf=0.1, 0.2, 0.4, 0.8 pF
  - Positive input pulse
  - Power : 2 mW (unpulsed)

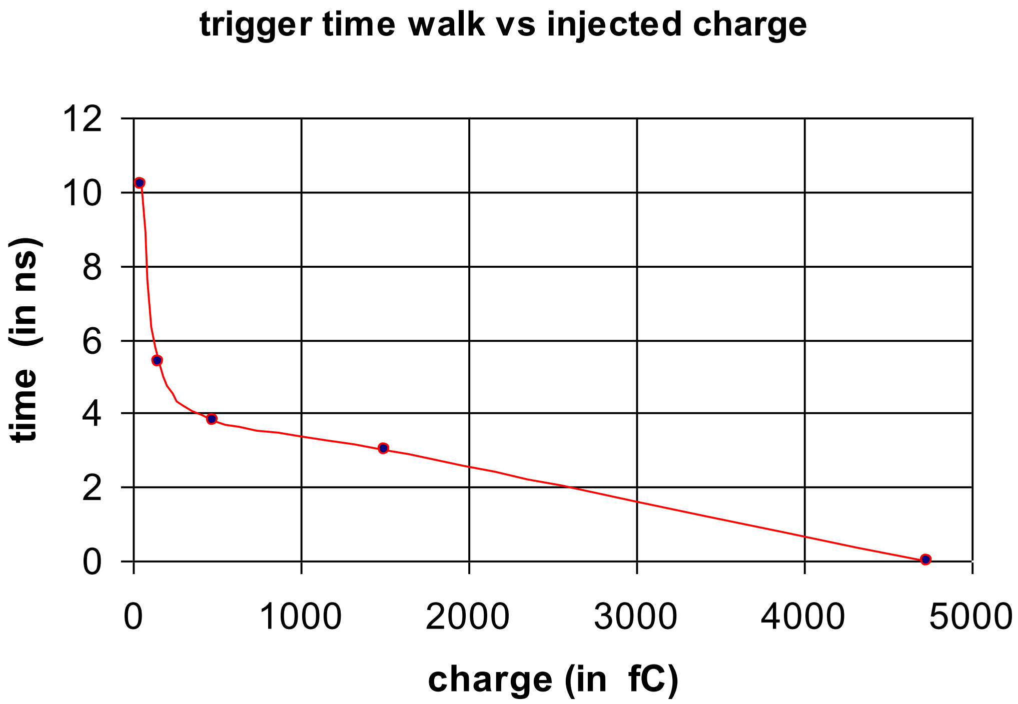


- High gain :
  - 15pF coupling capacitor
  - 8 mV/pe in High Gain
  - Noise : 1.4 nV/sqrt(Hz)

- Low gain at preamp level
  - 1.5pF coupling capacitor
  - 0.8 mV/pe, MAX : 2000 pe (300pC) *[@Cf=400fF]*



TRIGGER TIME WALK



ANALOG CROSSTALK

- **Very low electronic cross-talk : 0.3% (long distance cross talk due to slow shaper voltage reference: If this voltage decoupled with 100µF, it becomes negligible ~0.04%)**