Beam Loss Monitors operating at Cryogenic Temperature with FPGA- Based TDC Signal Processing

Arden Warner and Jin-Yuan Wu
June 10th, 2011

Introduction

- Loss monitor design and characteristics
- Recycling Integrator Signal Processing
- FPGA-TDC test with Loss monitor
- Loss monitor test (cryogenic/room temperature)
- Cryomodule Interface

Cryogenic Beam Loss Monitors (Ionization chamber)

Monitors and recycling integrator electronics fabricated and calibrated by Bridgeport Instruments, LLC.

Highlights

- operation in air and high vacuum
- Operates from 5K to 350K
- Stainless steel vessel, 120cm^3, filled with He-gas
- He-gas filling at 1.0- 1.5 bar pressure
- Sensitivity: 1.9 pA/(Rad/hr)
- Readout via current-to-frequency converter (1.9 Hz/(Rad/hr) and FPGA-TDC
- Pulses can be sent through long cables

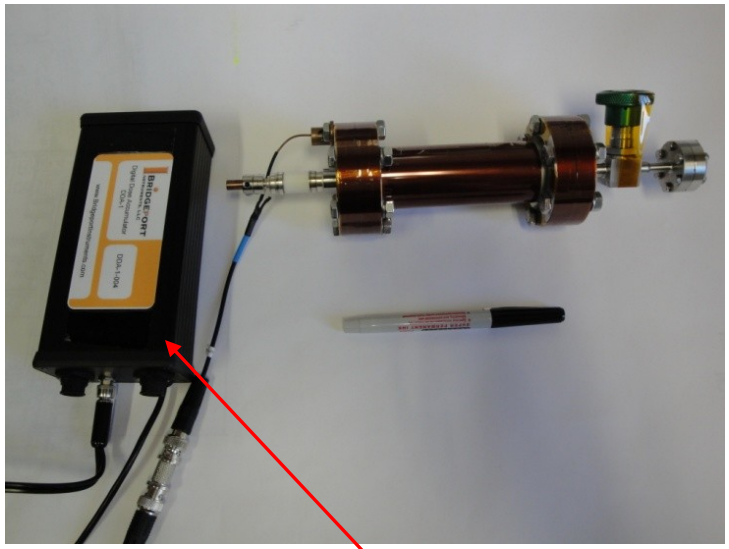
Features

- Custom-built prototype detector for operation as a beam loss monitor at cryogenic temperatures
- Helium filled ionization chamber with signal current proportional to dose rate
- All material radiation hard and suitable for operation at 5K
- Current is measured with a recycling integrator I-F converter for low current and a wide dynamic range. A Fermilab designed FPGA based TDC measures time intervals between pulses output from the recycling integrator ensures a fast response along with current measurement resolution better than 10-bits.

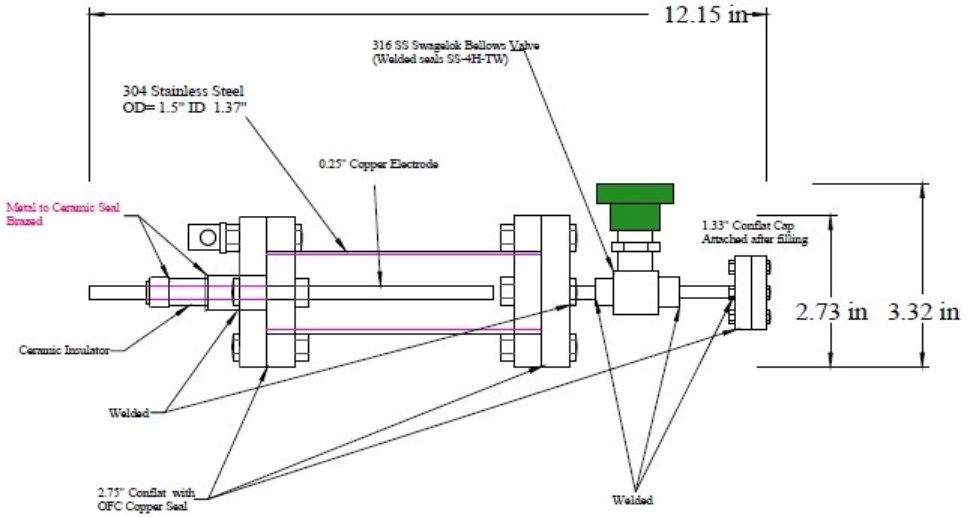
Cryogenic Beam Loss Monitors Specifications

Parameter	*Symbol*	*Min*	*Typ.*	*Max*	*Comment*
Mechanical					
He-volume	V		120 cm^3		
Fill pressure	p		1.0 bar		absolute
Diameter			2.73 inch		without shroud
Length			11.2 inch		without shroud
Detector Operation					
HV			-95 V	-120 V	on chamber body
Sensitivity			1.9 pA / (Rad/hr)		calculated
			6.84 nC/Rad		calculated
Electronic I/O					
Ballast resistor	RB		1.0 MΩ		safety resistor
Supply voltage	Vdd	4.5 V	5.0 V	5.5 V	
Supply current	Idd		105 mA		
Charge per pulse	Qp		**2.286 pC**		
Frequency out	f		**0.831Hz / (Rad/hr)**		after offset of 100 Hz nominal
Offset current	Ioff		100 pA		
Offset current drift	dIoff/dT			10 pA/K	
Environmental					
Operating temperature	T	5K		350K	chamber only
Magnetic field				TBD	

Cryogenic Ionization chamber 5k – 350K



Bias voltage and electronics



- The electronics is self-contained and requires no computer to operate.
- Helium was chosen because of its properties (boiling point 5K) and the fact that it will be in a helium environment during operation anyway.

Fill port

Cryogenic Loss Monitor operation

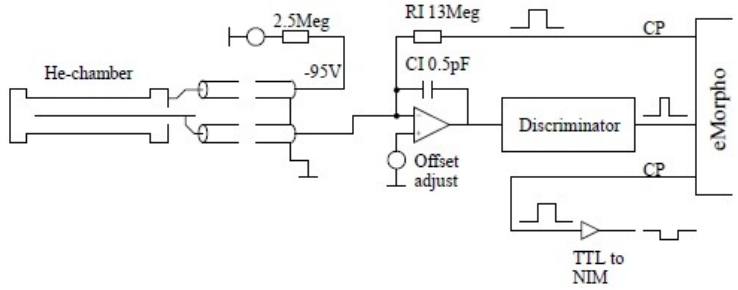
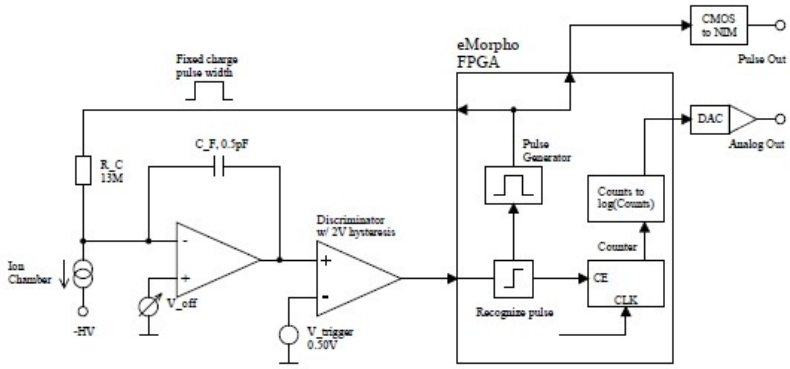


Figure 1: Schematic view of the dose rate monitor.



Drawing 1: Simplified schematics of the digital dose accumulator using a recycling inegrator and the eMorpho platform. Future versions may use a lower-cost platform.

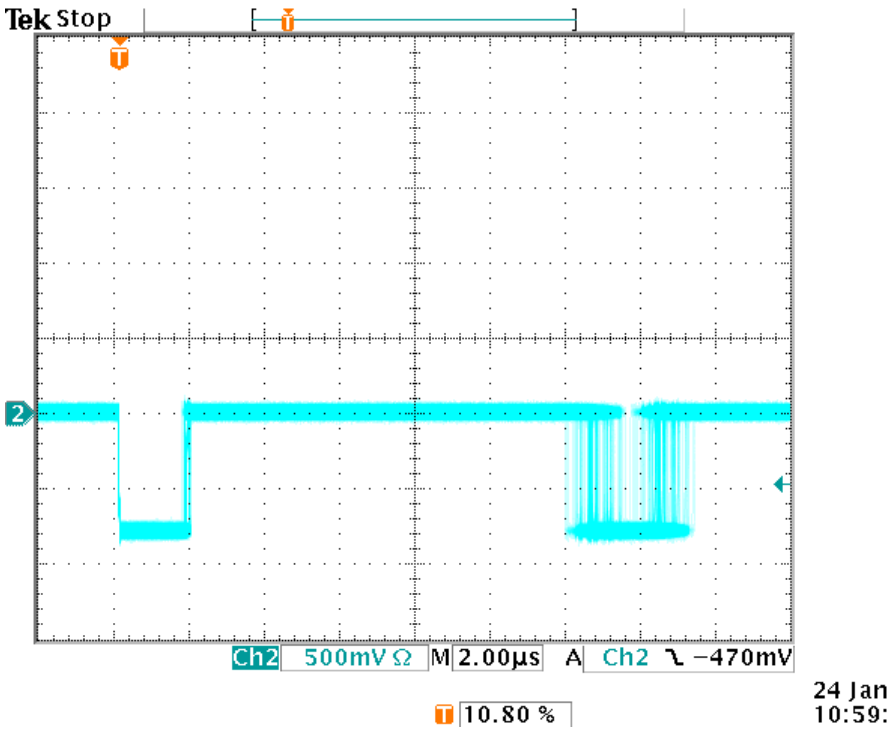
The chamber housing is held at negative potential and negative charge is collected on the center electrode. The HV is -95 V and is kept well below the minimum breakdown voltage of 156V in Helium.

The electronics uses a recycling integrator as a current to frequency converter with a wide dynamic range. The charge per pulse is 1.63pC or 238μR at 1 atm (room temp) of He.

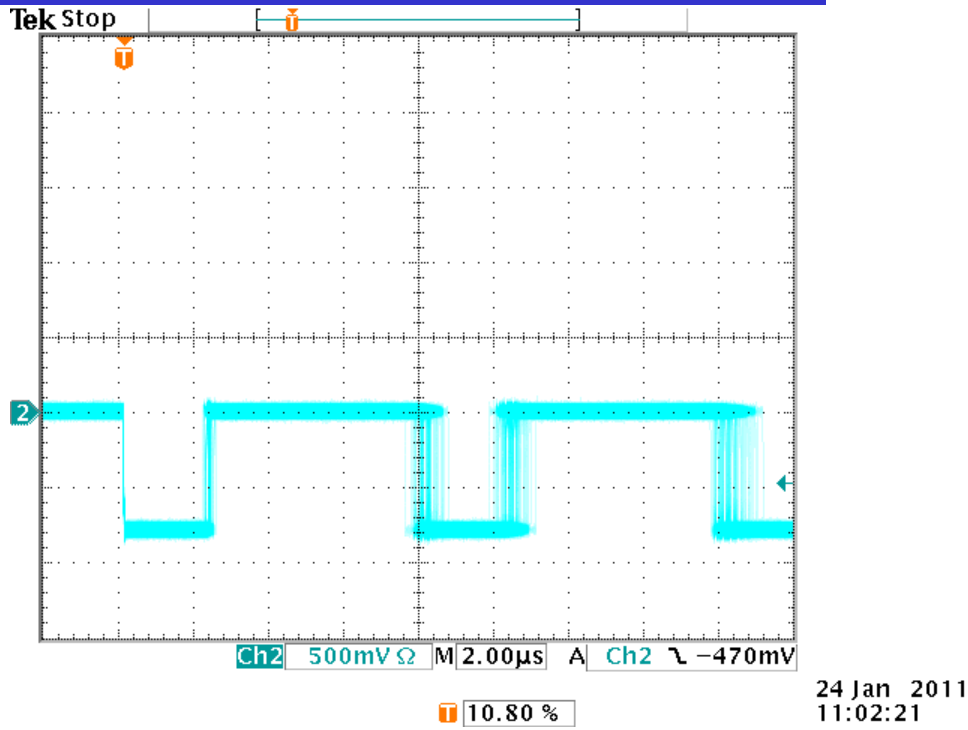
The recycling integrator consist of a charge integrating amplifier with a 0.50 pF capacitance followed by a discriminator which senses when the capacitor is fully charged.

The FPGA generates a fixed-width (1.2μs) discharge pulse with an amplitude of 3.3V. It connects to the amplifier input via a 13 MΩ resistor, creating a 254 nA discharge current

Bench top measurements



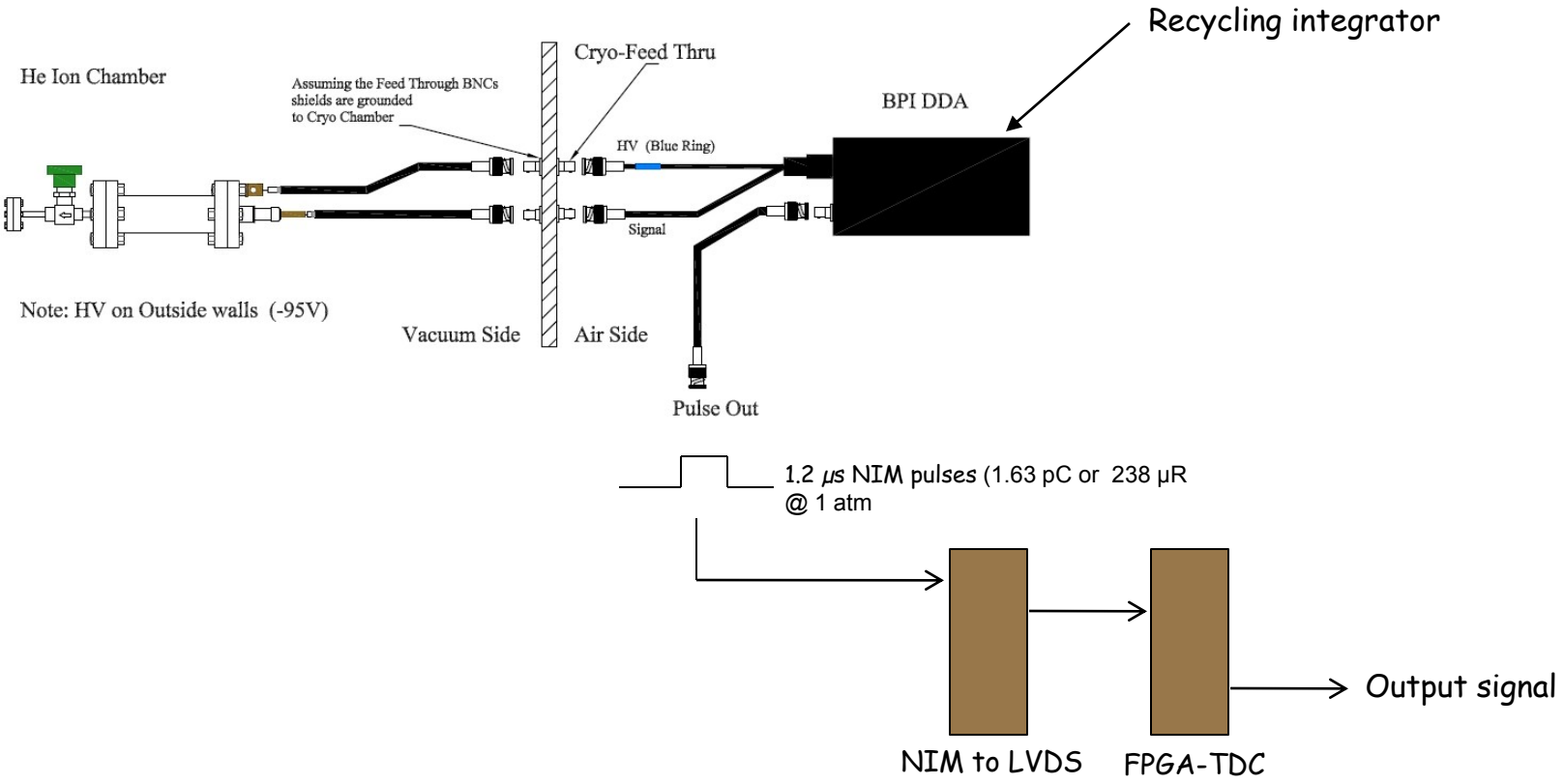
Pulses with 150nA input current



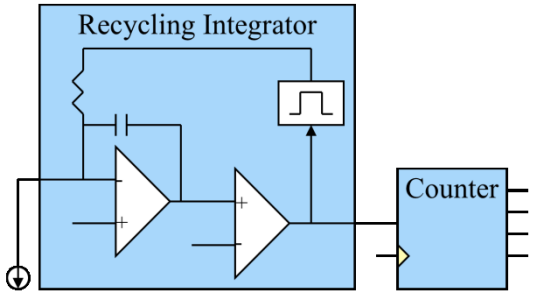
Pulses with 300nA input current

The maximum periodic pulse rate at the output is close to 700 KHz. The corresponding maximum chamber current is 1.60 μA or 842 KR/hr. Pulses can be sent loss-free over great distances and the technique allows to measure radiation levels with dynamic range of 100,000: 1

Cryogenic Loss Monitor Connection and signal path

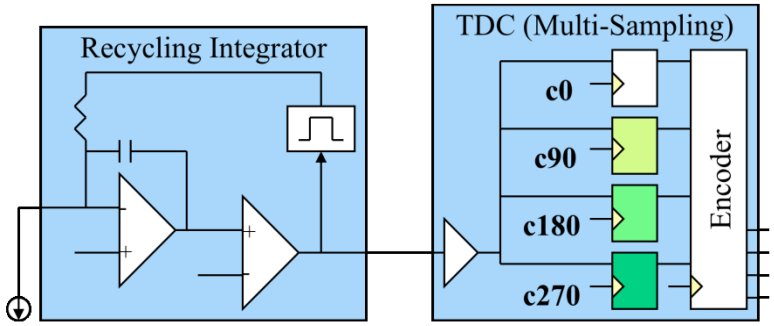


In typical digitization/readout schemes as shown in Fig., a counter is utilized to accumulate the number of pulses generated by the recycling integrator to digitize the total charge. In order to calculate current with reasonable resolution, a long period must be waited for each sample. For example, to achieve 7-bit resolution, the sampling period corresponds to 128 pulses when input current is at upper limit. This scheme provides a total dosage of the radiation over long period but is not fast enough for accelerator beam protection.



Typical digitization scheme with a counter.

In our new scheme, the same recycling integrator output is sent to an FPGA in which a time-to-digital converter (TDC) is implemented. The TDC is based on a multi-sampling scheme in which the input transition is sampled with four different phases of the system clock. With system clock rates of 250 MHz and four-phase sampling, a 1-ns time measurement resolution can be achieved.

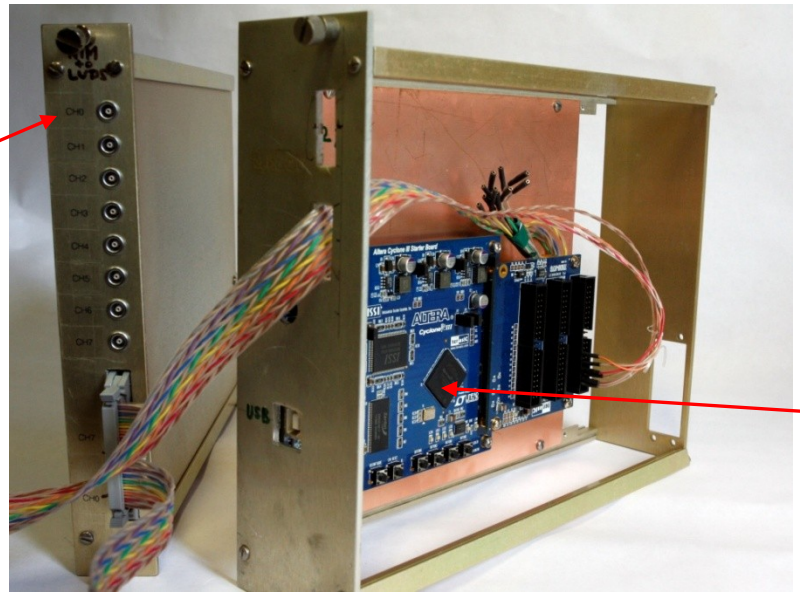


digitization scheme using an FPGA based TDC.

TDC Implemented with FPGA

- There are two popular schemes for FPGA TDC:
  - Multiple sampling based scheme: LSB: 0.6 to 1 ns.
  - Delay line based scheme: LSB: 40 to 100 ps.
- We are currently working on a variation of the delay line based TDC called Wave Union TDC. Colleagues with requirements of TOF level resolution (< 50 ps) are welcome to contact us.

pulse input to 8 Channel LVDS

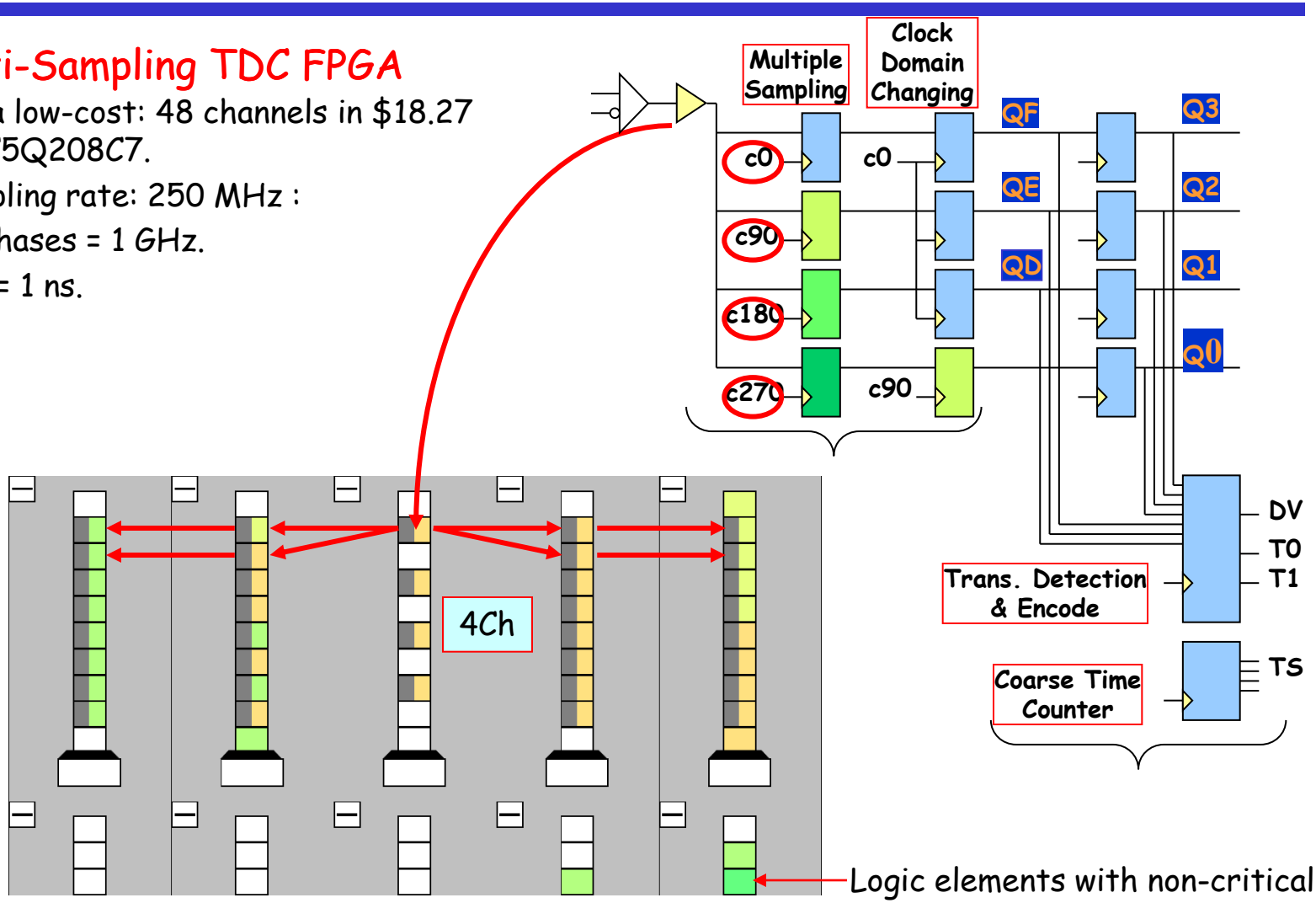


Cyclone III FPGA

Jan. 2011, Wu Jinyuan, Fermilab jywu168@fnal.gov

Multi-Sampling TDC FPGA

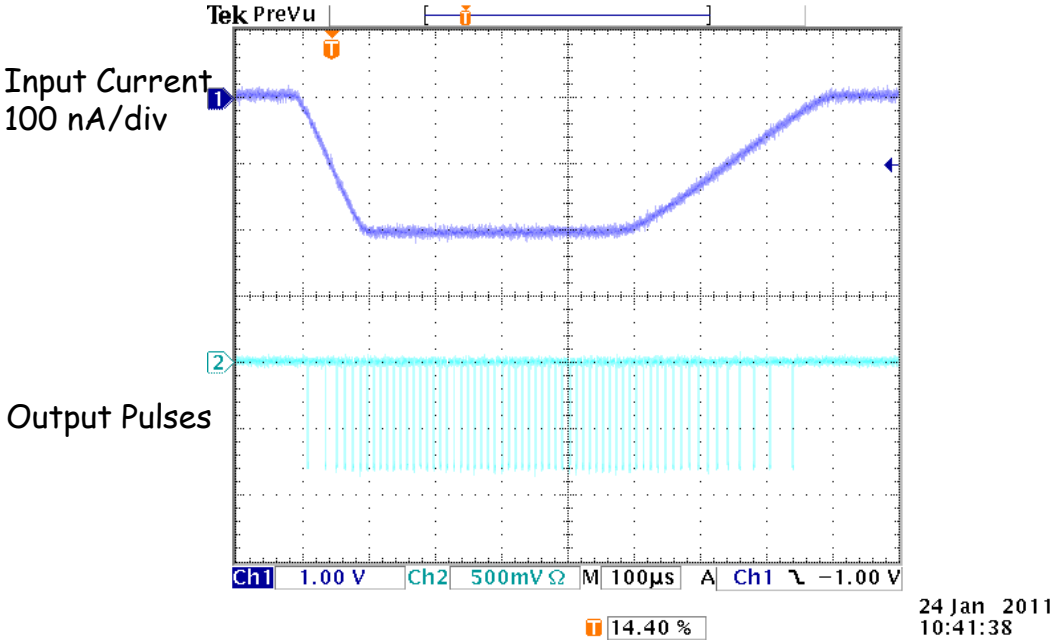
- Ultra low-cost: 48 channels in $18.27 EP2C5Q208C7.
- Sampling rate: 250 MHz : x4 phases = 1 GHz.
- LSB = 1 ns.



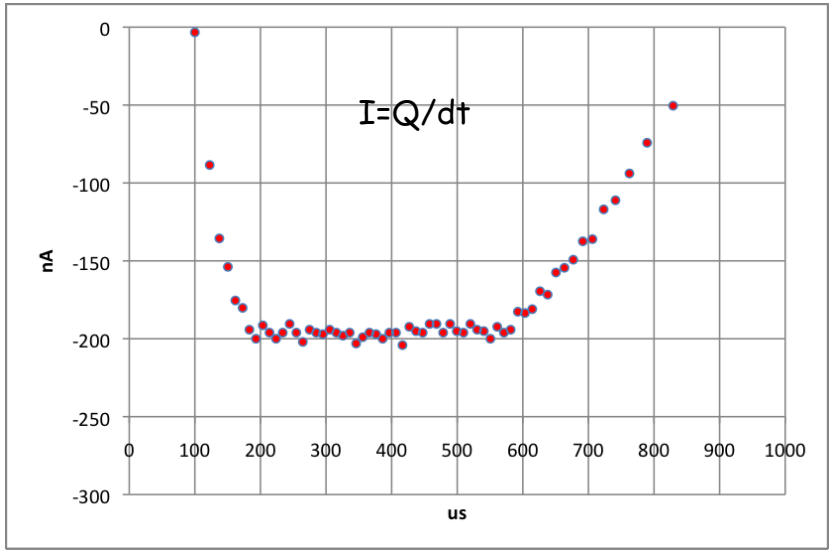
This picture represent a placement in Cyclone FPGA

Logic elements with non-critical timing are freely placed by the fitter of the compiler.

Bench-top measurements with FPGA-TDC



Input current and out-put pulses



FPGA-TDC data generated by measuring time between pulses

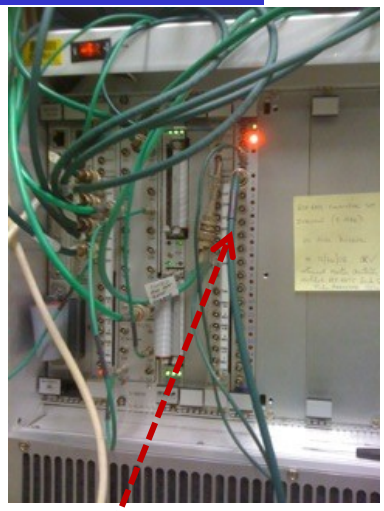
A Scheme using FPGA-based time-to-digital converter (TDC) to measure time intervals between pulses output from the recycling integrator is employed to ensure a fast beam loss response along with a current measurement resolution better than 10-bit.

Dark current measurements at Photo-injector and HTS

Counter/timer show 630 counts = 150 mR

Initial cold measurements were done at the horizontal test stand (HTS) shown here. A VME based counter timer board was used to count pulse in ACNET: Counter/timer showed counts corresponding to 150mR

Test cavity



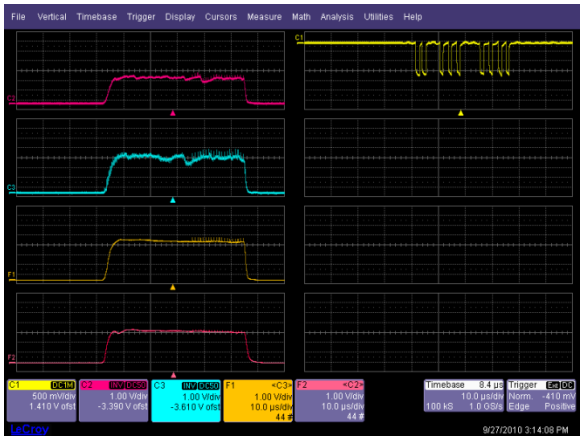
VME based counter/Timer board

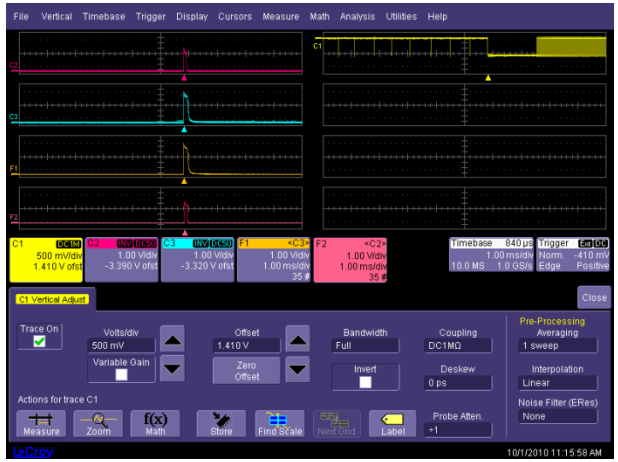
HTS installation

Test are now being done using the FPGA-TDC method which is faster with better resolution

Loss due to Dark current background at A0-photo-injector. Measured to be ~ 400 nA downstream of bend magnet

40 μs rf gate (dark current only no photo-electrons injected)





Design improvements and modifications

Final test are underway with FNAL designed FPGA-TDC at HTS

- We have increased the pressure from 1bar to 1.5bars to establish the best operating point for the device. The calibration "S" of the monitors is almost completely determined by the volume "V" of the enclosed gas and by the type of gas:

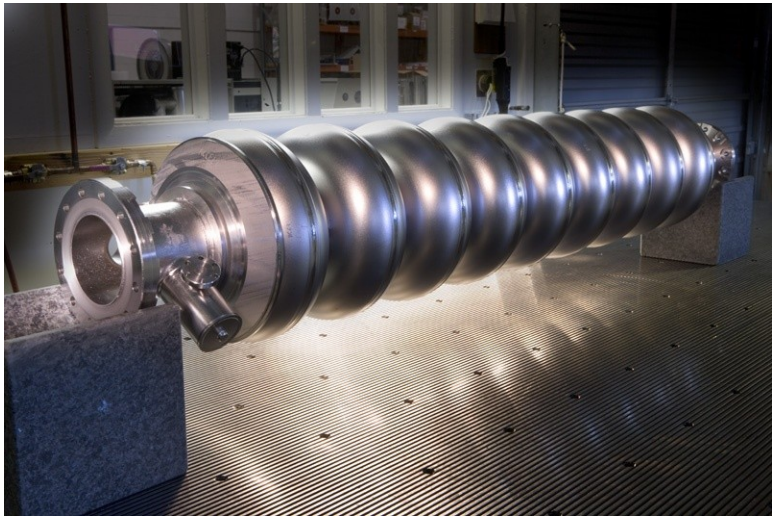
$$S \approx V \rho \, . \, e/E_{ion}$$ ("ρ" is gas density and E_{ion} is mean energy deposition to create electron-ion pairs)

- We had Bridgeport Instruments modify they FPGA code in the recycling integrator electronics box so that the leading edge of the discriminator can be seen at the NIM port output. This improves would improve the resolution of the TDC measurement between pulses.

- A mechanical scheme to easily mount the loss monitor in a cryomodule near the quads and BPMs is being done as shown in the following example.

SCRF Research at Fermilab

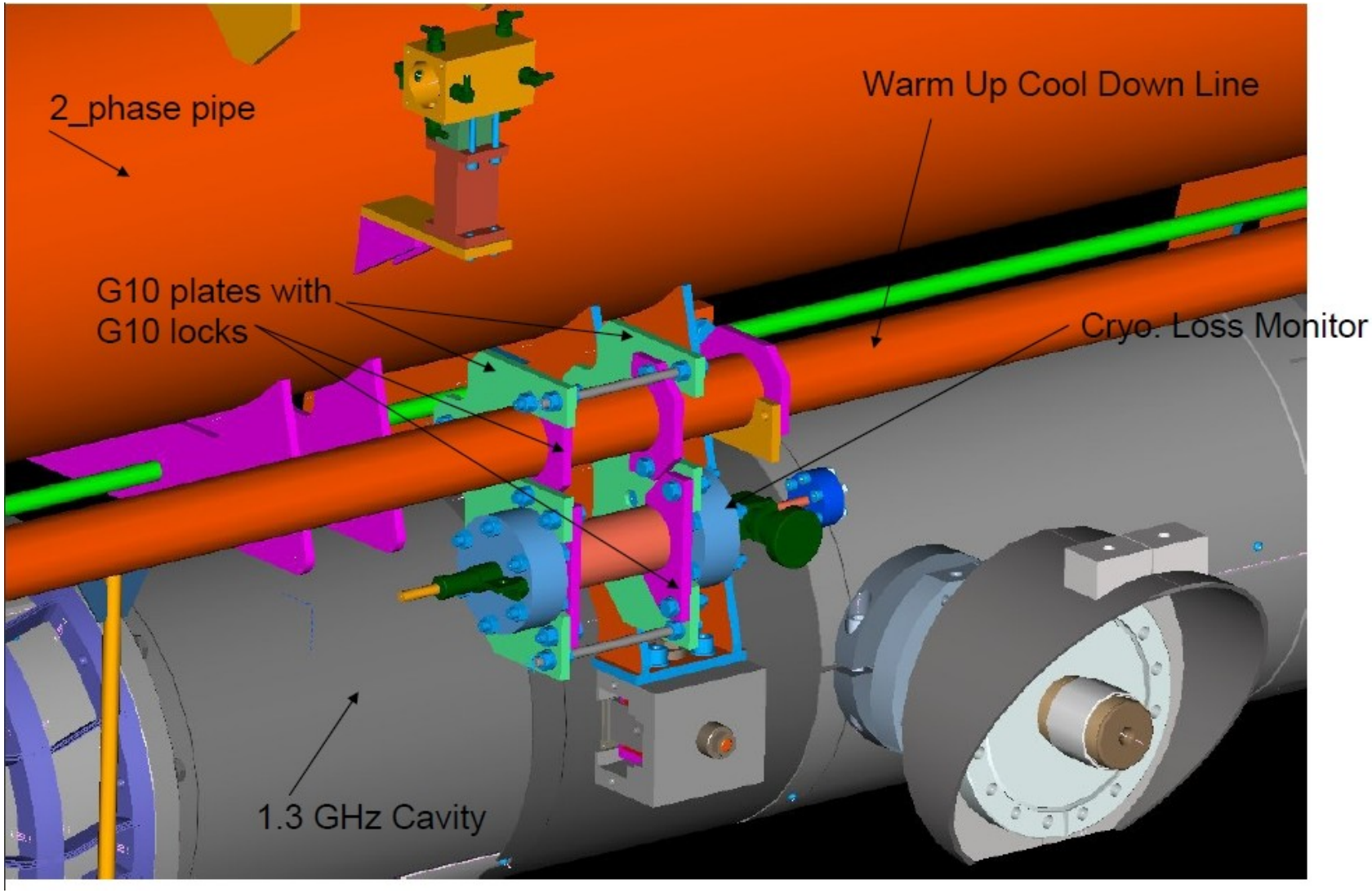
SRF=Superconducting Radio Frequency



1.3 GHz 9-Cell SRF Cavity

8 Cavity SRF Cryomodule

Cryogenic Loss Monitor proposed installation in CM2



Proposed installation in cryomodule II