ASKARYAN RADIO ARRAY

SOUTH POLE

Station electronics for the Askaryan Radio Array testbed and first prototype

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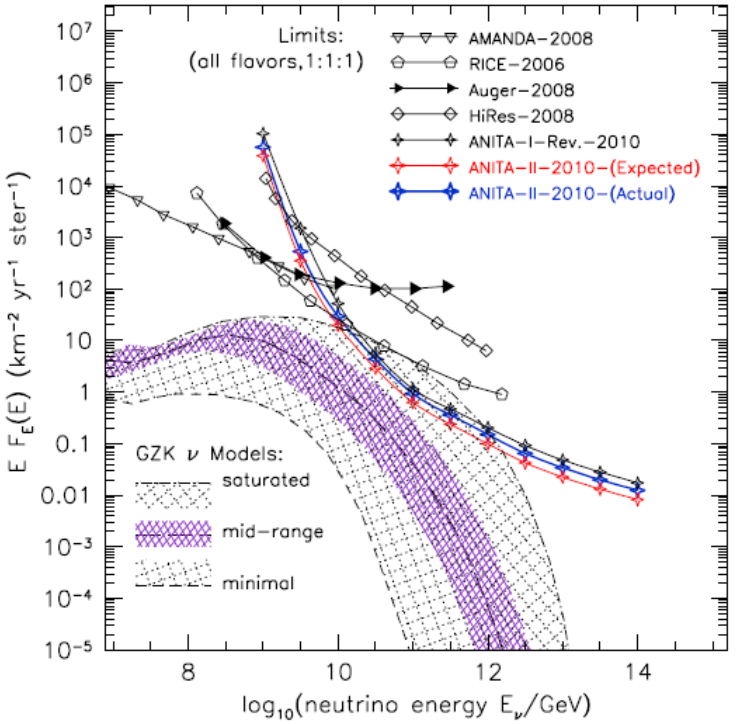
for the ARA Collaboration

GZK Neutrinos

- Above ~50 EeV, protons (and heavy nuclei) interact with photons from cosmic microwave background
  - Protons: photopion production via Δ resonance
  - Nuclei: photodisintegration (e.g. giant dipole res.)
- Both processes (which end the cosmic ray spectrum – "GZK cutoff") produce neutrinos
- We know ultrahigh energy cosmic rays (UHECRs) exist, we know the CMB exists…
  - Guaranteed flux of neutrinos
- But neutrinos are hard to detect…
  - We're close, just not quite there yet



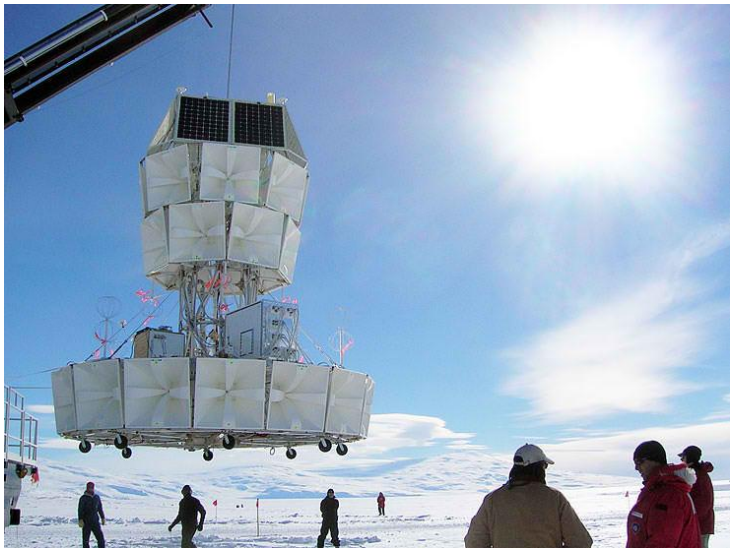
P.W. Gorham et al., 2010

Detecting GZK neutrinos

- Need a large amount of matter (greater than 1 Gton) due to low interaction cross-section
- Antarctic ice: prime candidate
  - Neutrinos interact in ice
  - Produce electromagnetic cascade
  - Coherent radio pulse produced due to Askaryan effect
    - Charge imbalance in electromagnetic cascade: relativistic dipole
  - Ice is transparent to radio: propagates very far
- One detector can view an extremely large volume
- Used by many previous experiments: ANITA, RICE
  - Bandwidth of interest is approx. 100 MHz -1 GHz
- No physics backgrounds: look for radio pulse from ice with no source

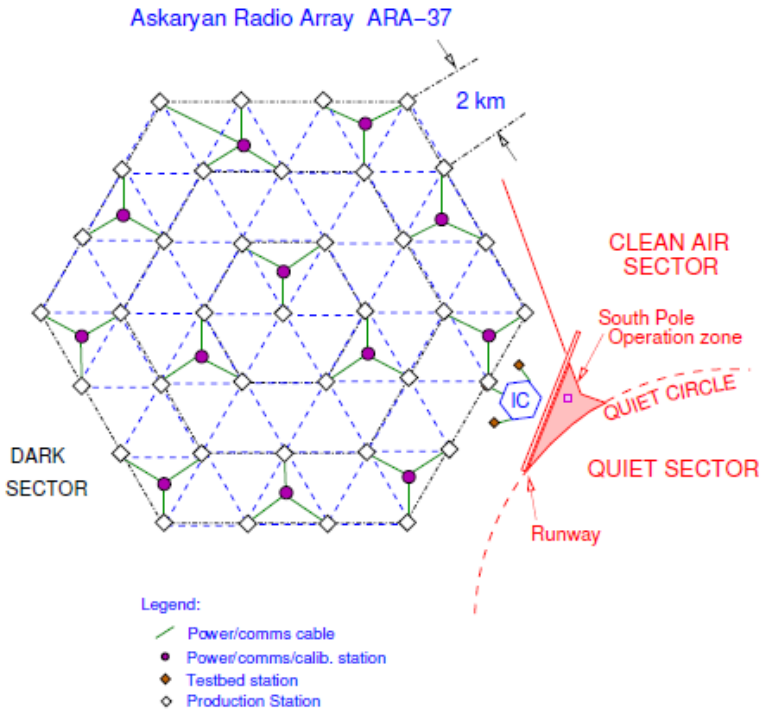
ANITA

- Balloon-borne experiment over Antarctica to search for GZK neutrinos
- 2 successful flights (third planned)
- No neutrinos seen, but detected 20+ UHECRs through geosynchrotron radiation in “background” box (H-pol)
- Very large detection volume (continent of Antarctica!), but very far away from source (10-100 km) so very high threshold
- Validates Antarctic ice neutrino method: it is possible to search for particle interactions in radio in Antarctica



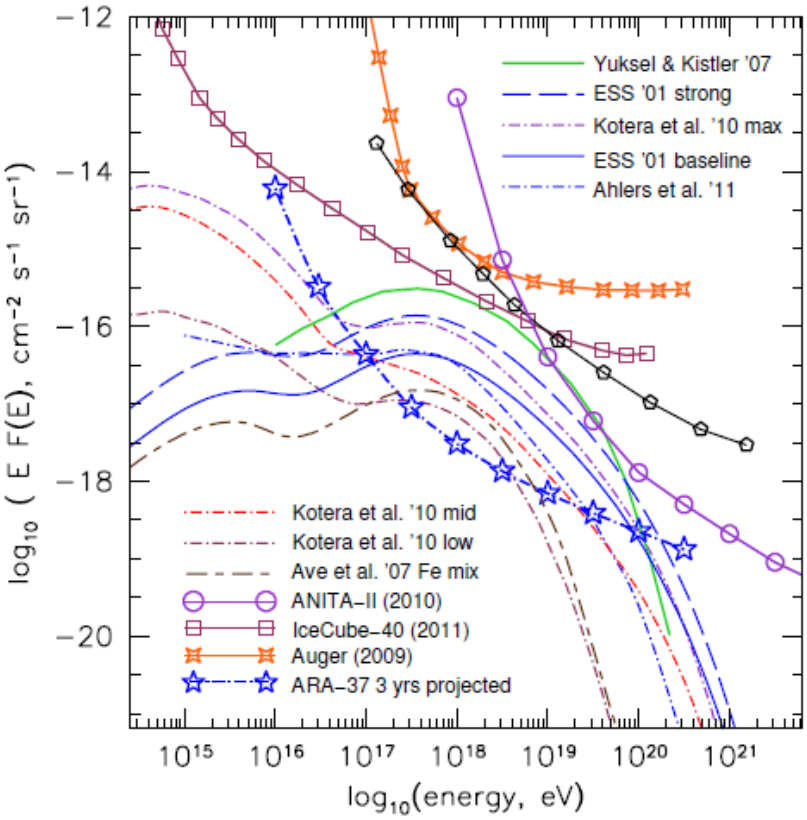
Askaryan Radio Array

- Designed to detect GZK-process neutrinos in quantity
- 200 km^2 array at South Pole
- Self-powered, 2 km interstation spacing
- Testbed station deployed in 2010-2011 polar season to determine radio environment



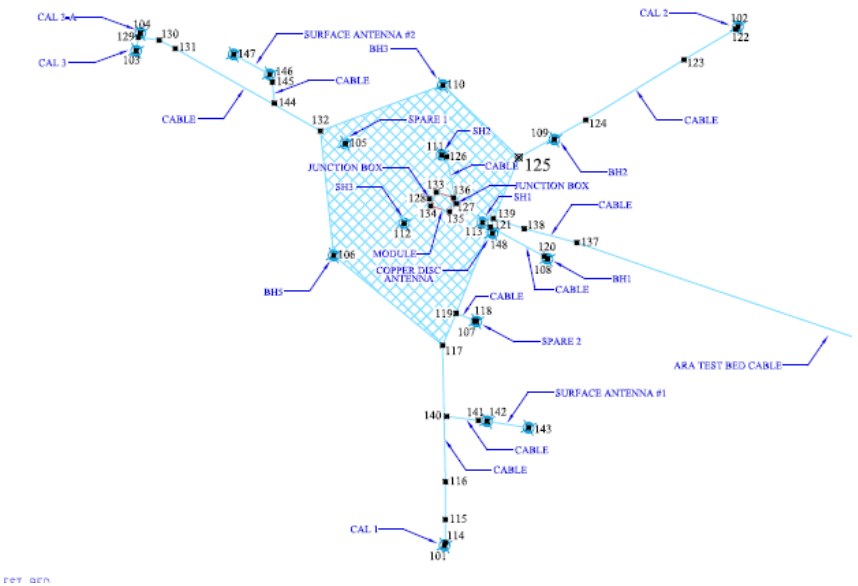
GZK neutrinos with ARA

- ARA-37 will extend the search for GZK neutrinos into and past the “mainline” models
  - Factor of 100 improvement or better depending on model
- Modular (station-based) design of ARA lends itself easily to extension to Tton scale detector

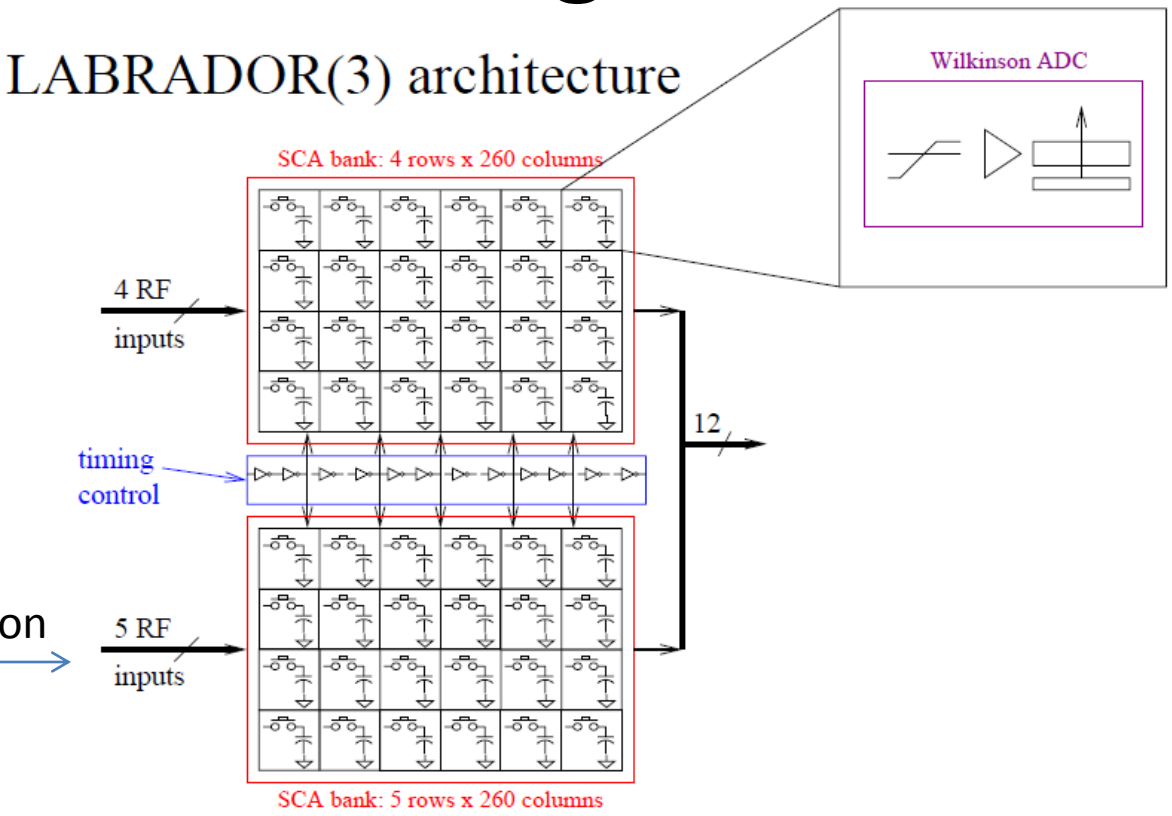


ARA Testbed

- Designed to determine if RF environment at South Pole suitable for ARA stations
- Similar to full ARA stations, but shallower depth
  - 4 primary boreholes with 2 antennas each (8 total) – 1 Vpol, 1 Hpol
  - 30 m depth, 5 m vertical spacing between antennas in borehole
  - 2 surface antennas, plus 4 shallow antennas, 2 additional Hpol boreholes for calibration
- Transit time of an RF signal across testbed: ~100 ns
  - Required compromises with ANITA technology



LAB3 digitizer

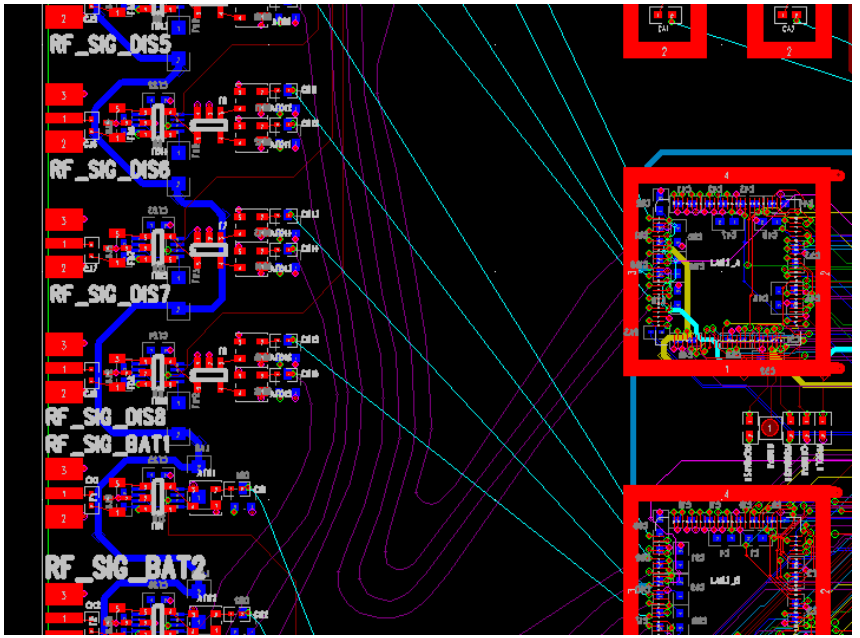


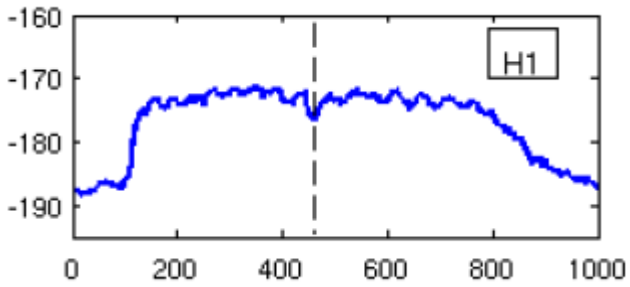
One used for reference clock for synchronization

- Custom low-power RF sampling ASIC from UH used in ANITA
- 260 samples total: for 1 GHz signal, at Nyquist sampling (2 GSa/s), this is 130 ns
- Not long enough!
- Also is a single buffered design: when signal is being read out, system is dead
- ANITA solved this by brute-force: include 4 separate LAB3 ASICs

Compromise: interleaved sampling

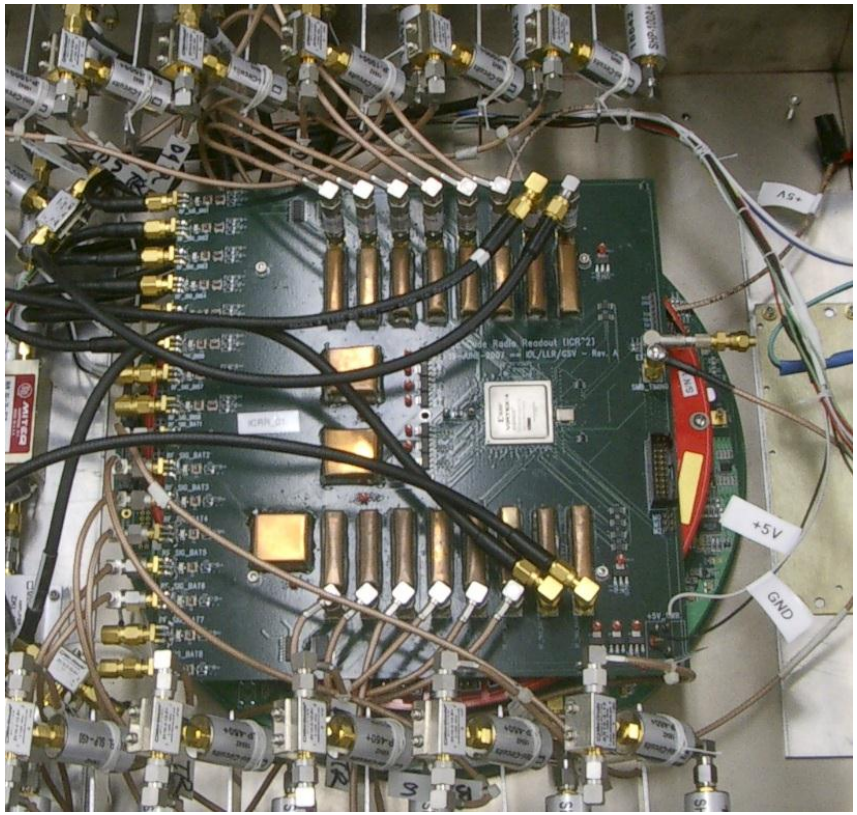
- Split RF inputs
- Delay one side by 500 ps onboard
- Digitize both sides
  - Effectively get 520 sample length (260 ns)
- Reconstitute signal afterwards
- Requires very good calibration!





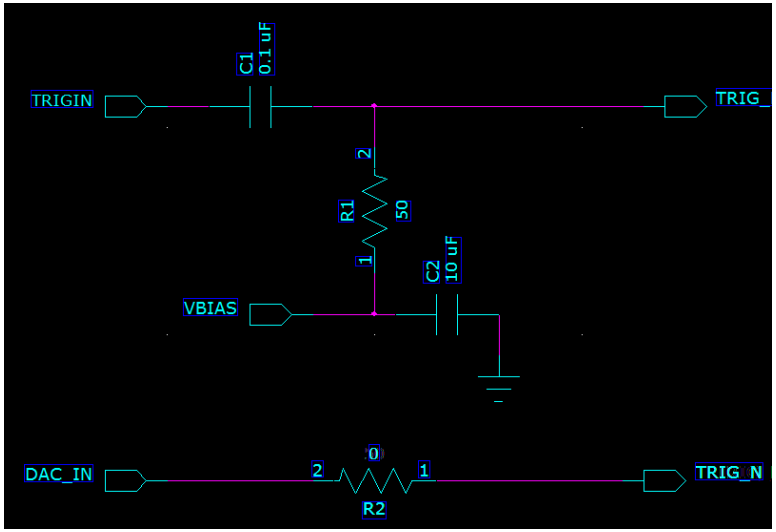
Ice Cube Radio Readout (ICRR)

- 3 LAB3 ASICs: 24 RF input channels
  - 8 interleaved (2 GSa/s)
  - 8 non-interleaved (1 GSa/s)
    - Shallow & surface antennas (low-freq)
- 16 RF triggering channels
- Virtex-4 FPGA for readout/control
- 28 DAC outputs
  - 24 trigger thresholds, 3 for maintaining LAB3 sampling rate, 1 spare
- 8 temperature sensors
- 2 successive approx. ADCs for measuring RF power



Triggering scheme

- 8 channels used triggering scheme used in ANITA
  - RF signal through square-law detector (‘tunnel diode’)
  - Amplified, filtered, biased to mid-range LVDS (~1.2V) and sent to positive input of FPGA differential pair
  - DAC output sent to other input
  - Effectively uses diff. input as fast comparator
- 8 channels attempted to trigger directly on RF signal
  - Split and sent into two separate diff. pairs of FPGA (opposite pol.)
  - DAC outputs sent to other polarity
  - Not nearly as effective as tunnel-diode scheme in practice



Data readout and acquisition

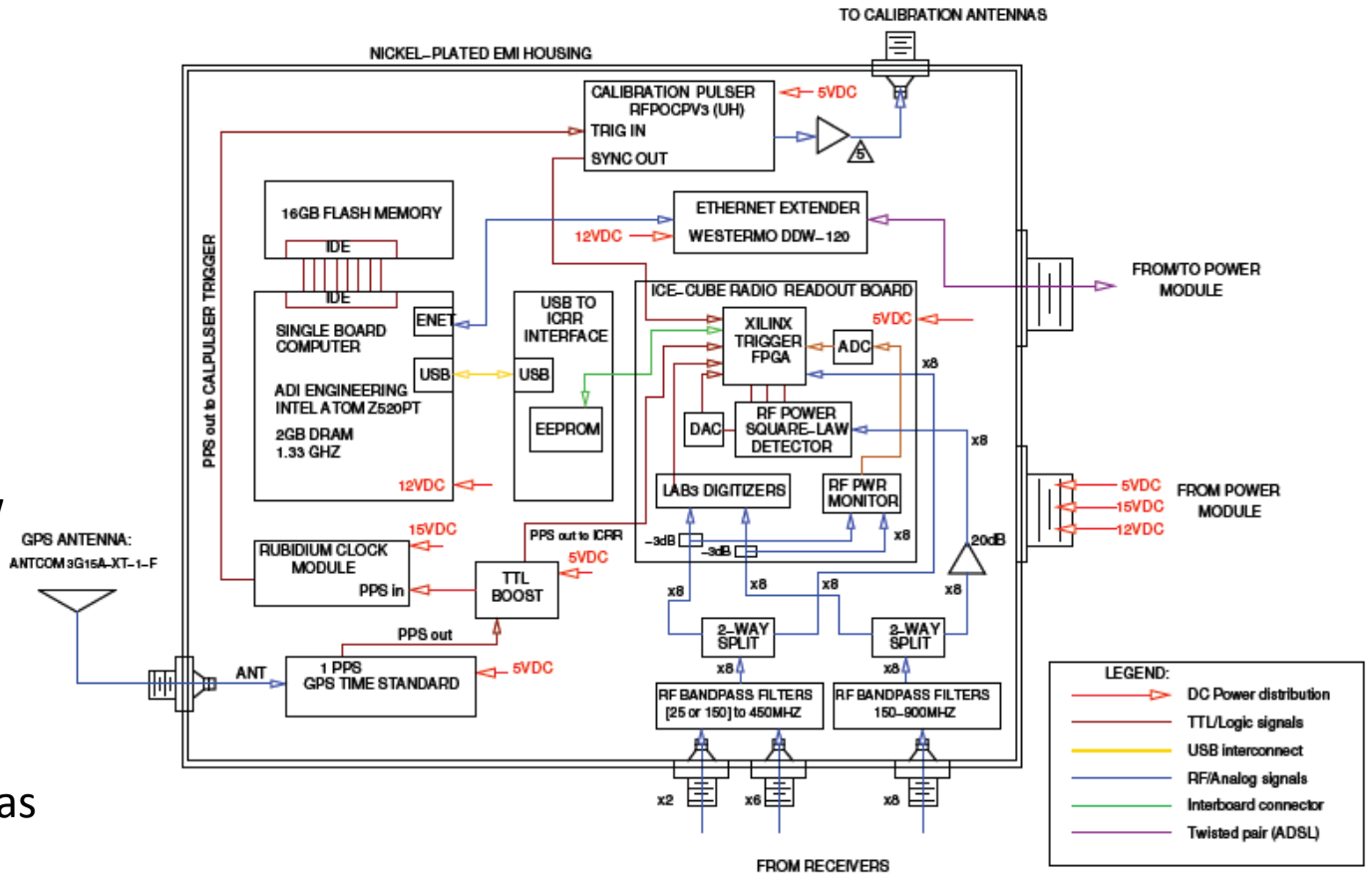
- Initially attempted to use existing IceCube infrastructure ("digital optical module (DOM) board"), adapted through a separate board used in AURA project ("TRACR")
  - Advantages: DAQ, communications already exist
  - Disadvantages: old, slow
- Also had a USB interface (using Cypress FX2LP USB bridge) for debugging
- However: modern SBCs are very fast, low power, thanks to cellphones
- Commercial low-power long distance communications exists, thanks to DSL
  - Lesson learned: "believe in the market"
- Abandoned DOM+TRACR+ICRR in favor of much simpler design
  - How much simpler? Replaced entire previous system (with 2 custom boards) with commodity components in ~2 months

Electronics system block diagram

Communications:
Westermo ethernet extender: ~3 W

DAQ computer:
ADI Engineering
Cinnamon Bay SBC A520
1.33 GHz Atom, ~5W total

Readout via USB because of existing interface: SBC also has PCI-Express link available

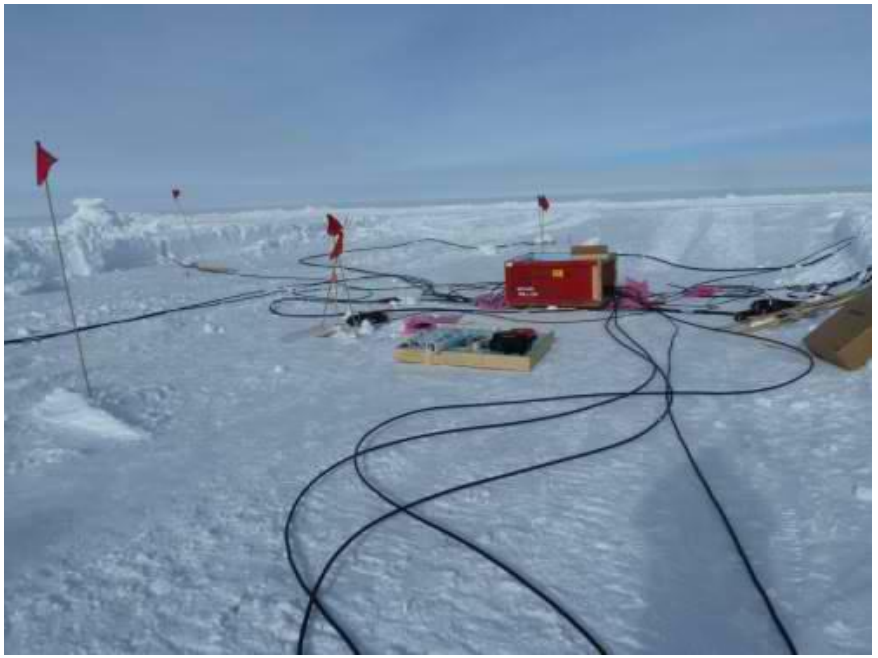


DAQ readout

- USB interface based on USBP project firmware (http://www.fpgaz.com/wiki/doku.php?id=fpgaz:usbp:fw)
- Adapts EZ-USB FX2LP slave FIFO interface to an OpenCores WISHBONE bus master and a simple streaming FIFO interface
- Original plan was control, housekeeping through WISHBONE bus, event data through FIFO interface
- Time constraints forced everything through WISHBONE bus
- Slowed readout down considerably (~25 Hz throughput) due to unbuffered interface and lack of FPGA-to-PC (i.e. interrupts) communication – software needed to poll for new events
- Single-buffered design means ~few Hz for low deadtime

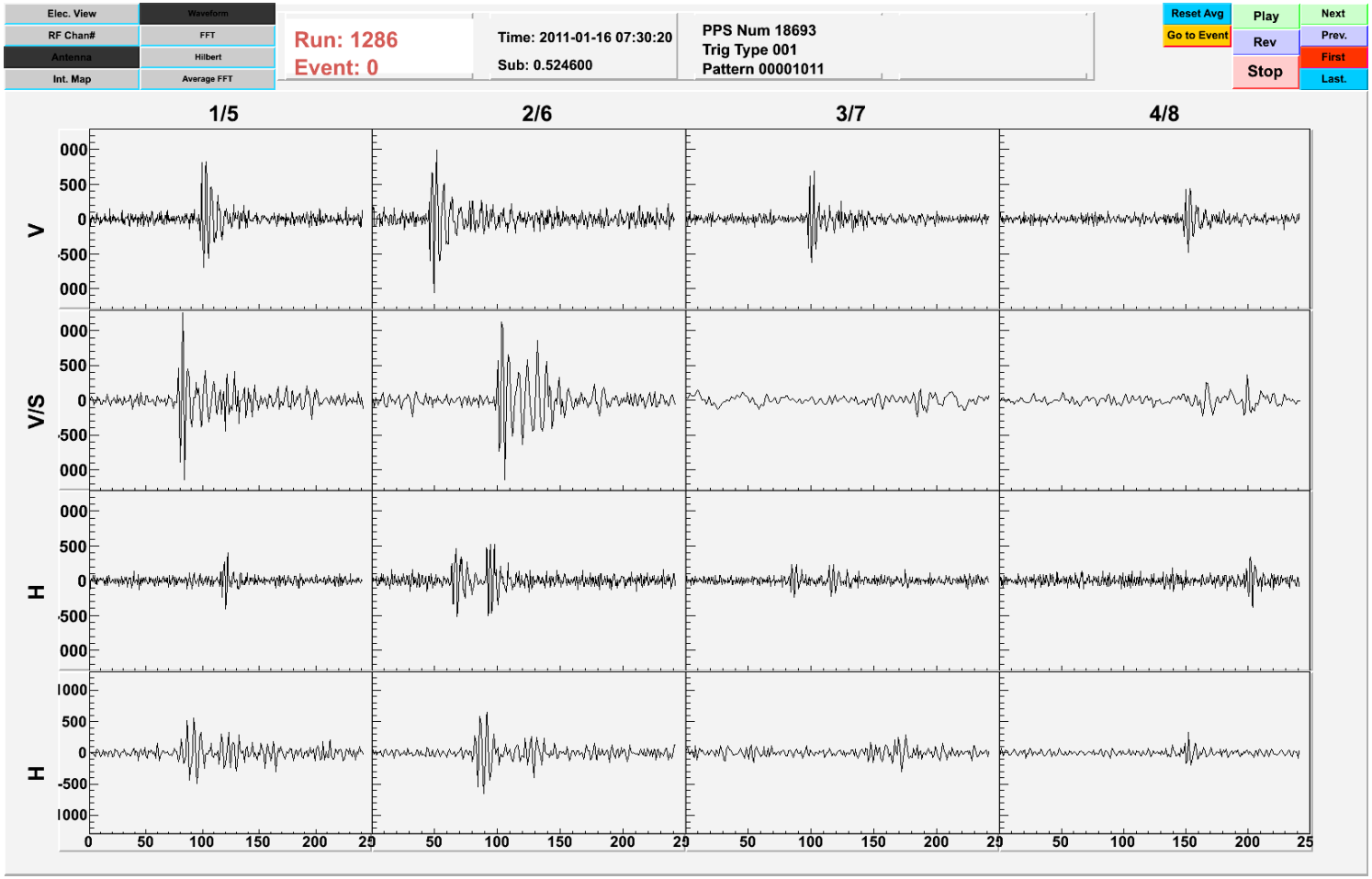
Deployment 2010-2011

Testbed electronics plus DC-DC converter box



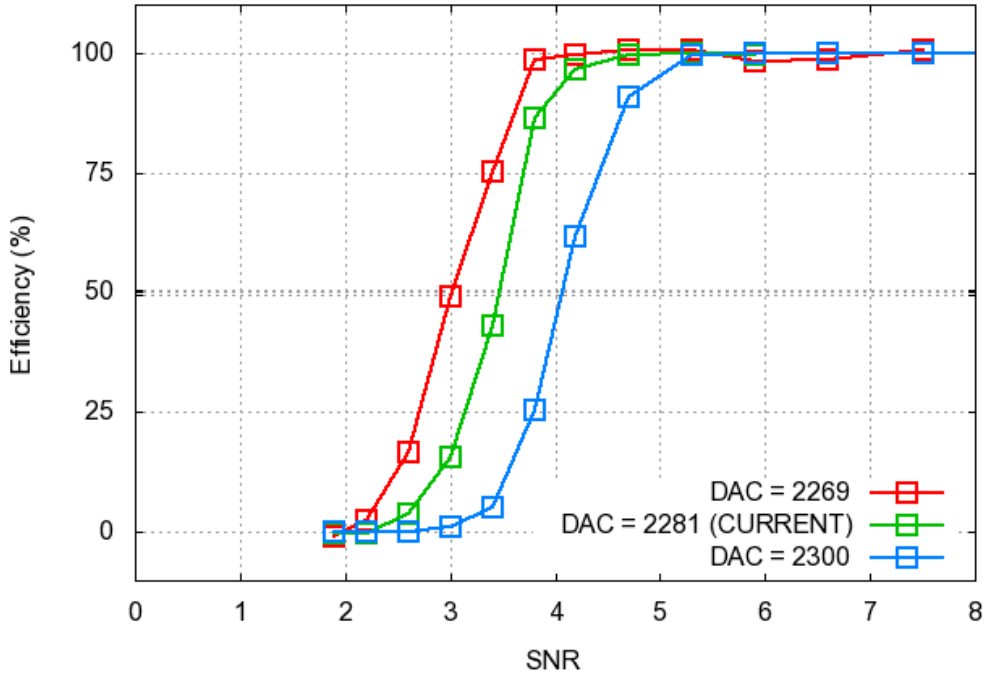
Electronics at deployment site

Example calibration pulser event



Trigger efficiency

- Trigger occurs when any 3 of 8 primary antennas trigger
- Driven by the requirement for ~Hz readout rate
- Still has a 50% trigger point at an SNR of ~3.5

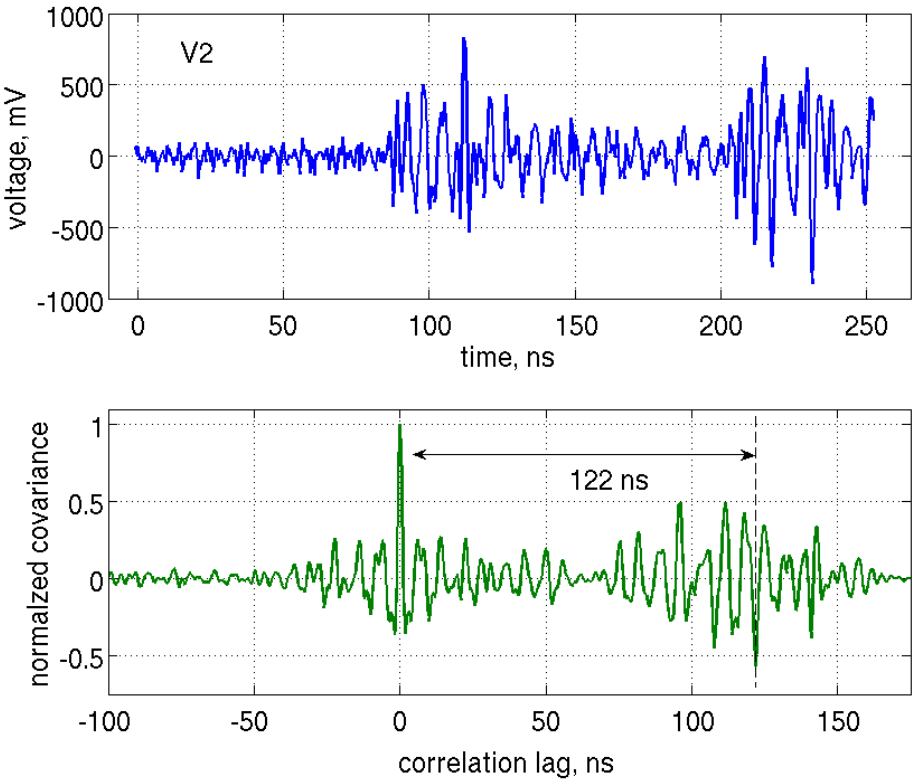


Simple attenuation length measurement

- Deep pulser (IceCube depths) installed to attempt to view signals at km-scale distance
- Most saturate the testbed (!)
- For the few that do not, a simple estimate of the attenuation length gives (for 150-350 MHz)

$$\langle L_\alpha \rangle = 760^{+60}_{-40}\ \mathrm{m}$$

- In addition, surface reflection observed, inverted, at expected time

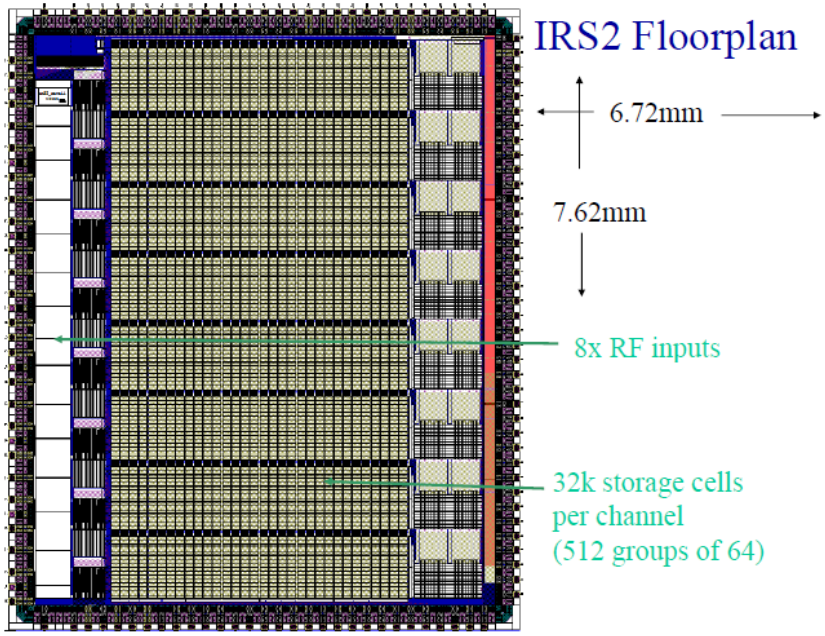


Required improvements from testbed to full ARA station

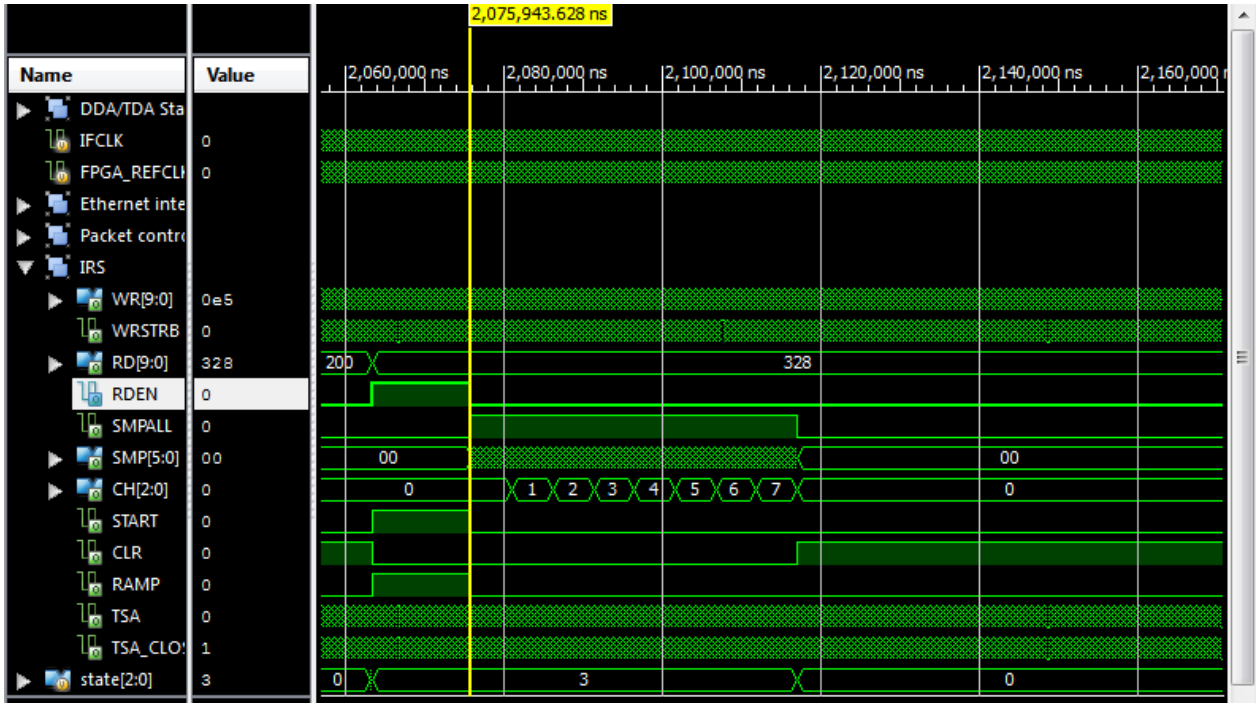
- Higher sampling speed
  - 4x highest frequency of interest (2x Nyquist)
  - Antennas fall off around 800 MHz, so 3.2 GSa/s
  - Requires a new digitizer: deeper buffer required for same length of time!
- Faster readout speed
  - Slow readout primarily due to lack of buffering, also poor interface implementation
  - Cinnamon Bay SBC has PCIe link and new Spartan-6 FPGAs from Xilinx have built in PCIe link
    - instant Gbit/s interface

Ice Radio Sampler (2)

- Based on Buffered LABRADOR (BLAB) architecture from UH
- 8 channel, 32768 samples, up to ~4 GSa/s, 3 dB analog bandwidth of 1 GHz
- Contains 2 64-capacitor sampling cell array and 512 64-sample storage blocks
- Analog samples transferred to storage array from one array while the other is sampling
- Blocks are random-access, so readout can occur while still sampling



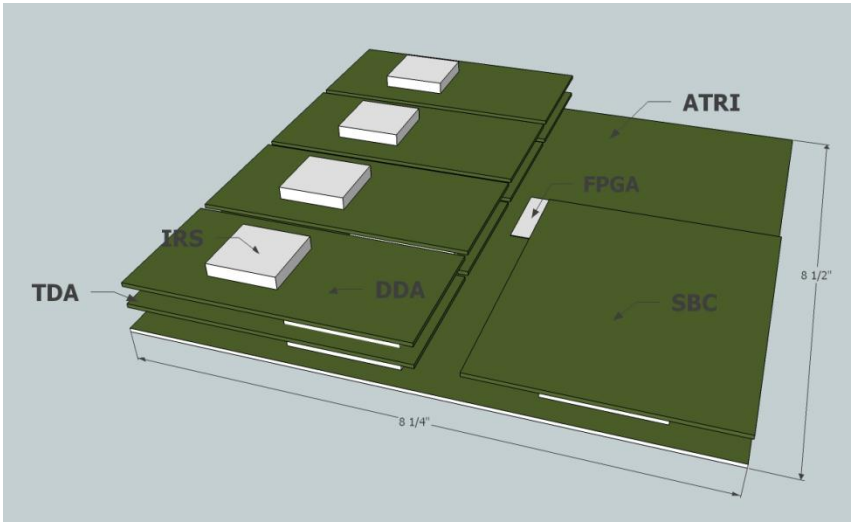
IRS control



- 512 blocks separated into 384 “active” and 128 “free” or “locked” blocks
- 384 active blocks maintain 7.68 μs history in IRS
  - Some possibility for multi-station coincidence
- 128 “free” block queue provides blocks for active buffer when readout occurs
  - 20 block (400 ns) readout: 6 deep buffer
- Sampling speed controlled by a DAC voltage, servoed against a time-to-digital measurement of the delay through the IRS delay line
  - Implemented using delay line in the Xilinx DCM: only one needed for all 4 channels, no calibration needed
  - ~40 ps TDC resolution

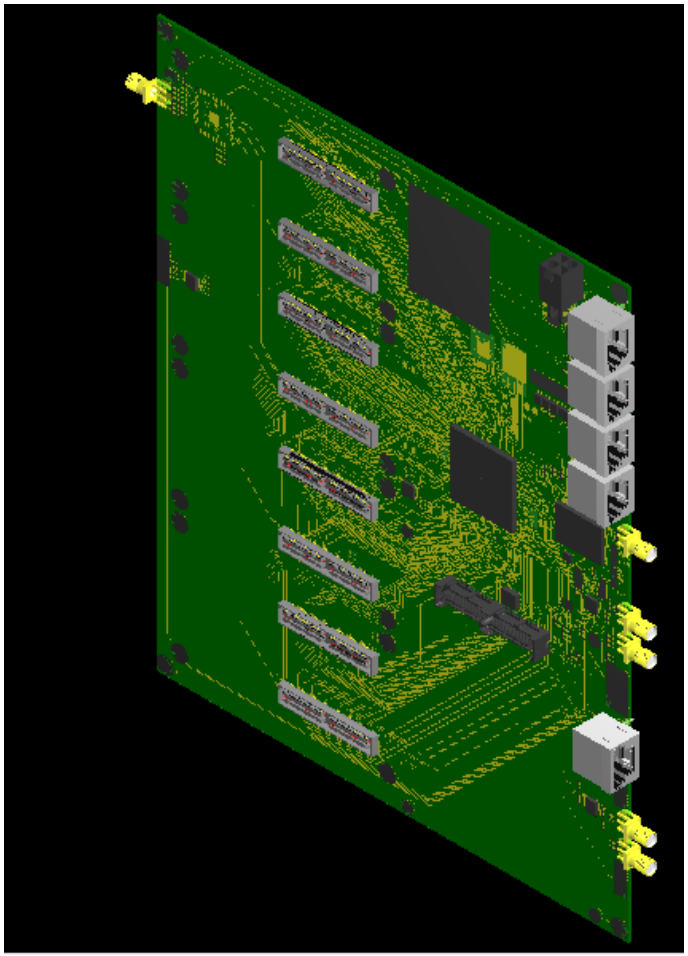
ARA Station Electronics

- Split electronics into 3 boards
  - ATRI: FPGA, other boards
  - DDA: IRS2 digitizer
  - TDA: triggering chain
- Daughterboard bus: Stacking bus made of back-to-back Samtec QSE/QTE connectors
- Expandable: many pins left reserved on bus and routed to FPGA

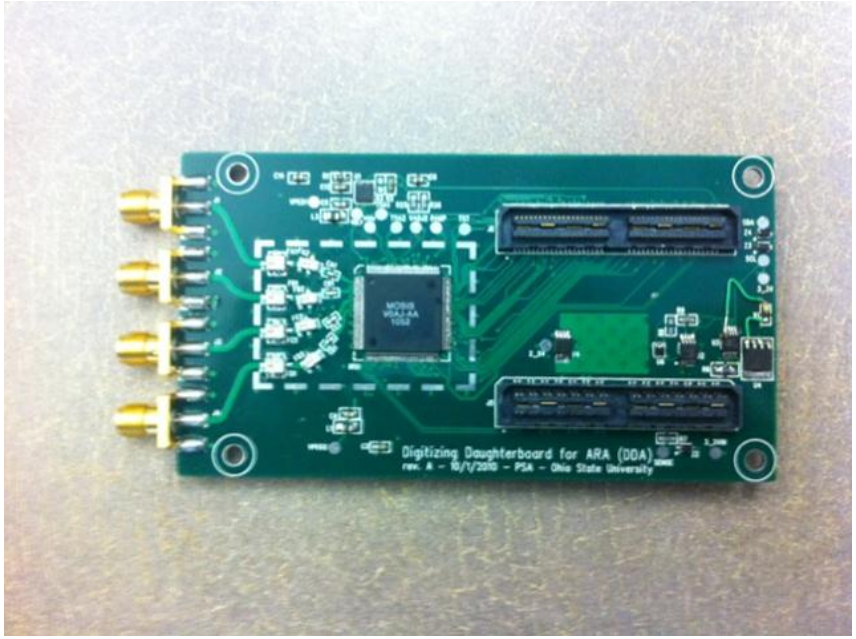


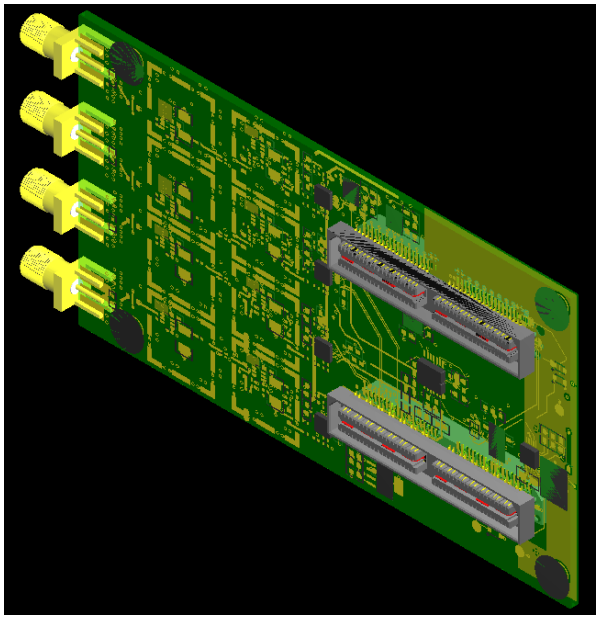
ATRI

- 4 daughterboard stacks, SBC, GPS, and external device controls (via I^2C)
- Spartan-6 LX150T FPGA
  - PCIe link to SBC
- Cypress EZ-USB FX2LP USB bridge
  - Provides redundant data path + FPGA programming interface + I^2C device control
- Reference clock multiplication and distribution
  - Si5367 ultralow jitter programmable clock multiplier
- Voltage+current monitoring, plus power control (for FPGA+daughterboards, through FX2LP)
- Optional onboard chip-scale rubidium clock (not available this year)



Daughterboards





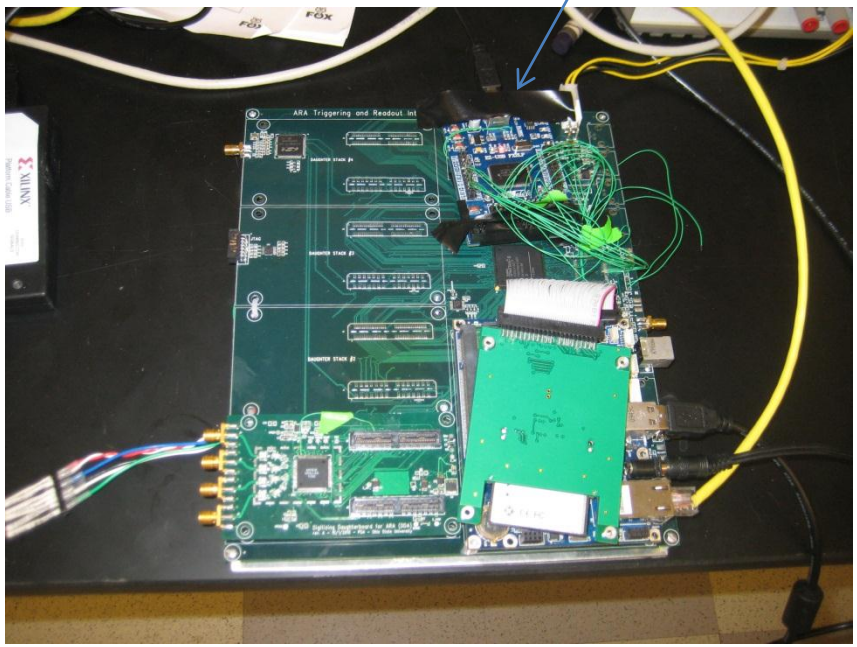
DDA:
IRS2 sampling ASIC, 4 RF inputs, 1 reference clock input, 2 test inputs, 1 unused
Voltage/current/temperature monitoring, board identification, and power control

TDA:
4 triggering channels, using modified ANITA design

Current prototypes

- ATRI, DDA prototypes fabricated and tested
- Major problems fixed and final versions (hopefully) currently in production
- RF input path on DDA needed to be tuned to compensate for SMA connector
  - 25% signal loss even at ~200 MHz!
  - Voiding planes under connector improved situation dramatically

("always double check part footprints")



Conclusion

- ARA testbed detector currently operational at South Pole and taking data
  - Not a great neutrino detector: too shallow
- Full ARA station electronics, based on new deep, buffered RF sampling ASIC currently in production to be deployed this year