Front End Readout Electronics of the MicroBooNE Experiment

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On behalf of the MicroBooNE FEE Working Group
June 9th, 2011
Outline

- **Introduction**
  - MicroBooNE Experiment
  - Liquid Argon Time Projection Chamber (LAr TPC)
  - LAr TPC Signal Properties

- **MicroBooNE Front End Readout Electronics**
  - Readout Electronics System Architecture
  - Cryogenic Electronics
  - Front End Readout Electronics Development
  - Front End Electronics (FEE) Test Stand at BNL

- **Summary**
MicroBooNE (Booster Neutrino Experiment)

- A 150 ton (~63 ton fiducial) volume LAr TPC on the BNB/NuMI at FNAL
  - Collaboration formed in 2007
  - 10 univ+labs/50 phys.+eng.
  - Successful DOE CD-1 review in Mar. 2010
  - Prepare for CD-2 review in 2nd half of 2011

- http://www-microboone.fnal.gov

- MicroBooNE physics
  - Low energy excess events observed by MiniBooNE
  - Low energy neutrino cross section measurements

- MicroBooNE serves as the necessary next step in a phased program towards massive LAr TPC detectors
  - Test of purity in un-evacuated, fully instrumented vessel
  - Continued development of purification and filtration systems
  - Cold electronics development

- Evacuable, passive (foam) insulation vessel

- TPC: 2.5 x 2.3 x 10.4m long
  - 2.5m drift @ 500V/cm

- 3 readout planes
  - 3mm wire pitch
  - 2 induction planes (U,V at ±60° from vertical)
  - 1 collection plane (vertical wires, 2.5m long)

- Readout based on cryogenic analog front end
  - 0.18µm CMOS technology
  - 8,256 channel
  - Warm feed-through
MicroBooNE Experiment

On-axis BNB
- 8 GeV protons on Be target
- Focusing horn: $\pi^+, K^+$
- Decay channel 50m
- 450m dirt
- 2-3x10$^{20}$ POT/year
- 3-2 years running (6x10$^{20}$ POT)

Off-axis NUMI
- 110 mrad off NUMI target
- 4x10$^{20}$ POT/year

Proposed MicroBooNE site
How Does a LAr TPC Work?

- Why use LAr TPC
  - High spatial and energy resolution
  - Particle identification \((e/\gamma/\pi^0)\) by \(dE/dx\) measurements \((e/\gamma\) separation \(>90\%\))
  - Detailed 3D event reconstruction – 3 Mega-voxel for MicroBooNE detector
  - High detection efficiency and excellent background rejection
  - Scalable to multi-kiloton size

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![Energy loss in the first 24mm of track: 250 MeV electrons vs. 250 MeV gamma rays](image)

- 250 MeV Particles, first 24 mm
  - \(e\)
  - \(\gamma\) \((e^+e^-)\)

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![Particle ID](image)

- 3D event reconstruction – 3 Mega-voxel for MicroBooNE detector

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![Heavily ionizing particle](image)

- Proton
  - Track length=25 cm
  - Kin. Energy=194 MeV (in agreement with expectations [GEANT-Nist tables])

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![m.i.p. particle](image)

- Muon
  - \(dE/dx\) along the track \~ 2 MeV/cm
Charge Signal Formation

- Induction by and Collection of electrons on wires (by a track at 0 degrees and perpendicular to the wire planes)

- Induction (small, bipolar)
- Collection (large, unipolar)

Drift Distance (cm)

Time (µs)

Current Out of Wire
MicroBooNE Readout Electronics System

Single Vessel Cryostat with 8-10% Ullage
Foam Insulation

8256 TPC channels
LAr

30 PMT channels
GAr

CMOS Analog Front End ASIC in LAr @ ~90K
Decoupling and Wire Bias

"Cold"-Twisted Pair Cables (~2-5 m)

Warm Flange 2x8 + 2x7 rows pin carriers 32 readout channels/row

Intermediate Amplifier Line Driver

Faraday Cage Extension

TPC Readout Board
Digitizing Section
Data Handling Section
On Board Memory

FEM (Front End Module)
FPGA
D-SER
Optical Transmitter
Transmit Module
Optical Link
To DAQ PC

DAQ in Detector Hall

Intermediate Amplifier Line Driver

"Warm"-Shielded Twisted Pair Cables (~10-20 m)

Warm Flange 2x8 + 2x7 rows pin carriers 32 readout channels/row

Shaper

PMT Readout Board
Digitizing Section
Data Handling Section
On Board Memory

FEM (Front End Module)
FPGA
D-SER
Optical Transmitter
Transmit Module
Optical Link
To DAQ PC

Flange

PMT

Decoupling and Wire Bias

Beam Gate

PMT Readout Board
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Data Handling Section
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Optical Link
Covered in this talk

See C-Y Chi's TIPP2011 poster for more details in Back End Readout Electronics and DAQ system.
Why Use Cryogenic Electronics

SNR computed for
\( C_w = 20 \text{ pF/m} \)
\( C_C = 100 \text{ pF/m} \)

Signal for
(1/e drift)
3x3 5x5

10^4e

Signal collection (induction) electrode
From signal electrode to preamp
§ JFET based preamplifier designed for MicroBooNE
  • Bulk mobility and transconductance increase as temperature decreases, carrier freeze out causes ENC increasing when temperature lower than ~100K

§ CMOS technology – preliminary test result of existing ASIC in 0.25 µm (not designed for LAr)
  • CMOS in LAr has less than half the noise as that at room temperature, higher mobility and higher transconductance/current ratio

§ MicroBooNE has adopted the cryogenic CMOS analog front end ASIC developed for LBNE LAr TPC program

See Craig Thorn’s TIPP2011 talk for more details of cryogenic electronics development
MicroBooNE Cryogenic Electronics

- **CMOS Analog Front End ASIC**
  - 16 channels per chip
  - Charge amplifier, high-order filter
  - Adjustable gain: 4.7, 7.8, 14, 25 mV/fC (55, 100, 180, 300 fC)
  - Adjustable filter time constant (peaking time): 0.5, 1, 2, 3 µs
  - Selectable collection/non-collection mode (baseline)
  - Selectable dc/ac (100 µs) coupling
  - Rail-to-rail analog signal processing
  - Band-gap referenced biasing
  - Temperature sensor (~ 3mV/°C)
  - 136 registers with digital interface
  - 5.5 mW/channel (input MOSFET 3.6 mW)
  - ~ 15,000 MOSFETs
  - Designed for long cryo-lifetime
  - Technology CMOS 0.18 µm, 1.8 V, 6M, MIM, SBRES

- **Cold Mother Board**
  - House front end ASIC
  - Rogers 4000 series base material
  - Provide detector signal interconnections
  - Provide ASIC control and monitoring signals, calibration network
  - Provide bias voltage distribution for wire planes
  - Horizontal version
    - 96 “Y” channels, 48 “U” channels and 48 “V” channels
  - Vertical version
    - 96 “U” or “V” channels
MicroBooNE Warm Interface Electronics

- **Intermediate Amplifier**
  - 32 channels per board
  - Differential driver to improve noise immunity
  - Provide an appropriate gain (~12 dB) to detector signals to make it suitable for long distance (10 – 20 m) transmission
  - Installed on the top of signal feed-through and housed by a Faraday cage to ensure good shielding and better noise performance

- **Service Board**
  - Provide low voltage (+1.8 V), control and monitoring to front end ASICs
  - Provide low voltage (+3.3 V, -3.3 V) filtering and distribution to intermediate amplifiers
  - Provide calibration pulse driver to front ASIC which has build in switch to turn on/off pulse injection to individual channels
  - Installed on the top of signal feed-through and housed by a Faraday cage

- **ASIC Configuration Board**
  - Provide ASIC configuration signals driver from commercial off-the-shelf digital I/O board
  - Provide interface between ASICs and PC
**MicroBooNE Receiver and ADC Board**

- **Receiver and ADC Board**
  - 64 channels per board
  - Receive detector signals and drive to ADC input
  - Each detector signal is digitized individually and continuously
  - 12-bit ADC AD9222 from Analog Devices
  - 8 channels per ADC
  - Mating with Nevis FEM (Front End Module) to form a TPC Readout Board
  - First TPC readout board assembly, mechanical integration in custom designed crate has been verified successfully
Signal Feed-through, Cable Assembly and PS

- **Signal Feed-through**
  - ATLAS LAr Calorimeter style feed-through, technology exists
  - Pin carriers welded on flange: 100% hermetical
  - 2x8 + 2x7 rows pin carriers: high signal density (1920 pins)
  - Custom designed bias voltage feed-through
  - Faraday box is built and mounted on feed-through

- **Cable Assemblies**
  - Cold cable: Teflon FEP insulation, 100 Ω ± 10%, AWG 26 solid core sliver plated
  - Cold cable terminate assembly: commercial connector and jackscrews with custom designed shells to provide reliable assembly and easy handling
  - Warm cable assembly is commercial off-the-shelf SCSI-3 Ultra LVD/SE MD68M/M cable
  - Warm cable connector: Micro-Density 68-pin, 34 pairs
  - Warm cable has aluminum-foil shielding with 10% overlap to provide Faraday cage extension

- **Power Supplies**
  - Front end power supplies: commercial power supply will be used to power front end electronics
  - Bias voltage power supplies: commercial power supply will be used to bias detector wire planes
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MicroBooNE FEE Test Stand

FEE Test Stand Warm Test Setup

FEE Test Stand Cold Test Setup
FEE Test Stand Warm Test

- Full front end readout electronics chain
  - Analog front end ASICs
  - Cold mother board
  - Cold cable
  - Signal feed-through assembly with Faraday cage
  - Intermediate amplifier
  - Service board
  - Calibration board
  - Warm cable
  - Receiver/ADC board
  - Data is acquired to PC through an interface board, FPGA board and Gigabit Ethernet

- FEE test stand is fully up and running
  - Warm test is being performed
  - Cold test will be followed
  - Without detector capacitance, noise is \( \sim 250e^- \) with 1us peaking time
  - With 150pF capacitance, noise is \( \sim 1000e^- \) with 1us peaking time
  - Nonlinearity is less than 0.4%, crosstalk is less than 0.7%

MicroBooNE FEE Test Stand Signal Readout Waveforms

64 channels of calibration pulse
Preliminary Warm Test Results

Gain & Peaking Time Measurement

Gain

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<th>Value</th>
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<tr>
<td>RMS</td>
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Gain/Ch

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Gain (mV/fC)

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Gain:Ch

Ramp Fitting

hOffset

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hOffset (ADC)

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hSlope

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hSlope (ADC/mV)

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hNlin

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hNlin [%]

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hChi2

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hChi2

Gain/Peaking Time Variation: ~3%

Non-linearity < 0.4%
Preliminary Warm Test Results

Noise Measurement

Pedestal [Ch0-31]
Mean: 2047
RMS: 3.985

Pedestal [Ch32-63]
Mean: 451.8
RMS: 5.897

RMS
Mean: 1.689
RMS: 0.02968

Crosstalk Measurement

Channel Injected
Channel Measured
Crosstalk [%]

Noise w/o Cdet w. 1µs t_p ~ 250 e−

Crosstalk < 0.7%
Summary

- LAr TPC is a high resolution imaging technology with excellent background rejection for neutrino oscillation measurement, proton decay with potential to reveal new physics
  - Cryogenic electronics installed close to the detector elements is critical to ease scaling issues and improve signal to noise ratio
  - MicroBooNE will be the first running neutrino experiment to use a specific implementation of cryogenic front end electronics

- MicroBooNE front end readout electronics system
  - Readout architecture and data flow are well defined to accommodate the different running modes
  - MicroBooNE will be instrumented with cryogenic CMOS analog front end ASIC
  - MicroBooNE front end electronics parts have been prototyped successfully
  - MicroBooNE FEE test stand has been constructed and is fully functioning
Backup Slides
1st Version of CMOS ASIC – Signal Measurement

Gain 25 mV/fC
Peaking time 1μs

Bandgap Reference

\[ V_{BGR} \approx \begin{cases} 
1.185 \text{ V at } 300 \, ^\circ\text{K} \\
1.164 \text{ V at } 77 \, ^\circ\text{K} 
\end{cases} \]
variation \approx 1.8 %

Temperature Sensor

\[ V_{TMP} \approx \begin{cases} 
867.0 \text{ mV at } 300 \, ^\circ\text{K} \\
259.3 \text{ mV at } 77 \, ^\circ\text{K} 
\end{cases} \]
\approx 2.86 \text{ mV / } ^\circ\text{K}

Pole-zero cancellation at 77K
to be addressed in next revision

Adjustable gain, peaking time and baseline

maximum charge 55, 100, 180, 300 fC

non-collecting mode

collecting mode

Peak time [μs]

0.5
1.0
2.0
3.0

Time [μs]

0 10 20 30 40 50
Measurements include:

- Input line parasitic resistance \( \approx 11 \ \Omega \)
  - \( \approx 350 \ \text{e}^- \) at 77 K
  - addressed in next revision
- \( C_{\text{IN}} \) dielectric noise (not present in wire)
  - \( \approx 100 \ \text{e}^- \) at 77 K

\[
d\text{ENC} \approx \sqrt{2kT C_{\text{IN}} t \tan \delta}
\]

- For NPO: \( 210 \ \text{e}^- \)
- For MICA: \( 100 \ \text{e}^- \)

**Input Line**
- \( L \approx 1 \ \text{mm} \)
- \( W = 3.5 \ \mu\text{m} \)
- \( (M3 + M4) \)
- \( R \approx 11 \ \Omega \)

**Input MOSFET**
- \( L = 270 \ \text{nm} \)
- \( W = 10 \ \text{mm} \)
- \( (50 \mu\text{m} \times 200) \)
- \( g_m \approx 40 \ \text{mS} \) (25 \( \Omega \))