SIS recommissioning for Run 3

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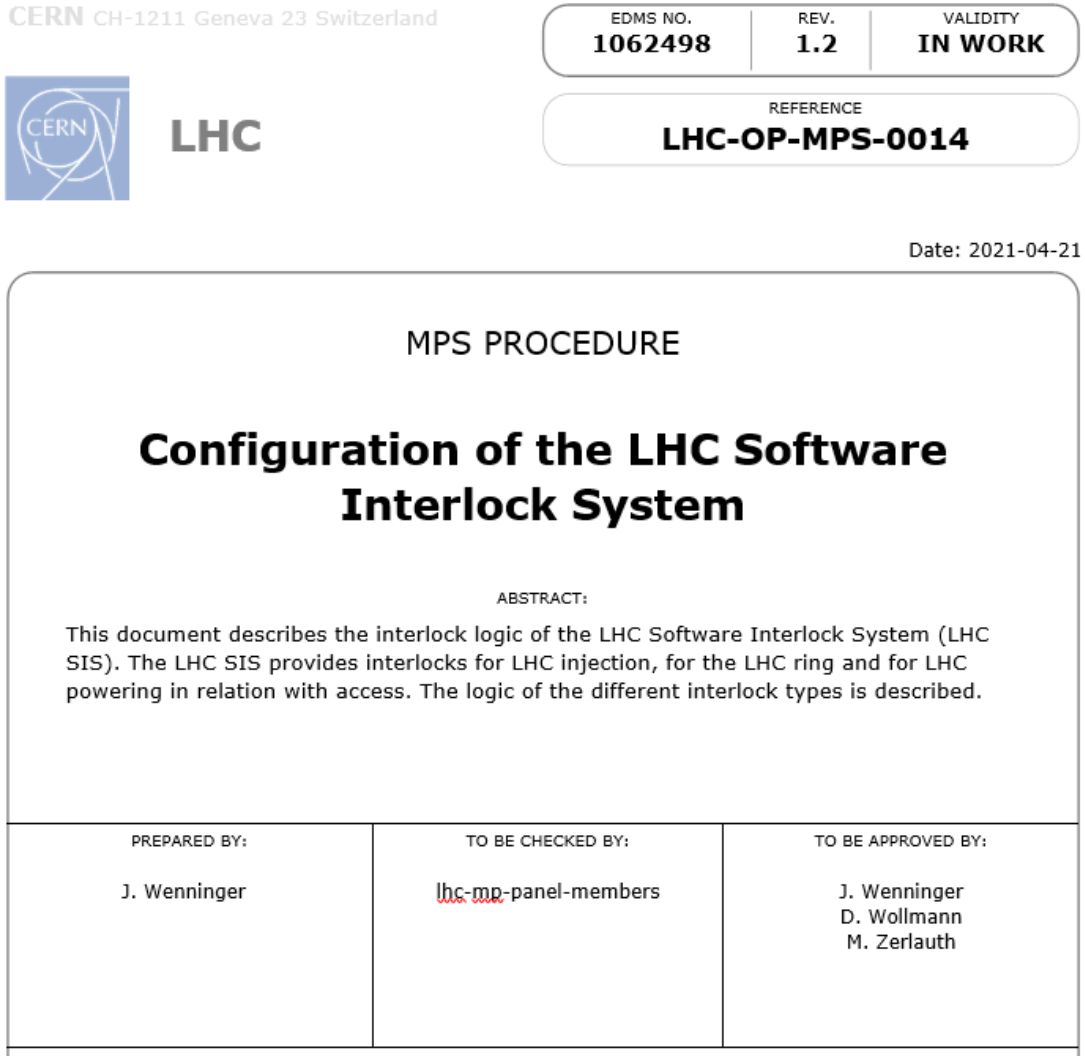
LHC SIS status

- There are no fundamental changes to LHC SIS wrt Run 2 besides the migration from JAVA 8 to JAVA 11.
  - The SIS server collects and processes all signals, dispatches actions to BIS, SMP and PIC.
- Migration of some logic or part of the signal processing to UCAP servers was considered, but the cost – benefit ratio did not seem sufficient at this stage.
  - **+** : smaller processing ‘units’,
  - **+** : possibility to log output/result signals in nxcals,
  - **-** : additional SW layer with more complicated online diagnostics,
  - **-** : loss/transmission of the signal status information,
  - **-** : difficulty to test loss of input information.
- All interlocks will be re-tested – some need beam in SPS and/or LHC.
  - Beam tests will be mainly commissioned in 2022.
- Interlocks with many inputs may be sampled randomly (for example orbit).

Document and checklist

- The document with the description of all tests has to be updated (~10% of the total text).
- Tests will be inserted into checklist tool, probably manually (TBC).



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EDMS NO.	REV.	VALIDITY
1062498	1.2	IN WORK

LHC

REFERENCE
LHC-OP-MPS-0014

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MPS PROCEDURE

Configuration of the LHC Software Interlock System

ABSTRACT:

This document describes the interlock logic of the LHC Software Interlock System (LHC SIS). The LHC SIS provides interlocks for LHC injection, for the LHC ring and for LHC powering in relation with access. The logic of the different interlock types is described.

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SIS input device status

- The majority of devices are running (> 95%), the interlocks are ‘working’, to be re-tested.
  - New orbit/tune feedbacks and new PC_interlock updated.
- List of ‘dead’ devices – dominated by RF and BI – expected back ~ June.

System	Missing data	Comment	
ADT	ADTBpos	FESA class dead	
RF	FullDetuning	FESA class dead	
RF	BQM LHC	FESA class dead	
RF	Misc data	FESA class dead	
BI	DOROS Bpms	FESA class dead	Expected June 2021
BI	BSRA SIS interlock	FESA class dead	
BI	BSRT mirror	FESA class dead	
BI	BTVs	Some devices dead	
ABT	MKI AGK-FIB	FESA class dead	
ABT	MKDTSPM (LBDS PS monitoring)	FESA class dead	
BIS	BIS preop checks	FESA class dead	
SMP	SMP preop checks	FESA class dead	
VSC	TDE Piezo pressure	Devices no longer exist	Obsolete?

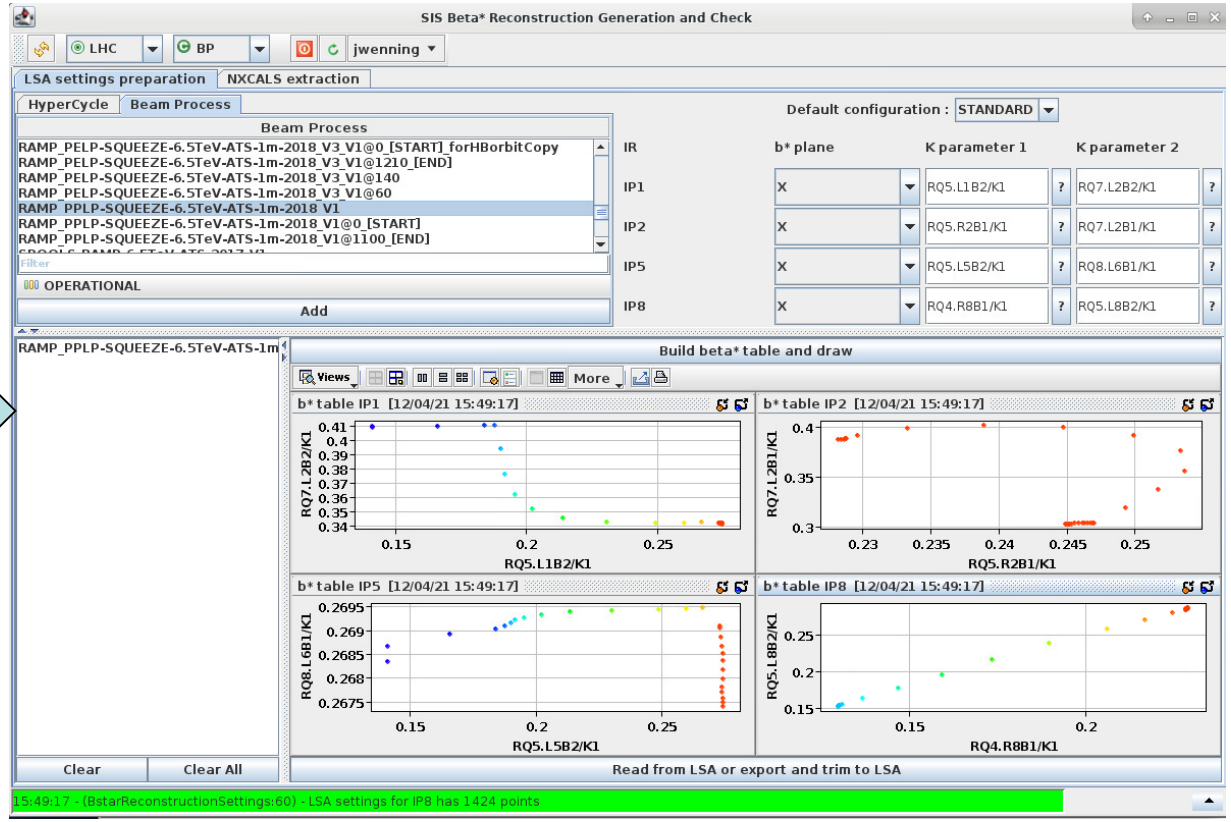
Powering interlocks

- The powering-access logic for personnel protection during phase powering 2 is **operational since the beginning of January**.
  - Full revalidation in December 2020 and during powering DSO tests.
- Circuit protection related powering interlocks:
  - **RBCX combined powering limits**,
    - "Deactivated" by raising limits during powering tests.
  - **Limiting current difference of RQD and RQF circuits to 2kA**,
  - **Redundant switch opening for RB, RQD and RQF**,
    - **Active on S34 and S78 according to SIS logs**. **Check arrival in PIC logs !**
  - **RQ9 and RQ10 current limits** – obsolete for 7 TeV ?
  - **MQXA1 current limit** (RQX+RTQX1) – **new** (proposed by M. Solfaroli),
    - Implemented, but not active and not tested
- The testing of the circuit protection interlocks to be performed at the end of the powering tests.

SIS-SMP : beta* reconstruction

Moving to 2D reconstruction of gradients – as proposed at MPP meeting and MPP workshop:

- **The code is in place in SIS** (in parallel to old method),
- Tool for reference settings generation and check wrt nxcals logging in place.
- Reconstruction and publication to SMP to be switched to new method.
- Test and integration tentatively next week (with PCs in simulation mode !).
- Warning: beta* generation is currently in simulation mode !



SIS-SMP : TL optics ID

- A long time ago, it was decided to generate by SIS the **equivalent of beta* for the TLs** – in the form of an **optics ID – inject it into SMP** and interlock the TCDI gaps with it.
  - Using the same principle as the beta* gap interlock for ring collimators.
  - Never implemented on the collimator side (TCDIs) in Run 2.
  - But the newly deployed classes for the TCDIs have settings for beta* and energy gap interlocks → implementation possible?
- The optics ID is generated by LHC SIS:
  - Reference setting in LSA with currents of TI2(8) quadrupoles and associated optics ID,
  - References are compared to actual interlock (FEI) reference in HW (0.5% tol).
  - Publish either **optics ID** (all ok) or **0** (invalid optics).
- The TL circuits are now split among two inconsistent FGC classes (different APIs).
  - Publication 'philosophy' of FGC classes are different, some testing and FGC 'behaviour' verification is required.
- If the implementation in the collimator FESA class does not work, one might consider **an interlock on the optics ID (!= 0) at LHC injection** to ensure that the TL optics is consistent with what the LHC expects (else the optics ID is just a useless value…).

PC currents interlocking

- The PC interlock server which is interlocking the PC currents – including dynamic phases – was recently improved by the BE-OP-LHC and TE-MPE SW teams.
  - **Corrector interlocks are split by beam and plane.**
  - **Quadrupole interlocks are split by beam**.
  - **Dipole (RB) and separation dipole (RD) interlock signals** were added.

  } **Improvements for MDs**
- PC interlock covers now all quadrupoles, orbit correctors and dipole circuits.
  - Not included: sextupoles, skew quadrupoles, spools. All difficult to interlock.
  - The BBLR is not included for the moment because of the absence of a proper model in LSA (was agreed with ABP, action open).
- The new server is deployed, LHC SIS has been adapted.
  - Big Sister (for vocal warnings) started but not completed.
- With the new functionality of PC interlock, some old SIS interlocks can be removed:
  - Interlock on RD currents at injection – removed.
  - BETS-like tracking of Q4s in point 6 (LBDS BETS redundancy) – to be discussed.
  - BETS-like tracking of all 8 RB circuits (LBDS BETS redundancy++) – to be discussed.

Changes : injection

- The TDI is replaced by 3 TDIS per beam (A,B,C).
  - On LHC page1 the gap of TDISA is displayed (as agreed with C. Bracco).
- SIS will interlock the up- and downstream gaps of all 3 TDIS.
  - Interlocks in place, interlock limits to be defined after beam commissioning.

- To close a loop-hole in the LHC/SPS MTGs error phase space in case of inconsistency between SPS destination and LHC ring telegram, a **check of the SPS dynamic destination** was added to the injection permits for B1 and B2.

Changes : collimator BPMs

- For the moment the collimator DOROS systems are not operational, devices are expected back in June.
- Extending the logic to the new channels is rather straightforward once the collimator information will be present in the LSA DB (including twiss information).
- In a first phase the existing channels will be restored, then the new channels will be added.
  - List of devices?
  - Do we have a list with recommended interlock settings?
- While the interlock infrastructure will be in place for the beam test, the actual validation of all channels will most likely only happen in 2022.

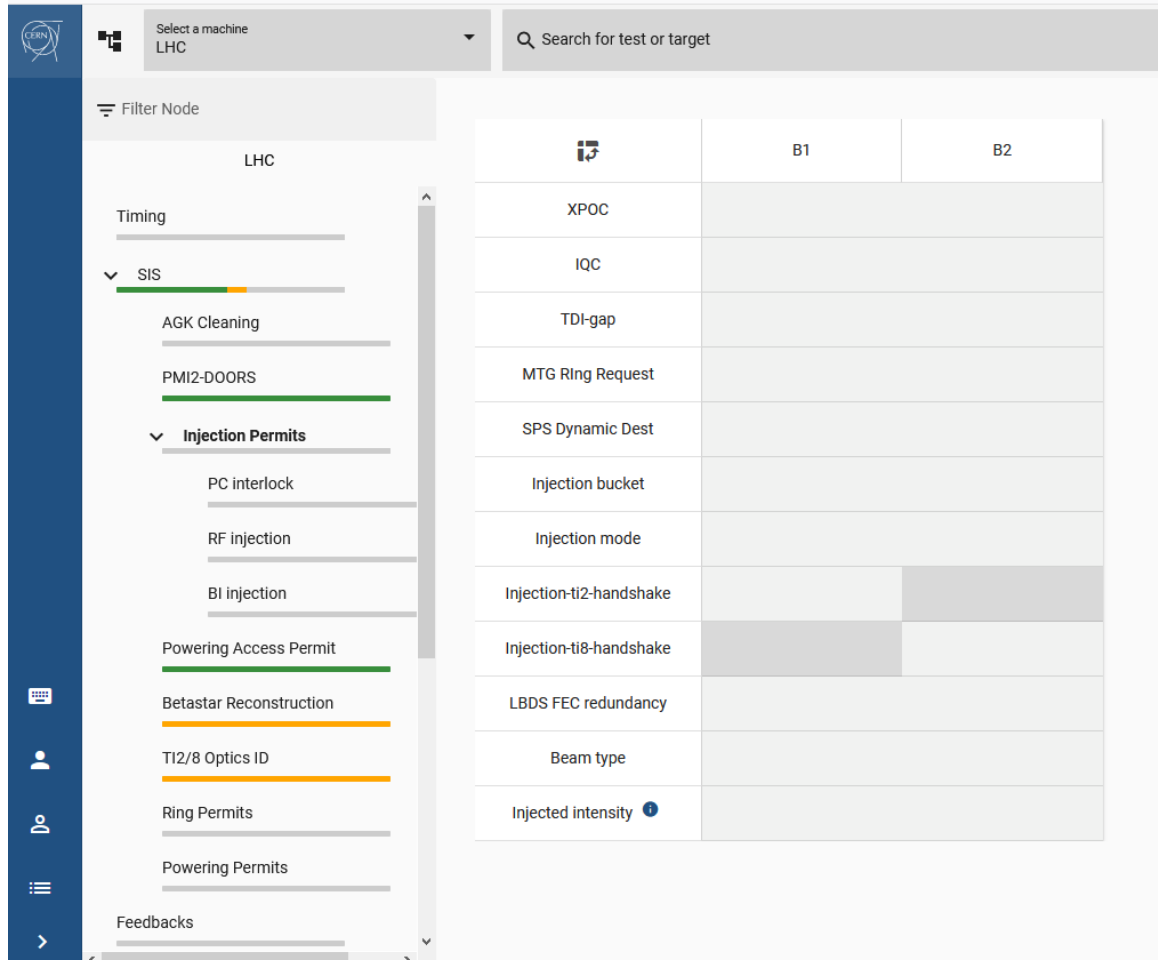
?

- What to do with the TDE N2 pressure interlocks after the upgrades? The vacuum devices seem to be disconnected…

- The entire BBLR logic needs to be redone.
  - For the moment the 2018 logic is still in place, not adapted to ABP's Run 3 goals.

Checklist

- The new version of the check list tool is released.
- Definition of OP and SIS tests in progress.
  - Eventually a manual configuration is better (for SIS), easier to define the desired granularity and structure.



Summary

- LHC SIS is already in quite good shape, expect to be almost completed by the end of June.
  - Operational for powering since January.
- Documentation to be updated for changes (beta*, PC interlock, TDI etc).
  - Overall some 10-20% of code/device types have been touched.
- Tests to be inserted into the checklist tool.
  - First tests and results in place.
- And then test, test, test, test….