



1

SIS recommissioning for Run 3

J. Wenninger



LHC SIS status



- There are no fundamental changes to LHC SIS wrt Run 2 besides the migration from JAVA 8 to JAVA 11.
 - The SIS server collects and processes all signals, dispatches actions to BIS, SMP and PIC.
- Migration of some logic or part of the signal processing to UCAP servers was considered, but the cost – benefit ratio did not seem sufficient at this stage.
 - + : smaller processing 'units',
 - + : possibility to log output/result signals in nxcals,
 - - : additional SW layer with more complicated online diagnostics,
 - -: loss/transmission of the signal status information,
 - : difficulty to test loss of input information.
- □ All interlocks will be re-tested some need beam in SPS and/or LHC.
 - Beam tests will be mainly commissioned in 2022.
- □ Interlocks with many inputs may be sampled randomly (for example orbit).





- The document with the description of all tests has to be updated (~10% of the total text).
- Tests will be inserted into checklist tool, probably manually (TBC).

CERN CH-1211 Geneva 23 Switz	erland EDMS NO. 1062498	REV. 1.2	VALIDITY IN WORK	
CERN LHC	LH	REFERENCE LHC-OP-MPS-0014		
			Date: 2021-04-21	
	MPS PROCEDURE			
Configurat I	tion of the LHC nterlock Syster	: Softw n	are	
This document describes the SIS). The LHC SIS provides in powering in relation with acco	ABSTRACT: interlock logic of the LHC Softwa nterlocks for LHC injection, for t ess. The logic of the different int	are Interlock Sy he LHC ring an erlock types is	vstem (LHC d for LHC described.	
PREPARED BY:	TO BE CHECKED BY:	то ве л	APPROVED BY:	
J. Wenninger	<u> </u>	J. V D. 1 M.	Venninger Wollmann Zerlauth	



SIS input device status



- □ The majority of devices are running (> 95%), the interlocks are 'working', to be re-tested.
 - New orbit/tune feedbacks and new PC_interlock updated.
- □ List of 'dead' devices dominated by RF and BI expected back ~ June.

System	Missing data	Comment	
ADT	ADTBpos	FESA class dead	
RF	FullDetuning	FESA class dead	
RF	BQM LHC	FESA class dead	
RF	Misc data	FESA class dead	
BI	DOROS Bpms	FESA class dead	Expected June 2021
BI	BSRA SIS interlock	FESA class dead	
BI	BSRT mirror	FESA class dead	
BI	BTVs	Some devices dead	
ABT	MKI AGK-FIB	FESA class dead	
ABT	MKDTSPM (LBDS PS monitoring)	FESA class dead	
BIS	BIS preop checks	FESA class dead	
SMP	SMP preop checks	FESA class dead	
VSC	TDE Piezo pressure	Devices no longer exist	Obsolete?





- The powering-access logic for personnel protection during phase powering 2 is operational since the beginning of January.
 - Full revalidation in December 2020 and during powering DSO tests.
- Circuit protection related powering interlocks:
 - RBCX combined powering limits,
 - "Deactivated" by raising limits during powering tests.
 - Limiting current difference of RQD and RQF circuits to 2kA,
 - Redundant switch opening for RB, RQD and RQF,
 - Active on S34 and S78 according to SIS logs. Check arrival in PIC logs !
 - RQ9 and RQ10 current limits obsolete for 7 TeV ?
 - MQXA1 current limit (RQX+RTQX1) new (proposed by M. Solfaroli),
 - Implemented, but not active and not tested
- The testing of the circuit protection interlocks to be performed at the end of the powering tests.





Moving to 2D reconstruction of gradients – as proposed at MPP meeting and MPP workshop:

- □ The code is in place in SIS (in parallel to old method),
- Tool for reference settings generation and check wrt nxcals logging in place.
- Reconstruction and publication to SMP to be switched to new method.
- Test and integration tentatively next week (with PCs in simulation mode !).
- Warning: beta* generation is currently in simulation mode !

Image: Contract of the contract		SIS Beta* Reconstruction Ge	eneration and Check			+ _ = ×
LSA settings preparation MXCALS extraction Process Default configuration : STANDARD * Beam Process Default configuration : STANDARD * Process Process <th>🔗 🖲 LHC 🖵 🕞 BP 🖵</th> <th>☑ ℃ jwenning ▼</th> <th></th> <th></th> <th></th> <th></th>	🔗 🖲 LHC 🖵 🕞 BP 🖵	☑ ℃ jwenning ▼				
Default configuration :: STANDARD * Default configuration :: STANDARD * Paule process NAMP PEL-SQUEEZE-6.5TeV-ATS-Im-2018 V3 V1:90 (START] forHBorbitCopy R RAMP PEL-SQUEEZE-6.5TeV-ATS-Im-2018 V3 V1:90 (START] RAMP PPL-SQUEEZE-6.5TeV-ATS-Im-2018 V1 RAMP PPLP-SQUEEZE-6.5TeV-ATS-Im-2018 V1 RAMP PPLP-SQUEEZE-6.5TeV-ATS-Im-2018 V1 RAMP PPLP-SQUEEZE-6.5TeV-ATS-Im-2018 V1 REGIME TO REAL TO R	LSA settings preparation NXCALS	extraction				
Beam Process NMMP_PELP-SQUEEZE-6.5TeVATS-1m-2018 V3 V1@120 [END] RAMP_PELP-SQUEEZE-6.5TeVATS-1m-2018 V3 V1@120 [END] RAMP_PELP-SQUEEZE-6.5TeVATS-1m-2018 V3 V1@120 [END] RAMP_PELP-SQUEEZE-6.5TeVATS-1m-2018 V1@100 [END] RAMP_PELP-SQUEEZE-6.5TeVATS-1m-2018 V1@100 [END] IP2 X RQ5.E321/A1 2 RQ7.L281/A1 RAMP_PELP-SQUEEZE-6.5TeVATS-1m-2018 V1@100 [END] IP3 X RQ5.L382/A1 RQ7.L281/A1 X RQ5.L382/A1 RQ7.L281/A1 RAMP_PELP-SQUEEZE-6.5TeVATS-1m-2018 V1@100 [END] IP3 X RQ5.L382/A1 RQ7.L281/A1 X RQ5.L382/A1 X RQ5.L382/A1 R RQ5.L382/A1 X RQ5.L382/A1 R RQ5.L382/A1 X RQ5.L382/A1 R RQ5.L382/A1 R RQ5.L382/A1 X RQ5.L382/A1 R RQ5.L382/A1 X <	HyperCycle Beam Process			Default configu	ration : STANDARD	-
RAMP_PELP-SQUEZZE-6.STeV-ATS-Im-2018_V3_V1@0_ISTARTI forHBorbitCopy RAMP_PELP-SQUEZZE-6.STeV-ATS-Im-2018_V3_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STeV-ATS-Im-2018_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STEV-ATS-Im-2018_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STEV-ATS-Im-2018_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STEV-ATS-Im-2018_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STEV-ATS-Im-2018_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STEV-ATS-Im-2018_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STEV-ATS-Im-2018_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STEV-ATS-Im-2018_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STEV-ATS-Im-2018_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STEV-ATS-Im-2018_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STEV-ATS-Im-2018_V1@0_ISTARTI RAMP_PPLP-SQUEZZE-6.STEV-ATS-Im-2018_V1@0_IS	Bea	m Process				
RAMP PEP-SQUEZZE-6.STeV-ATS-Im-2018 V3 V102140 IP1	RAMP_PELP-SQUEEZE-6.5TeV-ATS-1m-2 RAMP_PELP-SOUEEZE-6.5TeV-ATS-1m-2	2018_V3_V1@0_[START]_forHBorbitCopy 2018_V3_V1@1210 [END]	IR	b* plane	K parameter 1	K parameter 2
RAMP_PPLP-SQUEEZE-6.STEVATS.Im-2018 V1@0100_[END] IP2	RAMP_PELP-SQUEEZE-6.5TeV-ATS-1m-2 RAMP_PELP-SQUEEZE-6.5TeV-ATS-1m-2	2018 V3 V1@140 2018 V3 V1@60	IP1	x	RQ5.L1B2/K1	? RQ7.L2B2/K1 ?
IP5 x RQ5.L582/AL ? RQ8.L681/AL IP8 x RQ4.R881/AL ? RQ5.L882/AL ? RQ5.L882/AL RAMP_PPLP-SQUEEZE-6.5TeV-ATS-1IT IP8 x RQ4.R881/AL ? RQ5.L882/AL ? RQ5.L82/AL ? ? RQ5.L82/AL ? ? RQ5.L82/AL ?	RAMP_PPLP-SQUEEZE-6.5TeV-ATS-Im-2 RAMP_PPLP-SQUEEZE-6.5TeV-ATS-1m-2 RAMP_PPLP-SQUEEZE-6.5TeV-ATS-1m-2	2018 V1 2018_V1@0_[START] 2018_V1@1100_[END]	IP2	x	▼ RQ5.R2B1/K1	? RQ7.L2B1/K1 ?
Image: Control of the second secon	Filter		IP5	x	▼ RQ5.L5B2/K1	? RQ8.L6B1/K1 ?
Build beta* table and draw	000 OPERATIONAL	Add	IP8	x	▼ RQ4.R8B1/K1	? RQ5.L8B2/K1 ?
De table (PS (12)04/21 15:49:17) 0.2695 0.2695 0.2695 0.15 0.2 RQ4.R8B1/K1 Read from LSA or export and trim to LSA		Views Image: Balance Image: Balance </th <th>5 5 0.25</th> <th>b*table IP2 [12/04 0.4 0.35 0.35 0.3 0.23</th> <th>/21 15:49:17]</th> <th>۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲</th>	5 5 0.25	b*table IP2 [12/04 0.4 0.35 0.35 0.3 0.23	/21 15:49:17]	۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲ ۲
Clear Clear All Read from LSA or export and trim to LSA 54.40.17 Clear Statement (Clear All Statement for ISB has 1474 month) Clear Statement (Clear All Statement for ISB has 1474 month)		0.2695 0.2695 0.2685 0.2685 0.2675 0.15 0.2 ROS.LSB2/KL	0.25	D/280.25- 0.25- 0.15-	0.15 RO4.R881/r	0.2 a
15.40.17 . (RetarBeconstructionSattinge: 60) - 154 sattings for IPO has 1434 points	Clear Clear All		Read from LSA or ex	port and trim to LSA	4	
	15:49:17 - (BsterBeconstructionSettings 60) . I SA settings for IP8 has 1.424 points				-





- A long time ago, it was decided to generate by SIS the equivalent of beta* for the TLs in the form of an optics ID inject it into SMP and interlock the TCDI gaps with it.
 - Using the same principle as the beta* gap interlock for ring collimators.
 - Never implemented on the collimator side (TCDIs) in Run 2.
 - But the newly deployed classes for the TCDIs have settings for beta* and energy gap interlocks → implementation possible?
- □ The optics ID is generated by LHC SIS:
 - Reference setting in LSA with currents of TI2(8) quadrupoles and associated optics ID,
 - References are compared to actual interlock (FEI) reference in HW (0.5% tol).
 - Publish either optics ID (all ok) or 0 (invalid optics).
- □ The TL circuits are now split among two inconsistent FGC classes (different APIs).
 - Publication 'philosophy' of FGC classes are different, some testing and FGC 'behaviour' verification is required.
- If the implementation in the collimator FESA class does not work, one might consider an interlock on the optics ID (!= 0) at LHC injection to ensure that the TL optics is consistent with what the LHC expects (else the optics ID is just a useless value...).





- The PC interlock server which is interlocking the PC currents including dynamic phases – was recently improved by the BE-OP-LHC and TE-MPE SW teams.
 - Corrector interlocks are split by beam and plane.
 - Quadrupole interlocks are split by beam.

- Improvements for MDs
- Dipole (RB) and separation dipole (RD) interlock signals were added.
- □ PC interlock covers now all quadrupoles, orbit correctors and dipole circuits.
 - Not included: sextupoles, skew quadrupoles, spools. All difficult to interlock.
 - The BBLR is not included for the moment because of the absence of a proper model in LSA (was agreed with ABP, action open).
- The new server is deployed, LHC SIS has been adapted.
 - Big Sister (for vocal warnings) started but not completed.
- □ With the new functionality of PC interlock, some old SIS interlocks can be removed:
 - Interlock on RD currents at injection removed.
 - BETS-like tracking of Q4s in point 6 (LBDS BETS redundancy) to be discussed.
 - BETS-like tracking of all 8 RB circuits (LBDS BETS redundancy++) to be discussed.

4/29/2021





- □ The TDI is replaced by 3 TDIS per beam (A,B,C).
 - On LHC page1 the gap of TDISA is displayed (as agreed with C. Bracco).
- □ SIS will interlock the up- and downstream gaps of all 3 TDIS.
 - Interlocks in place, interlock limits to be defined after beam commissioning.
- To close a loop-hole in the LHC/SPS MTGs error phase space in case of inconsistency between SPS destination and LHC ring telegram, a check of the SPS dynamic destination was added to the injection permits for B1 and B2.





- For the moment the collimator DOROS systems are not operational, devices are expected back in June.
- Extending the logic to the new channels is rather straightforward once the collimator information will be present in the LSA DB (including twiss information).
- In a first phase the existing channels will be restored, then the new channels will be added.
 - List of devices?
 - Do we have a list with recommended interlock settings?
- While the interlock infrastructure will be in place for the beam test, the actual validation of all channels will most likely only happen in 2022.





- What to do with the TDE N2 pressure interlocks after the upgrades? The vacuum devices seem to be disconnected...
- □ The entire BBLR logic needs to be redone.
 - For the moment the 2018 logic is still in place, not adapted to ABP's Run 3 goals.





- The new version of the check list tool is released.
- Definition of OP and SIS tests in progress.
 - Eventually a manual configuration is better (for SIS), easier to define the desired granularity and structure.

	Select a machine . LHC	 Q Search for test or target 	et	
	➡ Filter Node			
	LHC	7	B1	B2
	Timing	XPOC		
	✓ SIS	IQC		
	AGK Cleaning	TDI-gap		
	PMI2-DOORS	MTG RIng Request		
	✓ Injection Permits	SPS Dynamic Dest		
	PC interlock	Injection bucket		
	RF injection	Injection mode		
	BI injection	Injection-ti2-handshake		
	Powering Access Permit	Injection-ti8-handshake		
-	Betastar Reconstruction	LBDS FEC redundancy		
•	TI2/8 Optics ID	Beam type		
2	Ring Permits	Injected intensity 0		
:=	Powering Permits			
>	Feedbacks			





- LHC SIS is already in quite good shape, expect to be almost completed by the end of June.
 - Operational for powering since January.
- Documentation to be updated for changes (beta*, PC interlock, TDI etc).
 - Overall some 10-20% of code/device types have been touched.
- □ Tests to be inserted into the checklist tool.
 - First tests and results in place.
- □ And then test, test, test, test....