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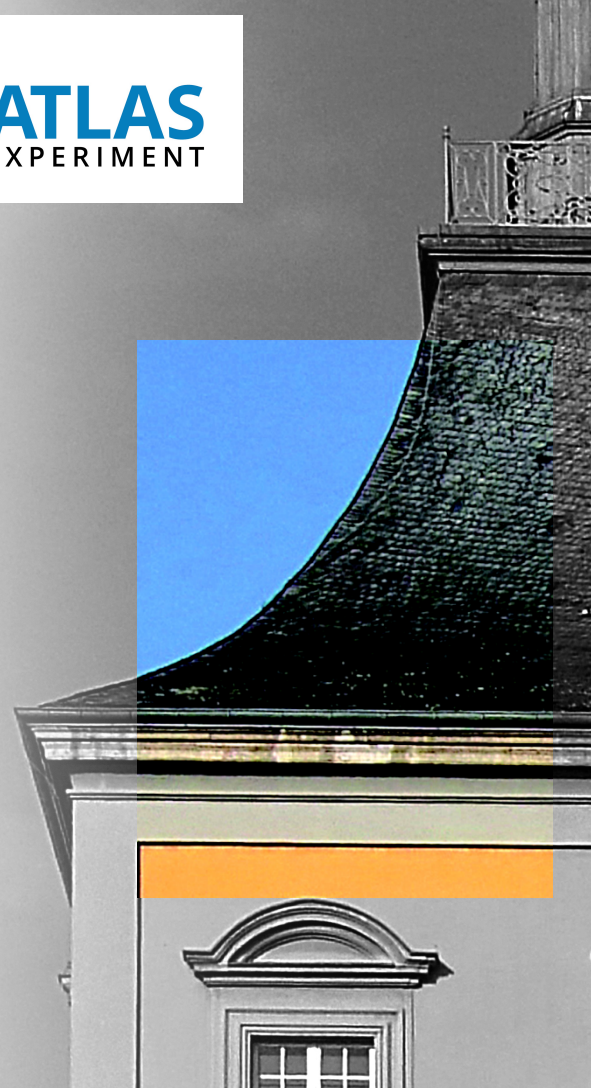
ATLAS ITk

ATLAS EXPERIMENT



NEW ATLAS ITK-PIXEL READ-OUT CHIP (AKA RD53B)

PARTICLE PHYSICS SEMINAR,
GÖTTINGEN, JUNE 25, 2021

FABIAN HÜGGING, UNIVERSITY OF BONN

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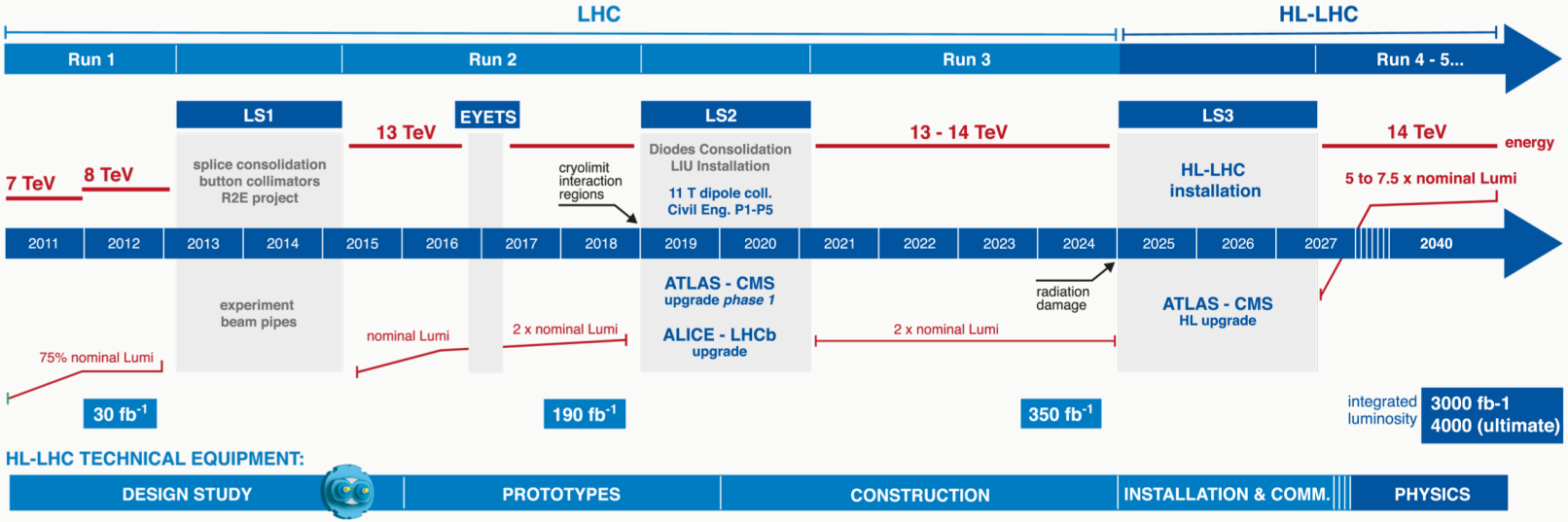
OUTLINE

ATLAS ITk

- Introduction
  - HL-LHC challenges
  - Layout of the ATLAS ITk Pixel Detector
- Pixel readout chip for hybrid pixel detectors:
  - Analog properties: Signal amplification and discrimination
  - Digital properties: Data flow and readout architecture
  - High speed data transmission
  - Radiation tolerance of CMOS pixel readout chips
- ITkPixV1 (RD53B)
  - General design strategy
  - Design features and test results
- Summary

HL-LHC SCHEDULE

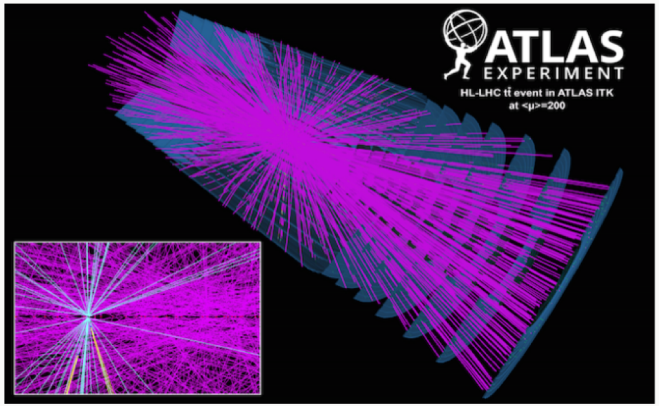


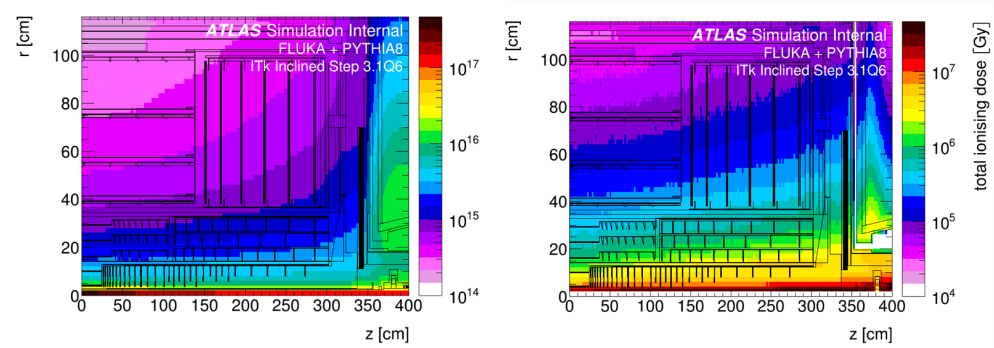
The LHC will be upgraded to the High Luminosity-LHC (HL-LHC) to produce up to 4000 fb^{-1} of integrated luminosity until 2035 and beyond

- benefits precision measurements in many physics channels
- allows studies of rare processes

INCREASING LHC LUMINOSITY: WHAT ARE THE CHALLENGES?

- HL-LHC luminosity ~$7x10^{34}cm^{-2}$
  - About x3.5 times Run-2 peak luminosity
- Increased luminosity → Increased pile-up:
  - Up to 200 pile-up events expected at the HL-LHC compared to ~34 in Run-II data
  - Increased pile-up compromises pattern recognition
  - Increased readout rates → increased trigger rates and latency requires multi-gigabit data transmission and large on-chip buffering
- Increased luminosity → Increased radiation damage:
  - Damage scales approximately linearly with luminosity ~x10 increase





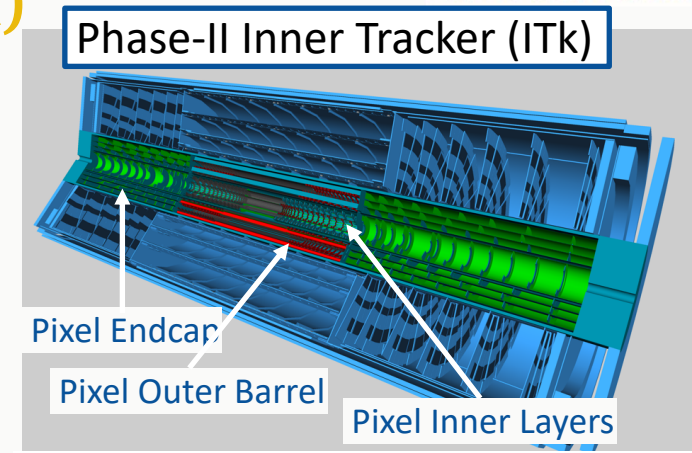
ATLAS INNER TRACKER (ITK)

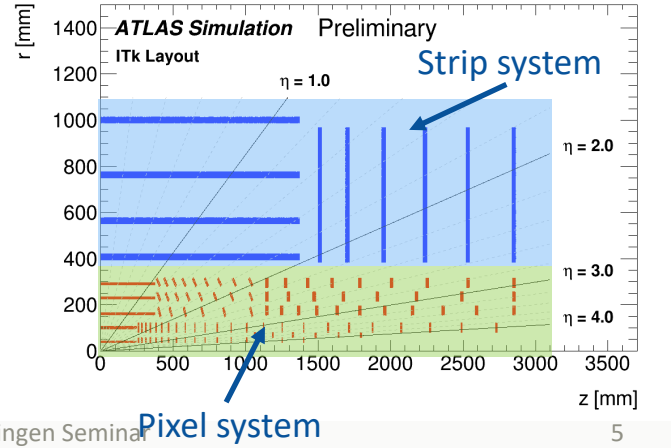
The current inner detector system will be replaced with a new all-silicon tracking system → ITk

- Coverage up to $|\eta| < 4$ with ≥ 13 hits / track (barrel) & ≥ 9 hits / track (forward)

<u>Requirements for ITk pixel detector:</u>

- Same or better performance than current Inner Detector:
  - Track reconstruction efficiency > 99% for muons & > 85% for electrons and pions
  - Increased granularity to maintain fake rate < 10^{-5}, occupancy < 1% and robustness against loss of 15% of channels
- Low mass mechanics, cooling and serial power to minimize material:
  - Material budget ~ 1.5-2.0% X/X_0 per layer
- Fast readout with trigger rate 1-4 MHz and output bandwidth up to 5.12 Gb/s per front-end chip
- Increased radiation hardness up to 2×10^{16} $n_{eq}cm^{-2}$ & 10 MGy (TID)

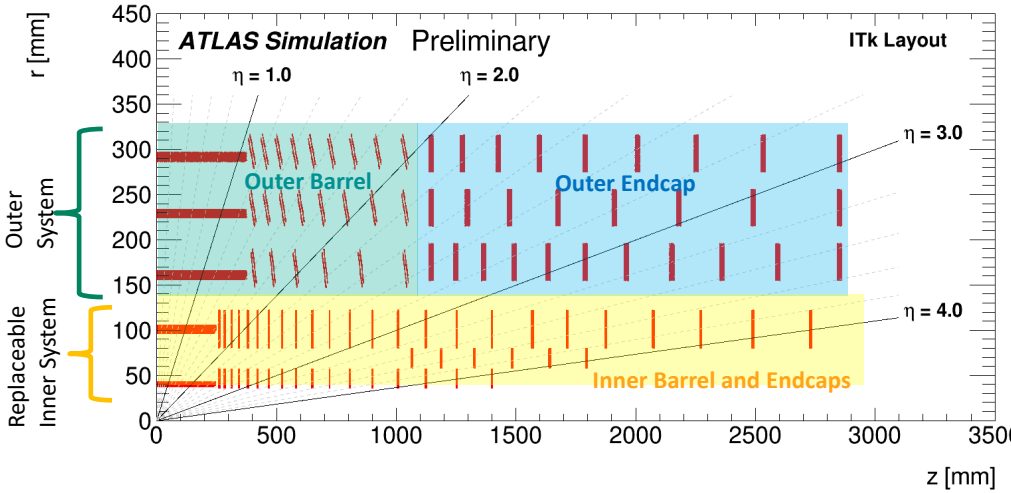




ITK PIXEL DETECTOR LAYOUT

Outer Barrel:
3 layers of flat staves and inclined rings
n-in-p planar quad modules
4472 quad modules, 7.2m^2
2.3x10^{15}n$_{eq}$cm^{-2} & 1.7MGy @4000fb^{-1}

Forward pixels:
3 layers of rings
n-in-p planar quad modules
2344 quad modules, 3.75m^2
3.1x10^{15}n$_{eq}$cm^{-2} & 3.5MGy @4000fb^{-1}



Layout and performance described in ATL-PHYS-PUB-2019-014

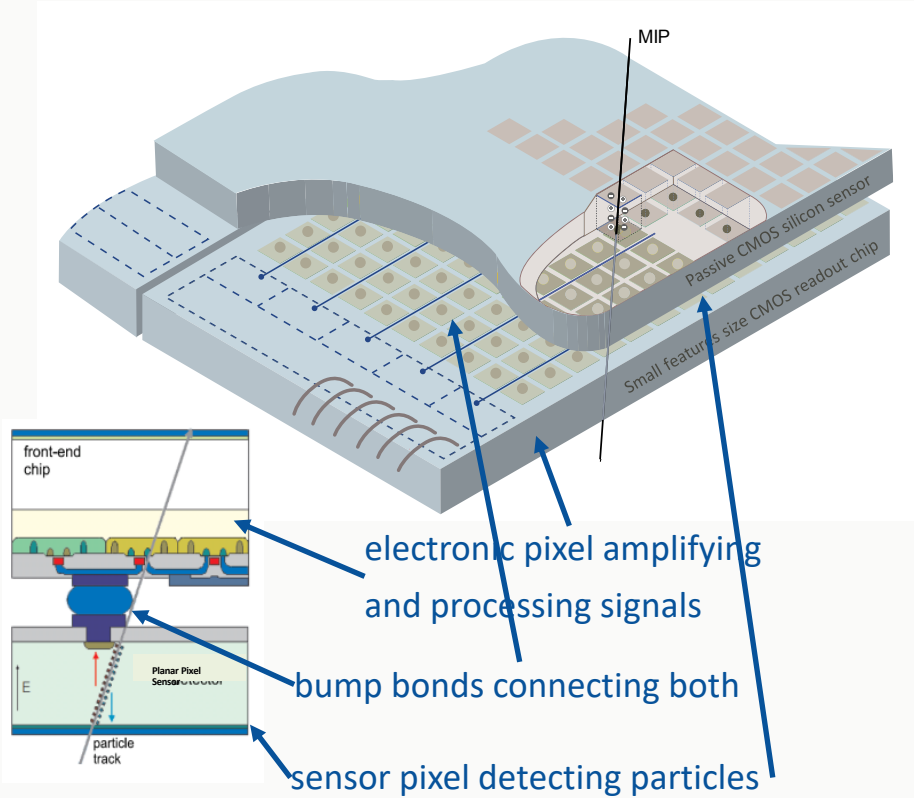
Current pixel system:
~92M pixels
~2000 modules
~1.9m^2 active area

ITk Pixel System:
~1.4G pixels
~9400 modules
~13m^2 active area

Inner System *Replaceable:*
2 layers of flat staves and rings
L0: 3D single modules, 1188 modules in 396 triplets, 0.5m^2
L1: n-in-p planar quad modules, 1160 modules, 2.0m^2
1.2x10^{16}n$_{eq}$cm^{-2} & 9.5MGy @2000fb^{-1} (layer-0 r=33/34mm)

HYBRID PIXEL DETECTORS

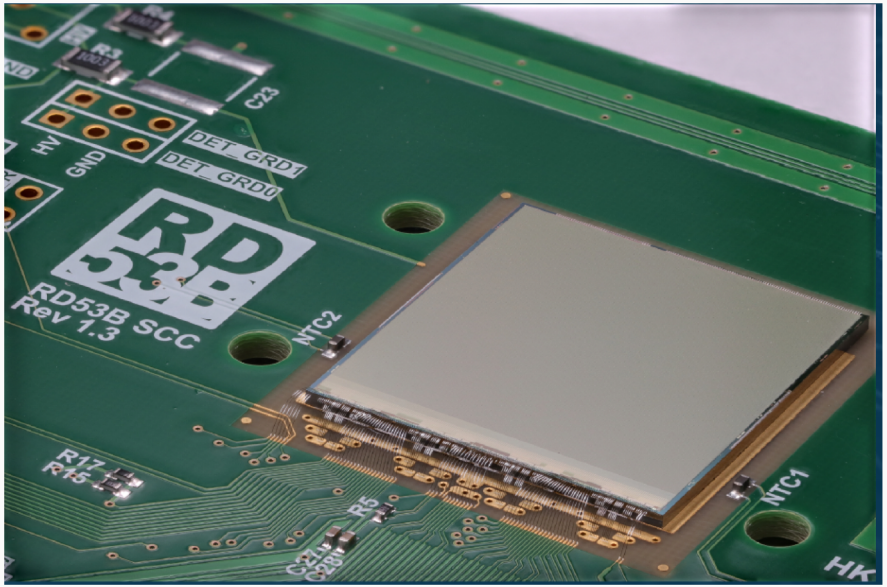
- State-of-the-art for high rate and high radiation application
- **Allows separate development of sensor and readout electronics to cope with radiation and rate levels:**
  - Typical pixel sizes ~50 - 100µm
  - e.g. 3D sensors, planar or passive CMOS sensors
  - Usage of smallest IC nodes (65 nm) for readout allowing more features and radiation tolerance
- Drawbacks:
  - Necessity of fine pitch bump bonding to connect sensor and electronics pixel by pixel
  - More material
- **Pixel detector readout chip is the essential and most critical part of the hybrid pixel detector**



HYBRID PIXEL READOUT CHIP

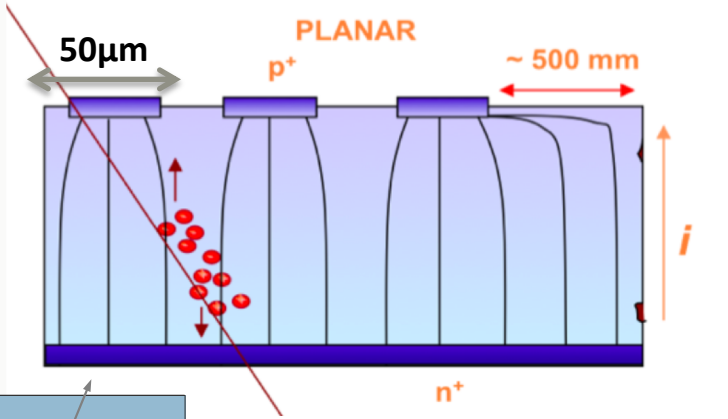
- Three main tasks for pixel readout chips at LHC/HL-LHC:
  - Amplification and discrimination (zero suppression) of signals in each pixel within 25 ns → Analog
  - Handling and storage of hit data on chip until trigger signal arrives (ATLAS latency ~10µs or ~400 bunch crossings) → Digital
  - Send out data with high speed (ATLAS: up 5 Gbit/s at 1 MHz trigger rate) → Data transmission
- Many more aspects need to be considered: powering, **radiation tolerance**, SEE/SEU tolerance, testability, calibration routines, slow controls etc.

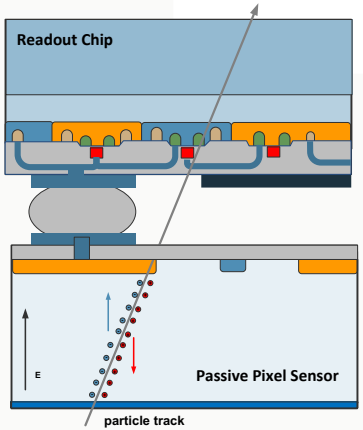
RD53B aka ITkPixV1

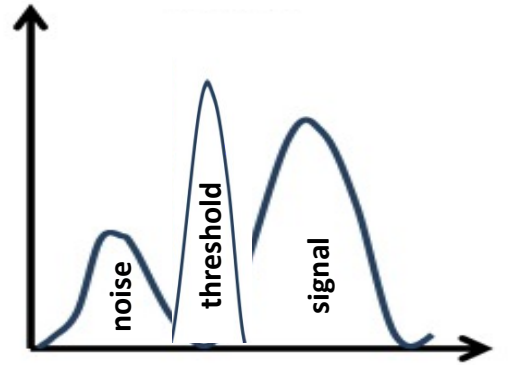


ANALOG: IN PIXEL SIGNAL AMPLIFICATION & DISCRIMINATION

- Analog properties are a complex optimization between pixel size, electrical noise, timing, threshold tuning capabilities and power consumption:
  - E.g. for 50 µm pixel size → ~4ke$^-$ input (charge sharing + radiation effects) → <2ke$^-$
  - Threshold need to be adjusted between noise and signal → for pixel per chip threshold dispersion contributes to noise: $\sigma_{eff}^2 = \sigma_{thres}^2 + \sigma_{noise}^2$
  - Signal/Amplifier rise time must be fast enough to allow detection within 25 ns for LHC
  - Smaller pixel are beneficial for analog performance
    - Smaller detector capacity C_D
    - Smaller sensor leakage current I_D per pixel
    - Noise ∝ C_D, I_D →lower noise →better S/N!
  - But for smaller pixel amplifiers, discriminator and hit storage need to fit in the pixel

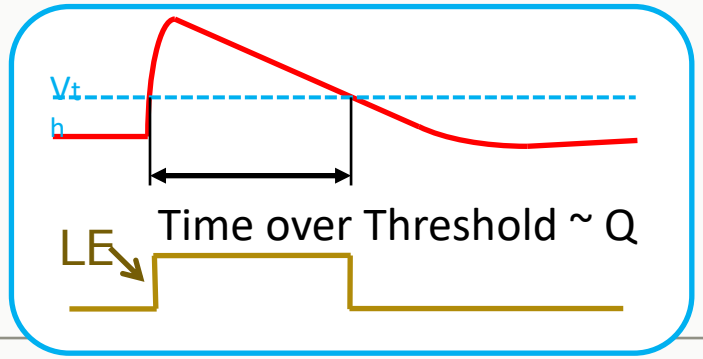


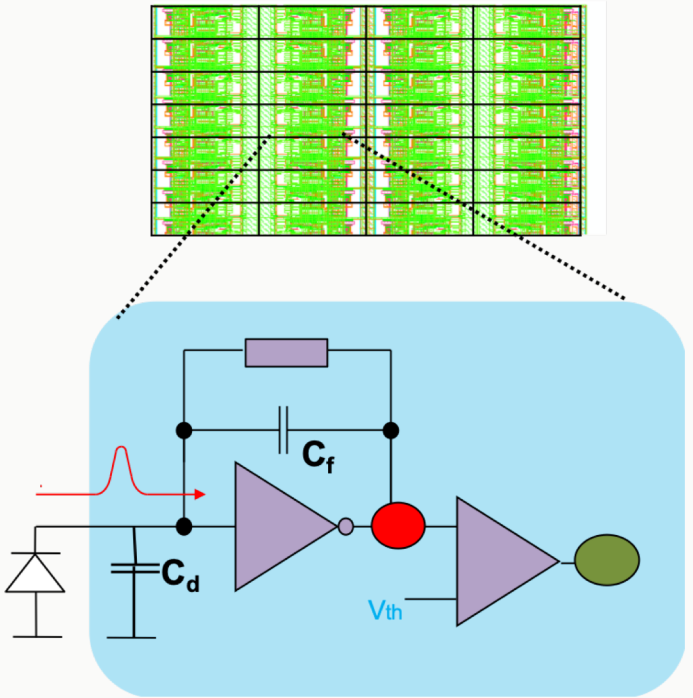




ANALOG: IN PIXEL SIGNAL AMPLIFICATION & DISCRIMINATION

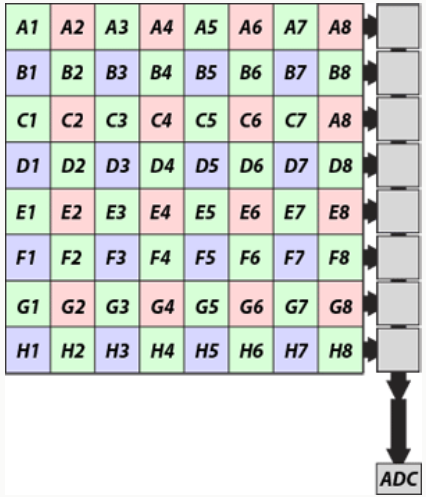
- Noise: $ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{\mathbf{C_d^2}}{\tau}$
- Timing: $\tau_{CSA} \propto \frac{1}{g_m}\frac{\mathbf{C_d}}{C_f}$
- need to increase g_m to compensate → power of the amplifier increases ($g_m \propto I_d$)
- Time-walk of discriminator to be taken into account → in-time threshold or time-walk correction

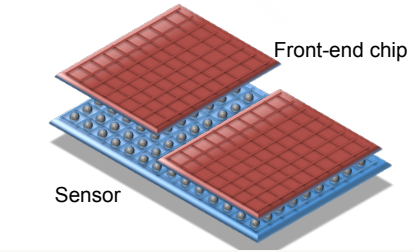




DIGITAL: ON CHIP DATA HANDLING & READOUT

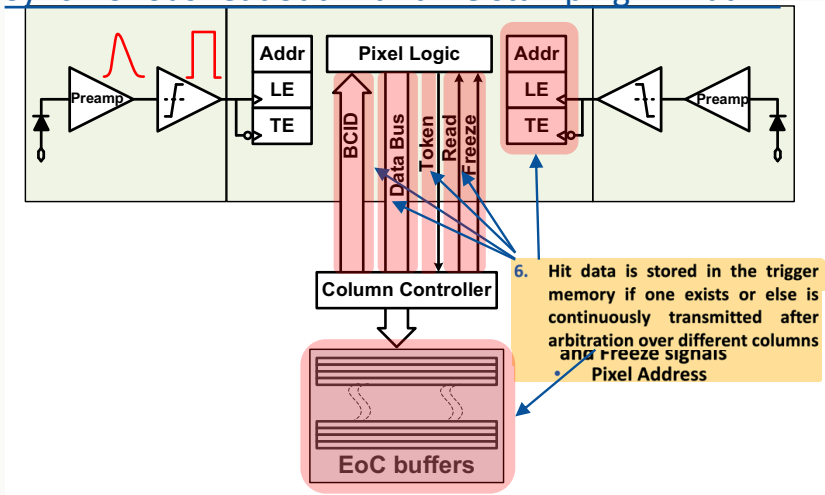
- After in-pixel discrimination hits are digital 2D position stored in pixel without ambiguities
  - Small area of segments are beneficial for digital readout
  - **low data rate per pixel → more time for read-out**
- Frame based readout:
  - Store hit information in pixel & activate one row at a time or shift row content
  - → **simple connection**, "shared" electronics **but too slow (~µs – ms) for LHC**
- **Parallel readout**:
  - One amplifier per pixel segment + zero-suppression
  - **Faster for high occupancies!**
  - Direct interconnection between each sensor pixel and readout pixel needed → **hybrid pixel**
  - **Challenge for the chip: integration of storage buffers and data flow on chip**





READOUT ARCHITECTURE: COLUMN DRAIN

Synchronous readout with time stamping in matrix

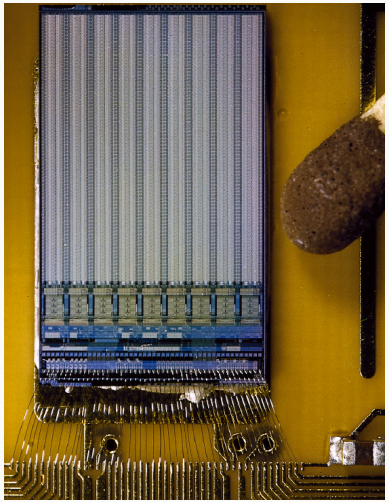


- BC ID (40 MHz) distributed in the column
- Hit timing stamped in pixel
  - LE: leading edge
  - TE: trailing edge

  => Time of arrival: LE

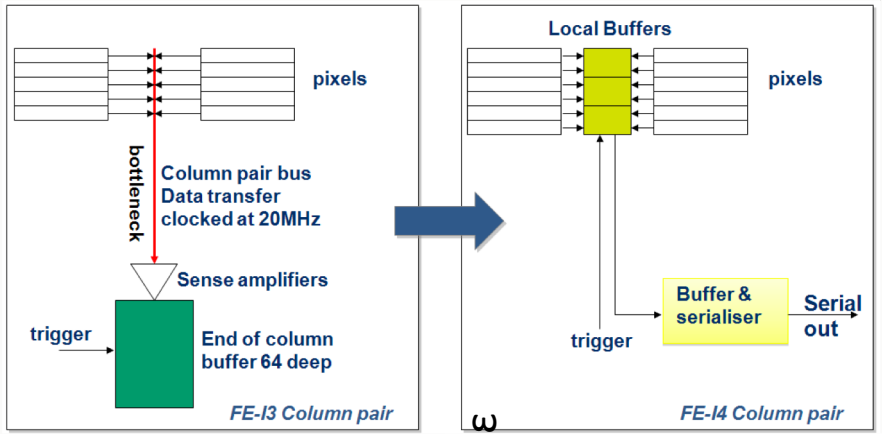
  => Ana. info. from ToT
- Hits read out sequentially, following a token passing scheme on a shared column bus

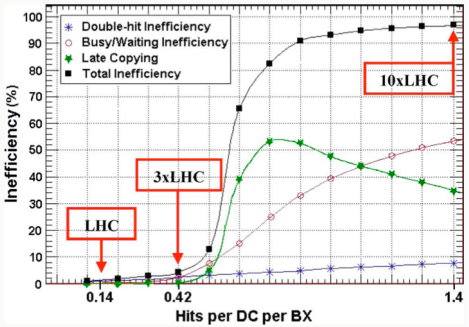
FE-I3 pixel chip

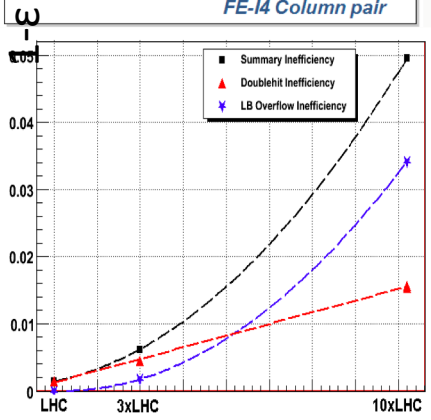


- Well established scheme in ATLAS – FE-I3 like (ATLAS phase 1 pixel detector)
- Demonstrated rate capability for current pixel detector (and ITk outer pixel layers) but not for innermost layers
- Affordable in-pixel logic (storage & digital R/O)
- **Problem: all hits are transferred to periphery → buffer size increases with rate**
- **“Column drains” get stuck at high rates esp. for large chips**

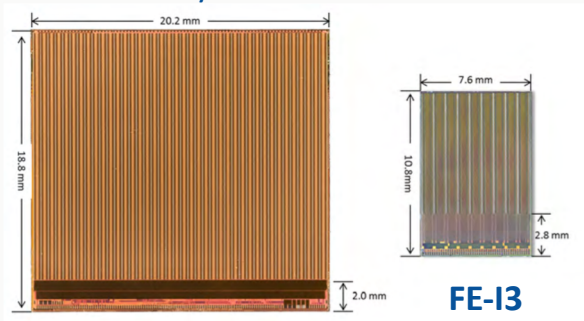
READOUT ARCHITECTURE: COLUMN DRAIN WITH LOCAL HIT STORAGE





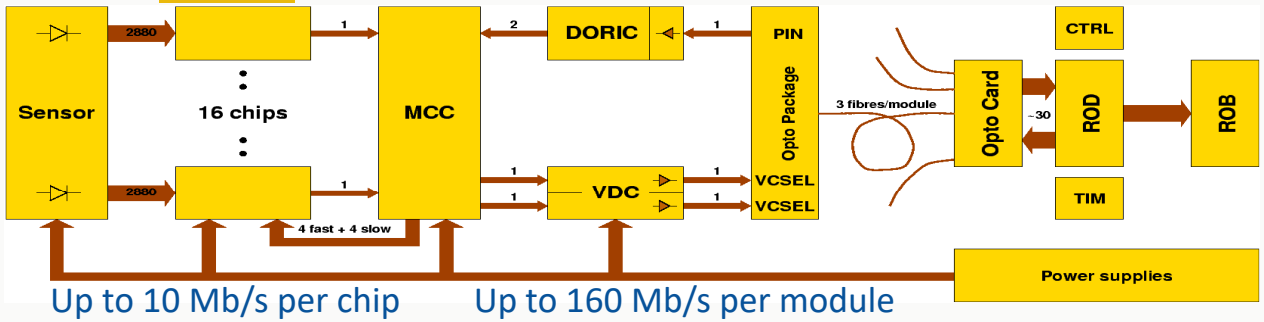


- Improved column drain architecture to reduce inefficiences at higher hit rates:
  - Local storage of hit in pixel matrix until trigger arrives.
  - Works fine up to 400MHz/cm^2 hit rate for much bigger chip size (~2x2cm^2)
  - But more space inside pixel needed → smaller technology node
  - Higher output bandwidth required
  - Used successfully in FE-I4 for the ATLAS IBL

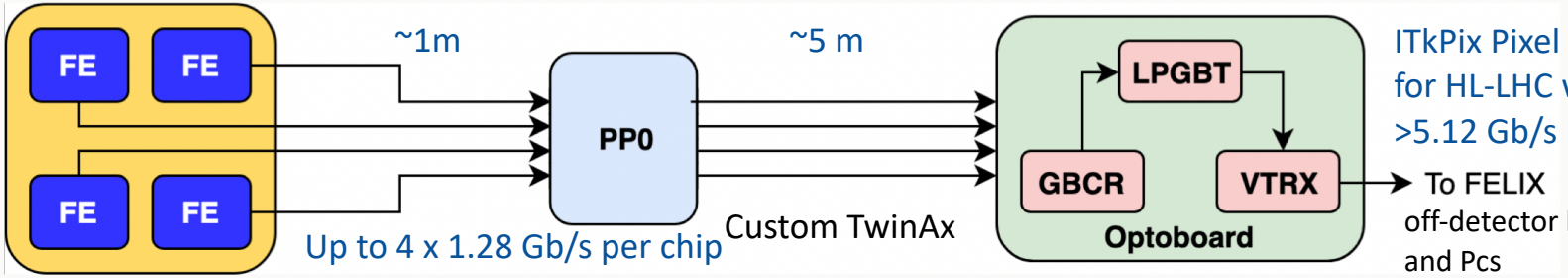


FE-I4 pixel chip

DATA TRANSMISSION



Phase 1 Pixel Detector with FE-I3 with 160 Mb/s maximum bandwidth



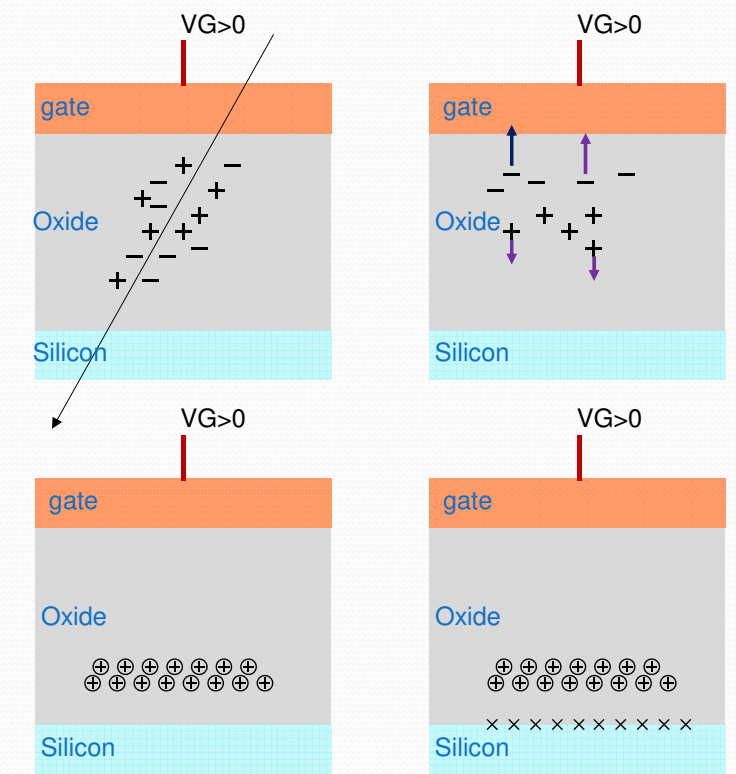
ITkPix Pixel Detector for HL-LHC with >5.12 Gb/s bandwidth

- Required **data transmission bandwidth** is driven by **hit rates and trigger rates** → both have been increased from Phase 1 to HL-LHC by orders of magnitude:
  - Maximum hit rate from **~100 MHz/cm²** to **3 GHz/cm²** and maximum trigger rate from **75-100 kHz** to **1 MHz**
  - Required chip out bandwidth increased from **~10Mb/s** (FE-I3) over 160(320) Mb/s (FE-I4) to **5.12 Gb/s** (RD3A/B)

RADIATION TOLERANCE OF CMOS PIXEL READOUT CHIPS

- Radiation effects in CMOS from ionizing dose (TID) in SiO_2 layers:
  - 1st step: Ionizing Radiation → electron/hole pairs produced in oxide. Depending on biasing, electrons swept out in ~ps. A fraction of e^-/h recombine
  - 2nd step: Hopping hole transport to Si/SiO2 interface
  - 3rd step: Holes at interface → long-lived trap states → Q_t → ΔV_t (<0 for nmos and >0 for pmos transistors)
  - 4th step: Interface traps build-up : → Q_{it} →
  - ΔV_{it} (>0 for nmos and pmos)
- Note:
  - For SiO_2: $\mu_e \simeq 10^6\ \mu_h$ with $\mu_e \simeq 20\ cm^2/Vs$ at T_{room}
  - Typical gate thickness $t_{ox} \simeq 2.6$ nm for 65 nm CMOS
  - $\Delta V_t \propto t_{ox}$ + annealing due to tunnel effects

→ **65 nm CMOS is intrinsically radiation tolerant**

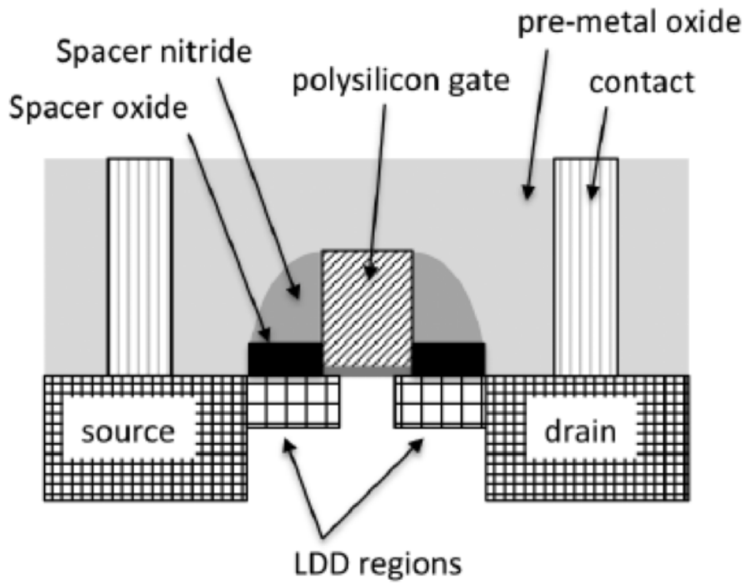


RADIATION EFFECTS IN CMOS FOR HIGHLY SCALED PROCESSES: RINCE & RISCE

- Thin gate oxide is very tolerant to the TID damage
- But thick oxide is used for isolation between transistors: Thick **S**hallow **T**rench **I**solation Oxide (STI)
- This thick oxide exists everywhere around the device and scales with smaller feature sizes

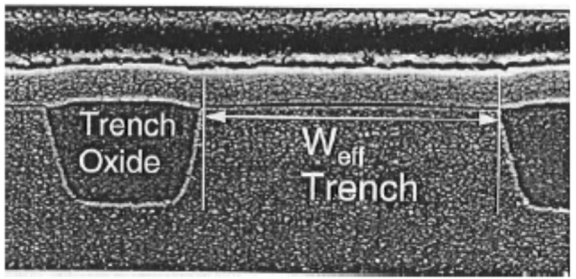
→Radiation Induced Narrow Channel Effect (RINCE)

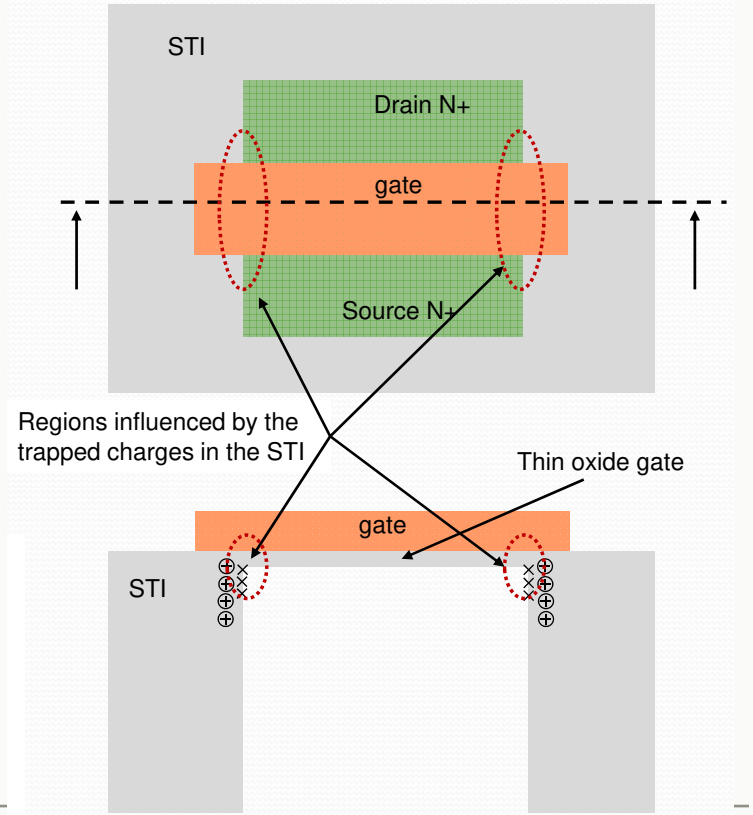
→Radiation Induced Short Channel Effect (RISCE)



RADIATION EFFECTS IN CMOS FOR HIGHLY SCALED PROCESSES

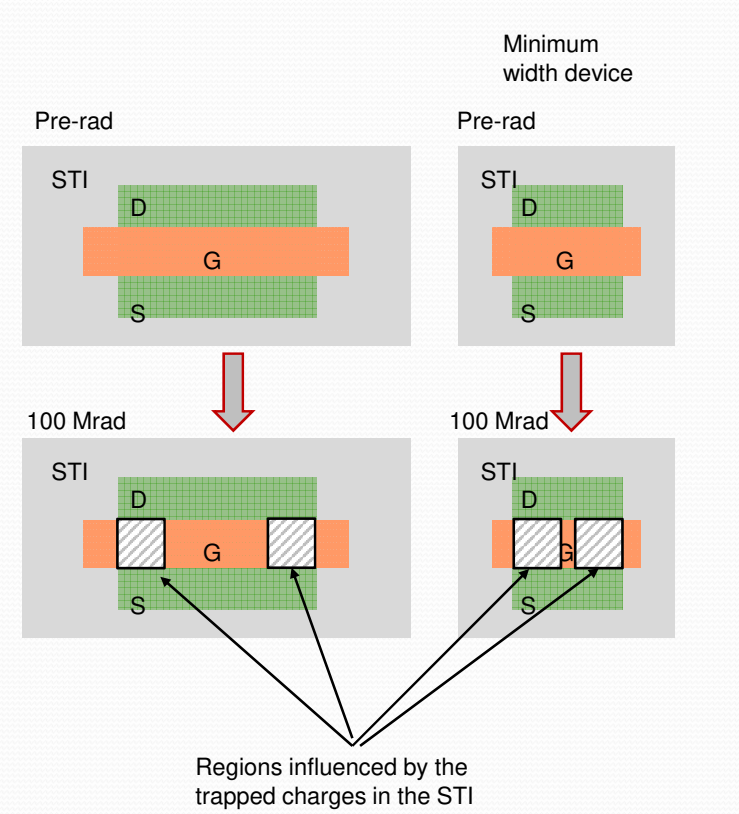
- Thick **S**hallow **T**rench **I**solation Oxide
  - STI depth of ~300nm
  - Radiation induced charge build-up:
    - Oxide trapping and interface trapping
    - May turn on lateral parasitic transistors → **leakage**
    - Affect electric field in the channel: V_{th} shift, mobility decrease, noise increase
- Doping profile along STI sidewall is critical
  - Doping increase with CMOS scaling
  - Doping decreases in I/O devices → less radiation tolerant





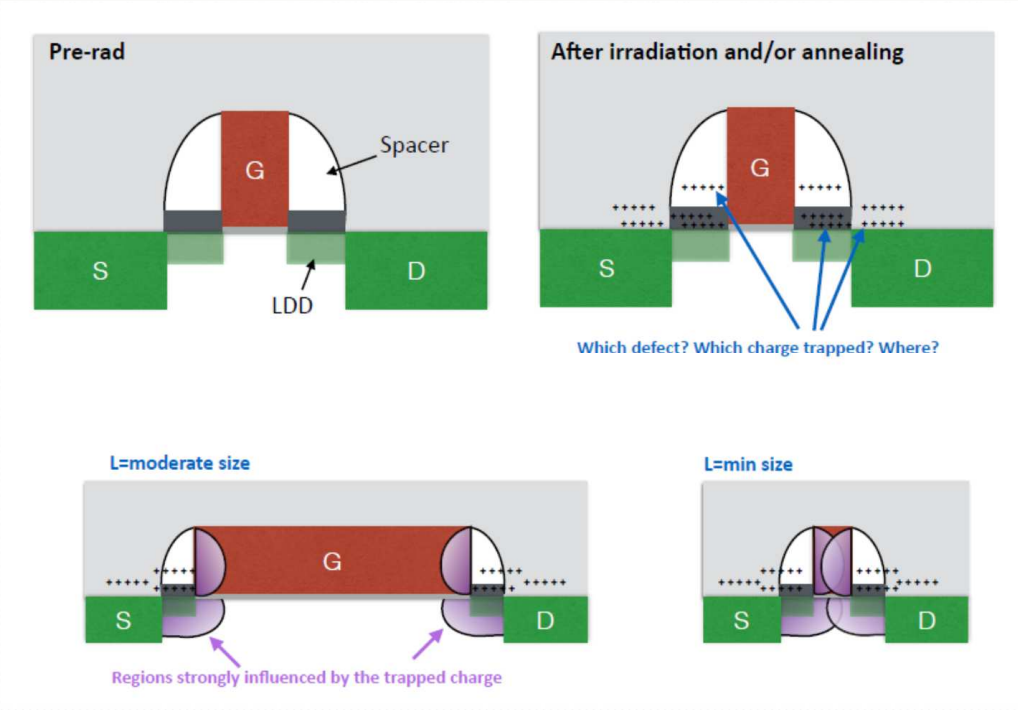
RADIATION INDUCED NARROW CHANNEL EFFECT (RINCE)

- RINCE is caused by the charge trapped in the STI
- This charge affects the electric field in the channel and modifies the transistor characteristics
- More relevant for narrow transistors



RADIATION INDUCED SHORT CHANNEL EFFECT (RISCE)

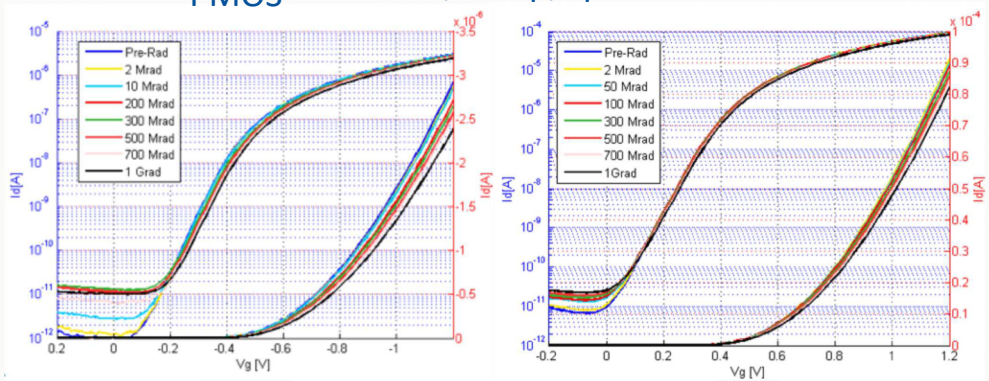
- RISCE is not related to the STI
- May be attributed to the charge induced in the spacer's oxide because of irradiation effects.
- This charge affects the electric field and then the surface potential in the LDD (Lightly Doped Drain)
- More damage for short channel device

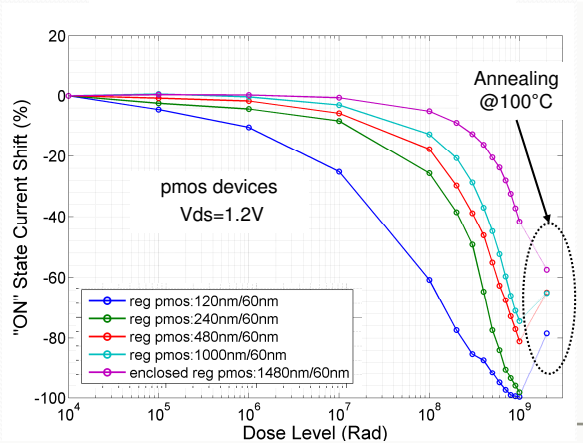


HOW MAKE A 65 NM CMOS CHIP RADIATION TOLERANT?

- Measure precisely the radiation effects (threshold shift, On-state current, leakage current etc.) on transistor level in dependency of temperature, annealing, dose rate etc.
- Parameterize the radiation effects and develop so called “radiation corner models” for all (used) transistor types to be used during the chip verification process
- Follow some simple rules:
  - Avoid the use of narrow and short transistors in analog parts since large size transistors are basically insensitive to TID
  - For digital design modify standard design cell libraries to not use minimum size transistors which are affected most by TID due to RINCE/RISCE
- Monitor radiation effects inside the chip by adding radiation monitor structure (ring oscillators) which can be calibrated to the expected damage
- Still not the whole story: Don’t forget about single event upsets (SEU) and single event effects (SEE)!

PMOS W/L = 1µ/1µ NMOS





RD53 Collaboration is a joint effort between ATLAS and CMS to develop readout chips for the HL-LHC pixel detectors

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ITKPIXV1 DEVELOPED BY RD53

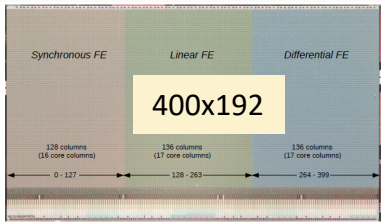
ATLAS ITk

1. Characterization of chosen **65nm CMOS** technology in radiation environment
2. Design of a **rad-hard IP library** (Analog front-ends, DACs, ADCs, CDR/PLL, high-speed serializers, RX/TX, ShuntLDO, …)
3. Design and characterization of **half-size pixel chip demonstrator (RD53A)** with design variations
4. Design of pre-production (**RD53B**) and production (**RD53C**) pixel readout chips

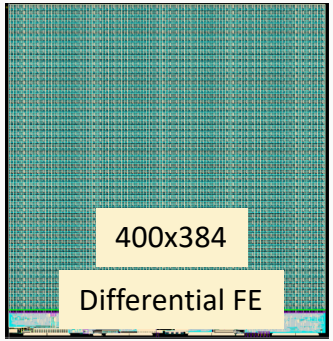
- **ATLAS and CMS chips are two instances of the same common design**, having different size and
- Analog Front-End, according to specific requirements of the experiments

	ATLAS/CMS
Chip size	20x21mm²/21.6x18.6mm²
Pixel size	50x50 µm²
Hit rate	3 GHz/cm²
Trigger rate	1 MHz/750kHz
Trigger latency	12.5 us
Min. threshold	600 e-
Radiation tolerance	500 Mrad @-15C
Power	< 1W/cm²

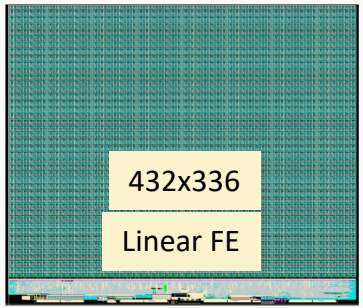
https://cds.cern.ch/record/2663161



RD53A
- submitted in August 2017
- Size: 20 x 11.5 mm2



RD53B-ATLAS (ItkPix_V1)
- submitted in March 2020
- size: 20 mm x 21 mm



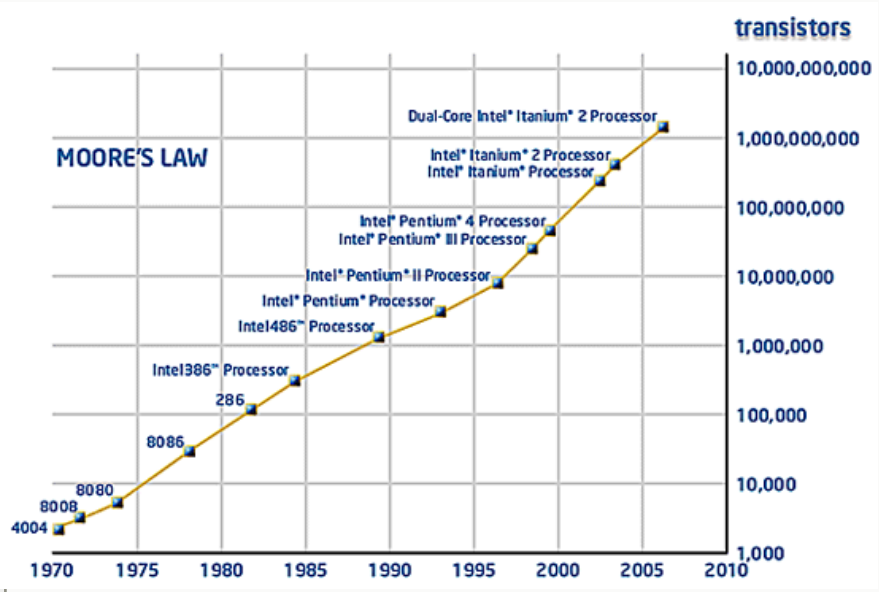
RD53B-CMS (CROC_V1)
- submitted in June 2021
- size: 21.6 mm x 18.6 mm

RD53B

RD53C-ATLAS: Q1 2022
RD53C-CMS: Q2-Q3 2022

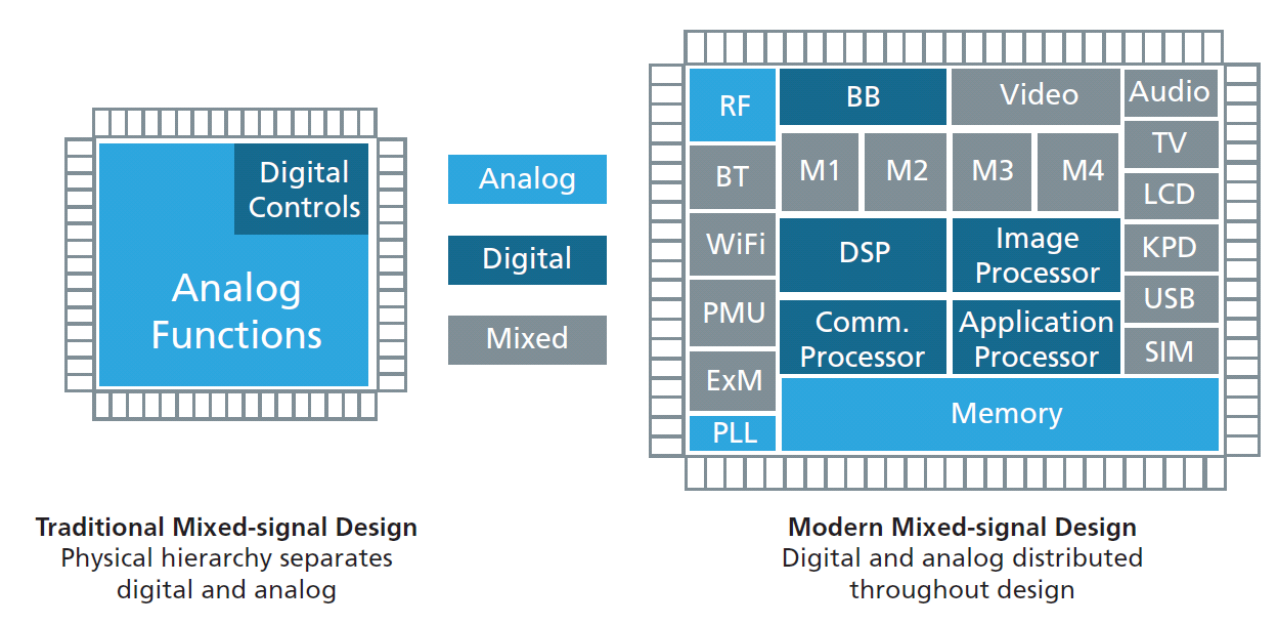
MOORE'S LAW IN HEP

- HEP chips are getting more complex, powerful and bigger → more digital



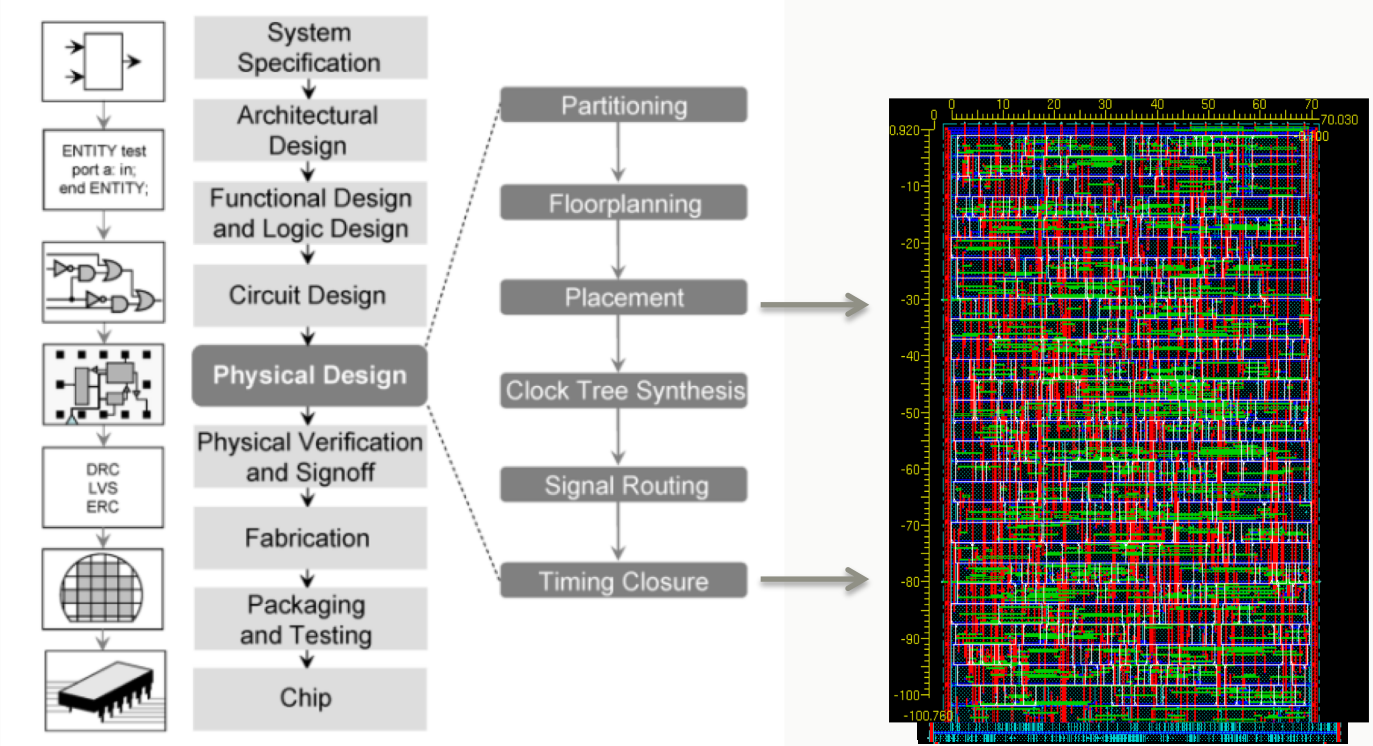
Name	D-OMEGA Ion	LHC1	FE-I3	FE-I4	RD53A	RD53B
Year	1991	~1996	~2005	~2011	2017	2020
Technology Node	3 µm	1µ	0.25 µm	0.13 µm	65 nm	65 nm
Chip size	8.3x6.6 mm^2	8x6.35 mm^2	10.8x7.6 mm^2	10.2x19 mm^2	20x10m m^2	20x20mm^2
Pixel size	75x500 μm^2	50x500 μm^2	50x400 μm^2	50x250 μm^2	50x50 μm^2	50x50 μm^2
Pixel array	16x63	16x127	18x160	80x336	400x198	400x396
Transistor count	???	800k	3.5M	80M	311M	600M

GENERAL DESIGN STRATEGY: SWITCH TO BIG "D", LITTLE "A"



- RD53A and RD53B are essentially full digital ASICs with anolog islands for in-pixel amplification, IO and powering

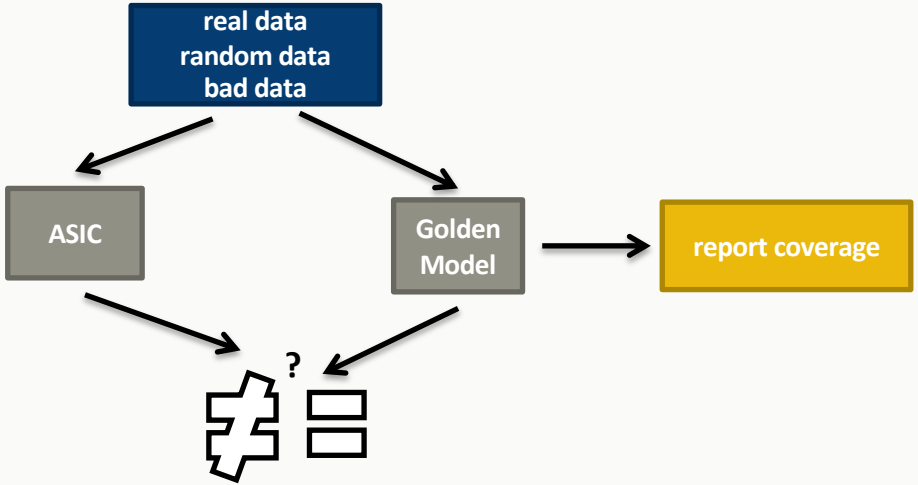
DIGITAL IMPLEMENTATION VIA MODIFIED STANDARD DESIGN CELL LIBRARIES



VERIFICATION IS MOST CRITICAL PART

Does not work for custom made analog cells!

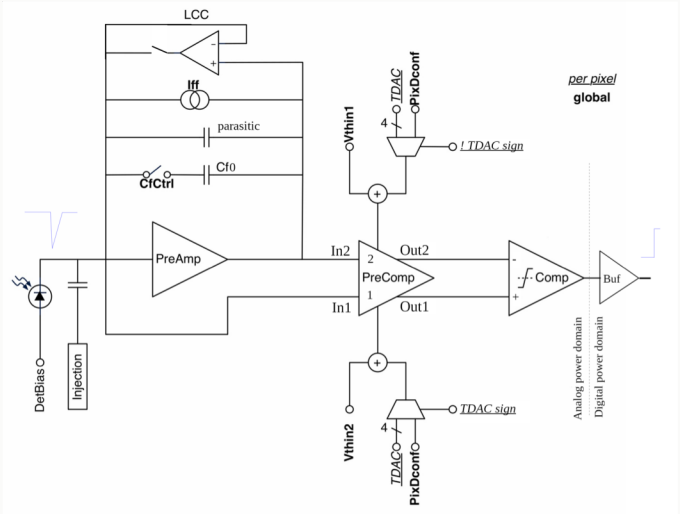
- Verification takes more time then design.
- It has to start before/together with the design.
- Failing a $1M chip (65nm) is not a good idea.
- No way out for complex digital chips.

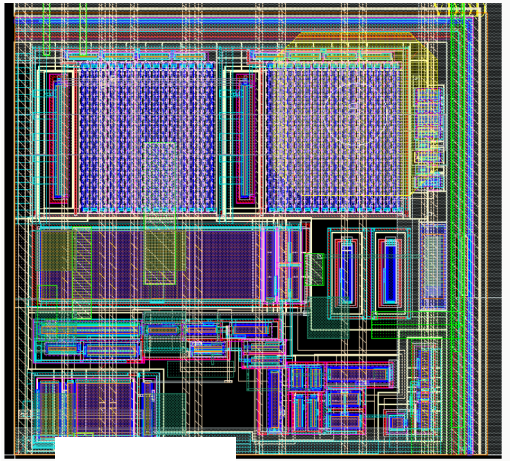


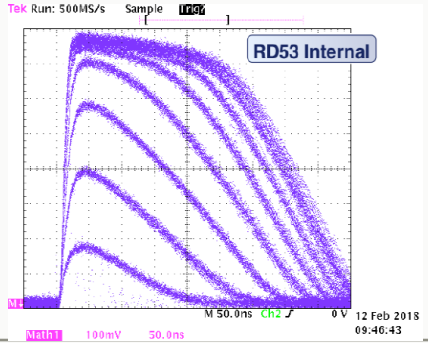
Verification Plan → Most important part (trash in trash out)

ITKPIXV1: DIFFERENTIAL FRONT-END

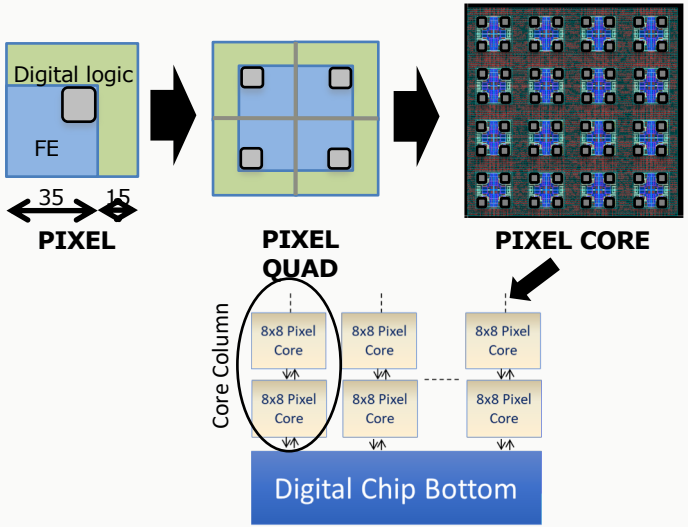
- Charge sensitive amplifier
- Leakage current compensation circuit
- Continuous reset integrator, with tunable feedback current (global setting)
- DC-coupled pre-comparator stage
  - 10-bit DAC for global threshold
  - 4+1 bit local trimming DAC for threshold tuning
- Fully differential input comparator

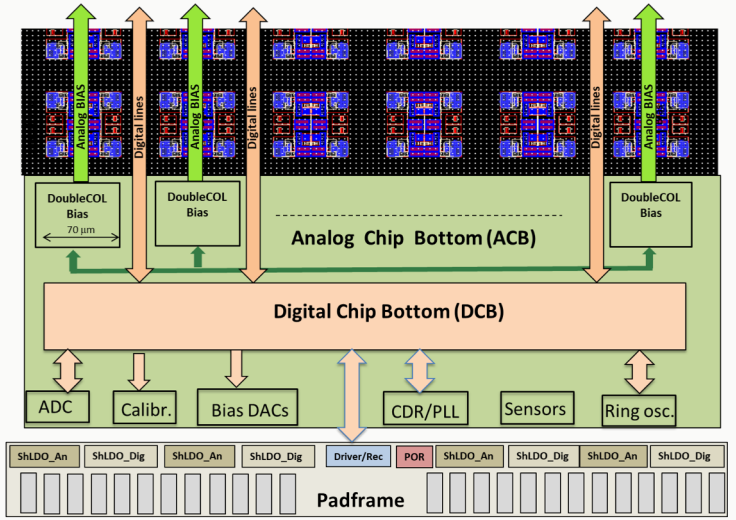






ITKPIXV1: FOORPLAN





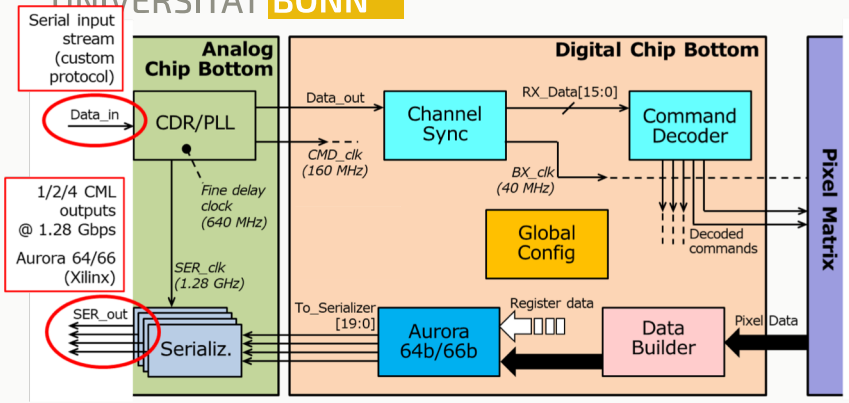
Pixel array:

- Built up of **8 x 8 Pixel Cores → 16 quads**
- All Cores are identical → efficient hierarchical verifications
- Cores are abutted: each Core receives all input signals from the previous one (closer to the DCB) and regenerates them for the next Core → no external routing for connections

Chip periphery:

- Analog Chip Bottom (ACB): analog and mixed/signals building block for Calibration, Bias, Monitoring and Clock/Data recovery
- Digital Chip Bottom (DCB): synthesized digital logic
- Pad frame: I/O blocks with ESD protections, ShuntLDO for Serial Powering

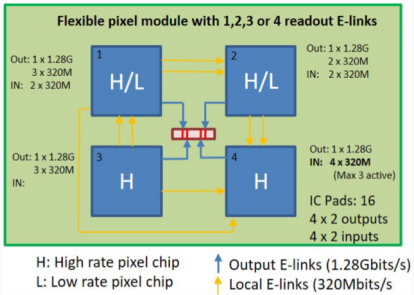
ITKPIXV1: DATA FLOW ARCHITECTURE

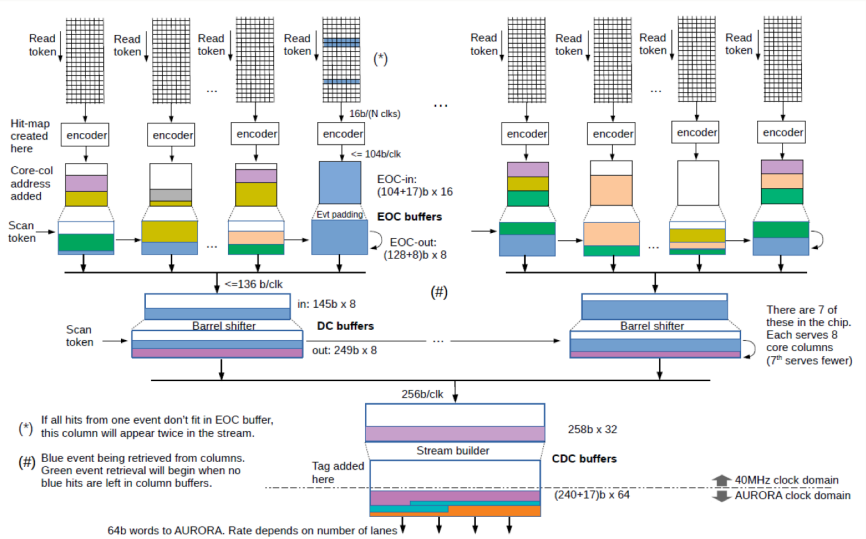


- Hits are stored as Time-over-Threshold, associated to a time stamp
- 6-bit ToT counter, but only 4 bits are stored and read-out
- Each pixel has 8x4-bit ToT memories
  - Support of 6-to-4 ToT mapping (dual slope)
  - Selectable counting clock: 40 MHz or 80 MHz
- The time stamp memory is shared among 4 pixels of the same 4x1 **Pixel Region**

- Token-based readout of hits, organized in Core Columns
- Multiple levels of data processing, event building, buffering and formatting before final readout via serial links

- **Command, control and timing** is provided by a **single 160 Mbit/s** differential control link, driving up to 15 chips (4 bit addressing)
  - CDR/PLL recovers Data and Clock
- **Readout via serial links** (1-4 x 1.28 Gbit/s) using Aurora 64/66 encoding
- **Multi-Chip Data Merging** available for low-rate outer pixel layers: one chip of the module can be configured as "primary" to aggregate serial data from one or more other "secondary" chips and merge them with its own output

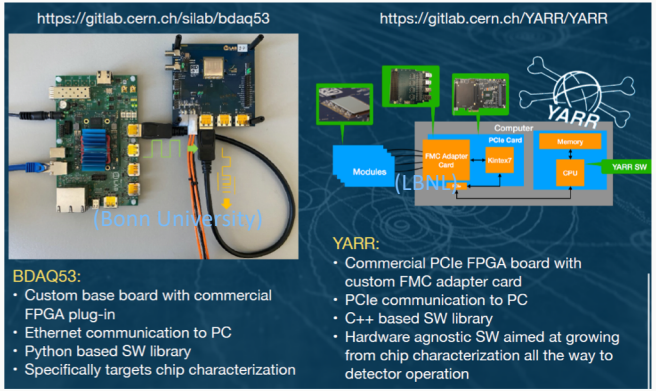




(*) If all hits from one event don't fit in EOC buffer, this column will appear twice in the stream.

(#) Blue event being retrieved from columns. Green event retrieval will begin when no blue hits are left in column buffers.

ITKPIXV1 TESTING

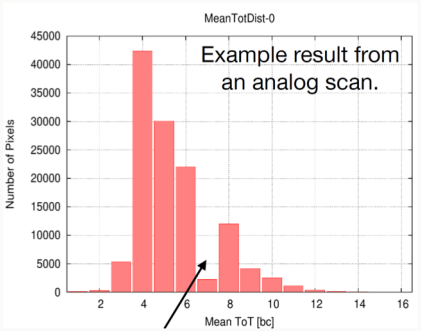


Upon first power-on, we observed an **abnormally large digital current (2-3A instead of 200mA)**

- Bug in the design of the custom 4-bit latch used to implement the ToT memory to save ~ 50% memory area, otherwise all the required functionalities could not fit in the constrained pixel area
- high current consumption when inputs differ from stored values in latched state. Since at power-up the latch state is random, this results in large current consumption upon power-up
- also causing corruption of stored ToT values when multiple bits are "1"

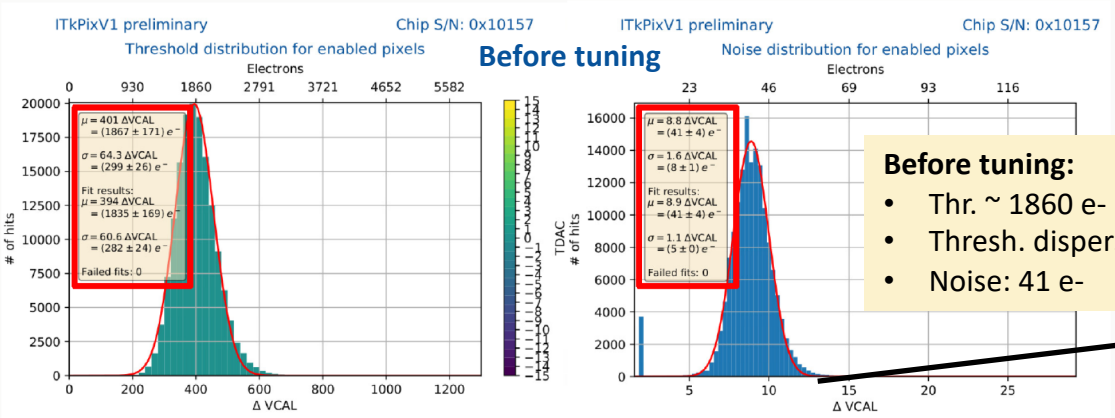
Despite this problem, **most blocks and all digital functionalities can be tested in this version:**

- setting all ToT memories to '0000', the chip is set in normal current state
- Analog front-end can be characterized using the precision ToT feature
- Radiation and SEU test could be performed
- Only limitation: high power-up current makes it impossible to use this chip for system testing of power chains
- High current issue solved by a patch in metal layers applied to 4 wafers being held at foundry without metallization → ATLAS ITk Pixel pre-production will rely on this patched chip **ITkPixV1.1**



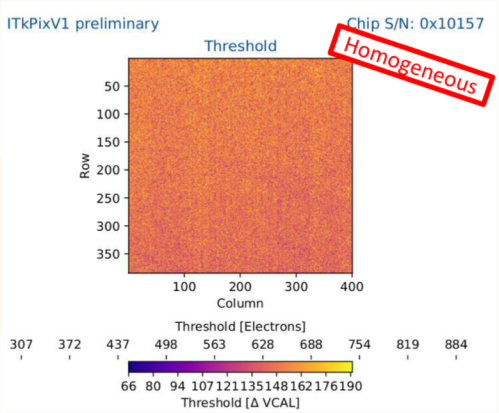
Missing hits for ToT=7

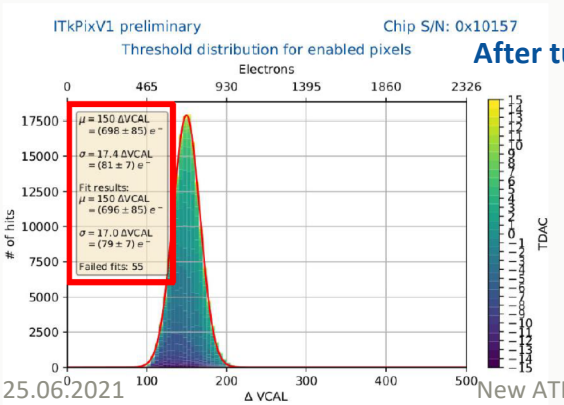
ITKPIXV1 FRONT-END THRESHOLD TUNING AND NOISE



Before tuning:

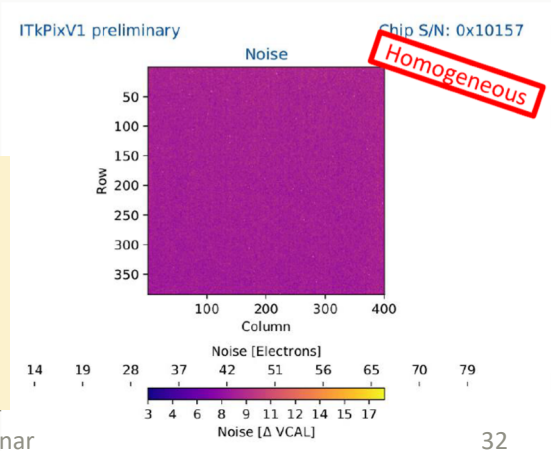
- Thr. ~ 1860 e-
- Thresh. dispersion: ~ 300 e-
- Noise: 41 e-



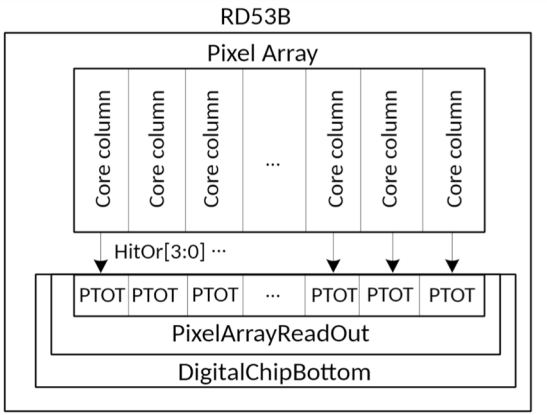


After tuning:

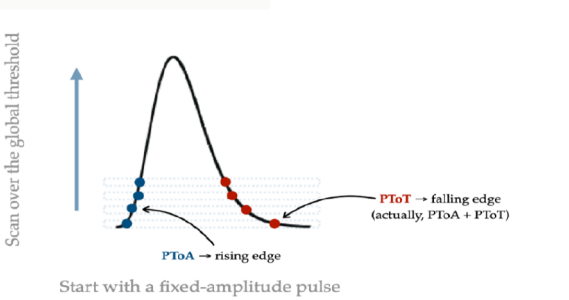
- Thr. ~ 700 e-
- Thresh. dispersion: ~ 80 e-
- Noise: 40 e-
- Noise increases by ~20 e- with sensor



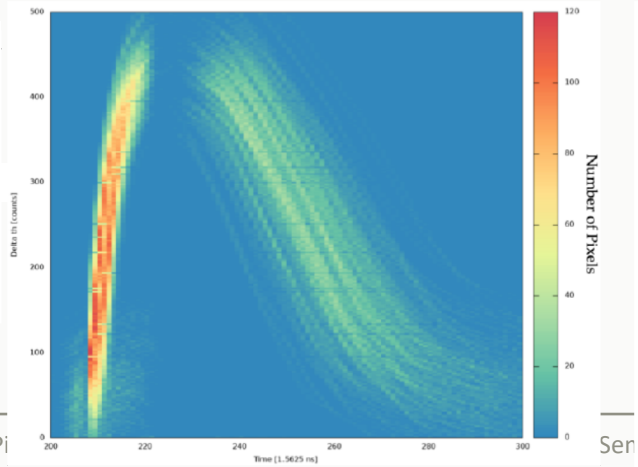
ITKPIXV1: PRECISION TOT AND TOA

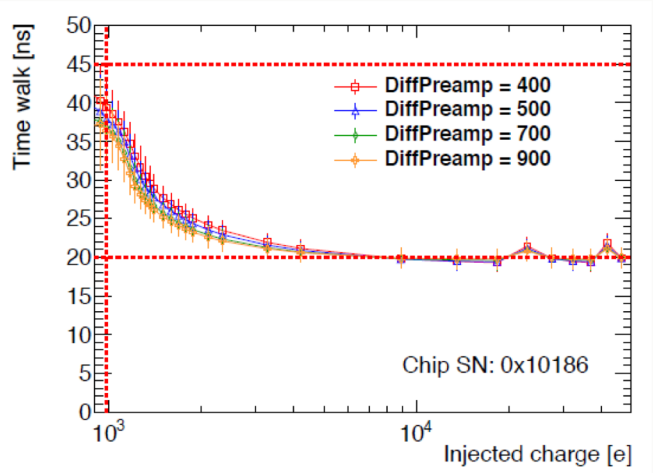


- PTOT module can be used for high resolution **Time over Threshold** and **Time of Arrival** measurement of the HitOR lines, using 640 MHz counting clock (1.5625ns resolution)
  - 11-bit PToT counters
  - 5-bit PToA counters, measuring the phase difference from HitOr leading edges and next BX clock rising edge
- Each Core Column is equipped with a PTOT module. Can be triggered for readout via the normal path, just like a Pixel Core
- Can be used to make precision measurements of analog front-end, like time walk, and also as a workaround for the bug in the pixel ToT memory
- Allows to reconstruct the amplifier output waveform (sort of oscilloscope)



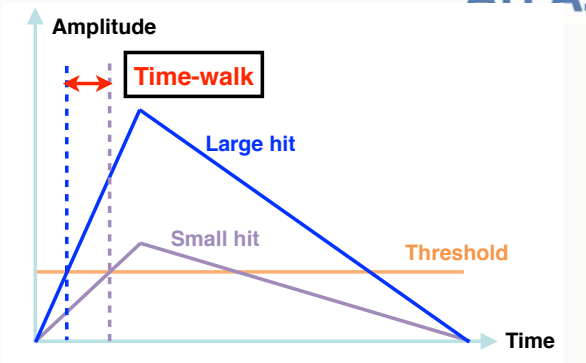
- Inject fixed calibration pulse
- Scan the threshold
- Sample PToA and PToT at each step

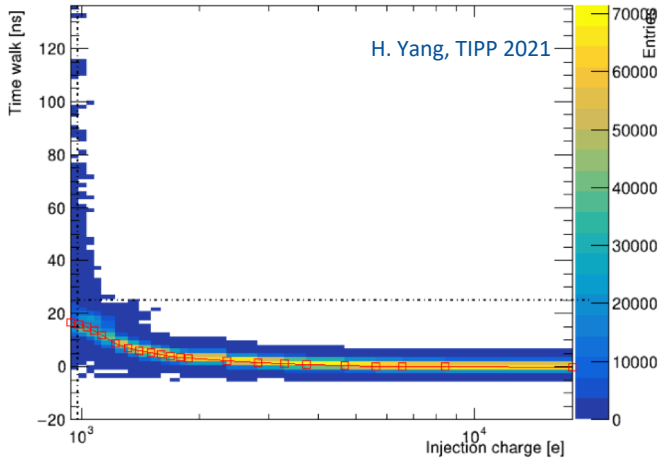




ITKPIXV1: TIME-WALK

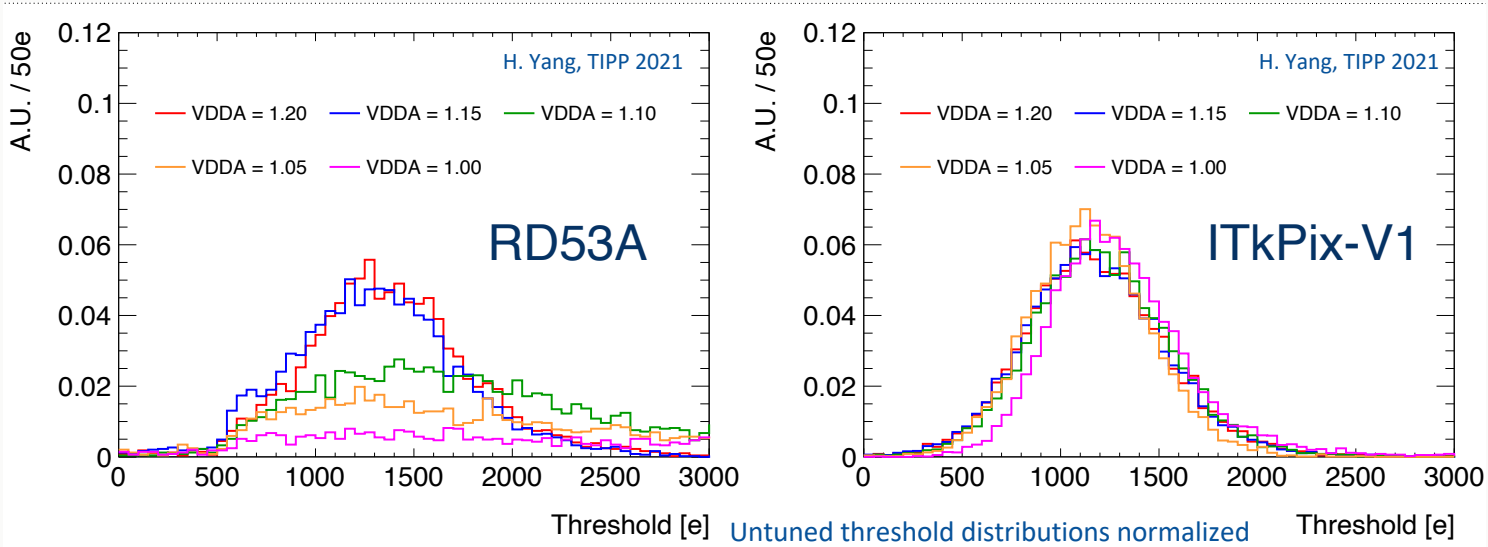
- Time-walk: ToA difference between a small and a very large signal injection
- LHC bunch crossing frequency is 40 MHz, so there are 25 ns before the signal gets assigned to wrong bunch crossing
- ITkPix-V1 differential analog FE time-walk **is well below 25 ns** on bare chip (to be revisited with a sensor attached)





Pixel threshold tuned to 1000e$^-$ on a bare chip

ITKPIXV1 VS. RD53A: RADIATION TOLERANCE



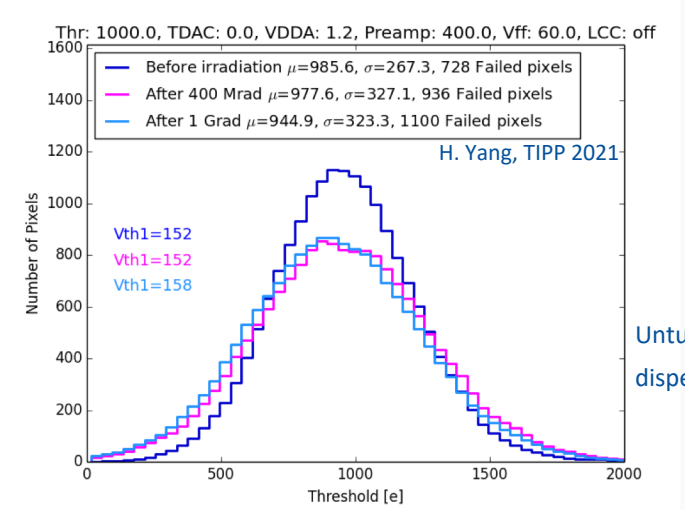
Untuned threshold distributions normalized to total number of good pixel

- Use low temperate (-40°C) and low VDDA to emulate radiation effect
- When RD53A stops working, ITkPix-V1 threshold distribution remains sharp at reduced VDDA

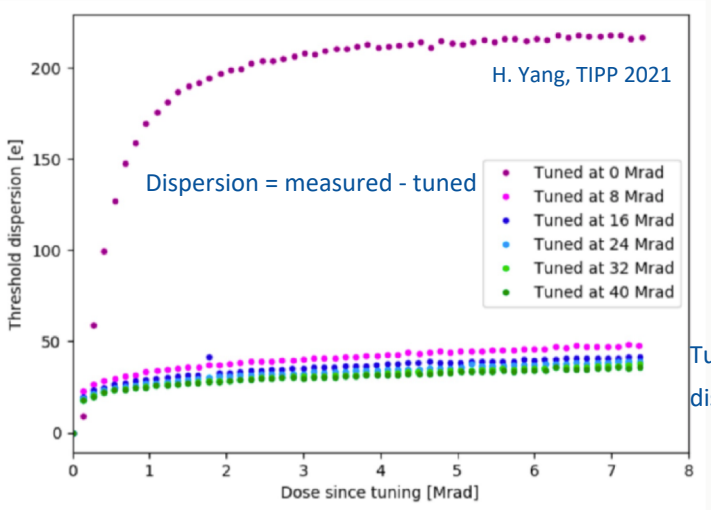
→ **ITkPix-V1 analog FE is more radiation tolerant than RD53A!**

ITKPIXV1: X-RAY IRRADIATION STUDIES

- X-ray machines are used to irradiate bare chips with high-dose rates (HDR: 4 Mrad/h) at low temperature (-20°C) and measure basic analog chip functions
  - Note: measurements on ring oscillators (RD53A and B) suggests that TID damage is roughly 2 x larger for low-dose (LDR) as in the experiment!
- **Chip is operable and analog performance is good until a HDR TID of 1 GRad (10 MGy) at cold temperature**
- Threshold dispersion increases rapidly at low radiation dose, then become stable
  - Need to monitor chip tuning closely at the beginning of HL-LHC data taking



Untuned threshold dispersion

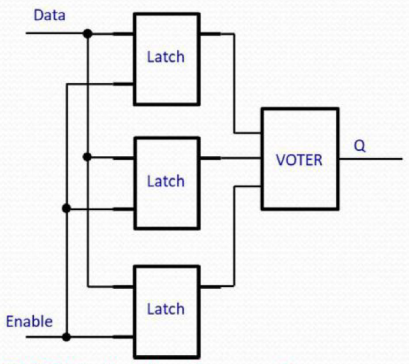


Tuned threshold dispersion

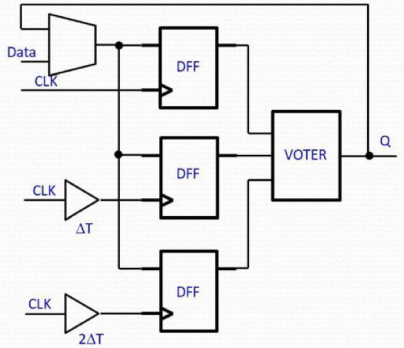
ITKPIXV1 RADIATION TOLERANCE: SEU

Adopted strategy for SEU mitigation

- The chip is protected with Triple Modular Redundancy (TMR) with the exception of the data path
- Pixel configuration registers: TMR without self-correction (limited area in pixel)
- Global configuration and state machines in the chip periphery: TMR with self-correction and triplicated clock tree with skew for SET filtering
- Only synchronous reset
- Possibility to "reset" the PLL without power cycling the chip
- Analog SEU/SET injection simulations on some critical blocks (PLL)
- Digital SEU injection in the digital logic on the gate-level netlist



TMR latch without correction



TMR with correction

SEU tests on ITkPixV1: 3 chips with heavy ions and 1 with 480 MeV protons (Louvain-la-neuve, GANIL, TRIUMF)

- No latch-up, no chip-stuck (no need of resetting or power cycling)
- evaluate the register cross-sections:
  - Unprotected latch ~1.5×10^{-14} cm^2/bit
  - Pixel configuration register (TMR without correction): gain factor between 10 to 100, depending on the refresh rate (error accumulation)
  - TMR latch with correction: 400 times more tolerant than the unprotect one
  - **Triplication in global configuration seems to be efficient**
- Possible SET issue on readout link, under study for possible improvements in the final chips

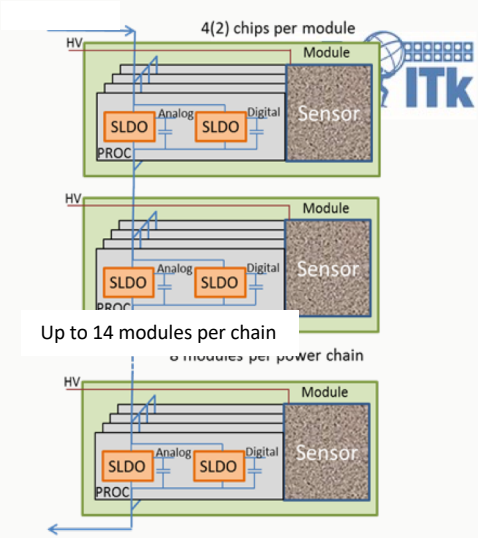
Further SEU test campaigns are needed:

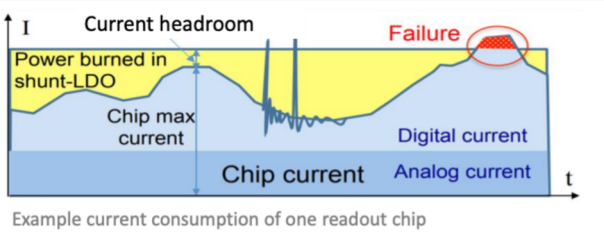
- Test for higher trigger rate
- Test for high hit rate
- Test of the communication and effects of the CDR/PLL SEE on the whole chip

ITKPIXV1: SHUNTLDO FOR SERIAL POWERING

ATLAS and CMS will adopt for the upgrade pixel detectors a **serial powering scheme:**

- **ShuntLDO** regulators in the readout chips (1 for Analog, 1 for Digital domain)
- **Constant input current I_{in}** is shared among chips (2÷4) on the same module (less cables)
- Modules are in serial chains: "recycle" current from one module to another
- I_{in} dimensioned to satisfy the highest load, with ~20% headroom for stable operation, absorbed by the Shunt device
- In case of chip failure, its current can be absorbed by the other chips of the module
- Not sensitive to voltage drops (low mass cables)
- On-chip regulated supply voltages, low noise
- Radiation hardness (> 500 Mrad) silicon proven
- **ItkPixV1 testing show that ShuntLDO works well and system tests with pixel modules have started**

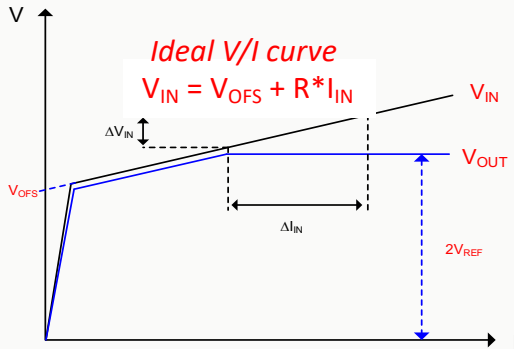




Example current consumption of one readout chip

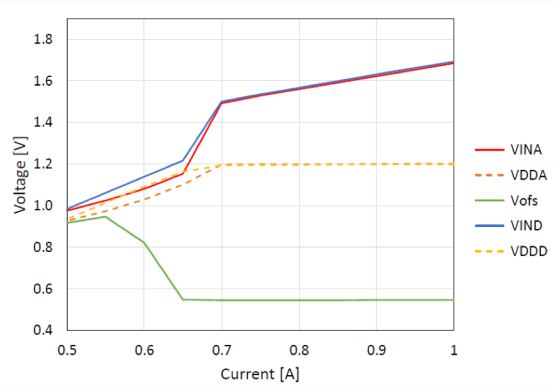
Protections:

- *Over-voltage protection*: V_{IN} clamped to 2 V
- *Under-shunt protection*: V_{OUT} decreased in case shunt current goes below a certain threshold (due to excess load current)



- V/I curve parameters (Voffset, slope) defined by external resistors
- V_{OUT} tunable by chip configuration

ITkPixV1.1 measurement at room T, pre-rad

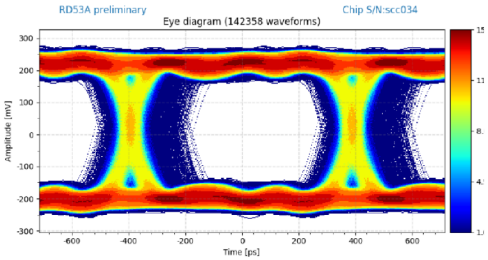


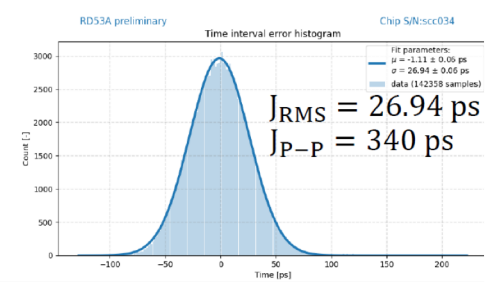
ITKPIXV1: DATA TRANSMISSION CDR/PLL

- Clock-Data-Recovery (CDR)/Phase Locked Loop (PLL) greatly improved compared to RD53A in terms of jitter and start-up reliability
- Aurora output link stable with good quality

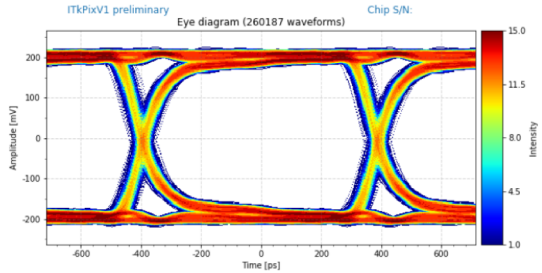
Input jitter = 5ps rms

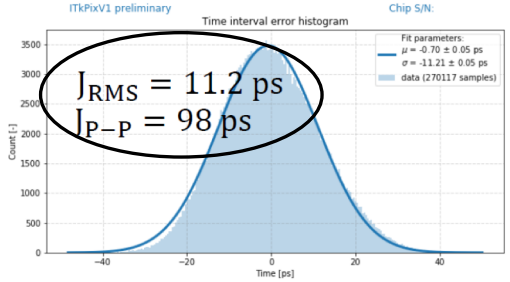
- **RD53A**
- Input: Threshold scan
- Output: Aurora (1.28 Gbps)



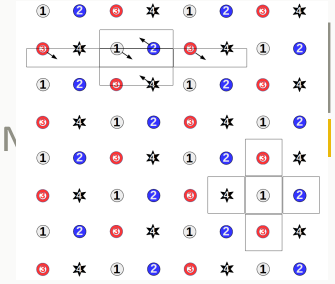


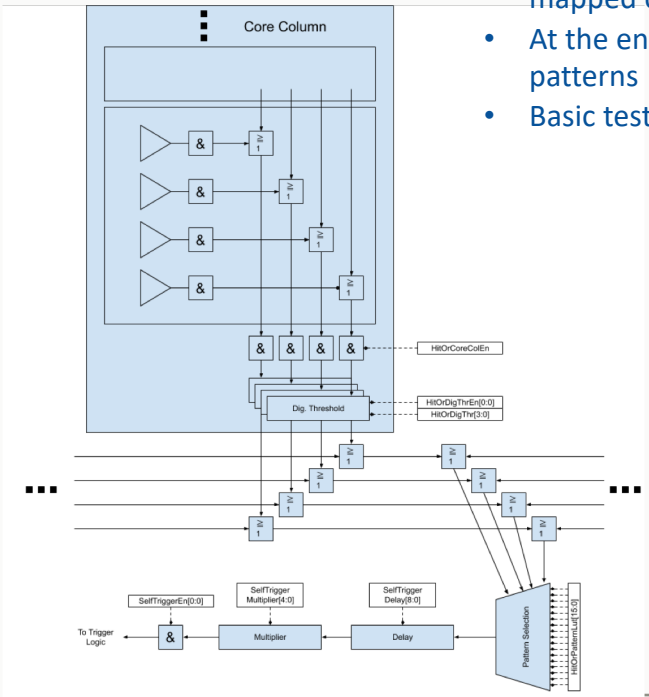
- **ITkPixV1**
- Input: PRBS5
- Output: Aurora (1.28 Gbps)



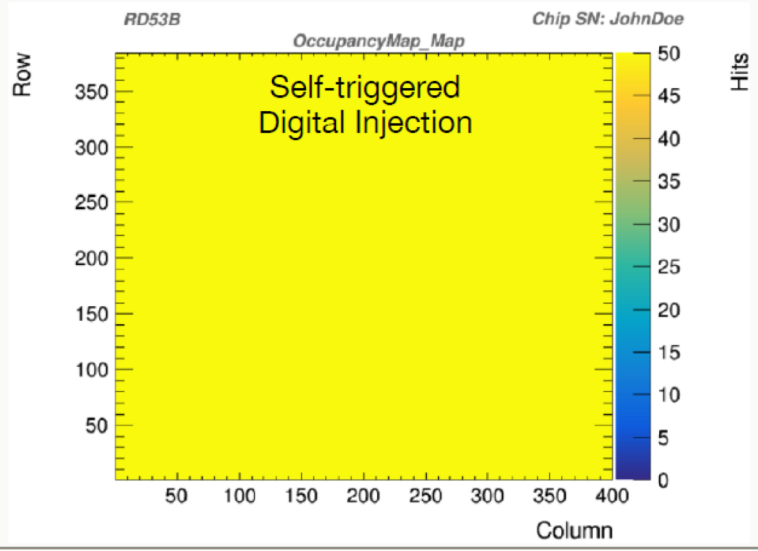


ITKPIXV1: SELF TRIGGER FOR TEST & DEBUGGING



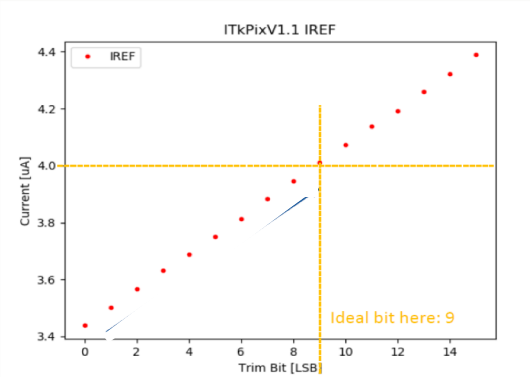


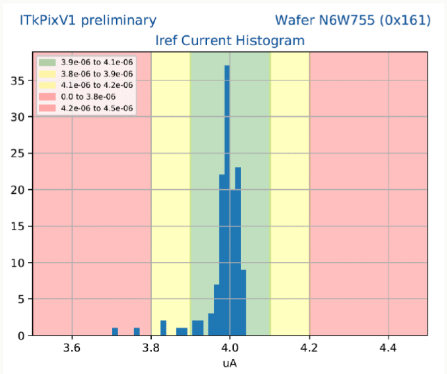
- Flexible auto trigger function, based on a Hit-OR network from the pixel array
- Hit-OR network consists of 4 OR lanes per Core Column, with a mapping such that neighbor pixels are mapped on different lines
- At the end of Core Column, the 4 lanes are combined to build the global Hit-OR with programmable patterns
- Basic testing with digital injection show that is **working as expected**

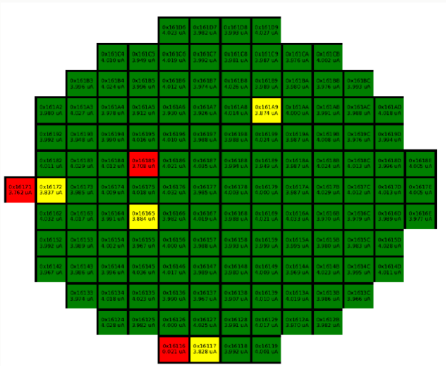


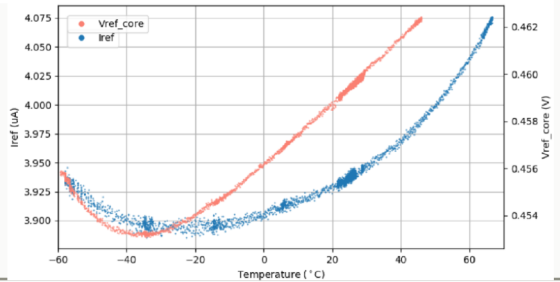
ITKPIXV1: BIAS CIRCUIT

- BIAS network is based on Bandgap reference circuits, to provide a reference voltage/current with low sensitivity to temperature variations
- Tuning by means of 4 wire-bond trimming pads (no risk of SEU bit flips), whose optimal value is found during **wafer probing**
- The tuned current I_{ref} is replicated and used as reference to 23 Digital-to-Analog converters to bias the analog Front-end, the CDR and other IPs

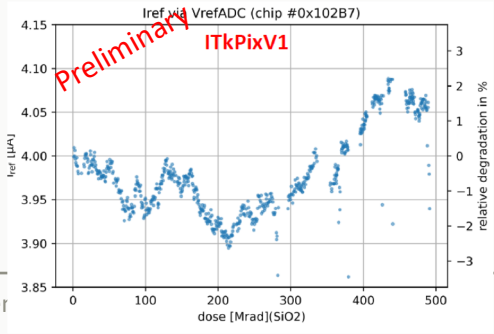






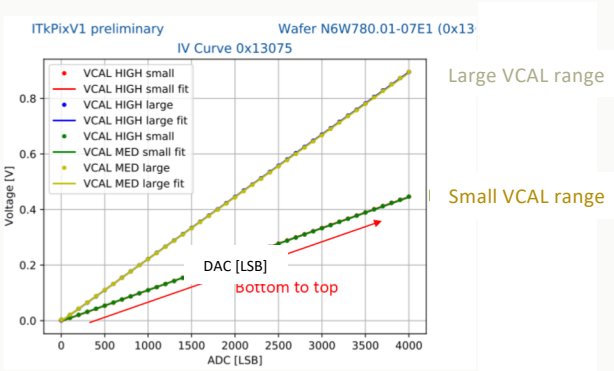


4% difference over 120°C temp. range



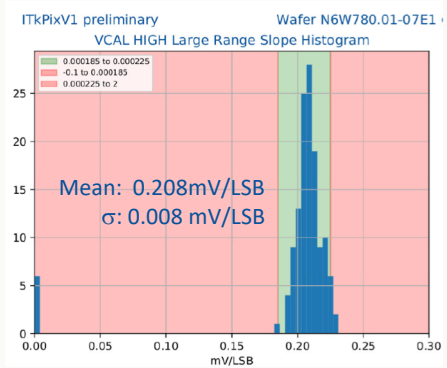
ITKPIXV1: CALIBRATION CIRCUIT

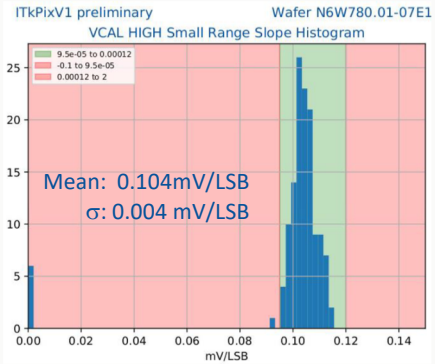
- Each pixel is equipped with a calibration injection circuit for test and calibration purpose
- The analog injection uses two distributed voltages, provided by two 12-bit voltage DACs, to generate a precise voltage step fed to an injection capacitor
- Two selectable ranges



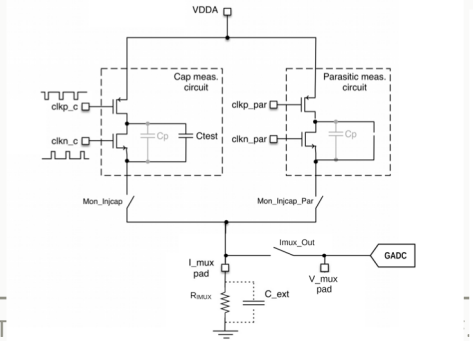
Large VCAL range

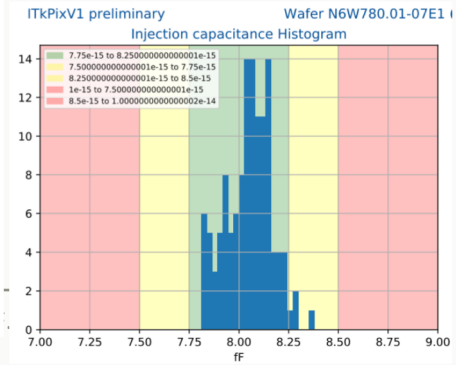
Small VCAL range





- Possibility to measure the value of injection capacitor using a dedicated circuit

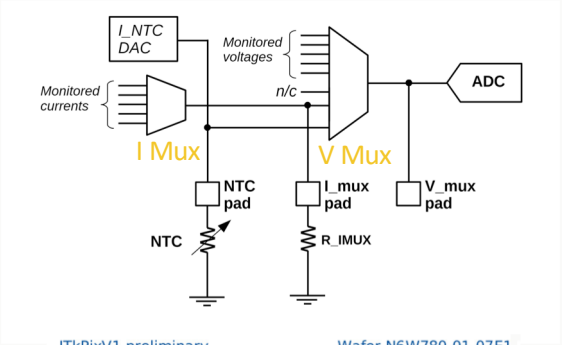


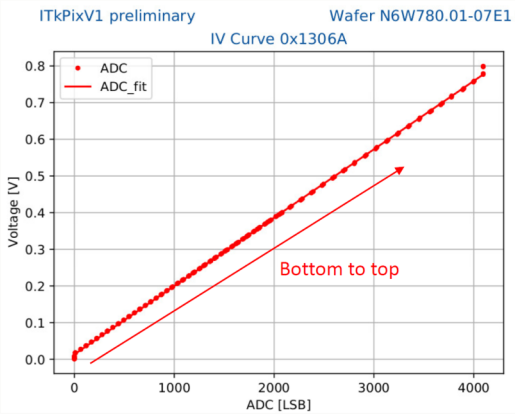


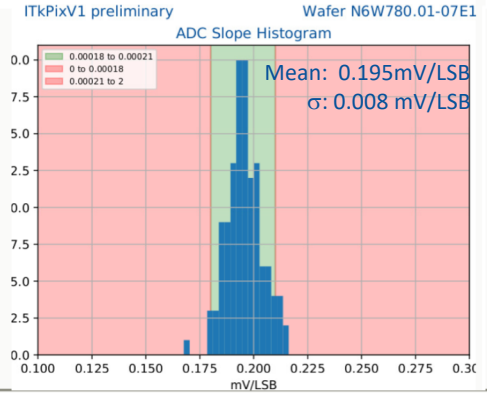
Mean: 8.05 fF (expected 8.02 fF)
σ: 0.11 fF

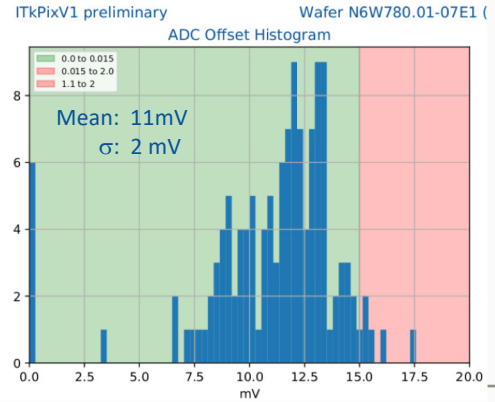
ITKPIXV1: MONITORING BLOCK

- The Monitoring block enables digitization and readout of internal parameters (T, voltages and currents from different parts of the chip)
- Consists of a current mux, a voltage mux and a 12-bit Analog to Digital Converter (ADC)
- Monitoring can be performed at any time, also during data-taking, via the normal data output links
- 5 temperature sensors in different positions
- Ring oscillators → measurements of digital cells speed degradation with TID









SUMMARY

- The readout chips for the ATLAS and CMS HL-LHC pixel detectors are being developed by the RD53 Collaboration
- RD53B is a configurable design in CMOS 65nm technology implementing the same chip in two versions having different sizes and different analog Front-ends
- RD53B-ATLAS (ITkPixV1) was submitted in March 2020. A bug in the ToT memory did not prevent its characterization, apart from some system tests
- A patched chip (ITkPixV1.1) was submitted to solve the high current issue. It will be used for ATLAS ITk pre-production and majority of system testing with sensor assemblies
- **All measurements up to now indicate that the chip is generally working fine**, with few other minor bugs that have been fixed for next submissions. X-ray and SEU irradiations are ongoing.
- RD53B-CMS (CROCv1) was submitted in June 2021. In addition to fixes for all known bugs, it also contains some additional features to improve calibration, monitoring and diagnostic. These will be present also in the ATLAS production chip
- Final production chips will be submitted in first half of 2022, after RD53B chips have been thoroughly tested at chip and system level