Single Programming Model to Deliver Cross-Architectural Performance

oneAPI Product for Intel® FPGAs:
Industry Initiative + Intel Products

Intel Programmable Solutions Group (PSG)
March 2021

A Unified Programming Model

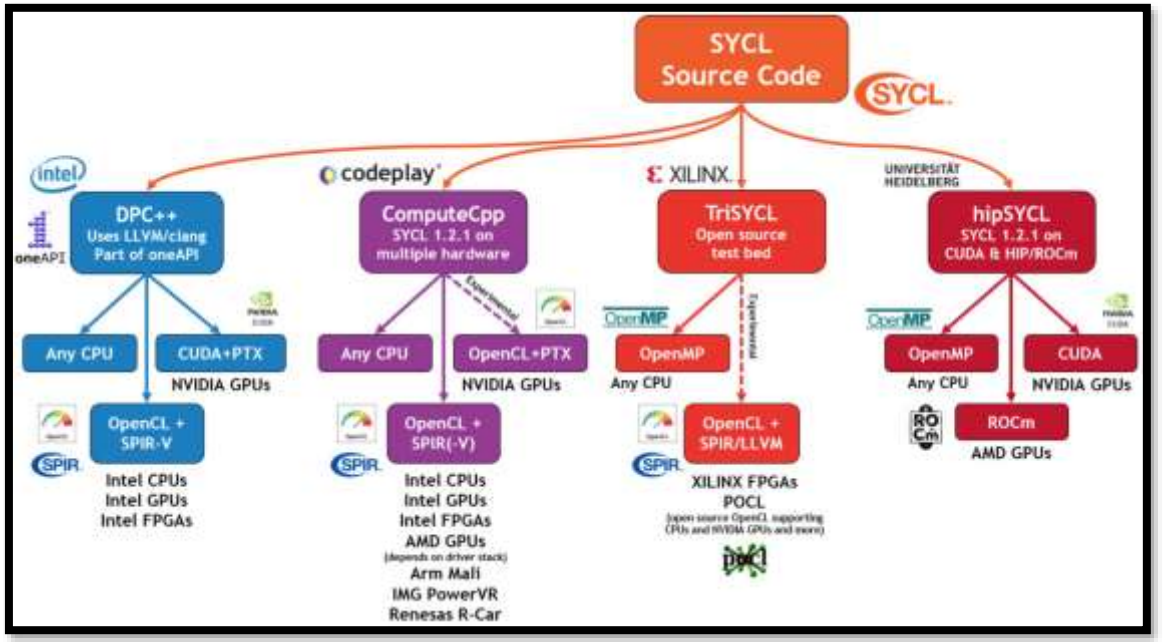
Multiple Architectures

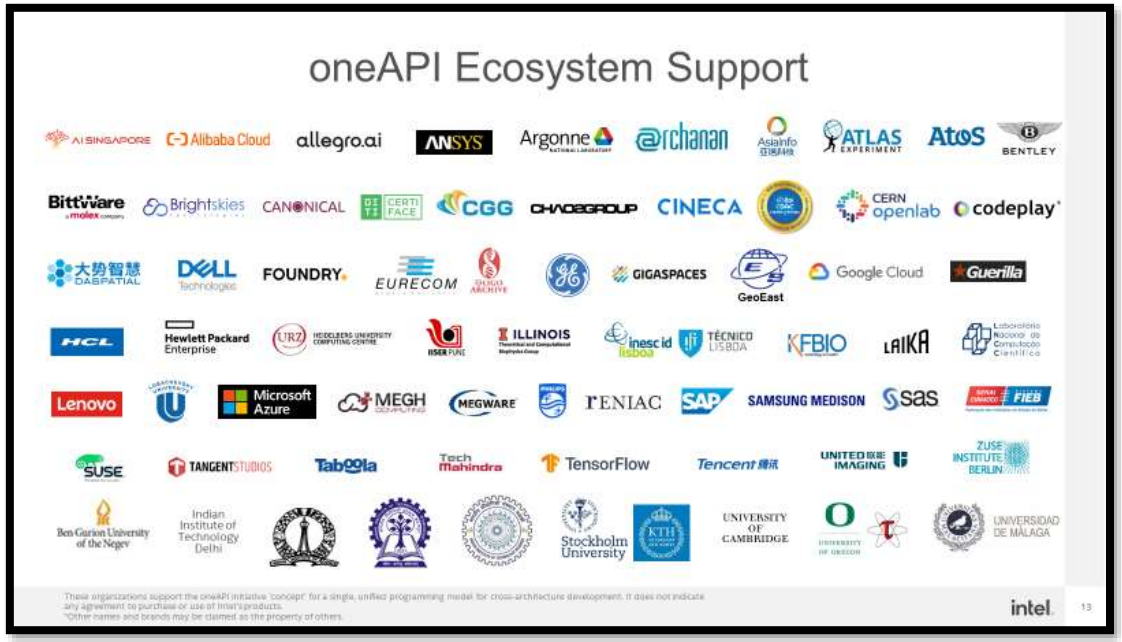
The **oneAPI** product delivers a unified programming model to simplify development across diverse architectures.

It guarantees:

- **Common developer experience** across Scalar, Vector, Matrix and Spatial architectures (CPU, GPU, AI and FPGA)
- Uncompromised native high-level language **performance**
- Industry standardization and open specifications

SYCL and oneAPI Product Ecosystem





Source: https://www.khronos.org/sycl/

Intel oneAPI Product

Faster Development

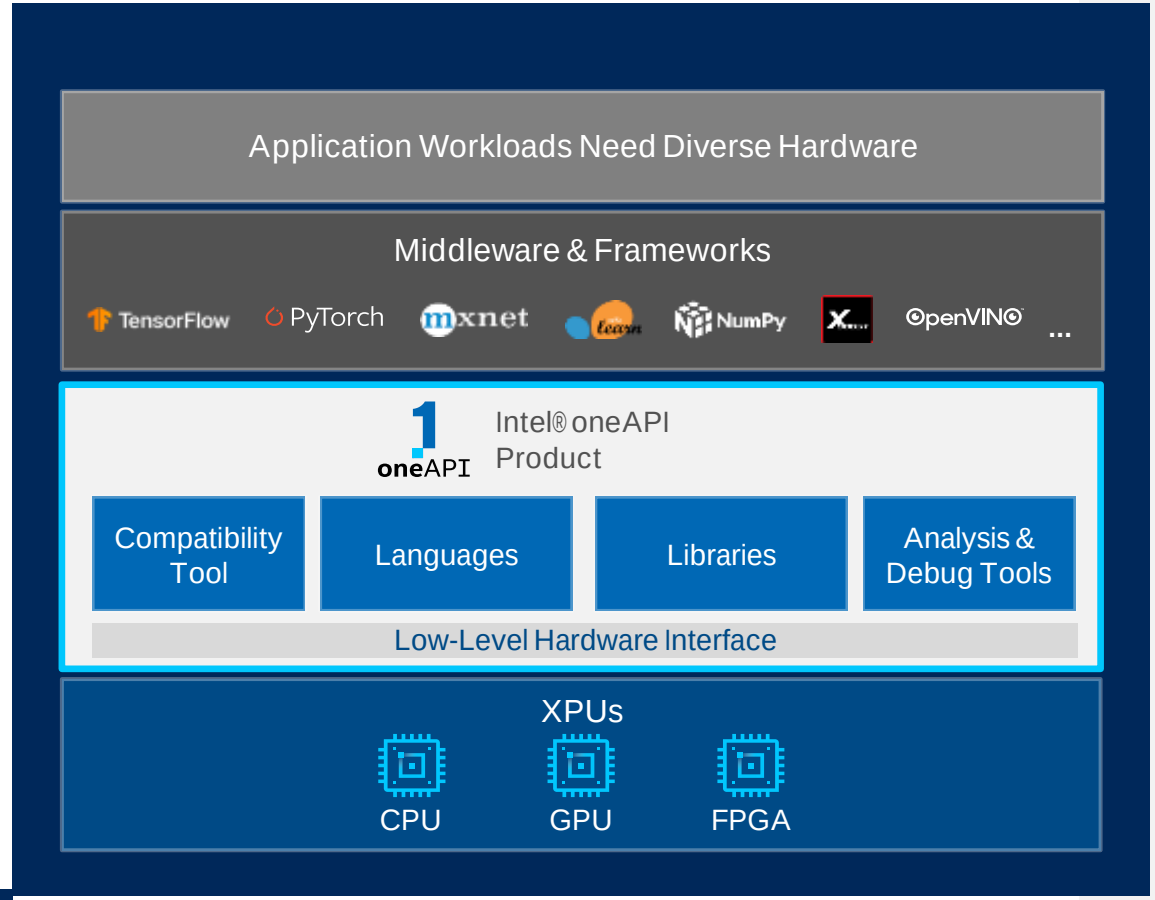
- Performance tuning and timing closure through **emulation** and **reports**.
- Runtime analysis via **VTune™ Profiler**
- Complex hardware patterns implemented through built-in language features: **macros**, **pragmas**, **headers**

Extensible Code

- **Code re-use** across architectures and vendors**.**
- Compatible with existing high-performance languages.

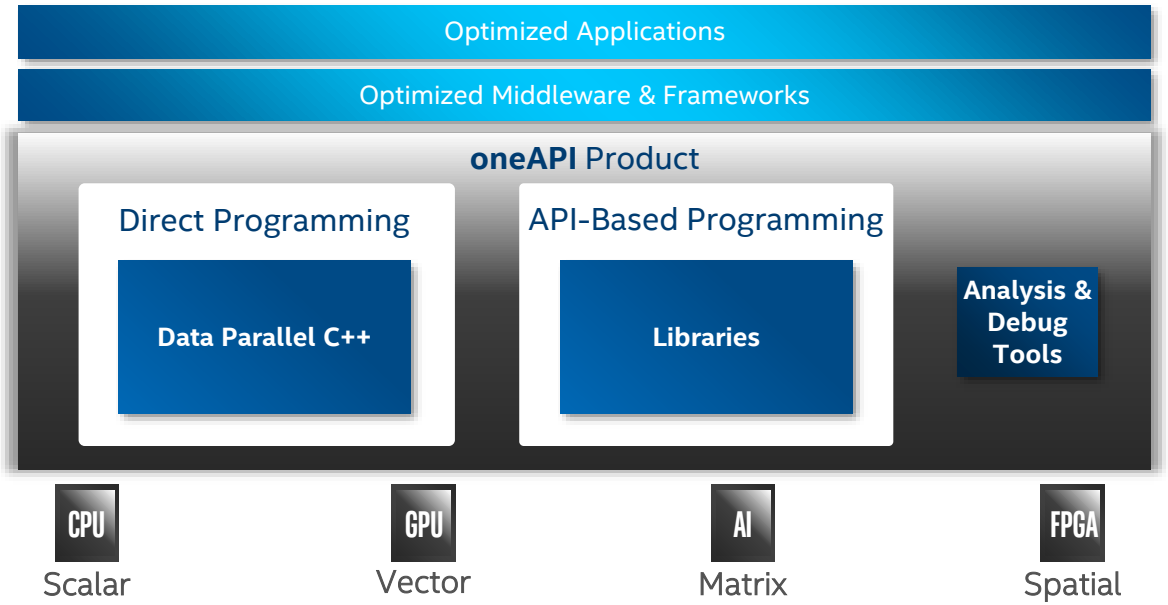
Reduced Barrier of Entry

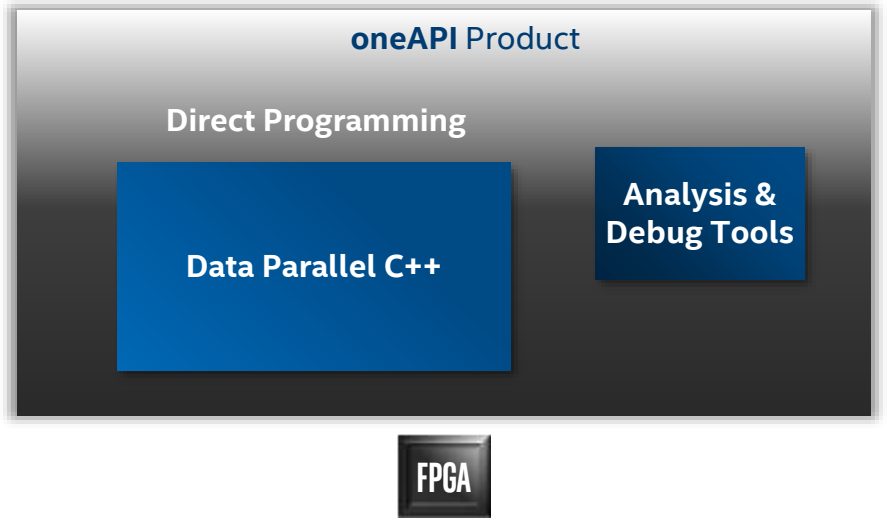
- Leverage familiar sequential programming languages: improved **ramp-up** and **debug** time.
- IDE Integration: **Eclipse, VS, VS Code**

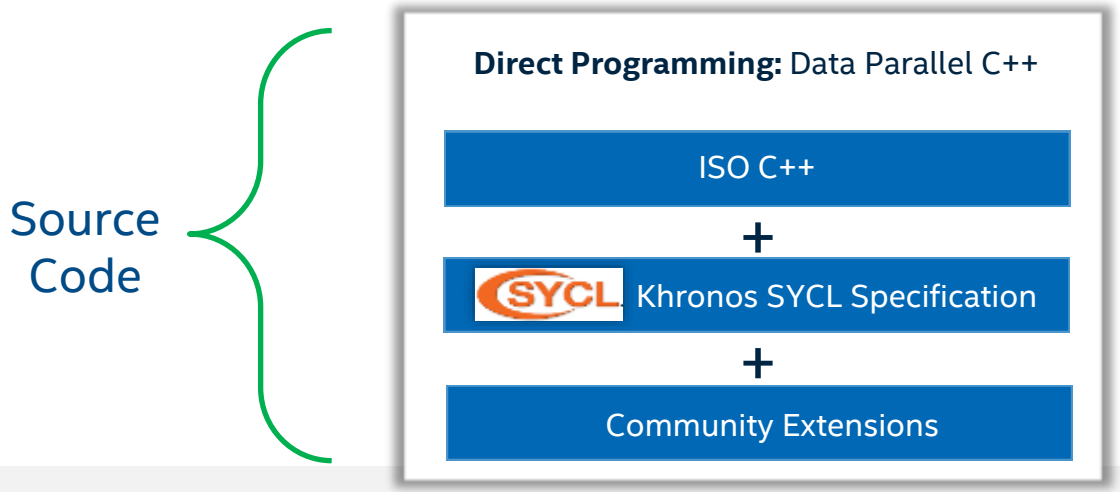


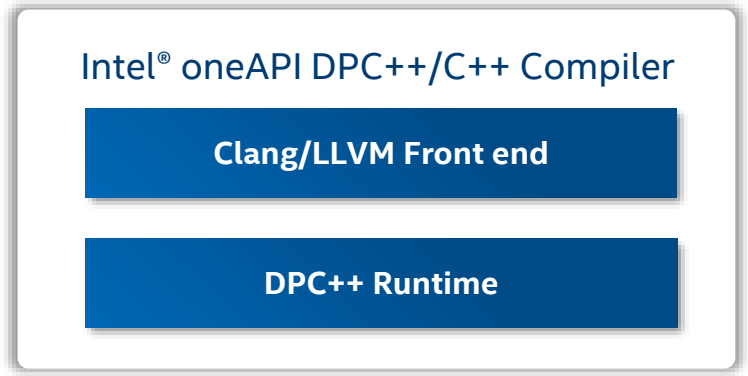
Available Now

Intel® oneAPI Base Toolkit for FPGAs

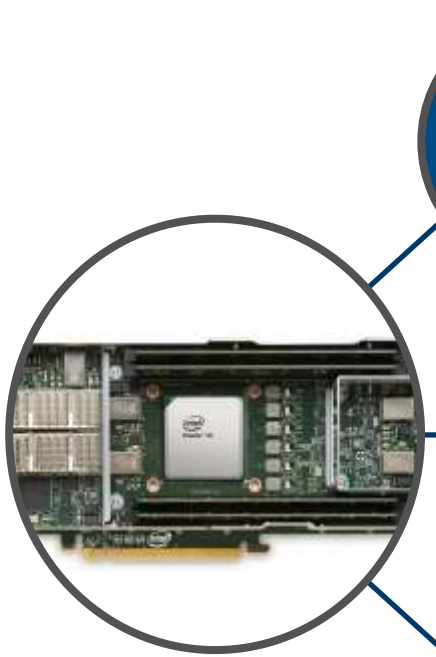








Value of the FPGA Made Easy!



Spatial Architecture

- Data-dependent parallelism
- Streaming and graph processing patterns

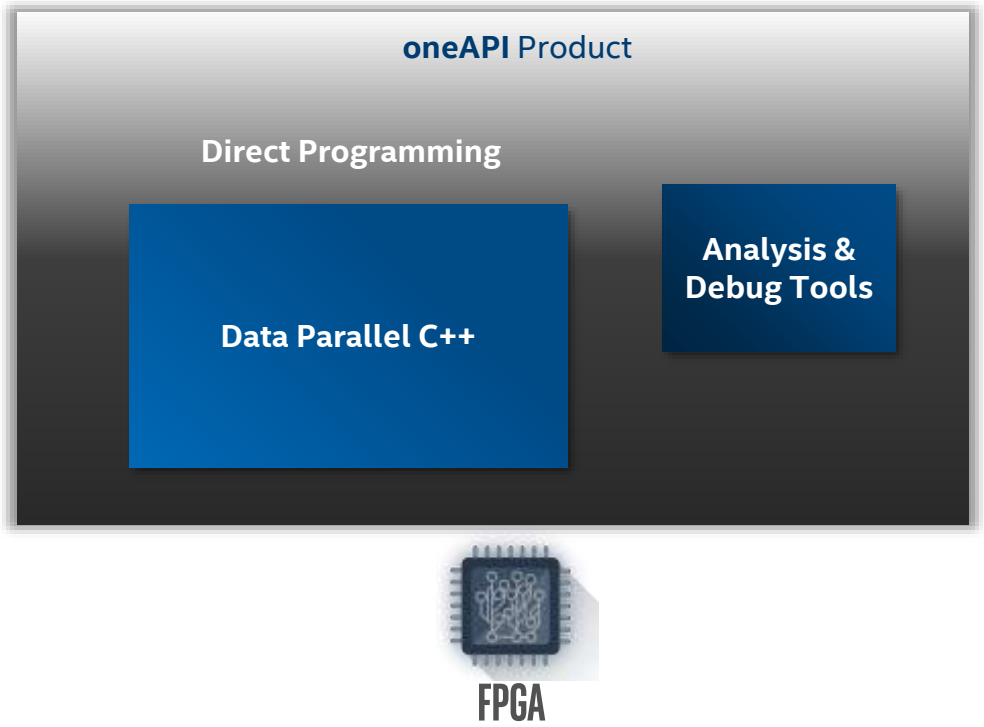
Rich I/O

- Low and deterministic latency
- Customizable network interfaces and protocols

Memory

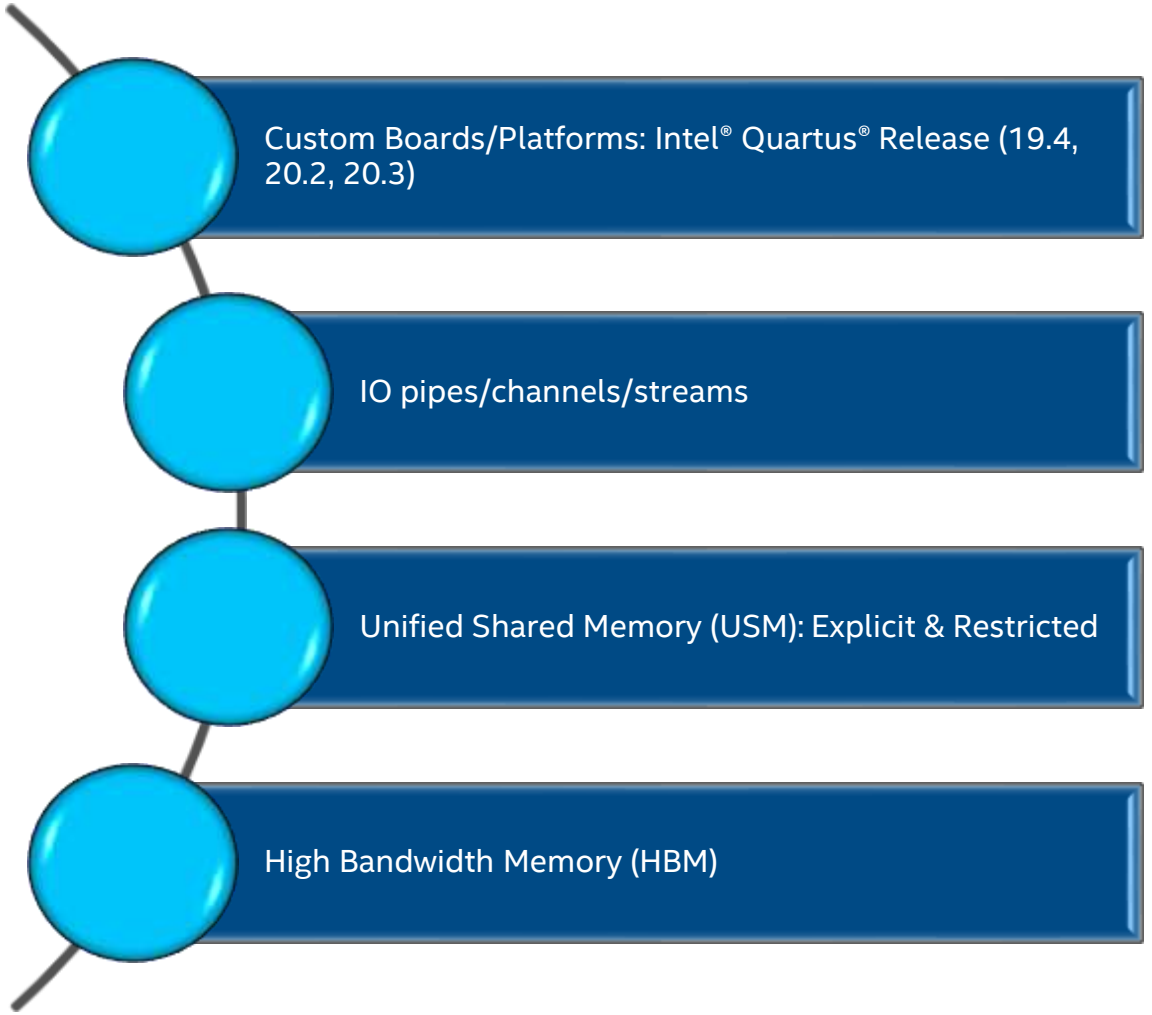
- Customizable memory architecture
- Distributed, high bandwidth, on-chip memory topology

+

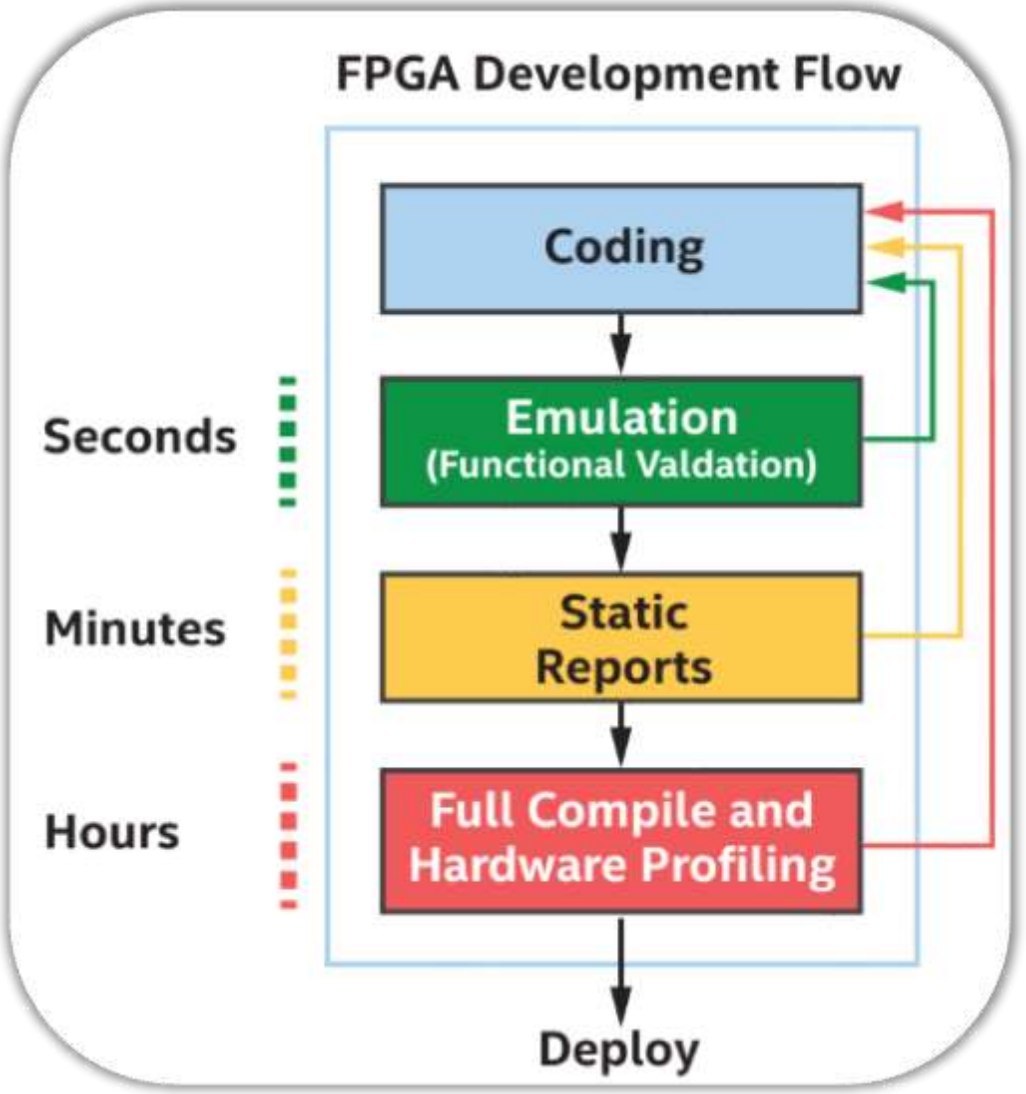


Intel oneAPI/DPC++ Feature Update

- 100% Performance parity with OpenCL



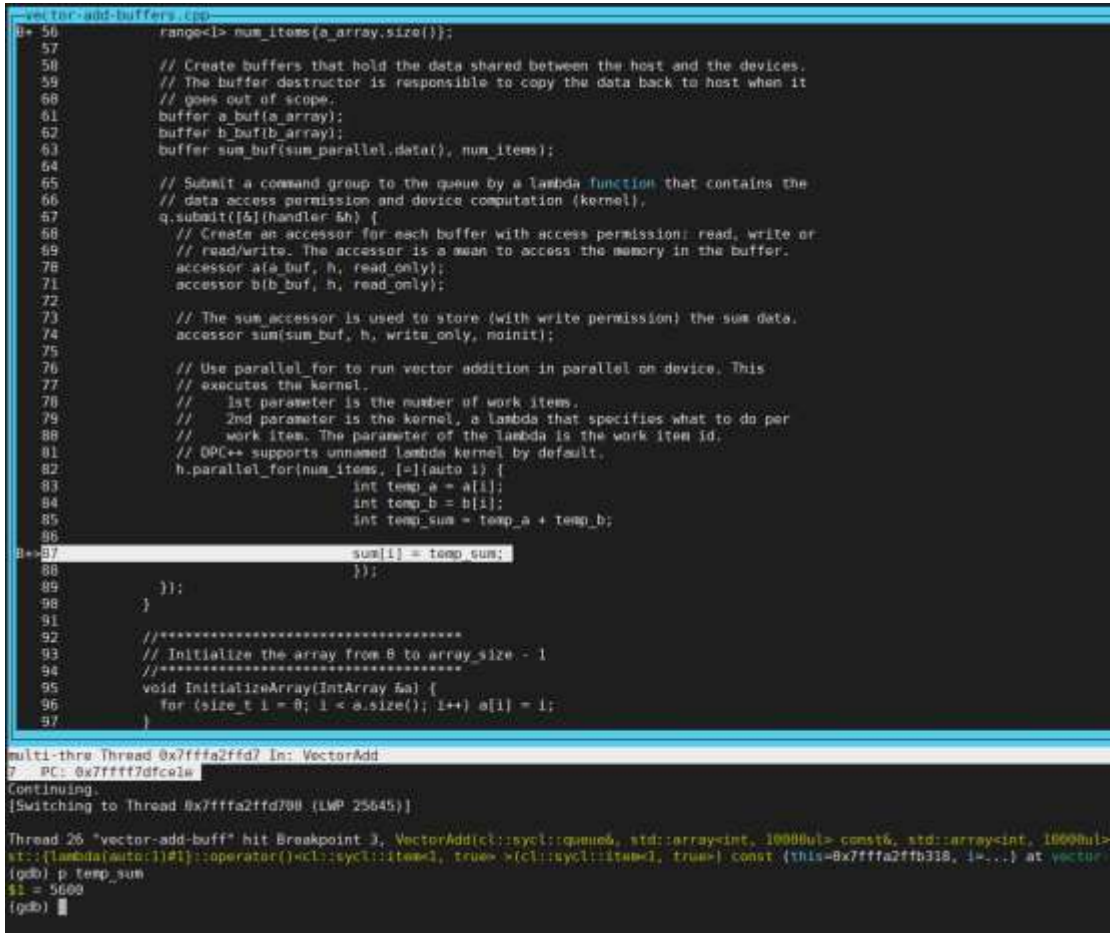
FPGA Development Flow for oneAPI Projects



Emulation
Seconds of Compilation

Developers can:

- Verify functionality of design through CPU compile and emulation.
- Identify quickly syntax and pointer implementation errors for iterative design/algorithm development.
- Enable deep, system-wide debug with Intel® Distribution for GDB.
- Functional debug of SYCL code with FPGA extensions.

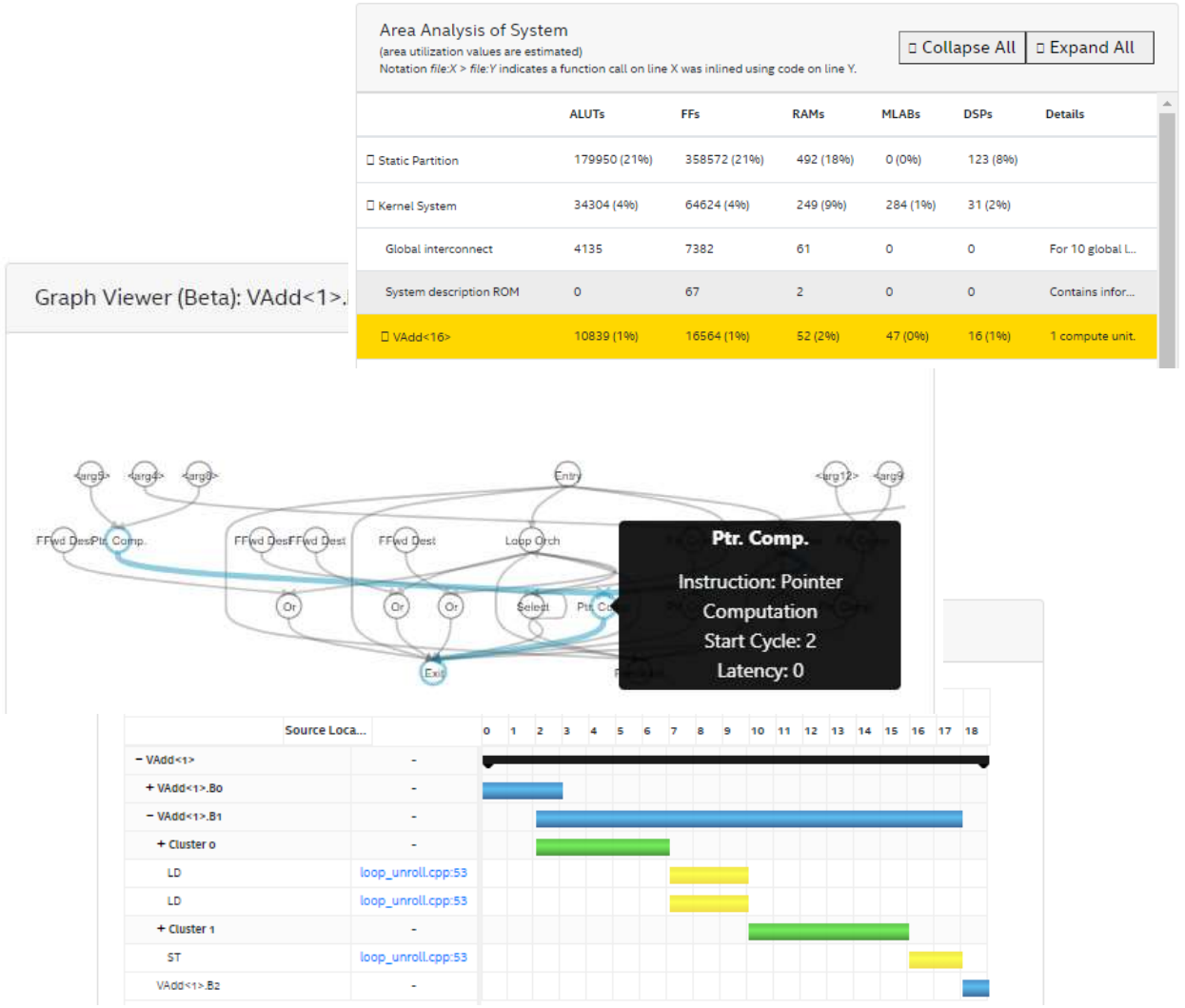


Report Generation

Minutes of Compilation

Developers can:

- Identify any memory, performance, data-flow bottlenecks in their design.
- Receive suggestions for optimization techniques to resolve said bottlenecks.
- Understand the implementation scheduling of the hardware built by the compiler
- Get area and timing estimates of their designs for the desired FPGA.

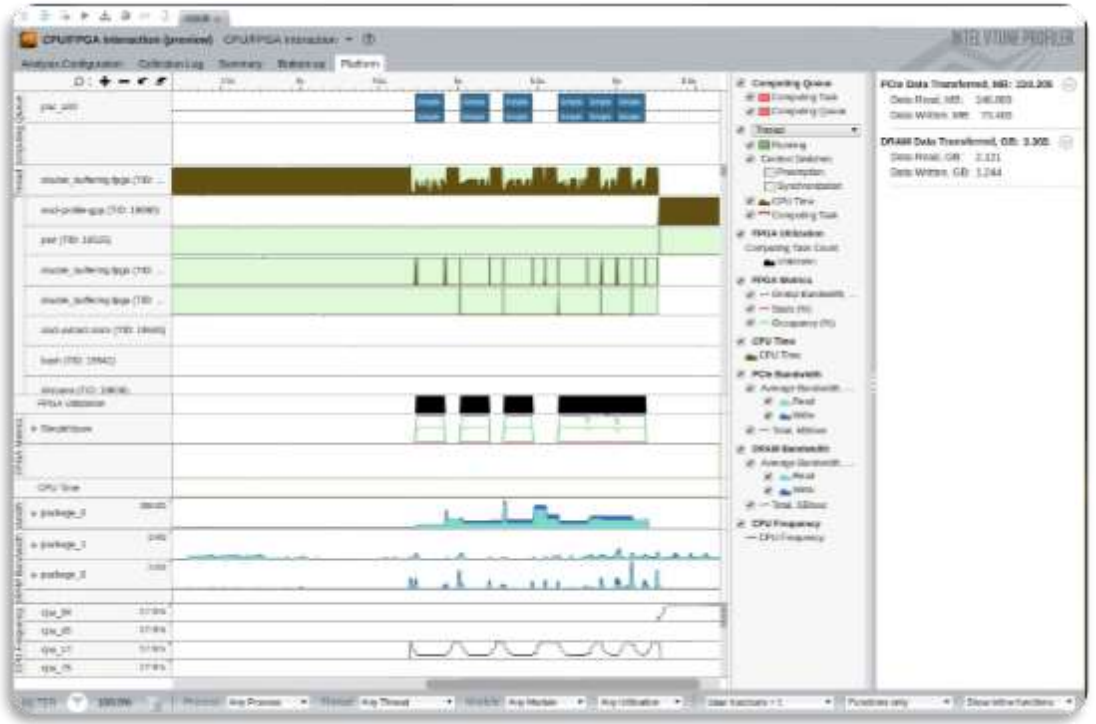


Bitstream Compilation

Intel® Quartus® + Intel® oneAPI DPC++ Compiler

Developers can:

- Compile FPGA bitstream for their design and run it on an FPGA.
- Attain automated timing closure.
- Obtain In-hardware verification.
- Take advantage of Intel® VTune™ Profiler for real-time analysis of design.

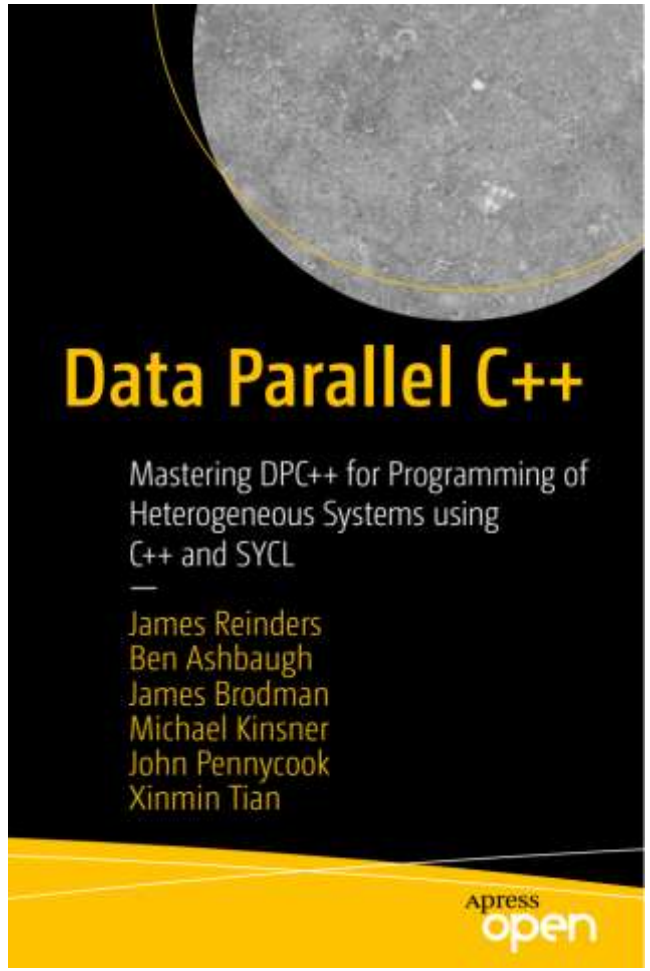


Resources

DPC++ Book

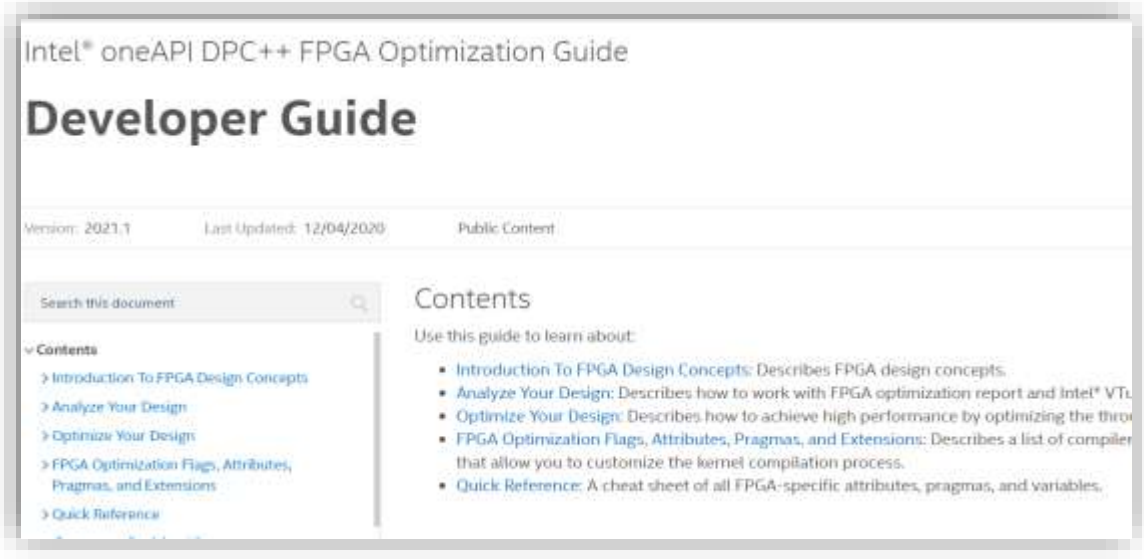
- Focus on the FPGA as the primary accelerator architecture throughout.
- First book on DPC++ or SYCL
- Written to facilitate better learning experience vs product specs.

- Just released and free in PDF form!
  - https://link.springer.com/book/10.1007%2F978-1-4842-5574-2



Intel® oneAPI DPC++ Specifications

Intel® oneAPI DPC++ FPGA Optimization Guide

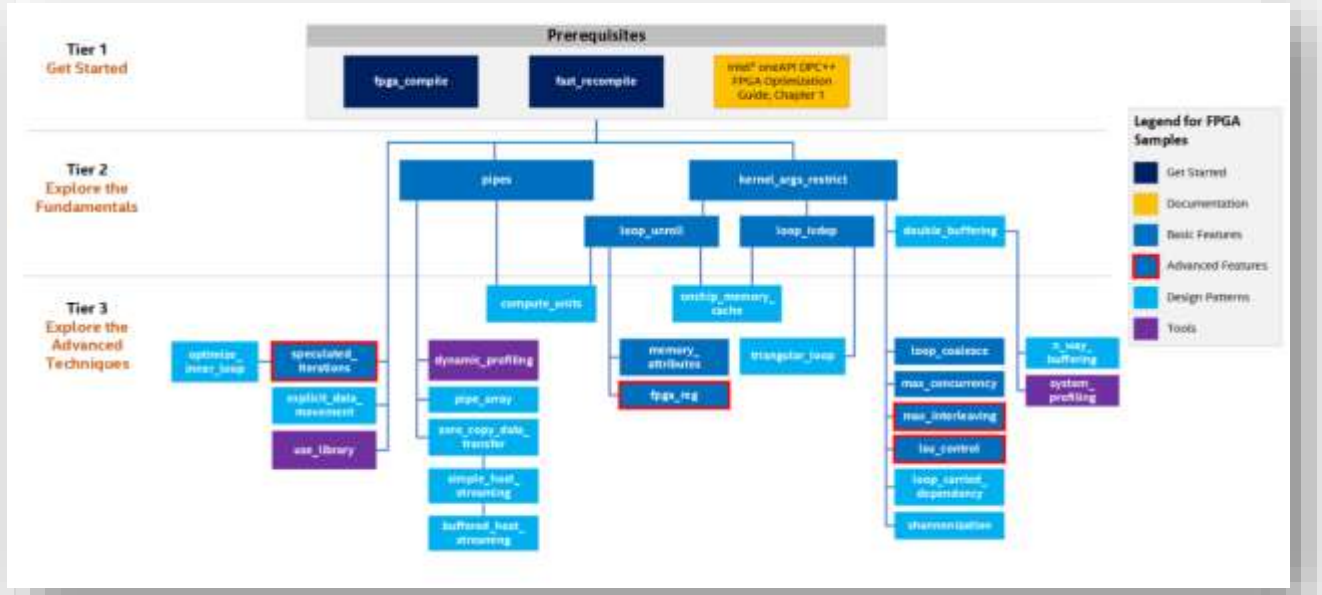


https://software.intel.com/content/www/us/en/develop/documentation/oneapi-fpga-optimization-guide/top.html

Intel® oneAPI Programming Guide

https://software.intel.com/content/www/us/en/develop/documentation/oneapi-programming-guide/top.html

Code Sample Tutorials (16)

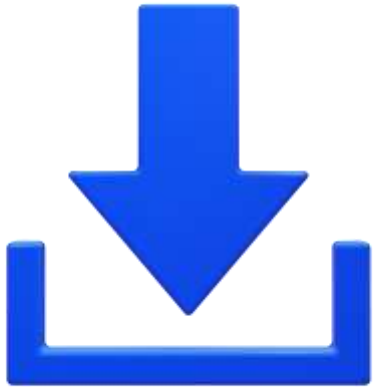


Refer: https://software.intel.com/content/www/us/en/develop/articles/explore-dpcpp-through-intel-fpga-code-samples.html

Access The Cloud

Develop, Test, and Run your oneAPI applications on the Intel® DevCloud for oneAPI across a range of Intel's CPUs, GPUs, and FPGAs

Get Access



Base Toolkit Download

Download the Intel® oneAPI base toolkit to get started with the DPC++ Compiler for host emulation & reports .

Get Base Toolkit

+

FPGA Add-on Download

Download the Intel® FPGA Add-on for oneAPI Base Toolkit to compile and run your designs on FPGAs.

Get FPGA Add-on

Notices & Disclaimers

- Performance varies by use, configuration and other factors. Learn more at www.Intel.com/PerformanceIndex
- Performance results are based on testing as of dates shown in configurations and may not reflect all publicly available updates. See backup for configuration details. No product or component can be absolutely secure.
- Your costs and results may vary.
- Intel technologies may require enabled hardware, software or service activation.
- Intel does not control or audit third-party data. You should consult other sources to evaluate accuracy.
- Database benchmark: OS: CentOS Linux release 7.9.2009; CPU: Intel(R) Xeon(R) CPU E5-1650 v3 @ 3.50GHz, RAM: 132 GB
  - Intel: Intel® oneAPI DPC++ Compiler, Hardware: Intel® FPGA Programmable Acceleration Card (PAC) D5005, https://github.com/oneapi-src/oneAPI-samples/tree/master/DirectProgramming/DPC%2B%2BFPGA/ReferenceDesigns/db
  - Xilinx: Vitis™ 2020.1, Hardware: Alveo U200, https://xilinx.github.io/Vitis_Libraries/database/2020.1/gqe_guide/kernel_demo.html#gqe-kernel-demo
- Gzip compression benchmark: Algorithms: (LZ77, Static Huffman and CRC)
  - Intel input file: Random 12 MB file, https://github.com/oneapi-src/oneAPI-samples/tree/master/DirectProgramming/DPC%2B%2BFPGA/ReferenceDesigns/gzip
  - Xilinx input file: silesia file set. (http://sun.aei.polsl.pl/~sdeor/index.php?page=silesia), https://github.com/Xilinx/Vitis_Libraries/tree/master/data_compression/L2/demos/gzip
- INFORMATION IN THIS DOCUMENT IS PROVIDED "AS IS". NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO THIS INFORMATION INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.
- The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.
- © Intel Corporation. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others.

Optimization Notice

Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice.
Notice revision #20110804


intel