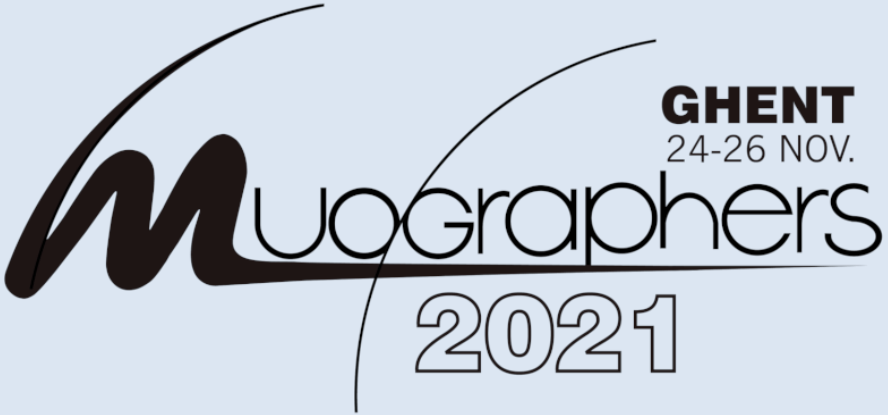

A Novel Readout Scheme for Muon Tomography Application in Material Identification

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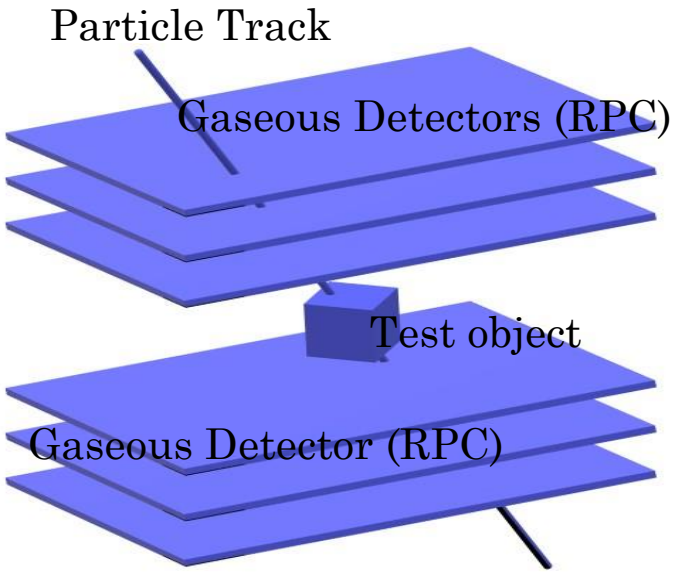
Motivation

- Tracking is an important objective in muon scattering tomography where the incident and scattered muon tracks are necessary for estimating the angle of scattering.
- Material discrimination can be done on the basis of the angle of scattering which depends upon the physical properties of the materials for a given muon mometum.
- A prototype muon tomography setup is under construction at SINP with a vertical stack of position-sensitive detectors to serve as muon trackers.
- Resistive Plate Chamber (RPC) is considered as trackers at this stage of R&D for comparatively simple fabrication, availability of raw materials locally etc.
- For the collection of position data from the tracking RPCs, R&D over a simple low-cost readout scheme based on FPGA is in progress.

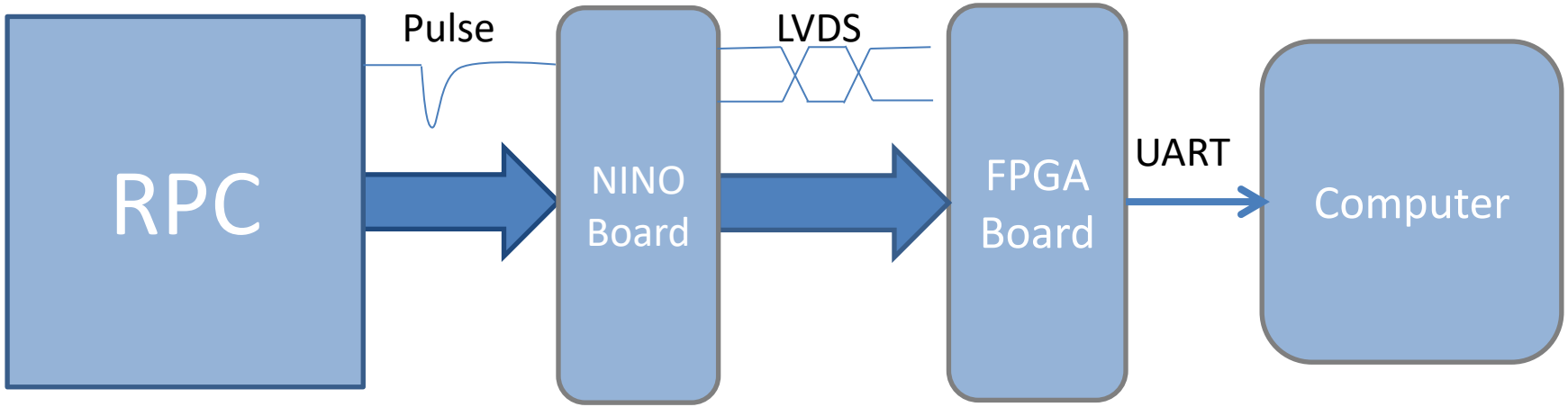
Muon Tomography Setup

- Contains two sets of three RPCs on either sides of the inspection volume for tracking incident and scattered tracks.
- RPCs made with bakelite / glass of dimension 30 cm x 30 cm with a gas gap of 2 mm are under construction and qualification.
- Design guideline of the tomography setup is optimized using numerical simulation of the imaging performance followed by its analysis for material discrimination *[S. Tripathy et al., JINST 15 P06029, 2020]*.
- The readout electronics comprising of NINO ASIC in the front-end followed by FPGA at the back-end is under testing *[S. Tripathy et al., JINST 15 C11013, 2020]*.



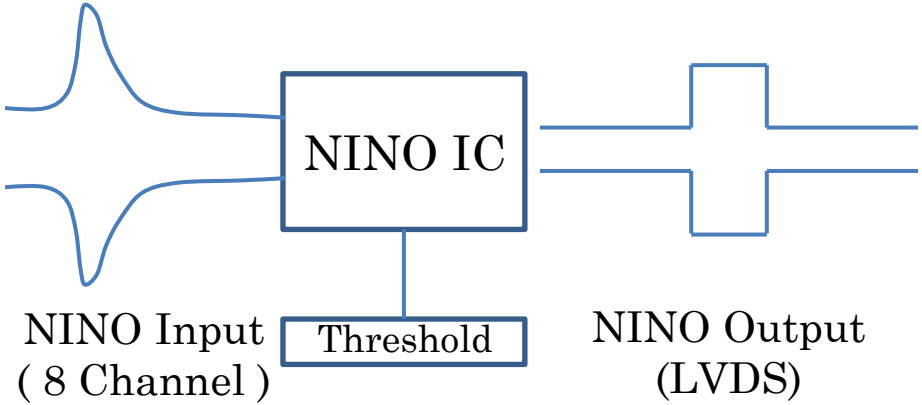
Muon tomography setup

Readout Scheme



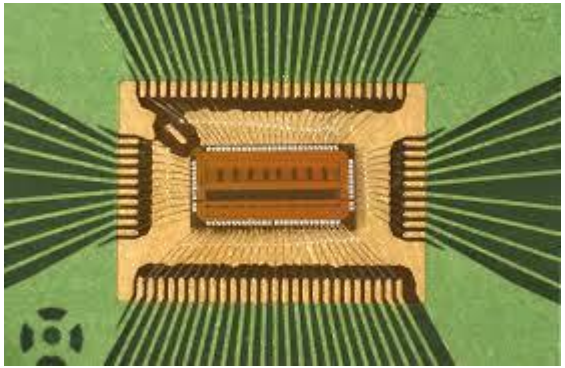
- NINO *[F. Anghinolfi et al., NIM A 533 (2004) 183]*
  - low power, amplifier discriminator chip
  - LVDS output
- FPGA for DAQ
  - MAX 10 FPGA

NINO ASIC

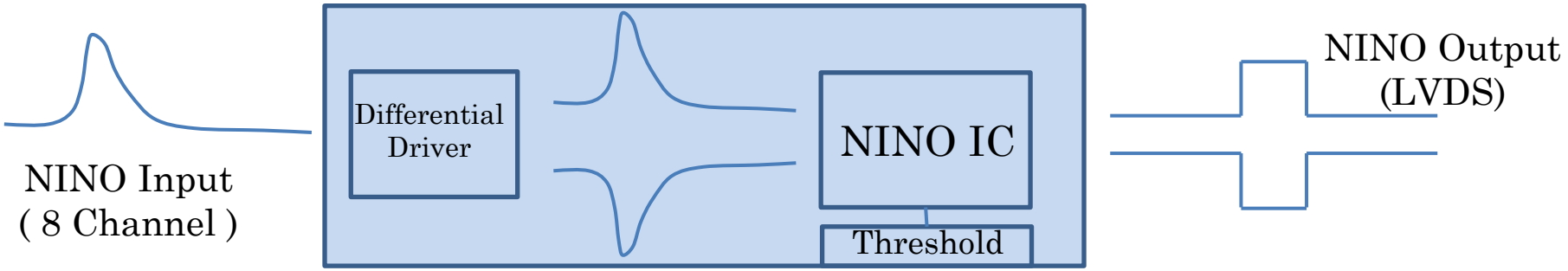


- Channels : 8
- Voltage supply : 2.5 V
- Input signal range : 30 fC – 2 pC
- Discriminator threshold : 10 fC – 100 fC
- Output : LVDS
- Power consumption : 25 mW per channel

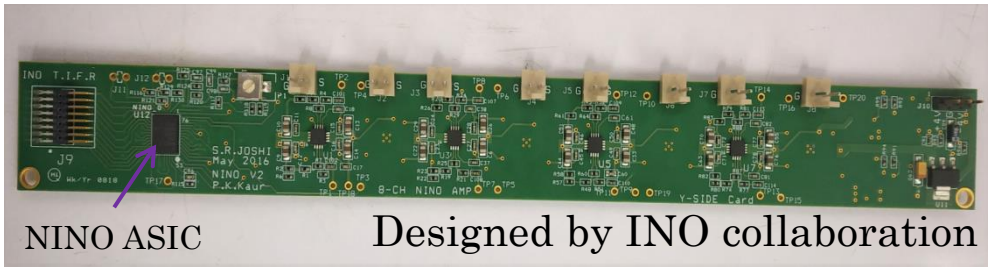
- Ultrafast front-end preamplifier discriminator chip
- Designed at CERN for ALICE TOF Experiment

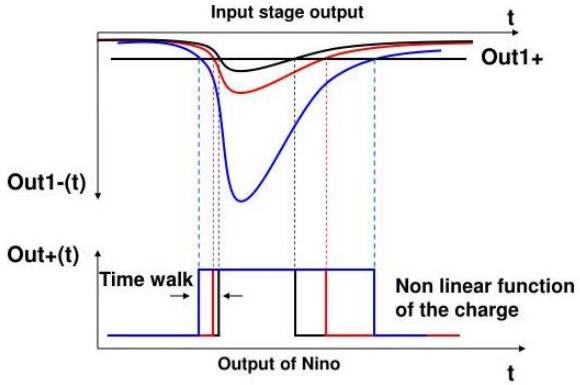


NINO Board



X Side NINO => Negative input
Y Side NINO => Positive input





FPGA (Field Programmable Gate Array)

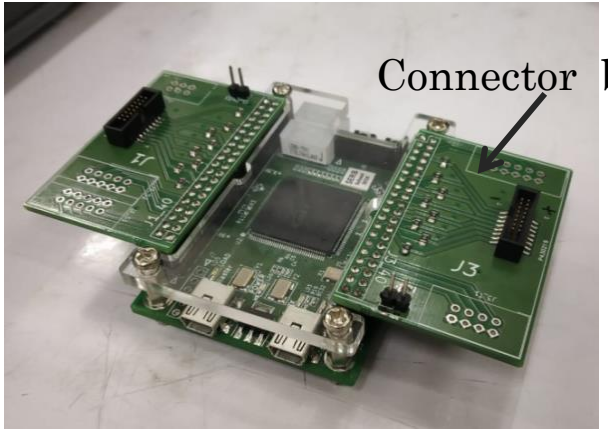
- It contains a million logic gates with programmable interconnection
- It can execute any logic operation.
- LabVIEW and/or VHDL used to program.
- In-built Memory Blocks (SRAM / Flash Memory).

- Advantages
  - Programmable, High speed
  - Large number of I/O pins
  - Low cost and easy to get

MAX 10 FPGA

MAX10 FPGA Board

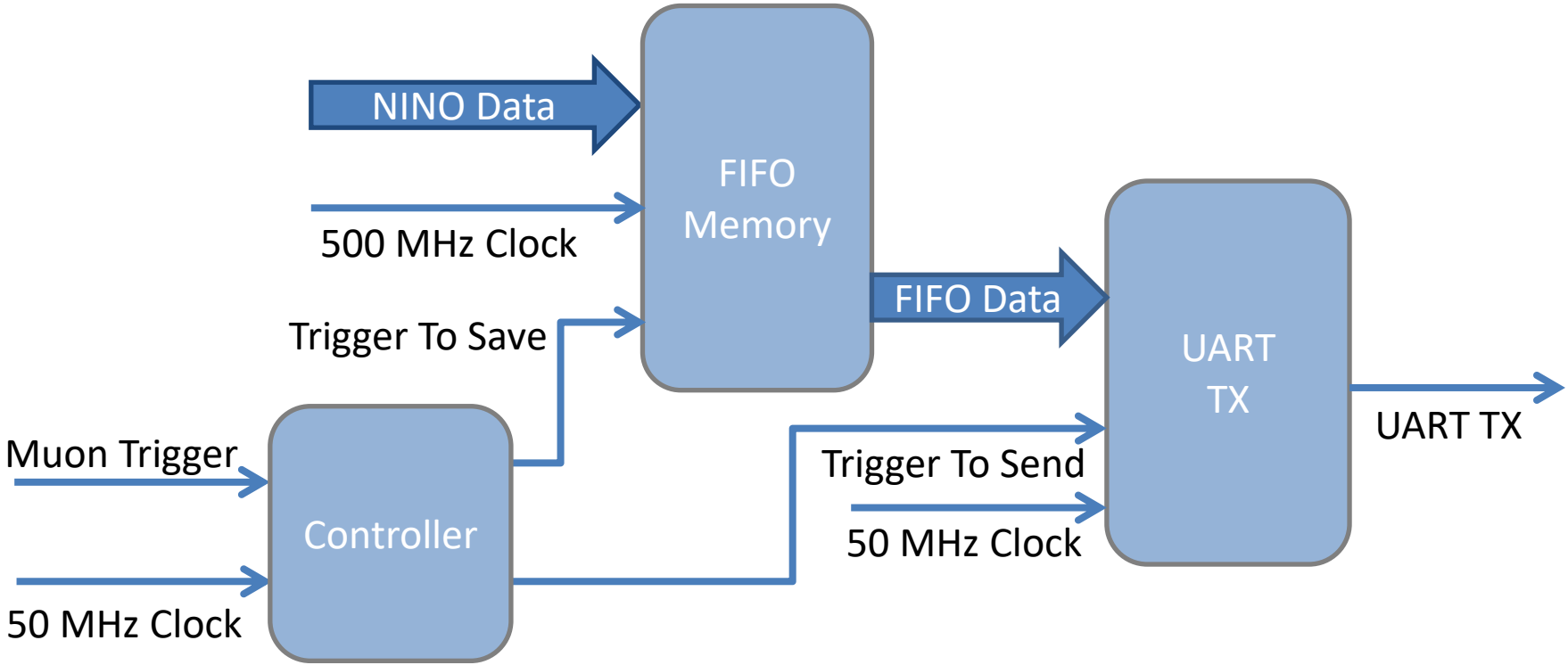
- 2000 Logic elements (LEs)
- 50 MHz on board clock.
- 108 Embedded memory (Kbits)
- 12 User flash memory (KBytes)
- Two 40-pin headers (GPIOs) provide 68 3.3V single I/O pins.
- Upto 27 LVDS Input and 5 LVDS Output pins.



MAX 10 FPGA Dev Board

- Designed by INO collaboration
- Connector board designed to map LVDS pin

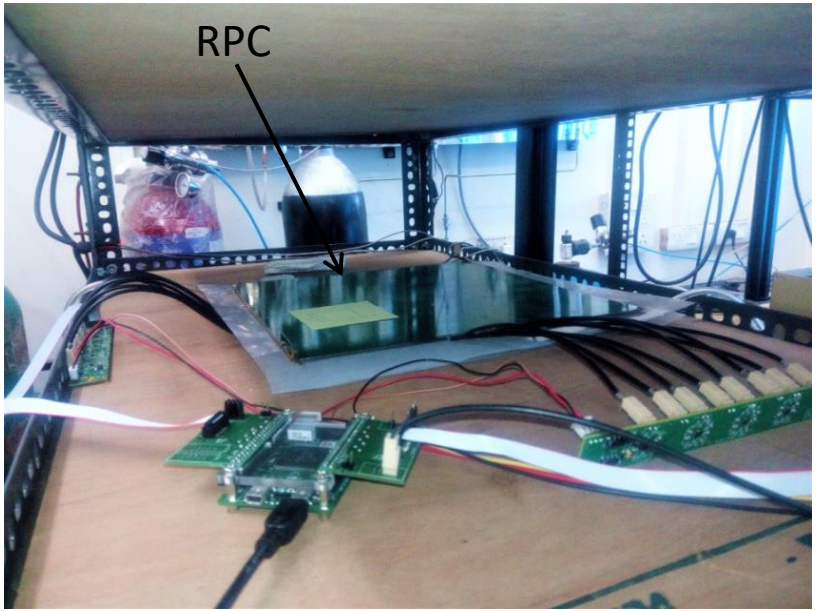
Logic Inside FPGA



FPGA Board Programing

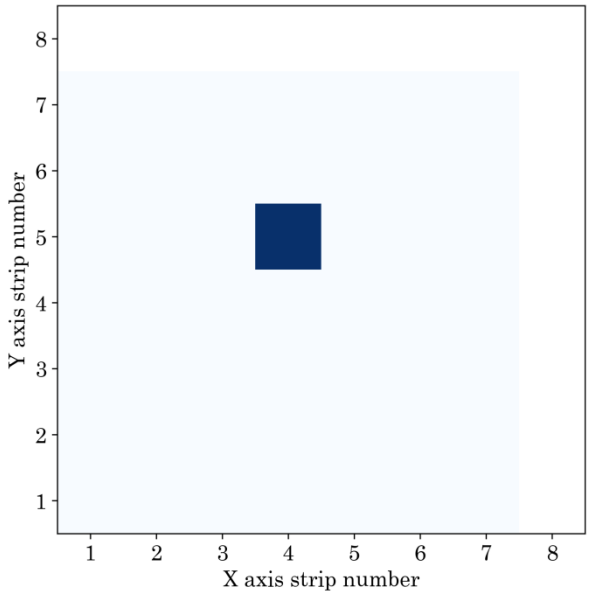
- Two SCN detector are used to provide muon trigger (25 cm x 35 cm).
- VHDL language (Quartus Prime Software) and Python programming language are used to program FPGA and collecting data.
- UART protocol for data transmission which is implemented in FPGA.
- Two clock signal used (Generated using PLL)
  - 500 MHz for TOT measurement
  - 100 MHz for others

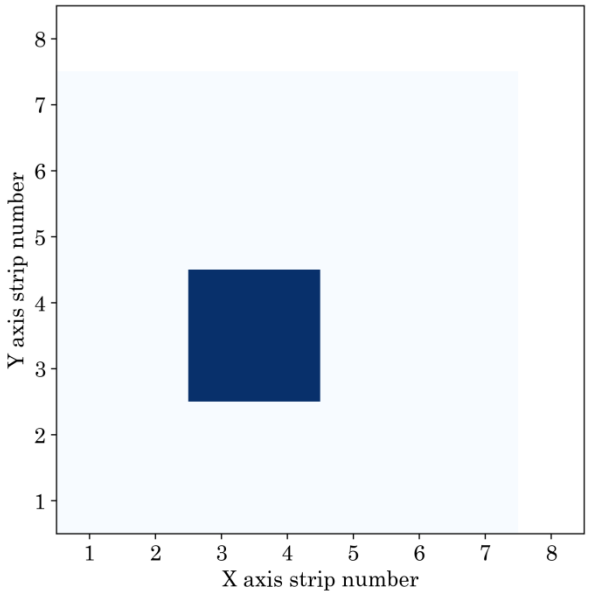
Experimental Setup



- Supply voltage : 5000 V (Anode = 5000 V and Cathode = - 5000 V)
- Gas mixture : Freon (95 %) and Isobutene (5%)
- RPC with X and Y pickup panels with strips (3 cm width)
- NINO board connected to each pickup panel (8 channels each)
- Triggered with coincidence of two plastic scintillator paddles (25 cm x 35 cm), and converted to TTL to provide FPGA.

Muon Position on 2D Plane

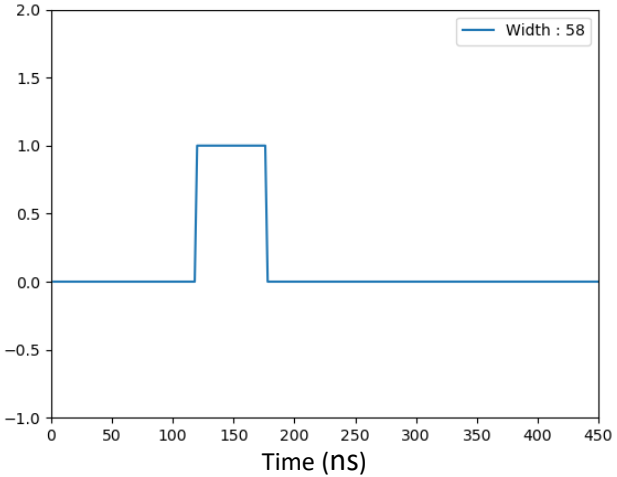




- Supply voltage : 5000 V (Anode = 5000 V and Cathode = - 5000 V)
- Gas mixture : Freon (95 %) and Isobutene (5 %)

Pulse Width Measurement

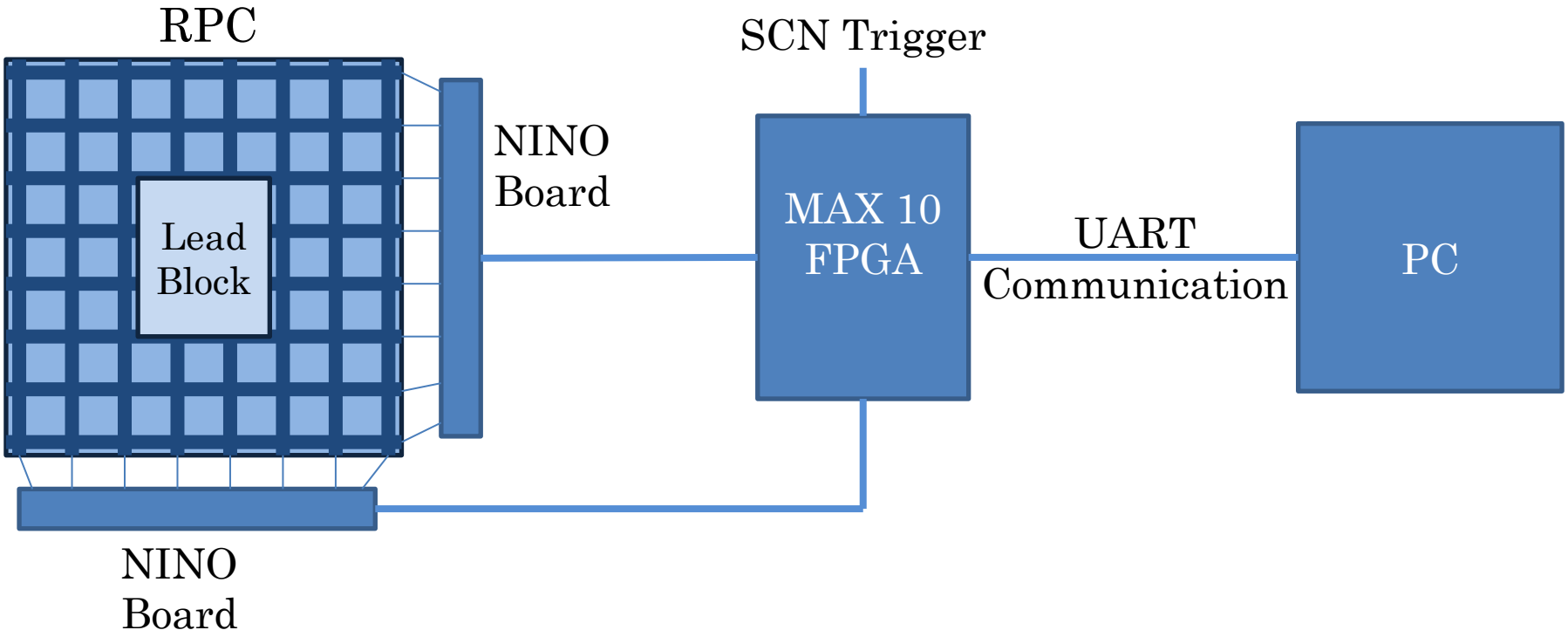
Pulse width using Oscilloscope
Pulse width = 57.6 ns

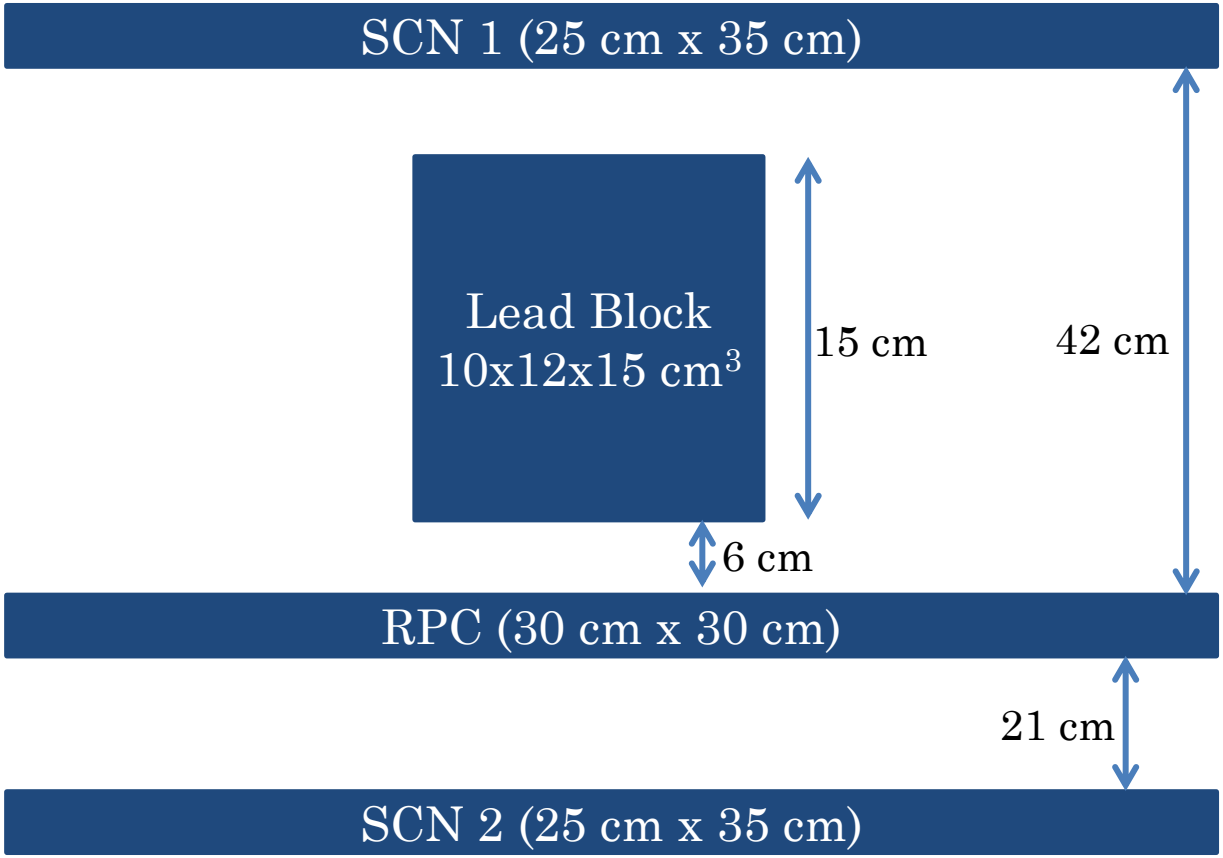


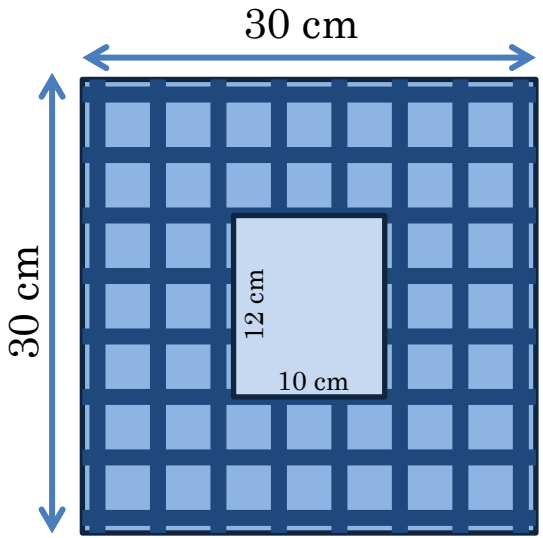
Pulse width using FPGA
Pulse width = 58 ns

- Pulse width comparison using generated pulse.
- Pulse width can be used to achieve better position resolution.

Experiment for Imaging



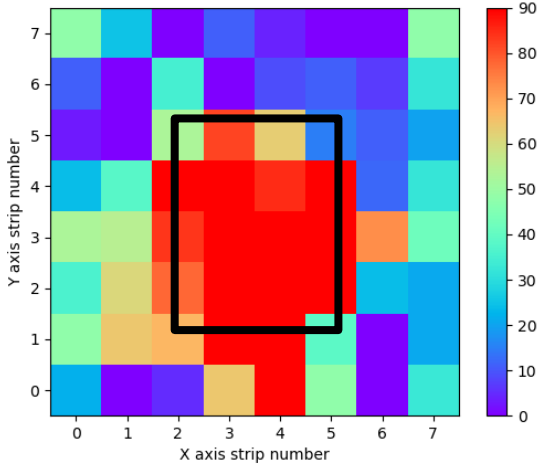




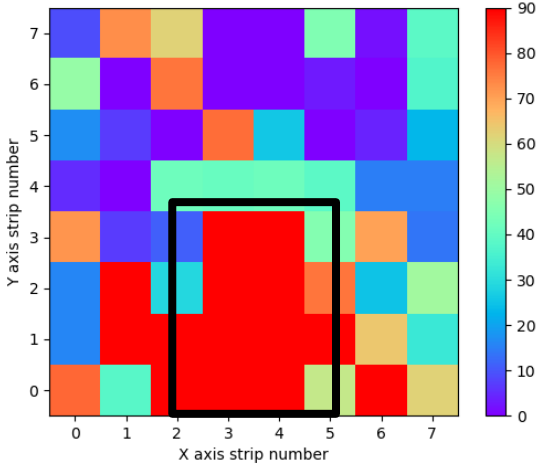
RPC Top View

Strip Pitch 3.2 cm
(strip 3 cm, Gap 0.2 cm)

Hit Map



Lead block placed at the center



Lead block placed at the edge

- Exposure time : Nearly 12 Hours, similar for background data.
- Python Programming used to compare background and absorbed data.

Summary and Future Plans

- The position of muon hit has been detected by using NINO and FPGA based DAQ.
- We are able to produce a shadow of the lead block using the muon absorption method with the proposed readout scheme.
- The pulse width of NINO output has been measured with maximum +/- 2ns error.
- In future, we have plan to build a complete tracking setup using DAQ board with high-end FPGA.
- Plan to fabricate detector for better performance, increase readout granularity.

- Collaborators
  - Sridhar Tripathy
  - Nayana Majumdar
  - Sandip Sarkar
  - Supratik Mukhopadhyay

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Thank You