Contribution ID: **120** Type: **talk**

The Integration and Commissioning of the Small-Strip Thin Gap Chambers for ATLAS New Small Wheel Phase-I Upgrade

Tuesday 13 July 2021 16:45 (15 minutes)

At the high luminosity Large Hadron Collider (LHC), the instantaneous luminosity will be up to $5-7.5\times 10^{34}cm^{-2}s^{-1}$. This necessitates the upgrade of the muon spectrometer of the ATLAS detector. The Small Wheel, the innermost station of muon end-cap system, will be replaced by the 'New Small Wheel (NSW)'. For the high luminosity runs, the new system is required to improve trigger selectivity for the end-cap region in a high background environment, while maintaining excellent tracking capability for the events in pp collisions at $\sqrt{s}=13$ TeV to 14 TeV with the ATLAS detector. To accomplish this, it should deliver hardware-based online track measurements with a pointing accuracy of 1 mrad at Level-1 in the end-cap region. All of this is achieved by two detector technologies, the Small-Strip Thin Gas Chamber (sTGC) and the Micro Mesh Gaseous structures (MM). The sTGC is the primary trigger detector because of its bunch-crossing identification capability. Along with this state of the art detector technology, radiation tolerant custom-made Application-Specific Integrated Circuits (ASICs) are built to create high-speed data inter-connections, which achieve up to 1 MHz of Level-1 data readout using the Back-End FELIX (Front End LInk eXchange) system. This complex system of $\sim$400K physical channels and more than $\sim$14K ASICs creates many challenges, which include achieving precise alignment of the readout channels for high spatial resolution and maintain simultaneous trigger and readout with a background rate of $\sim 20kHzcm^{-2}$. The sTGC detector quadruplets are assembled and aligned into wedges at CERN. We summarize our experiences during the sTGC integration and commissioning of the sTGC detector wedges. These studies are performed for the first time together with the final Front-End and Back-End electronics. Our work includes alignment survey of the detector channels, establishing proper connectivity between the detector and the Front-End channels, verifying the robustness of the detector performance against various noise sources, while tuning numerous clock phases and delays for synchronous trigger and readout at high data rate.

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Authors: ATLAS MUON COLLABORATION; ATMASIDDHA, Prachi (University of Michigan, Ann Arbor)

Presenter: ATMASIDDHA, Prachi (University of Michigan, Ann Arbor)

Session Classification: Particle Detectors

Track Classification: Particle Detectors