ETROC project for the CMS MTD Endcap Timing Layer (ETL)

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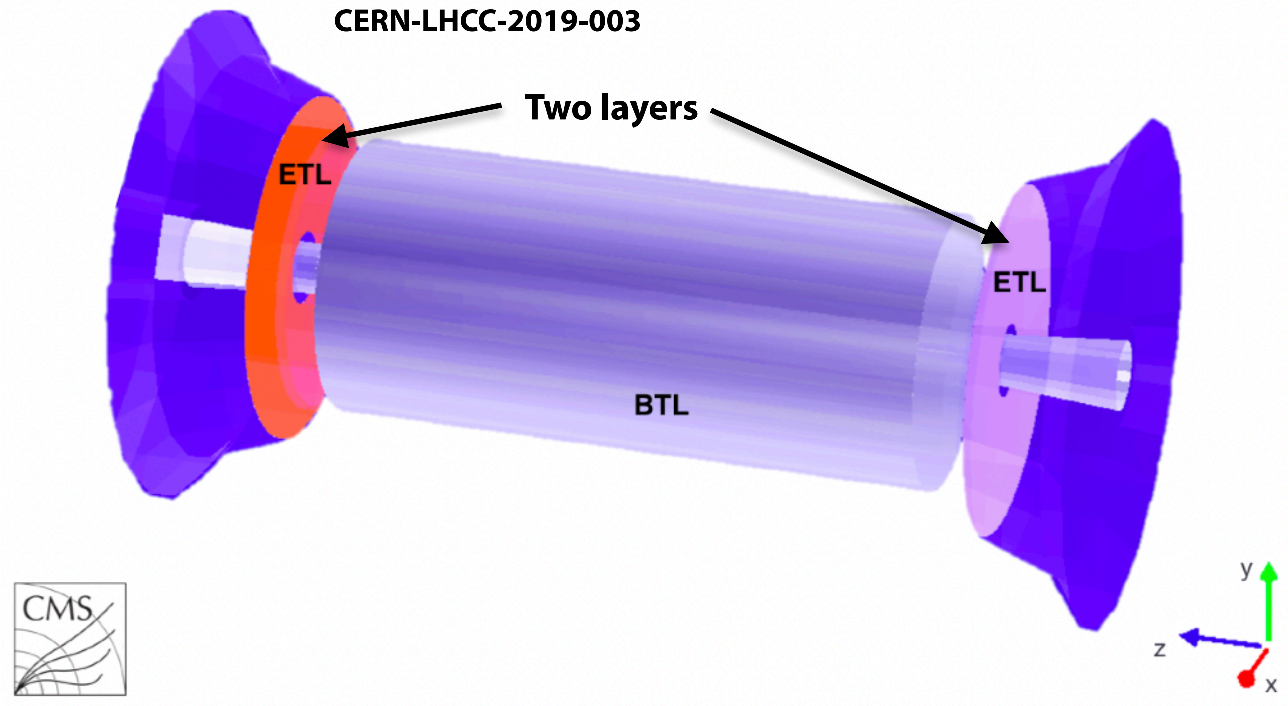
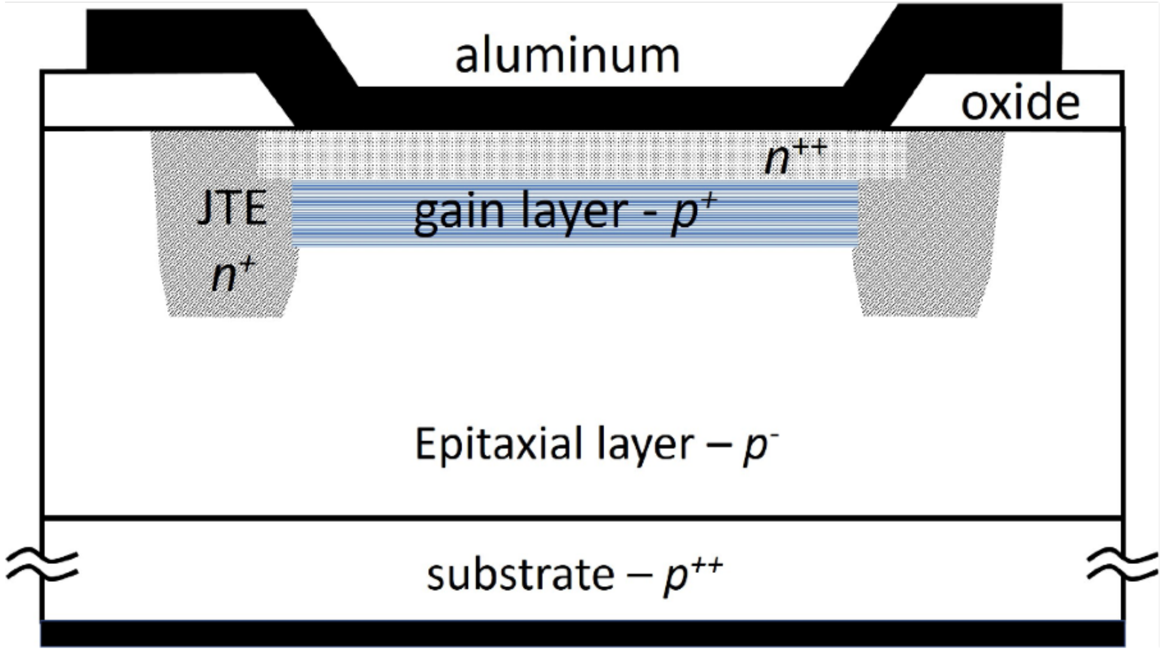
DPF 21

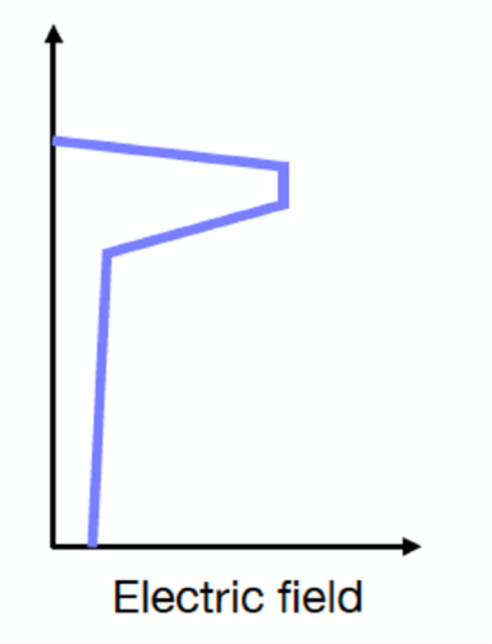
CMS MIP Timing Detector (MTD)



- MTD
  - Barral Timing Layer (BTL)
    - LYSO crystal scintillator
    - SiPM readout
  - End-cap Timing Layer (ETL):
    - Low Gain Avalanche Detector (LGAD)
    - ASIC readout (ETROC)
- ETL (coverage $1.6 < |\eta| < 3.0$)
  - Time resolution
    - 50 ps per hit and 35 ps per track with two layer hits at the beginning
    - < 50 ps per track as target upper limit

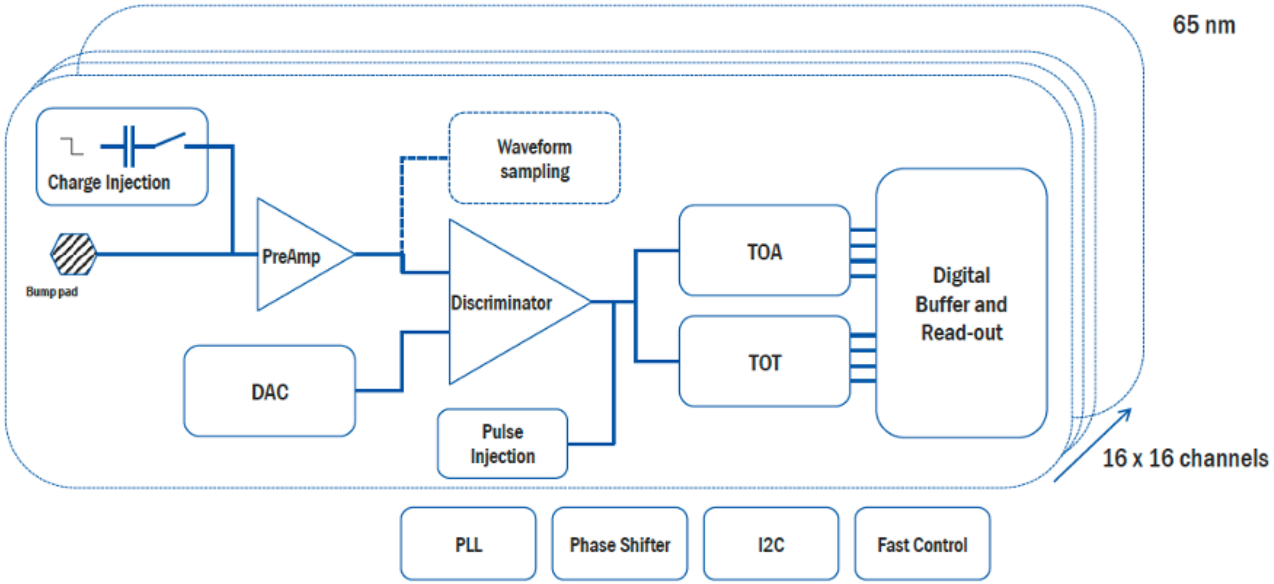
Low Gain Avalanche Detector (LGAD)

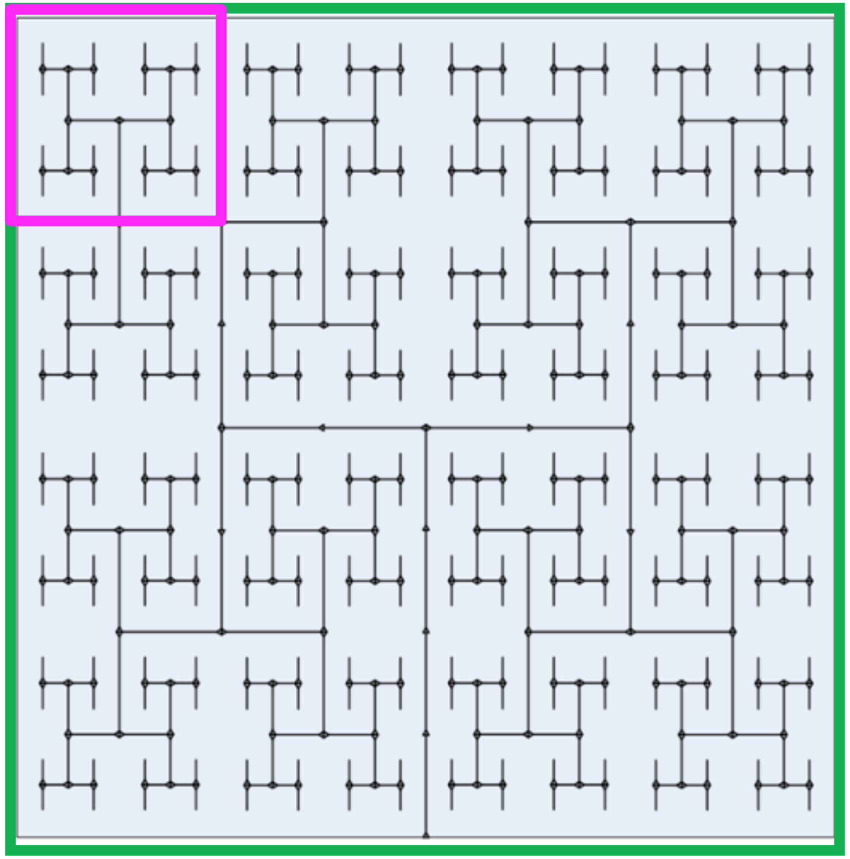




- **Extra p^+ type implant near the n^{++} electrode generates a large electric field, resulting in an electron-avalanche effect that offers a gain factor of 10-30**
- **Intrinsic gain lead to low noise, large slew-rate and fast rising pulse**
- **Sensor contribution ~ 30ps**
  - **ETROC + clock distribution and rest < 40ps to achieve ~50ps per hit**

Readout ASIC (ETROC)





- LGAD sensor size: 1.3*1.3 mm^2
- To achieve target of time resolution < 40 ps
  - low noise and fast rise time
  - power budget: 1W/chip, ~3 mW/channel
    - very low power TDC
      using simple delay cells with self-calibration

✓ ETROC0: single analog channel

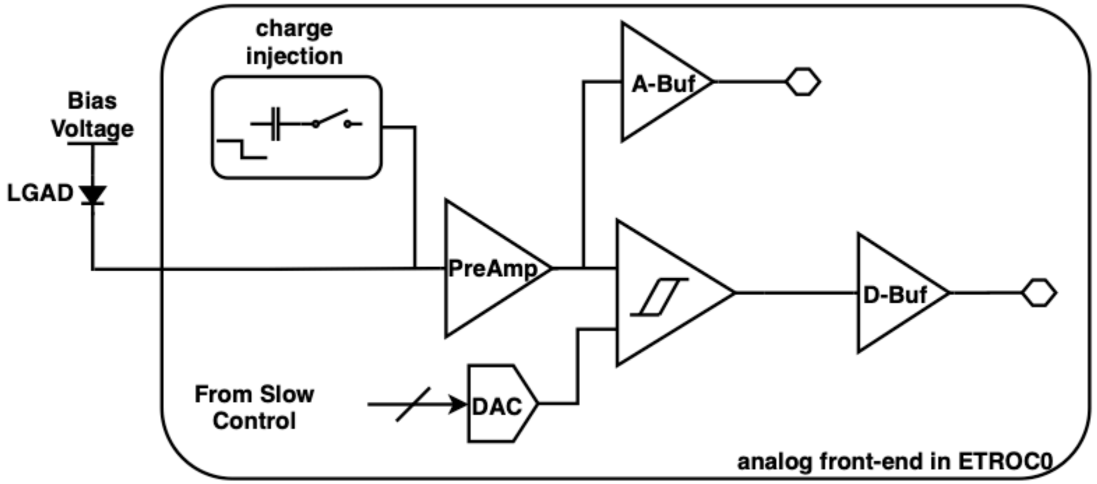
✓ ETROC1: with TDC and 4x4 clock tree

◉ ETROC2: full functionality

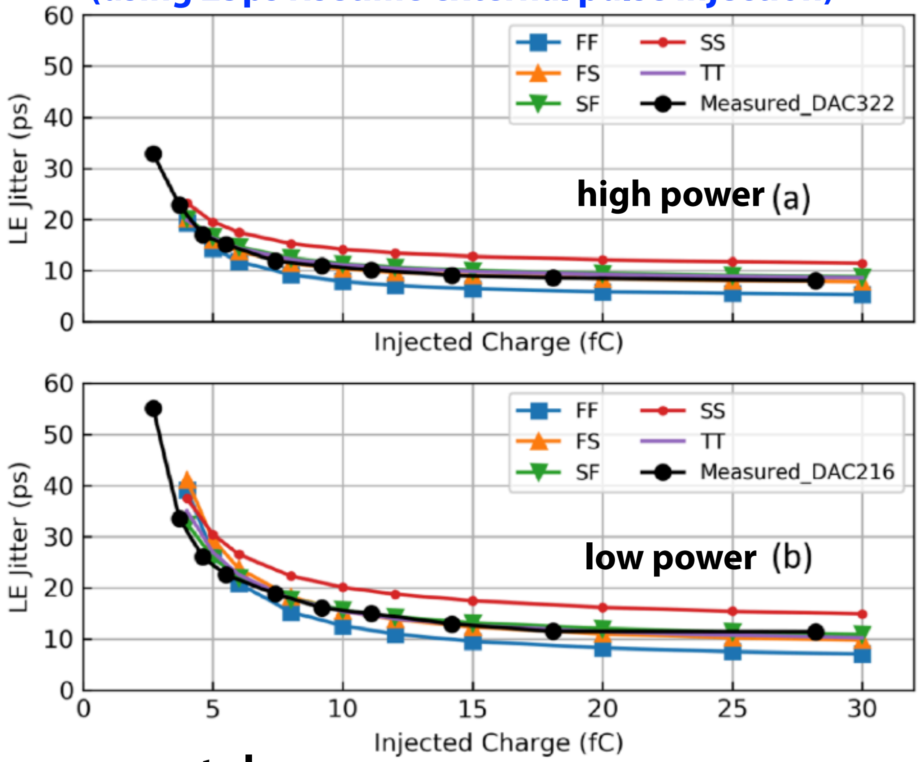
◉ ETROC3: 16x16 full size chip

ETROC0 Simulation vs Measured Jitter

ETROC0 diagram



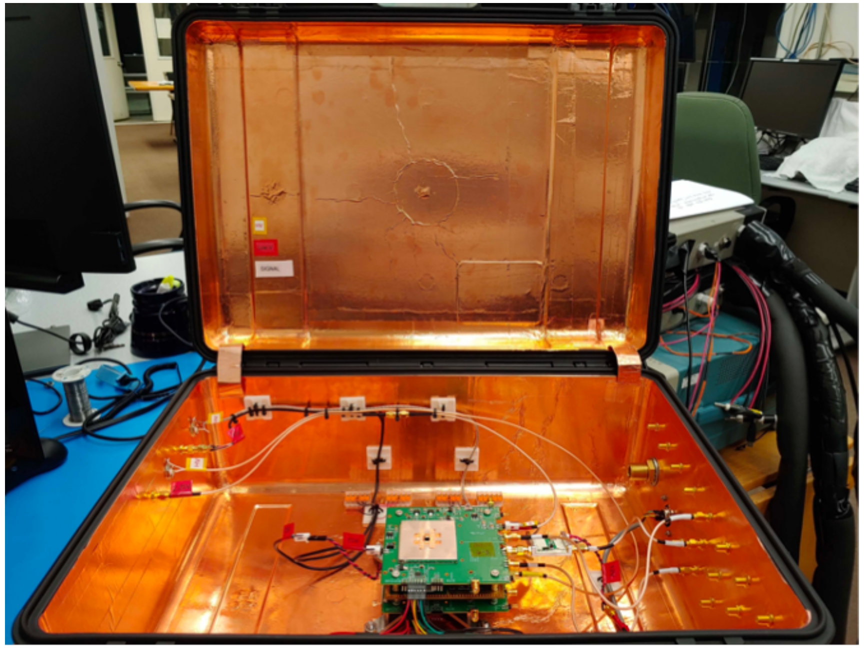
ETROC0 post-layout simulation vs testing results (using 25ps risetime external pulse injection)

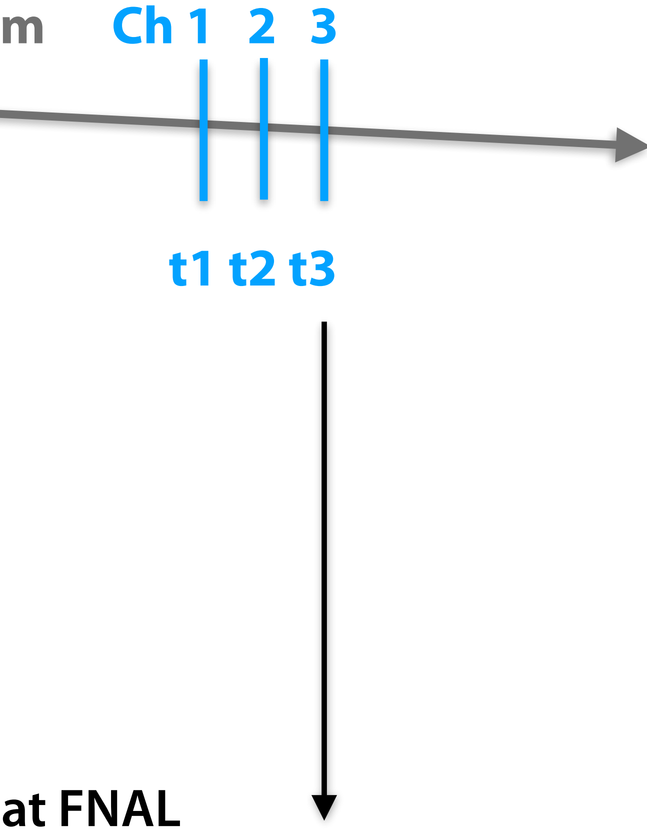


- ETROC0 goal: core front-end analog performance
  - All individual blocks have been tested
  - Power consumption have been measured for each section separately
- Summary of the charge injection testing
  - Discriminator LE (leading edge) jitter measurements agree with chip post-layout simulation
  - Power consumption for preamp and discriminator consistent with expectation
- TID (Total Ionizing Dose) test have been tested successfully up to 100 Mrad

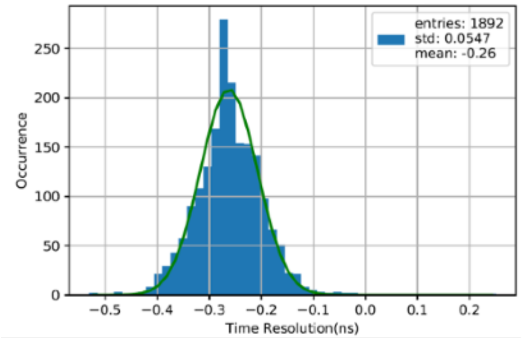
ETROC0: Test Beam Results

Jan-Feb 2020 Simple "suitcase" setup in parasitic mode running at FNAL MTest

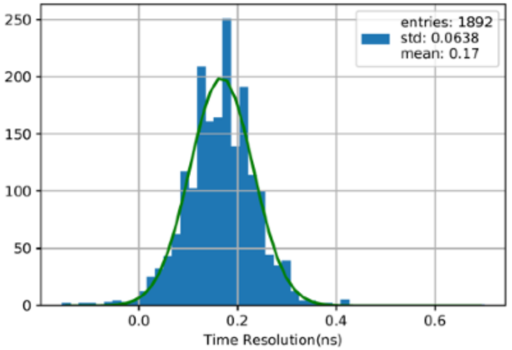




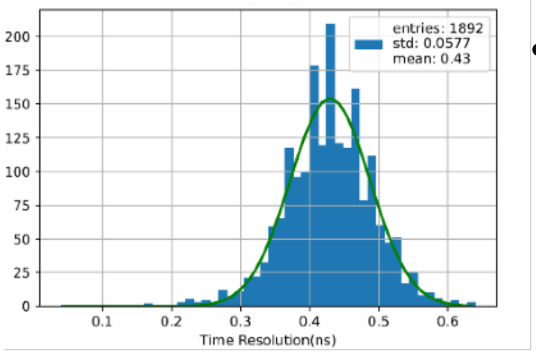
t3-t2



t3-t1



t2-t1



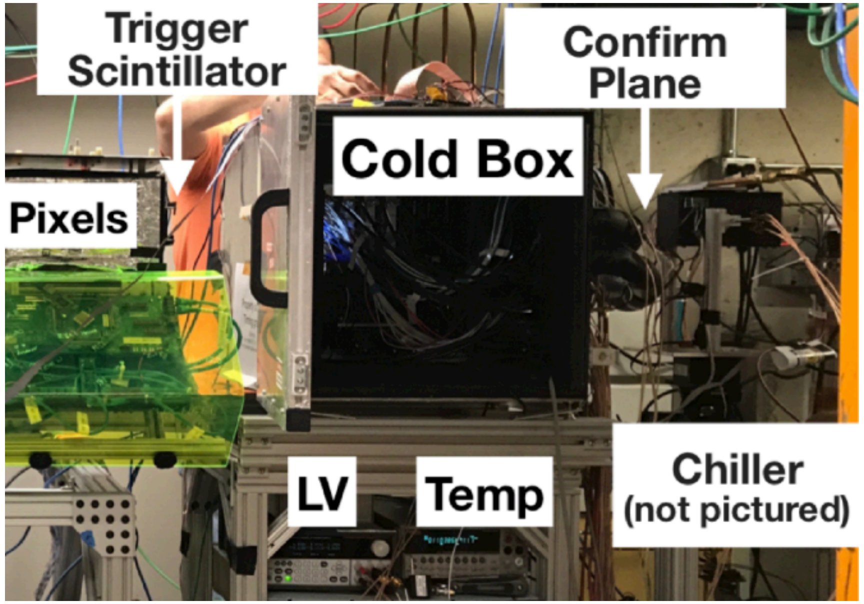
- Beam test at FNAL

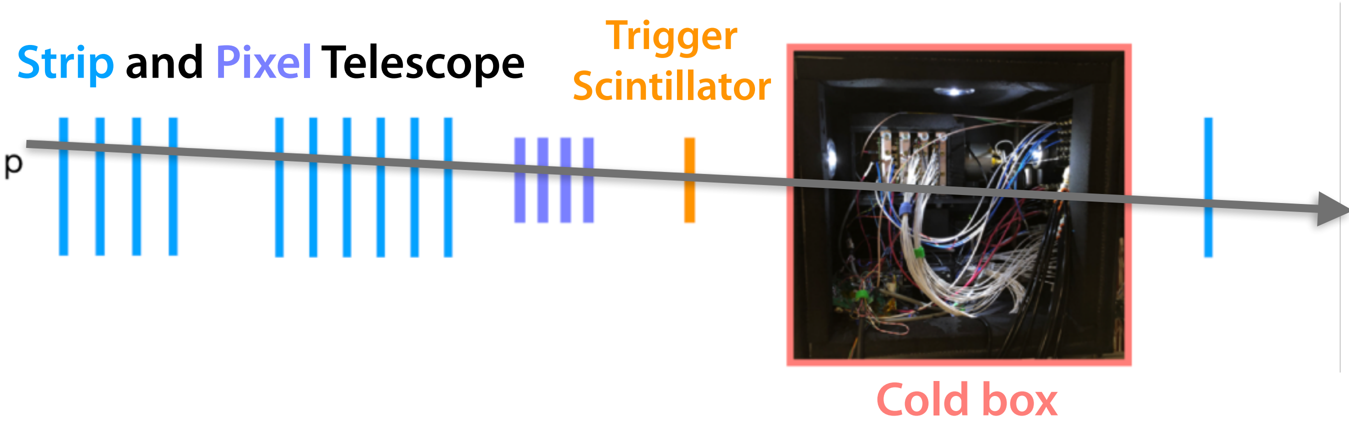
$$\sigma_2 = \sqrt{0.5 \cdot (\sigma_{21}^2 + \sigma_{32}^2 - \sigma_{31}^2)} \approx \textbf{33 ps}$$

from preamp. waveform analysis

ETROC0: Test Beam Results

Jan-Feb 2020 Advanced setup at FNAL MTest

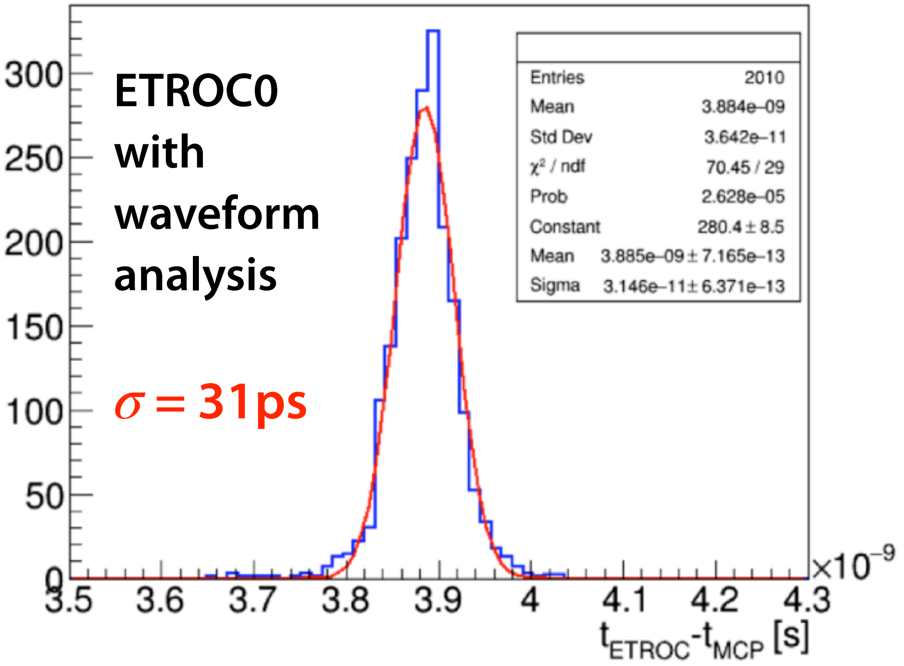




LGAD boards on cooling blocks

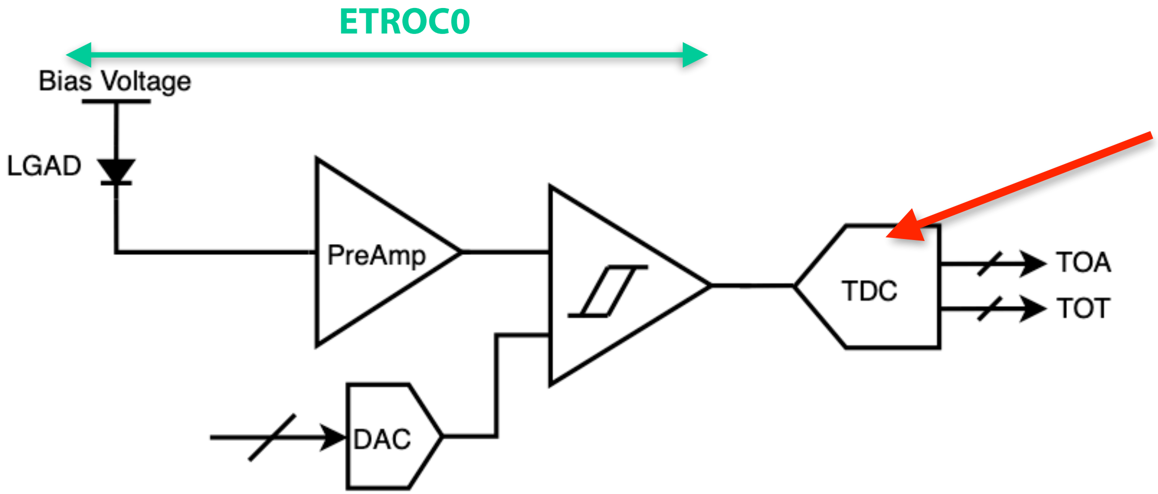
MCP (Photek) time reference

- MTD Beam Test Setup at FNAL Test
  - Independent scintillator provides trigger
  - Telescope provides proton track
  - Oscilloscope saves preamp waveforms
  - Study Δt (LGAD, MCP)



ETROC1 (4x4 pixels)

ETROC1 diagram



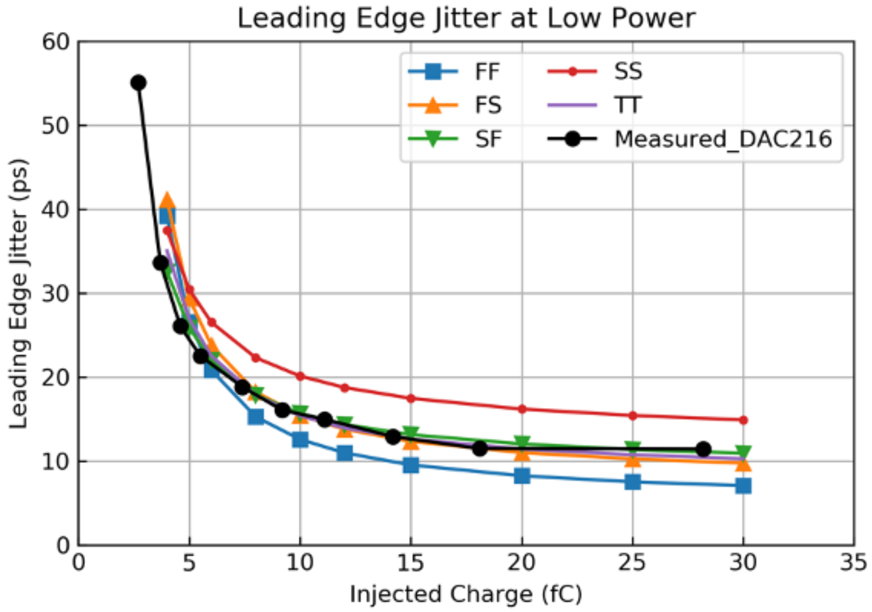
Submitted in Aug. 2019, Received in Dec. 2019

- ETROC0 front-end used directly in ETROC1
- New in ETROC1 TDC
  - TOA bin size: spec < ~30ps, ~20 ps achieved
  - TOT bin size: spec < ~100ps, ~40 ps achieved
  - Low power: spec < 0.2 mW per pixel, achieved ~0.1 mW per pixel

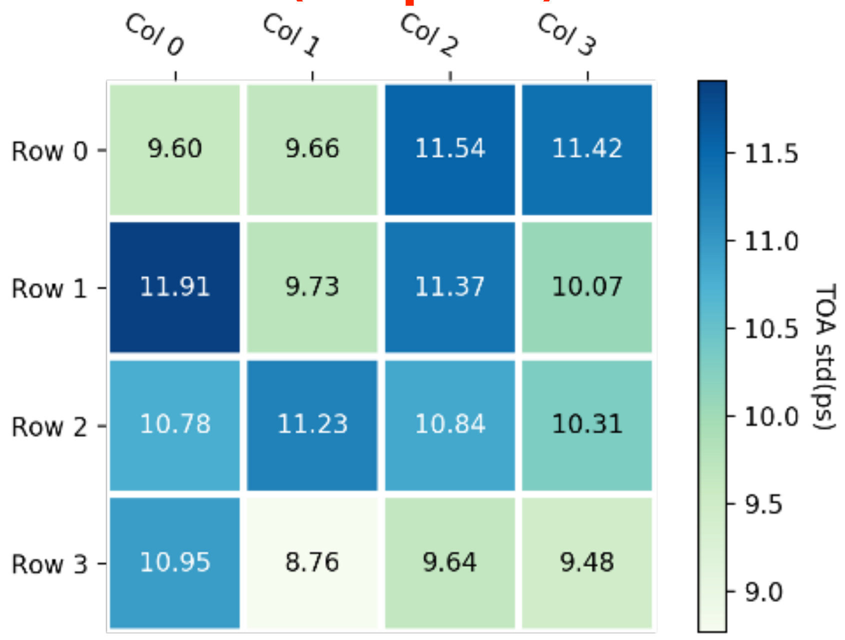
- ETROC TDC design optimized for low power
  - A simple delay line without DLL to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure both TOA and TOT at the same time.
- In-situ delay cell self-calibration technique
  - For each hit, use two consecutive rising clock edges to record two time stamps, with a time difference of the known 320 MHz clock period: 3.125ns.
  - Important to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power)

Bare ETROC1: Jitter from Charge Injection

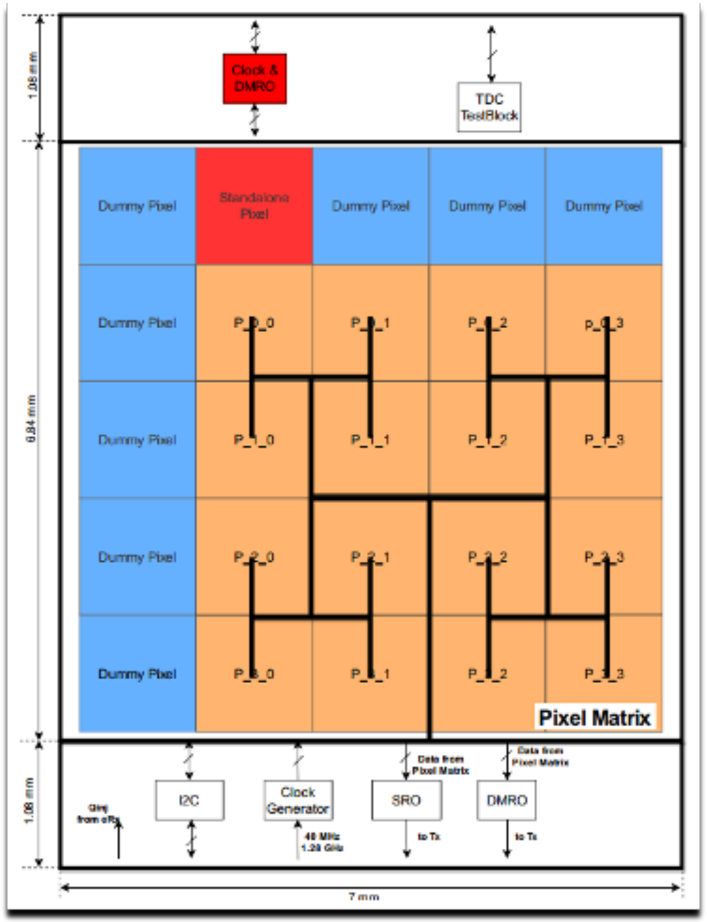
Jitter from ETROC0 Discriminator (Single pixel)



Jitter from ETROC1 TDC (4x4 pixels)

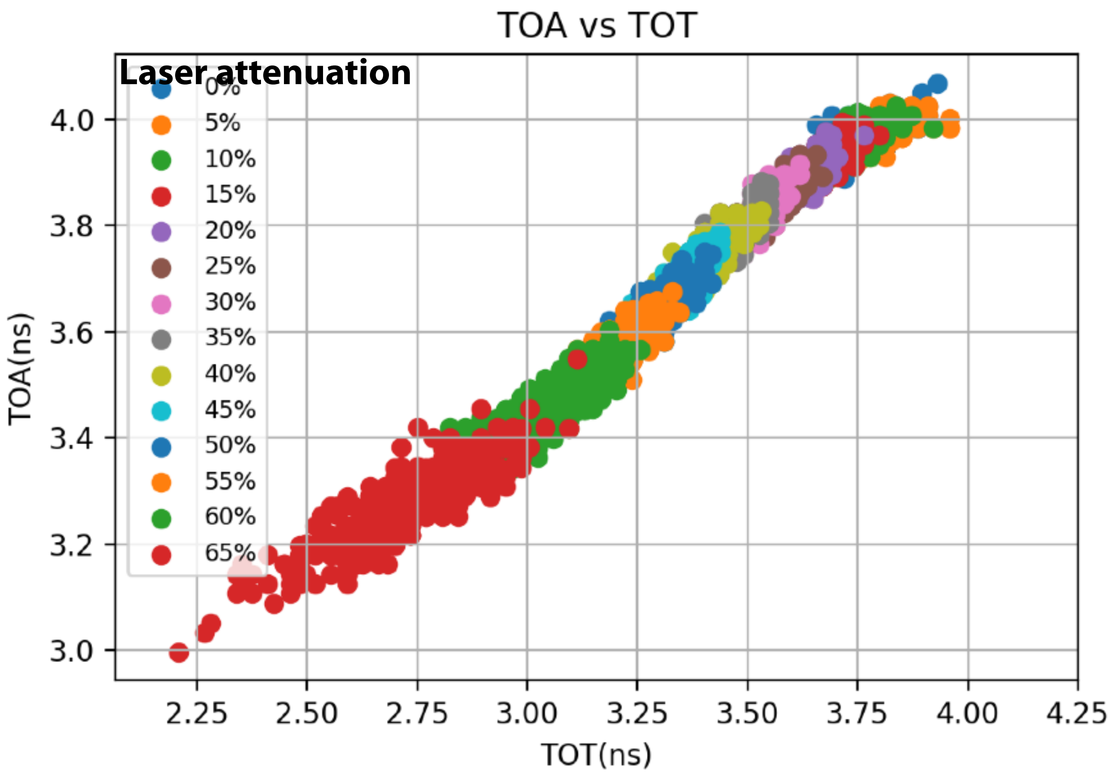


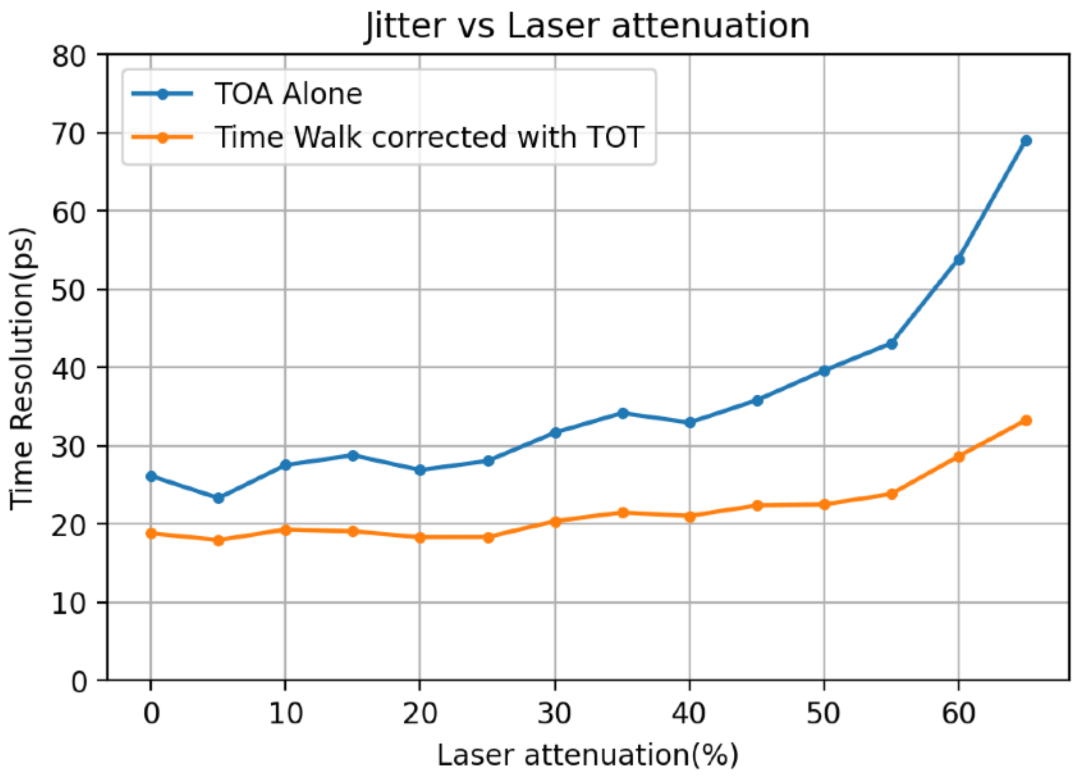
ETROC1 4x4 clock H-tree



- Bare ETROC0: Charge injection -> Preamplifier -> Discriminator -> Scope
- Bare ETROC1: Charge injection -> Preamplifier -> Discriminator -> TDC
- Bare ETROC1 works very well, consistent with expectation
- Observed 40MHz noise from bump-bonded ETROC1 + LGAD
  - coupled through the sensor due to 40MHz clock activity in the circular buffer memory
  - can be suppressed by setting the discriminator threshold to ~8 fC

LGAD+ETROC1: Jitter from Infrared Laser





- ETROC1 TDC data with laser: Laser -> Preamplifier -> Discriminator -> TDC
  - Jitter is below 20ps with preamp at low power

- For comparison
  ETROC0 preamp output waveform analysis with laser: Laser -> Preamplifier -> Buffer -> Scope
  - Jitter is ~17.6ps with preamp at low power

LGAD+ETROC1: Preliminary Test Beam Results

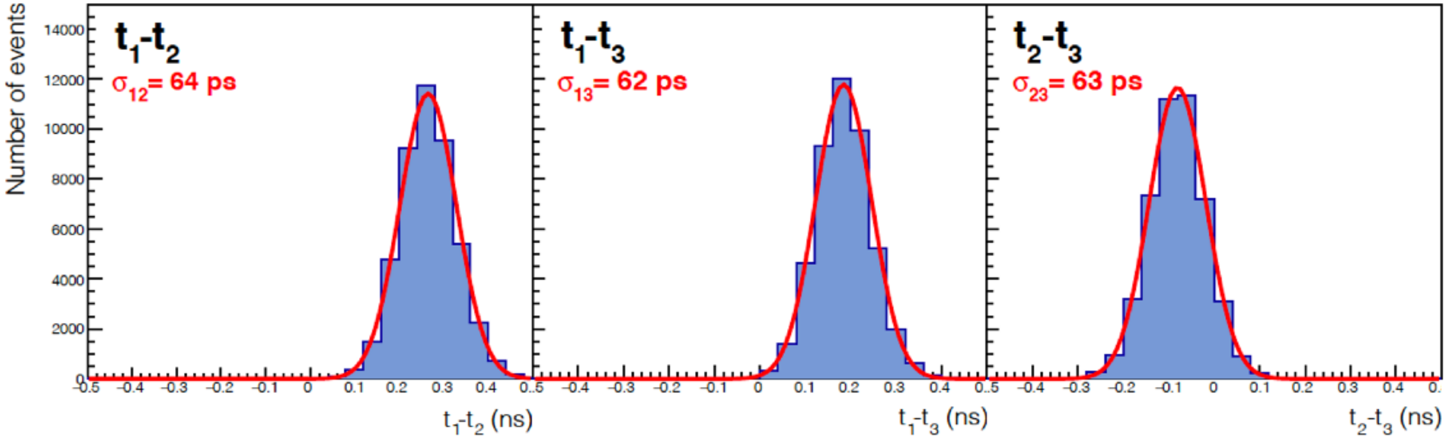
Feb-May 2021

120 GeV proton beam

Ch 1 2 3

t1 t2 t3

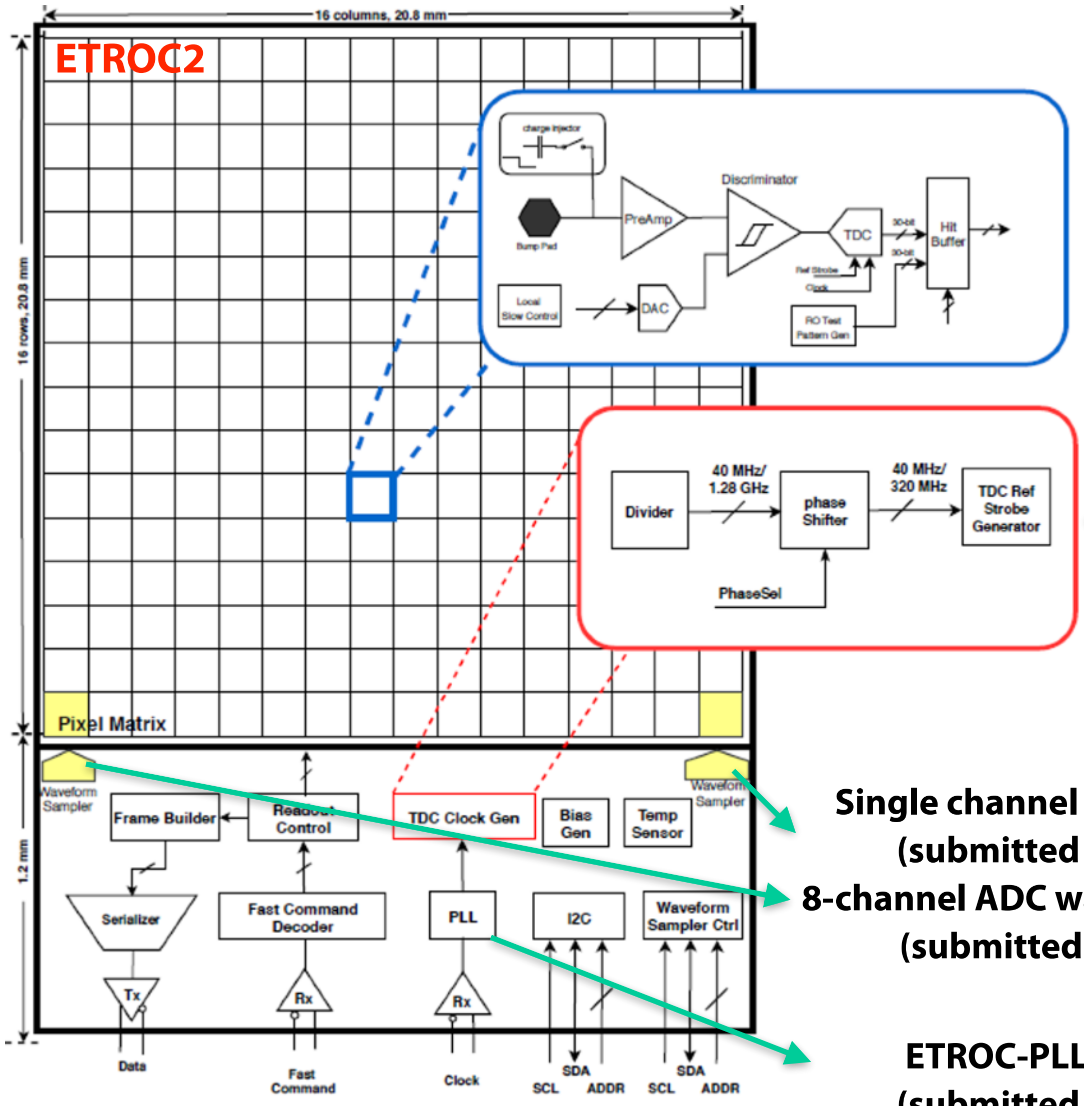
ETROC1 Test Board



- **Beam test at FNAL MTest**
- $\sigma_i = \sqrt{(\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2)/2}$ = **42 - 46 ps**

  (Time resolution of single LGAD+ETROC1)

Summary



Single channel ADC mini-ASIC (submitted May. 2019)

8-channel ADC waveform sampler (submitted Mar. 2020)

ETROC-PLL mini-ASIC (submitted May. 2020)

- ETROC0: front-end
  - Beam & TID tested
- ETROC1: front-end + TDC
  - Excellent TDC performance tested
  - Preliminary results promising, 40MHz noise under investigation
  - TID and SEU test to be done
- ETROC2: marching forward
  - All critical components are prototyped and work well
    - Waveform Sampler prototype chips
    - ETROC PLL Mini-ASIC chips
  - The rest of the digital circuitries & system interfaces: implemented/prototyped in firmware
  - Useful guide from ETROC1
    - to minimize 40MHz clock activities in the readout section

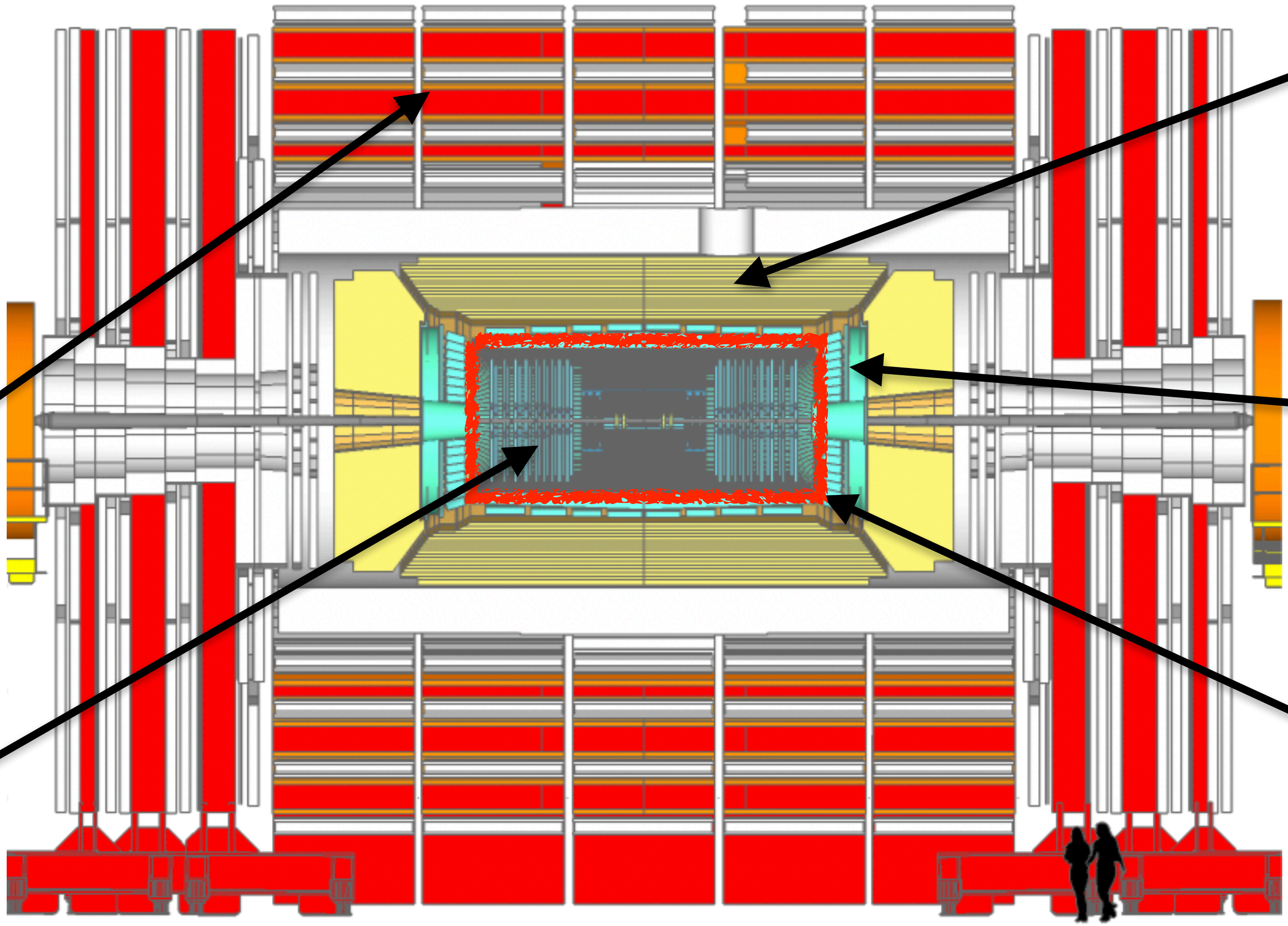
Thank you

CMS Phase-2 upgrades for HL-LHC

L1Trigger/ HLT / DAQ
- Track info. in L1 at 40MHz
- HLT rate: 100→750 kHz
- DAQ: 6→60 GB/s

Muon systems
- $|\eta| < 2.4 \rightarrow |\eta| < 3.0$

New Tracker
- High granularity
- Radiation tolerance
- $|\eta| < 2.4 \rightarrow |\eta| < 4.0$



Barrel calorimeters
- Replace FE/BE electronics

Endcap calorimeters
- Radiation tolerance
- High granularity

MIP Timing Detector
- Precision timing
- $|\eta|<3.0$