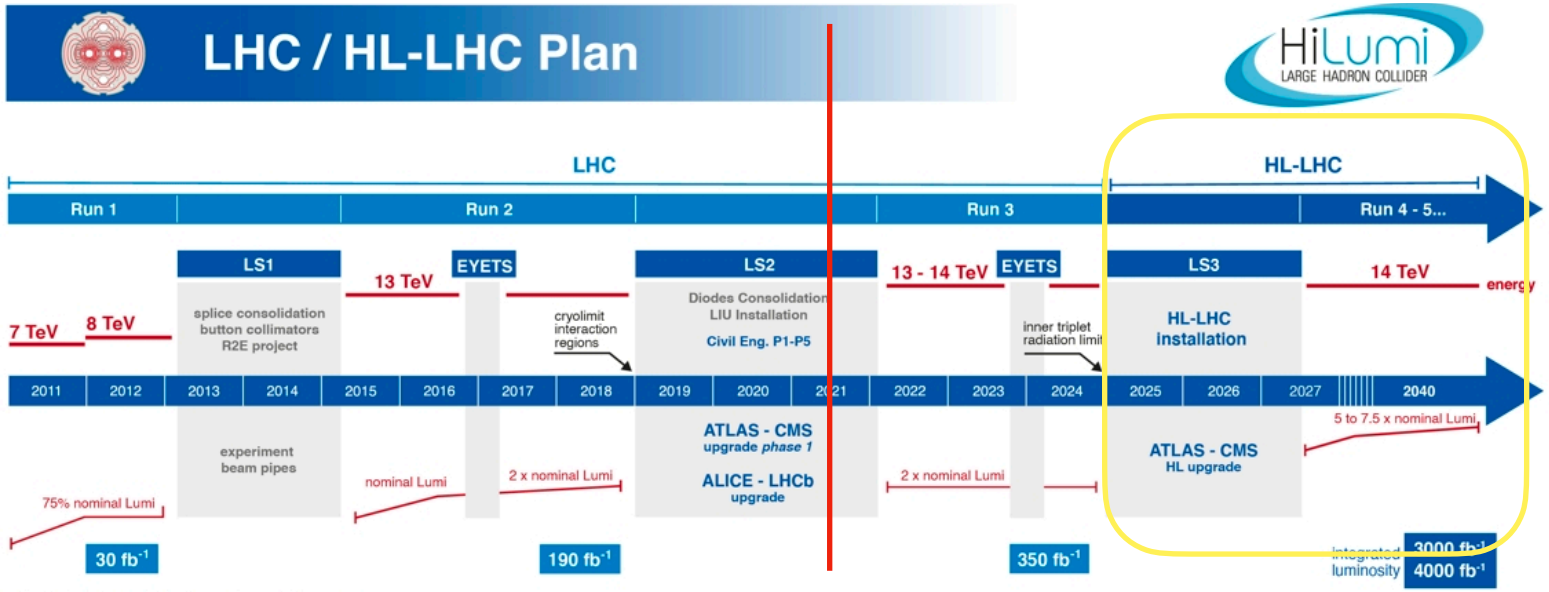
Electrical and functional performance of the first full loaded ITk Strip stave at Brookhaven National Laboratory

Francesca Capocasa
Brandeis University

2021 DPF Meeting

July 14, 2021

HL - LHC



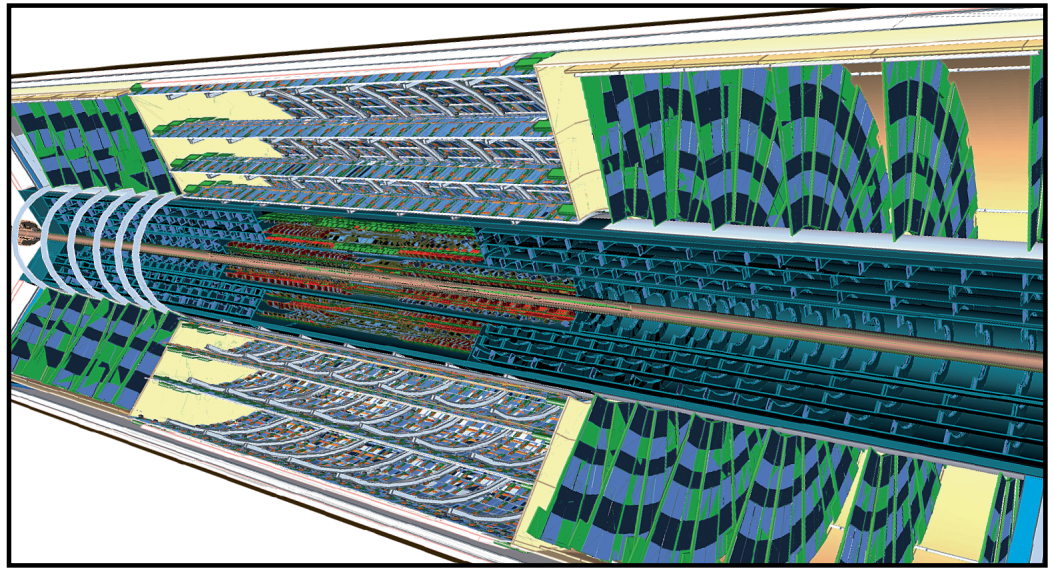
HL-LHC will deliver $\mathcal{L}_{peak}$ ~ 7.5 x 10^{34} cm^{-2} s^{-1}.

Super harsh environment for the current ATLAS Inner Detector (ID):

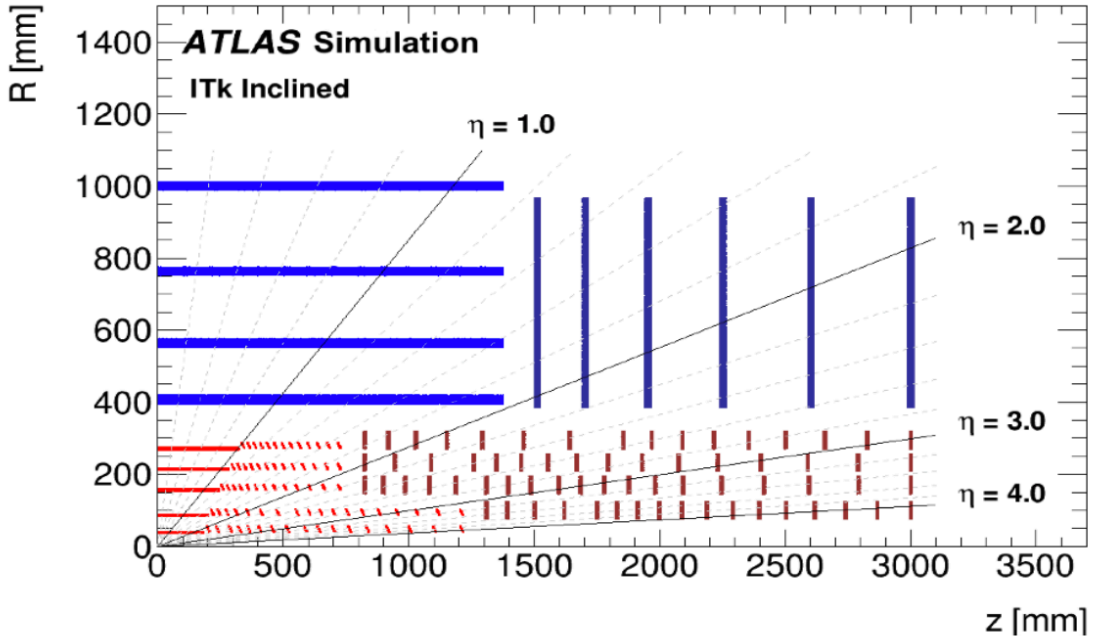
1. RADIATION DAMAGE: ID Pixel, SCT not designed to withstand the equivalent radiation damage. HL-LHC ~ 4000 fb^{-1}
2. PILE -UP: ID designed to accommodate a pile-up <μ> ~ 50, HL-LHC will have: <μ> ~ 200

The current ID will be replaced by an all-silicon Inner Tracker (ITk)

ITk Layout



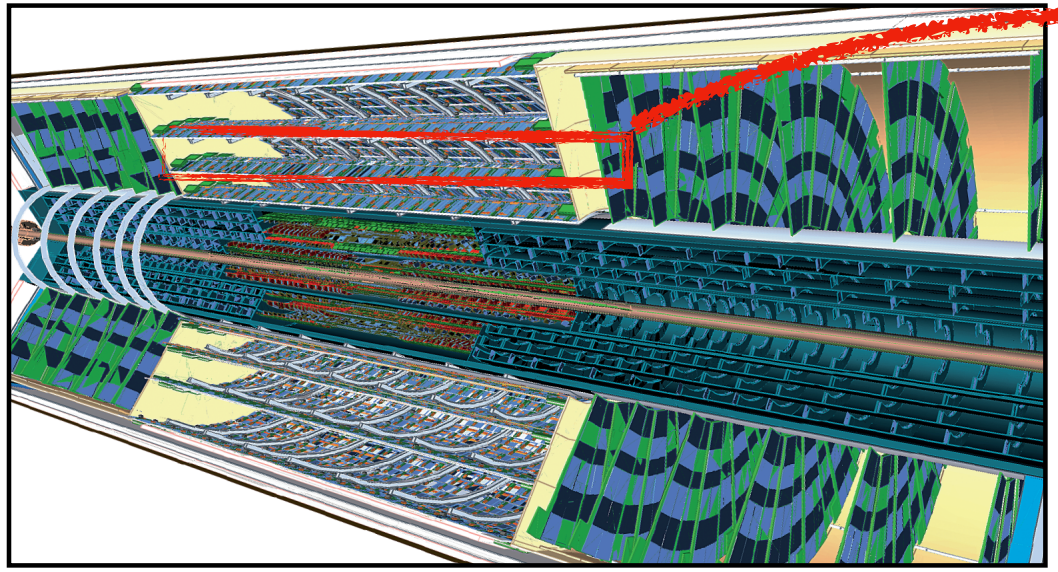
http://cdsweb.cern.ch/record/2257755/files/ATLAS-TDR-025.pdf

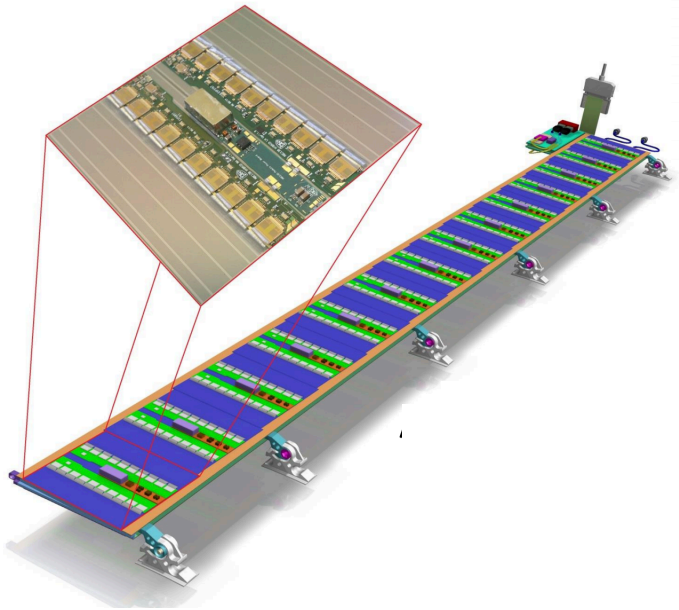


- ITK Pixel Detector
  - 5 barrel layers with inclined sensors in the forward region
  - End-Cap (EC) system containing individually located rings
- ITK Strip Detector
  - 4 barrel layers
  - 6 EC rings on both forward regions

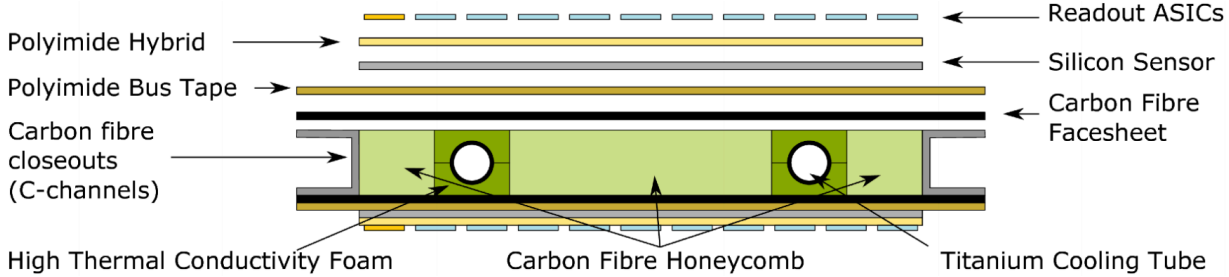
Brookhaven National Laboratory responsible for assembling and testing of half of the ITK's Strip Barrel Detector base units, the staves

Silicon Strips Stave





- Staves are the basic units of the ITk Strip Barrel detector
- It is made of a 1.4 m long support structure
  - provides **mechanical rigidity and support** by using high stiffness and high thermal conductivity carbon fiber
  - Provides **cooling** to modules
  - Polyimide bus-tape is co cured on both faces to channel power and data from and to the modules .
- 14 silicon modules are directly glued on both sides of the stave support structure



Silicon Strips Modules

- The units of the staves are the silicon modules
  - 2 module variant for ITk Barrel Detector having same architecture but different geometries

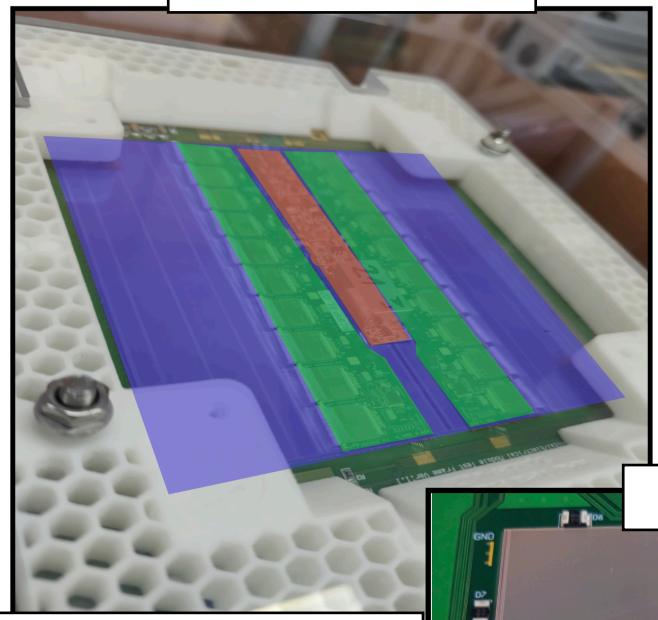
- Consists of one sensor and one or two low mass PCBs, called hybrids, and one power board

- The hybrid hosts the readout ASICS:
  - 10 front-end ABCStar chips and a control chip HCCStar
  - Each ABCStar has 256 strips channels
  - Each ABCStar has a point-to-point data path to the HCCStar, enabling fast readout

- Power board:
  - Has a DC-DC buck converter to step down the LV to 1.5 V used by front-end ASICs
  - Delivers the HV bias voltage (-400V)
  - Hosts a monitoring chip called AMAC

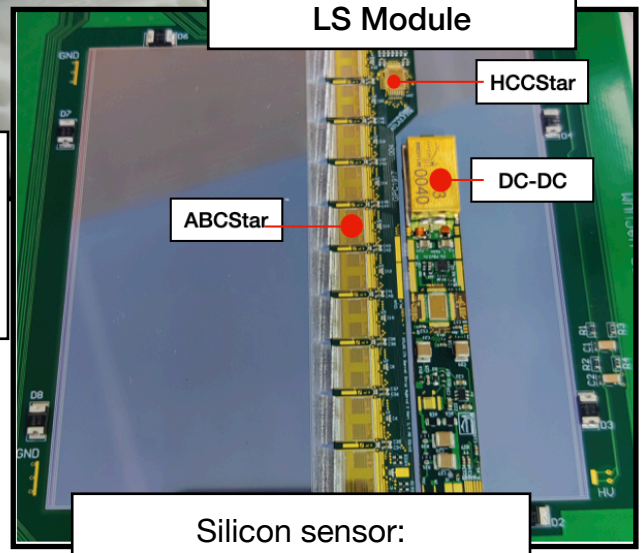
More information in the next talks

SS Module



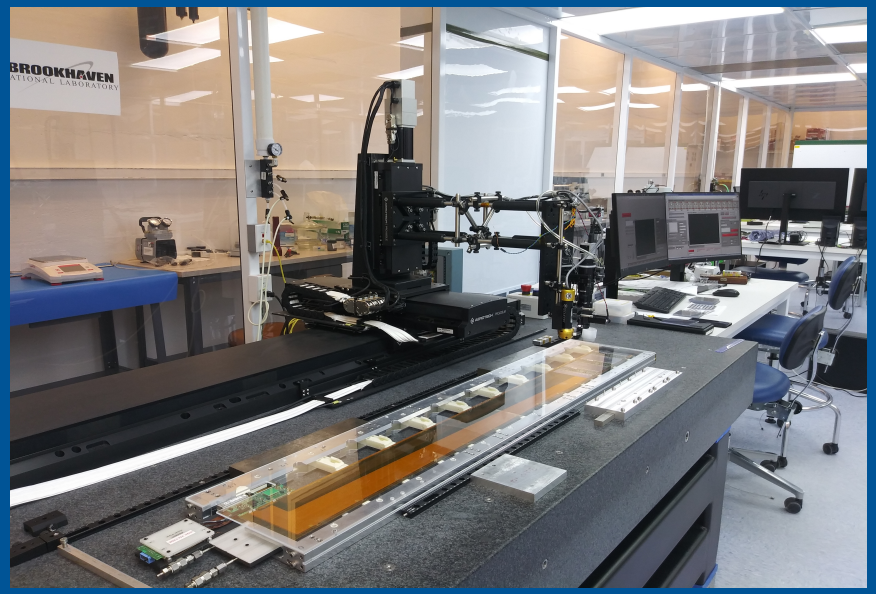
Silicon sensor: 4 rows of Short Strips
(24.10 mm) for higher occupancy regions

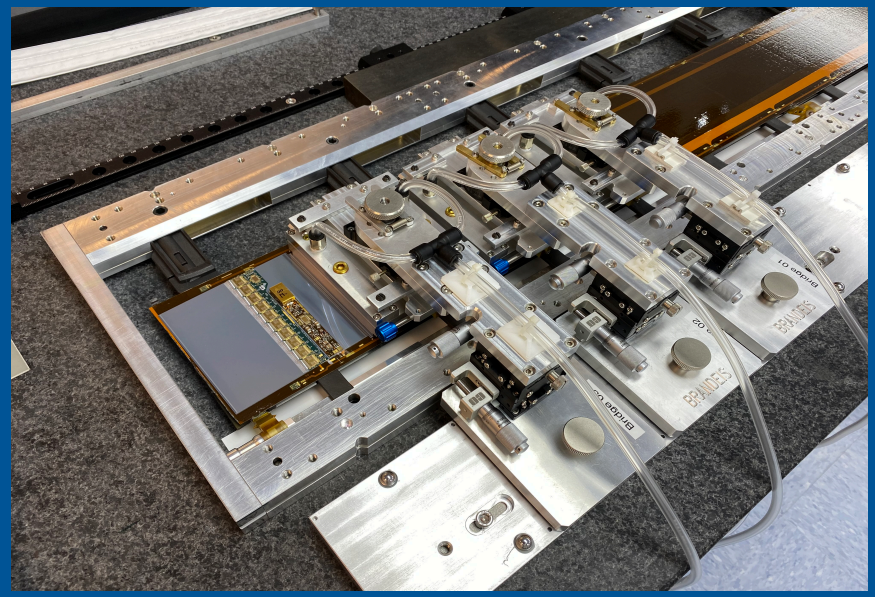
LS Module



Silicon sensor:
2 rows of Long Strips
(48.20 mm)

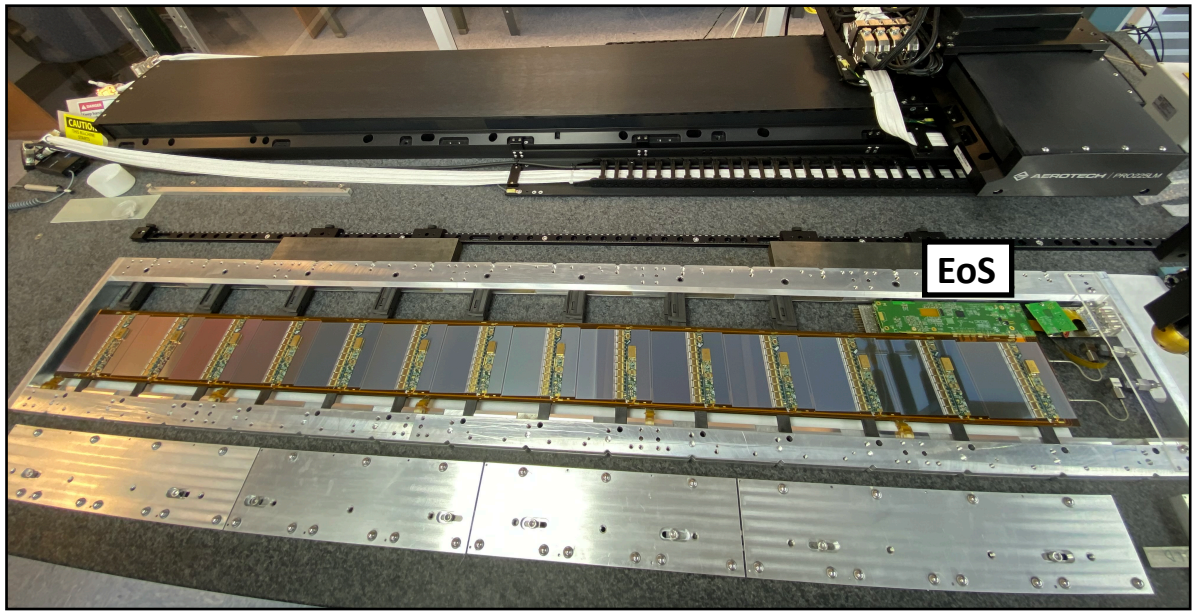
ITk Layout - Stave Assembly

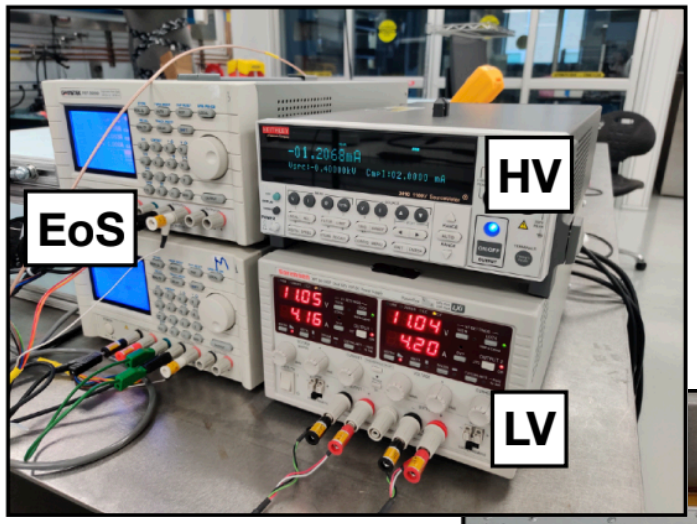


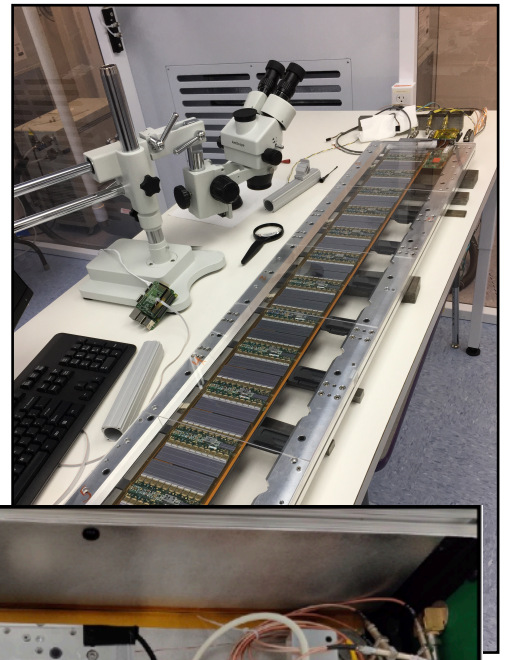


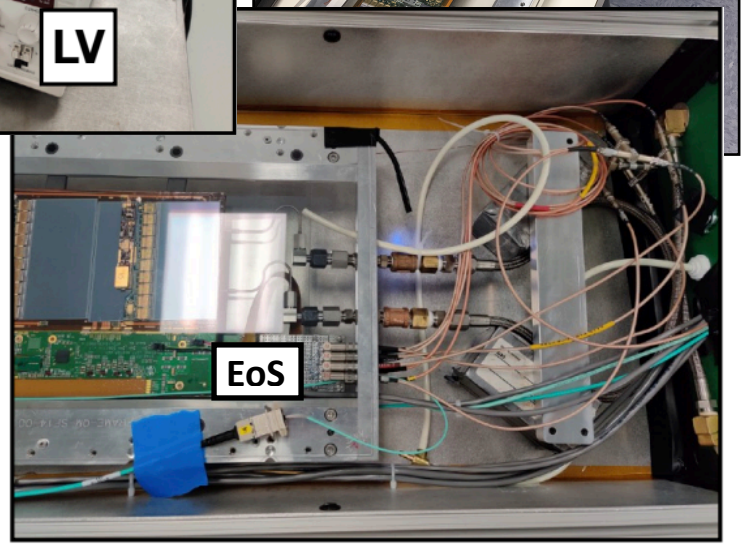
- Granite Table + XYZ stage that holds a 10-megapixel camera
- Fiducial marks on silicon sensor and reference point on stave core are used to reconstruct modules positions
- Modules directly mounted onto the stave core using thermal conductive glue (SE 4445)
- Vacuum Pick-up tools (bridges) with adjustment mechanism allows to guarantee in-plane position of the modules (<50um)

Stave Testing









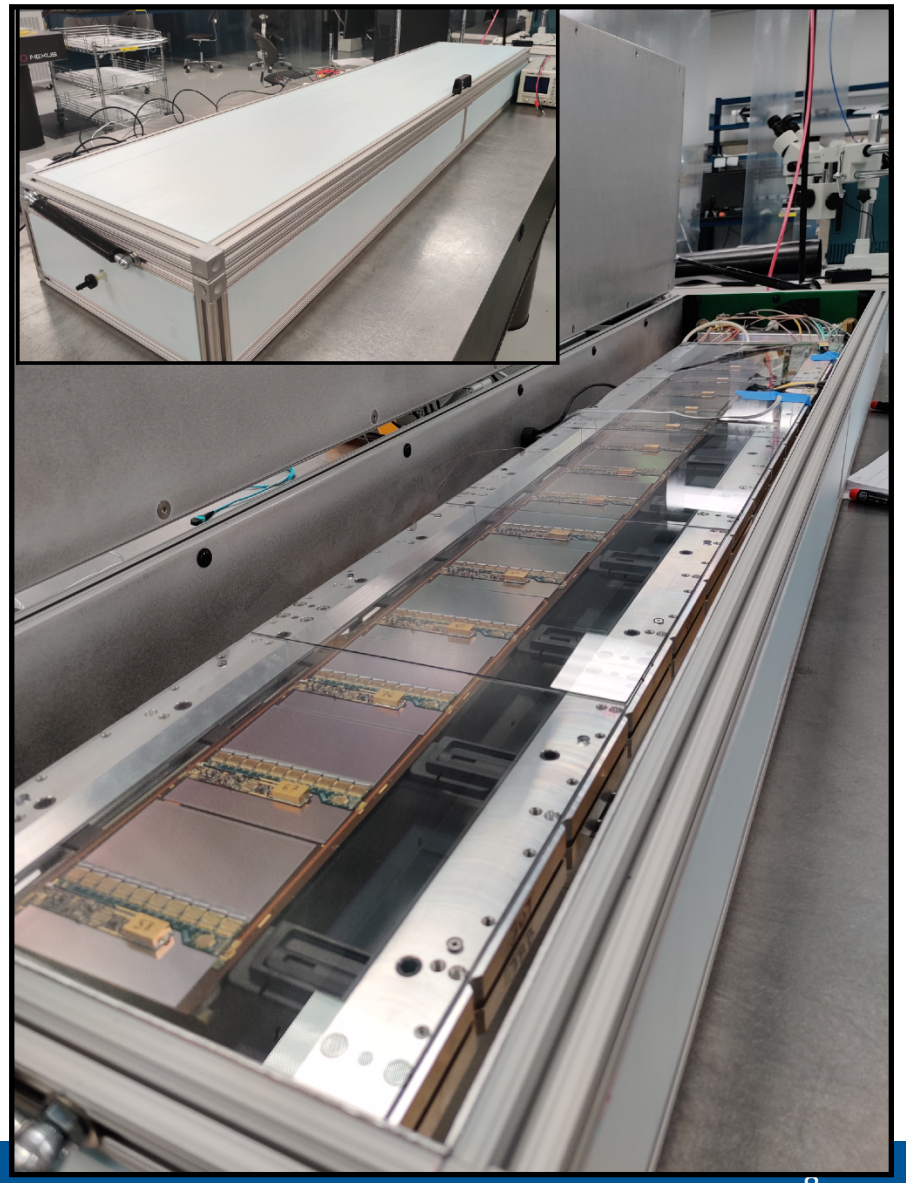
- First double-sided electrical stave with 28 long strip modules assembled at BNL at the end of 2019
- Of the 28 modules, 9 were built at BNL, 9 at LBNL and 10 at UC Santa Cruz

- End of Stave Card (EoS) board contains radiation hard lpGBT ASIC and VTRx+ fibre optics which serialize the data and drives the optical connection
- Data readout by an FPGA (Genesys 2) , connected to a PC through Ethernet

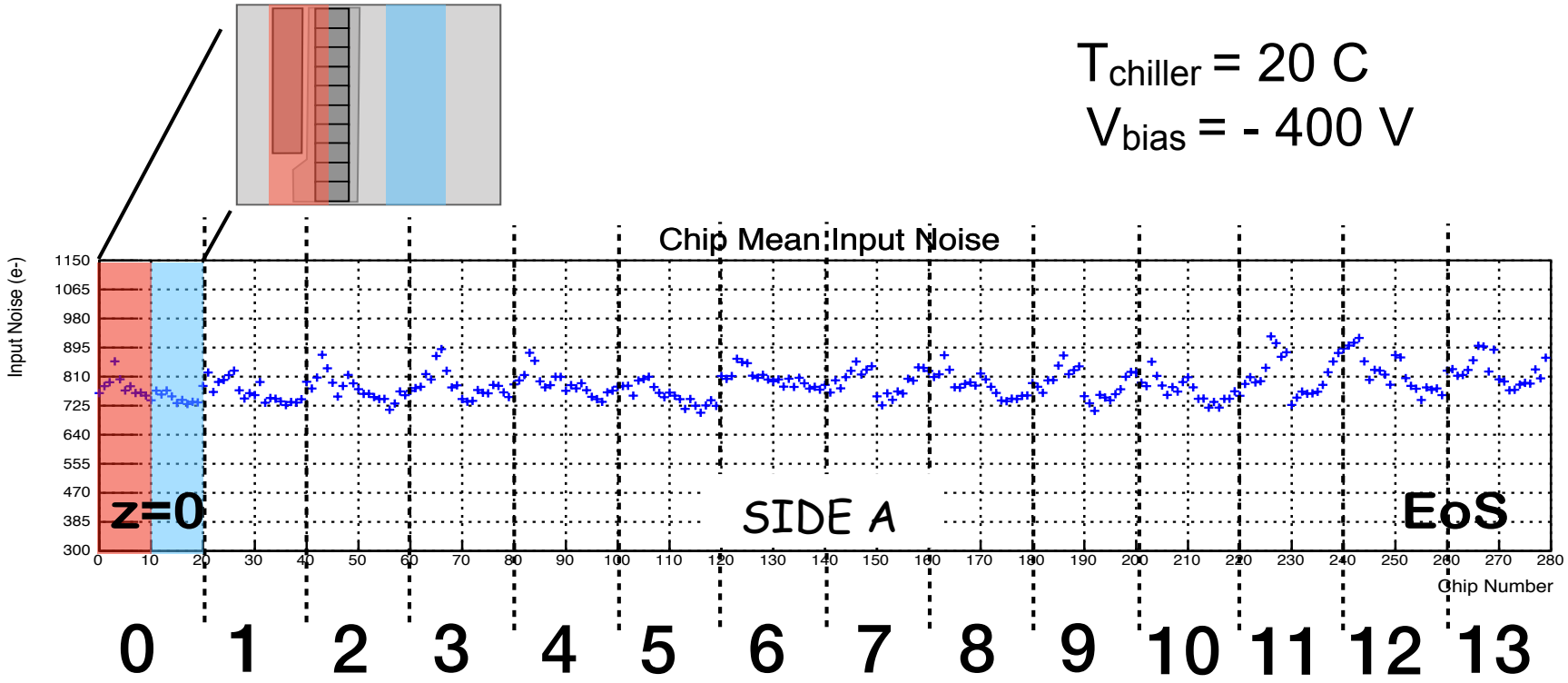
Stave Testing - Cold box

- Stave cold box to to facilitate thermal cycling and electrical tests at expected operating temperature
- Two humidity sensors (SHT85) and two temperature sensors (NTC 10k) readout by a Raspberry pi, monitored with web interface
- Dry air flushing ~ 20 SCFH
- SPS chiller + booster pump
- ~15C temperature gradient between chiller and stave inlet when running cold

$T_{setpoint}[^\circ C]$	$T_{chiller}[^\circ C]$	$T_{inlet}[^\circ C]$	$T_{outlet}[^\circ C]$	Pressure[PSI]
40	42.8	49.1	46.8	180
30	29.6	36.9	36.2	165
20	22.9	29.9	29	150
10	18.5	23.9	22.8	150
0	8.3	13.9	13.2	130
-10	-1.3	5.4	5.3	120
-20	-19.3	-6.6	-4.8	110
-30	-24.3	-14.6	-13	110
-40	-40.3	-26	-22.3	110
-50	-50.5	-35.5	-30.9	110
-60	-60.9	-45.8	-40	120
-60	-60	-45.6	-40.8	140
-60	-58.8	-45.6	-40.9	150
-60	-58.6	-44.4	-40.4	180

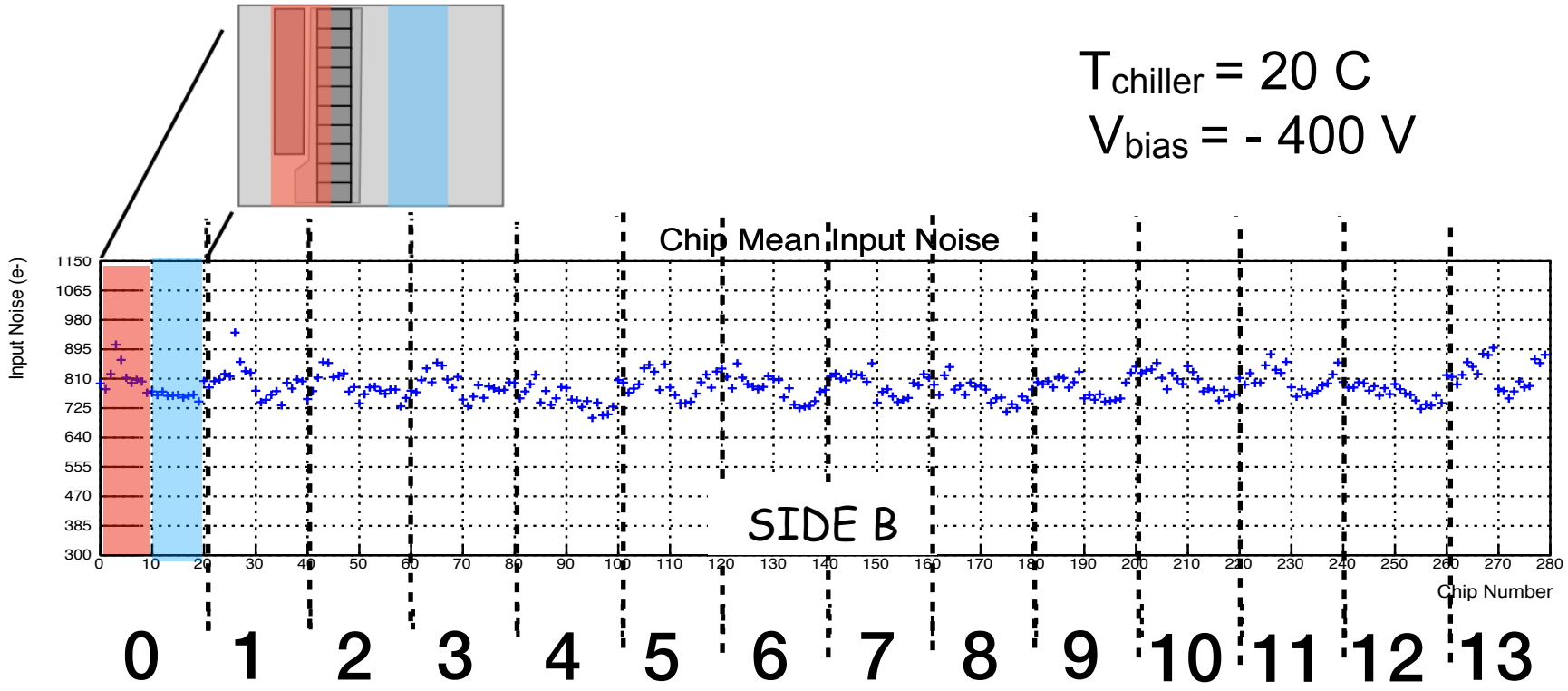


Room Temperature Results - Input Noise



- Input noise profile for all 14 modules on one stave side at Room Temperature
- Each point represents the mean of the input noise of 128 strips channels

Room Temperature Results - Input Noise

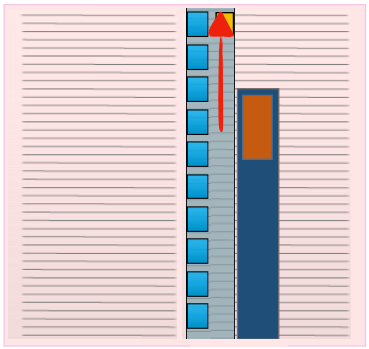


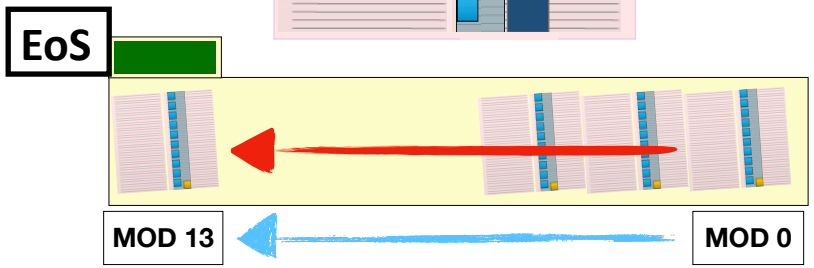
Input noise profile for all 28 modules on the stave at Room Temperature
Each point represents the mean of the input noise of 128 strips channels
All 28 modules and 280 ABCStar Chips are working properly!
Strip modules of several generations (ABCN25, ABC130, ABCStar) had been tested cold before showing good performance. We had no reason to suspect a complete stave would behave differently…**BUT**…..

Cold Temperatures Results - Input Noise

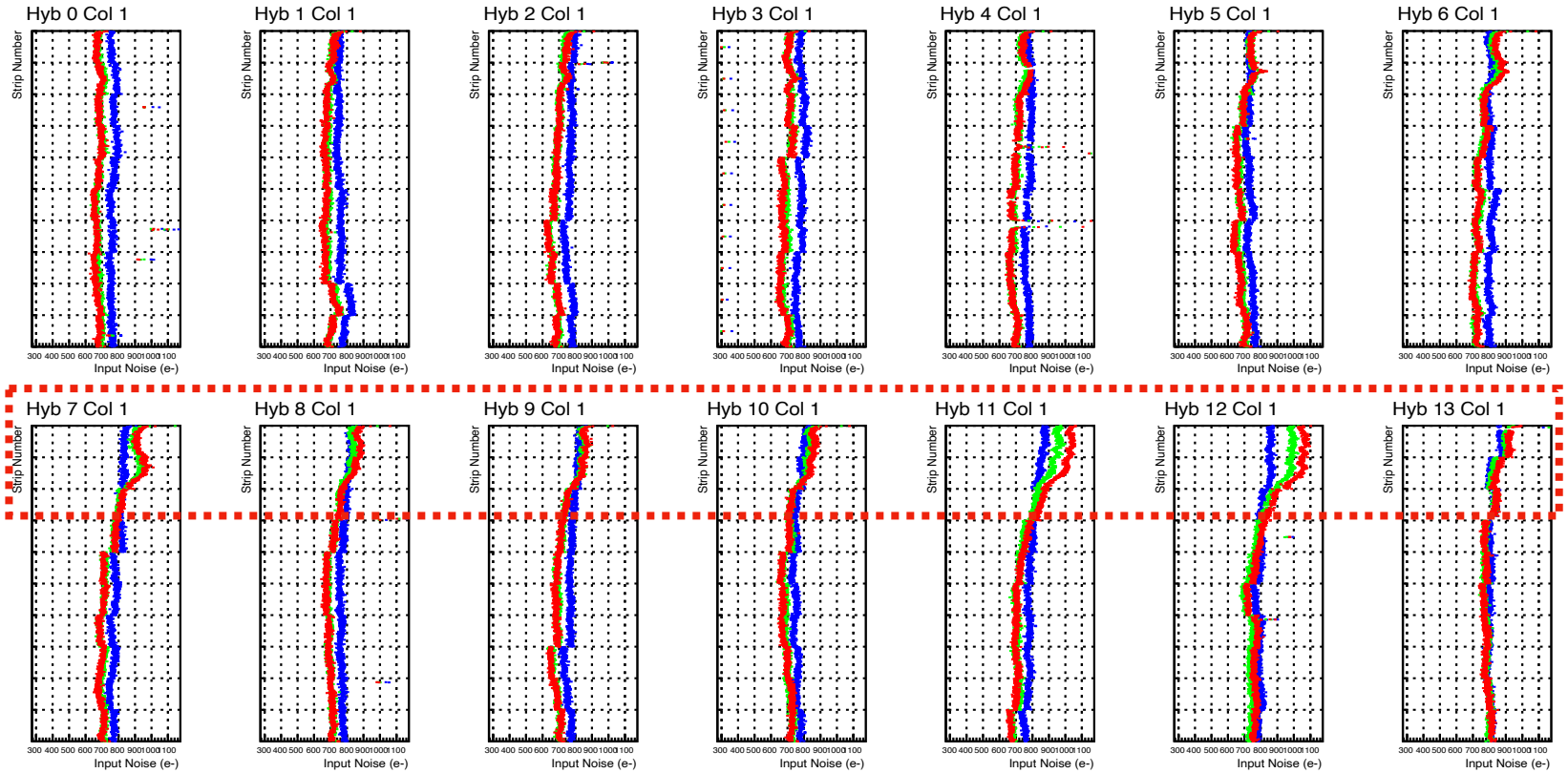
$T_{chiller}$ = 20 C, -40 C, -50 C
V_{bias} = - 400 V

- Input response for the 14 modules on one side of the stave
- Contrary to expectations, noise increases as temperature decreases in the upper half of the hybrid
- Noise increases towards the EoS card
- Same behavior for the other side of the stave





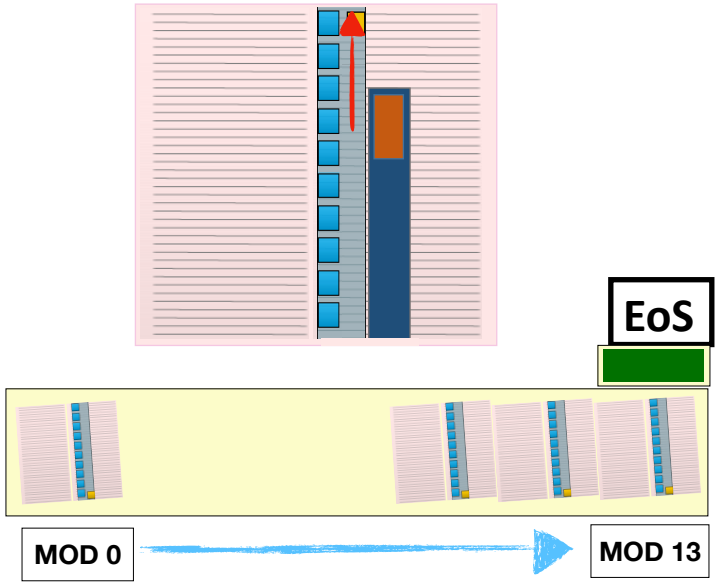
SIDE A



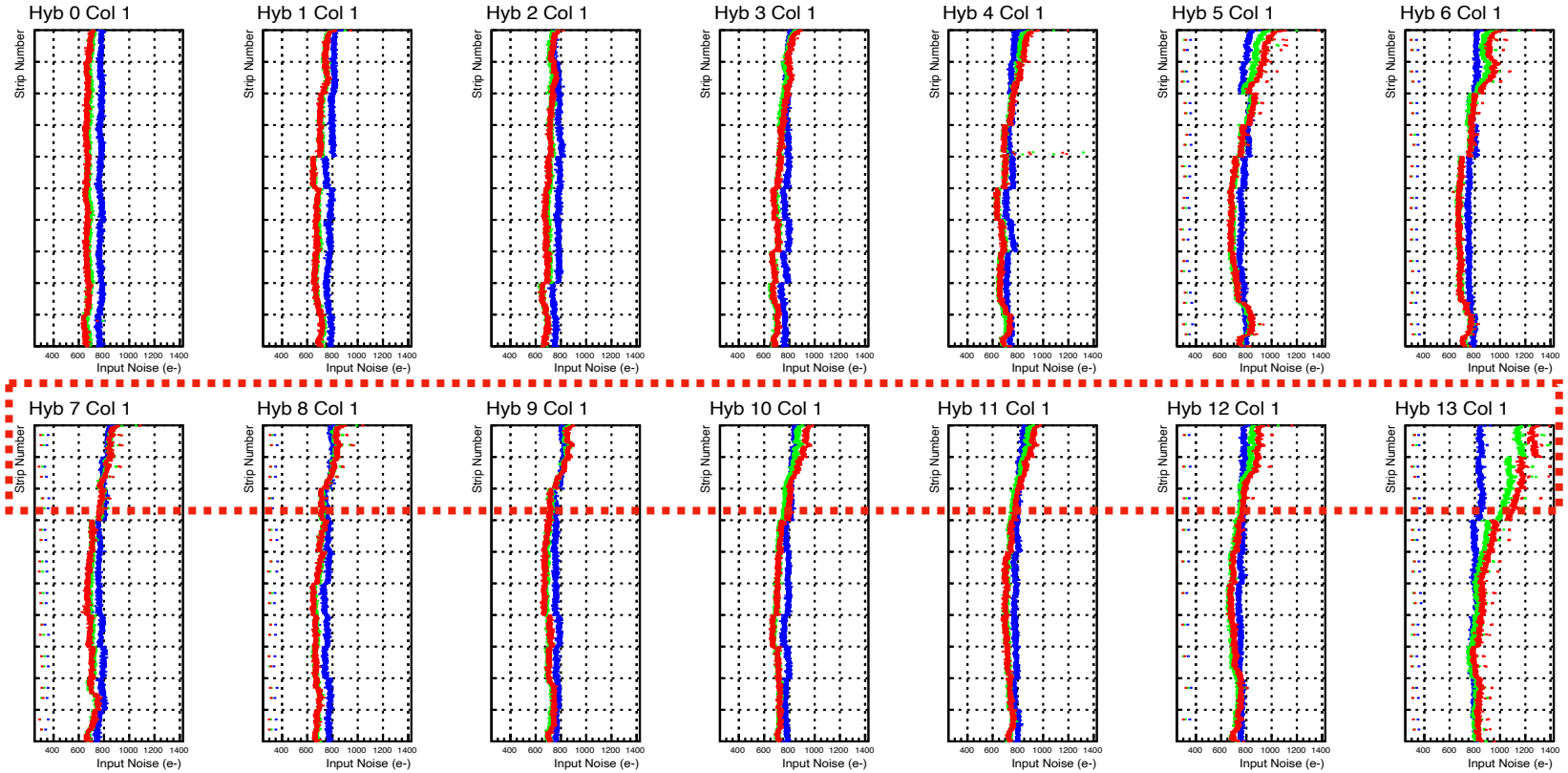
Cold Temperatures Results - Input Noise

$T_{chiller}$ = 20 C, -40 C, -50 C
V_{bias} = - 400 V

- Input response for the 14 modules on side B of the stave
- Same behaviour as for side A



SIDE B



To address this problem, several investigations have been performed….

Signal Ground Bonds OFF - Input Noise

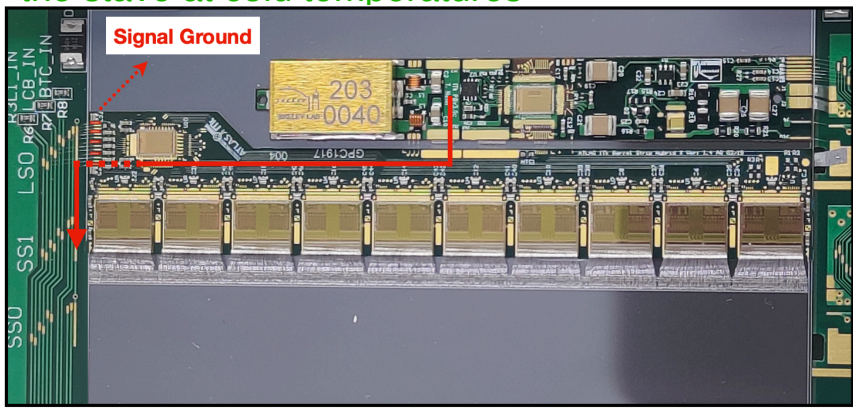
$T_{chiller}$ = -50 C

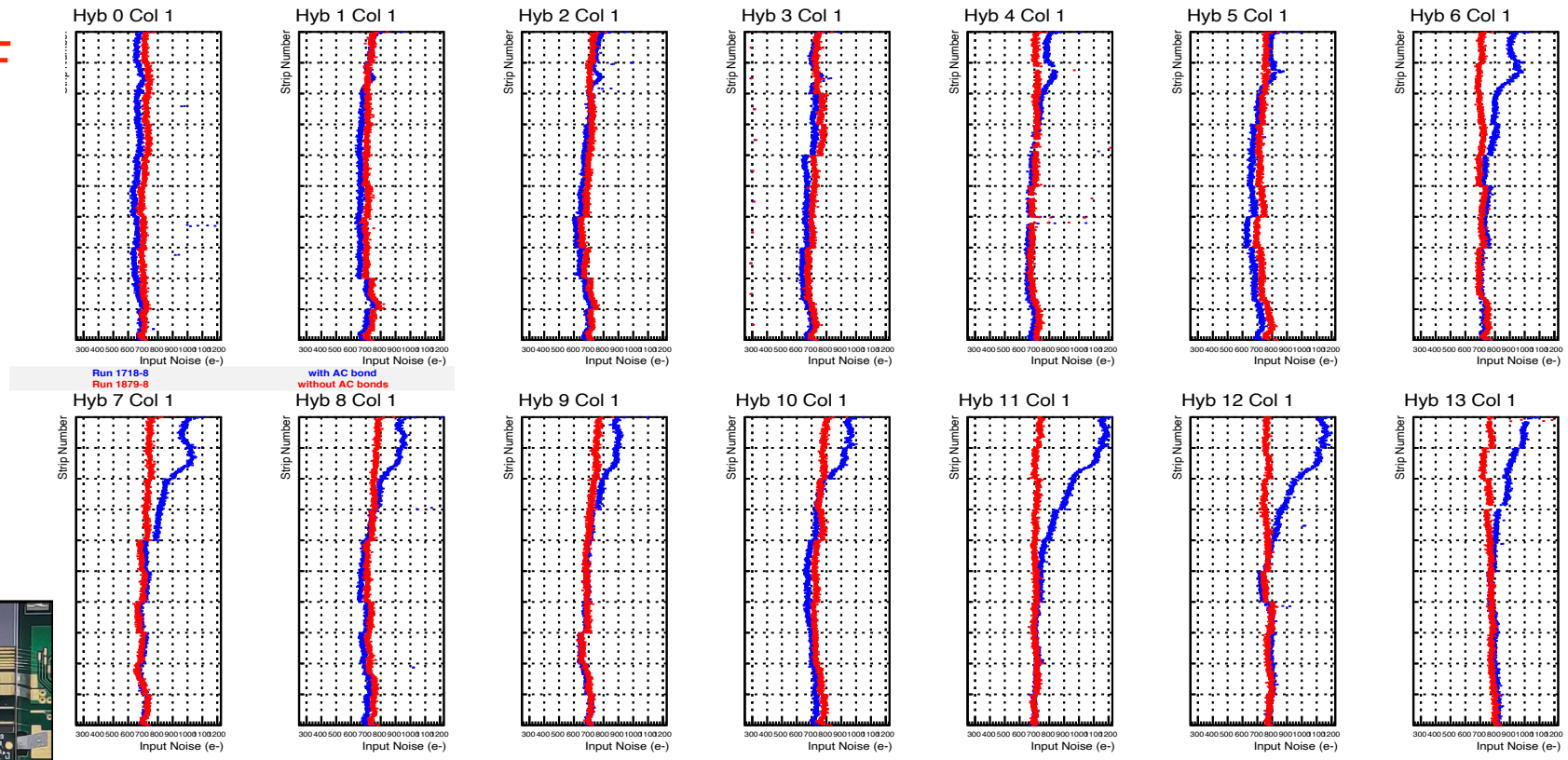
Signal Ground Bonds ON, OFF

V_{bias} = - 400 V

- The signal ground bonds on the hybrid can provide a path for noise current to flow in the upper half of the hybrid
- The removal of these bonds made this noise increase in the upper half of the hybrid disappear

- Removal of the signal ground bonds demonstrated to ensure good performance of the stave at cold temperatures



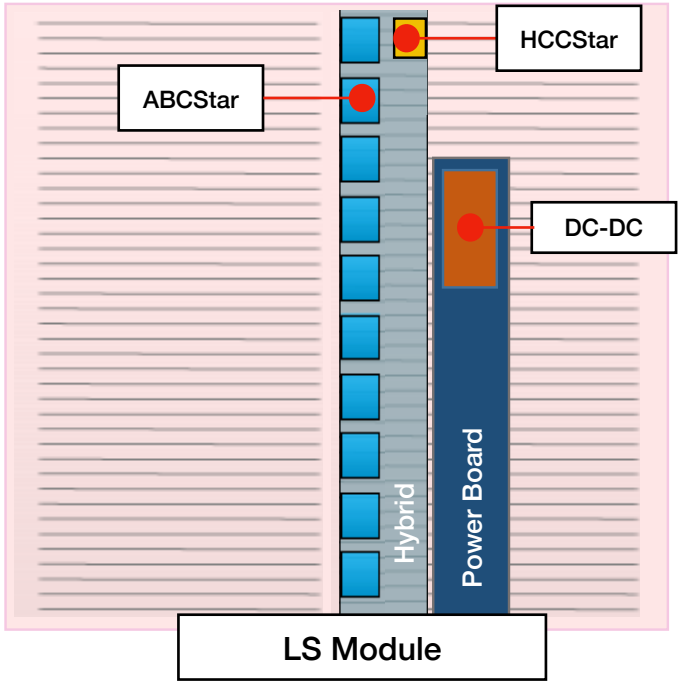


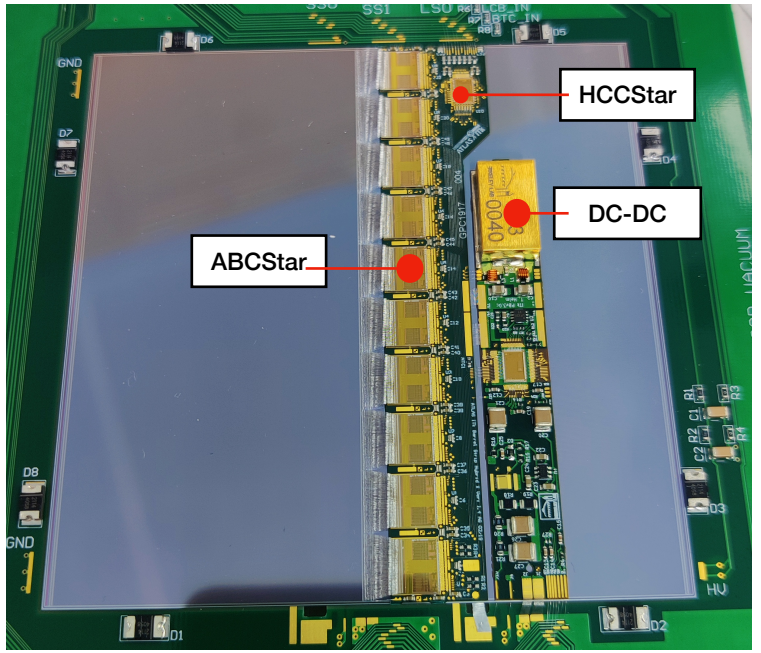
Summary

- To cope with larger radiation from the High Luminosity LHC, ITk will replace the current Atlas Inner Detector
- The inner layer will be made of silicon pixel detectors while the outer layer will be made of strips detectors
- The base component of the barrel Strip detector is the stave that houses silicon modules
- The first electrical double sided electrical stave assembled and tested at Brookhaven National Laboratory
- Unexpected increase of the noise found while testing the stave at cold temperatures. Solved by removing the fast signal ground bonds. This solution has been approved for the next generation of staves

Backup Slides

ITk Layout - Modules





Hybrid

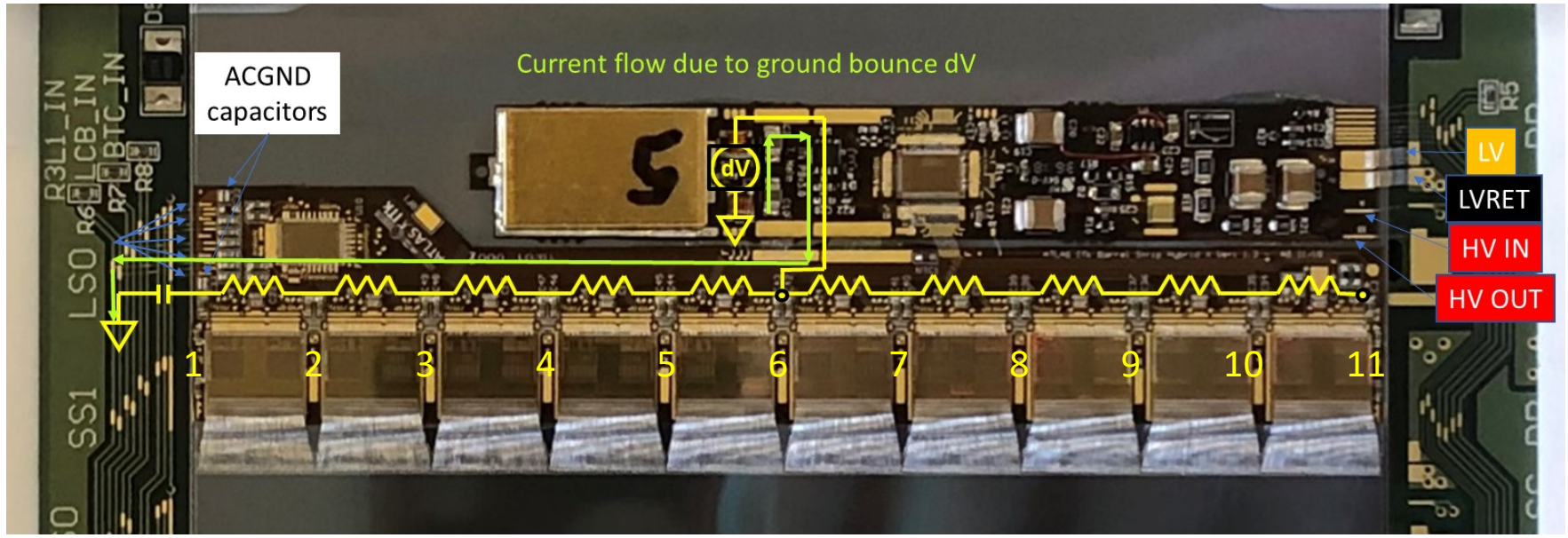
- Each hybrid has 2560 strip channels!
- Each hybrid hosts 10 from-end chips (ABCStar) and a control chip (HCCStar)
- Each ABCStar has 256 strip channels

- Each ABCStar has a point-to-point data path to the HCCStar, enabling fast readout

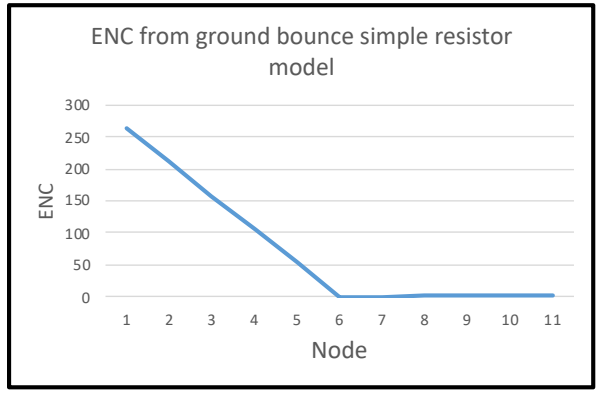
Power Board

- To minimize the material inside the tracker and to avoid extra cables, a DC-DC conversion powering scheme is used
- DC-DC converter : buck regulator used to step down the LV (11V) to 1.5 V used by front-end ASICS
- It uses an air core solenoid enclosed by a 100 um aluminium shield-box (shield EMI emission)
- The power board delivers also HV depletion voltage (- 400V)

BNL Model

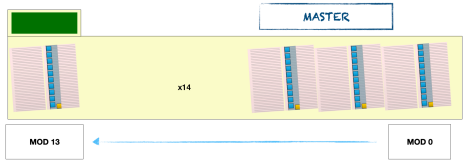


See Ltspice simulation in backups



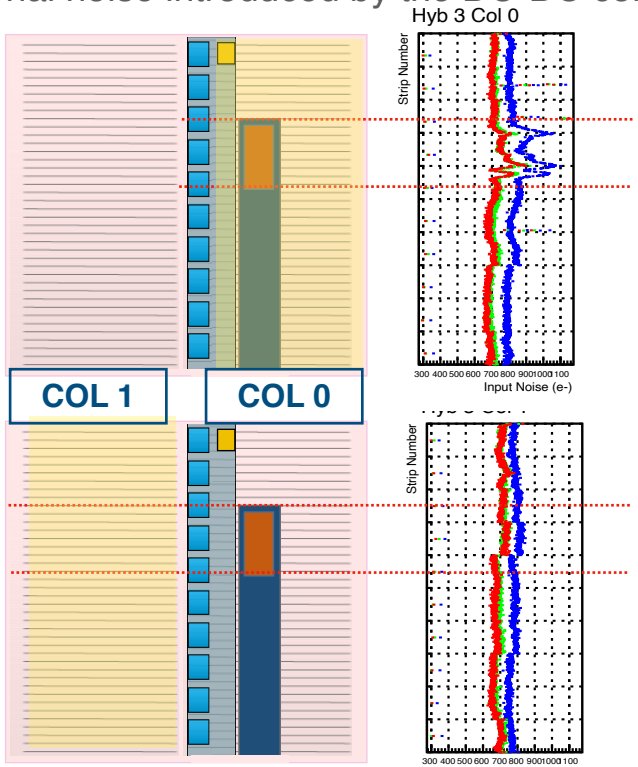
- DC-DC converter introduces a ground bounce(dV) at every clock cycle
- Ground bounce causes current flows through AC ground bonds connecting the hybrid ground to the bus tape ground.
- The current will create a position dependent voltage difference in the upper half of the hybrid, responsible to inject charge into the front-end channels
- Simple LTSpice simulation return a noise pattern similar to the one observed on the stave
- Further investigation needed

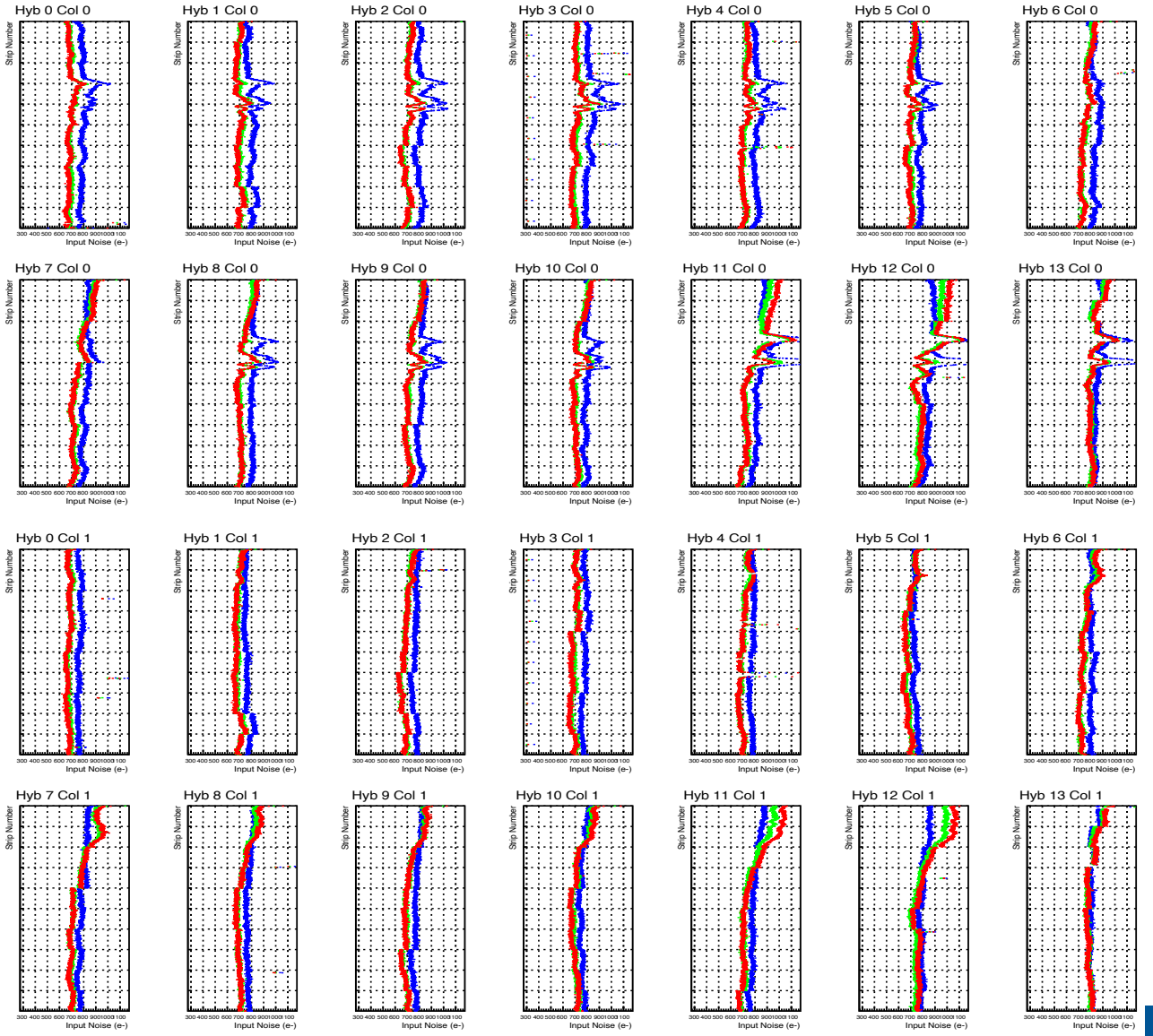
Cold Temperatures Results - Input Noise



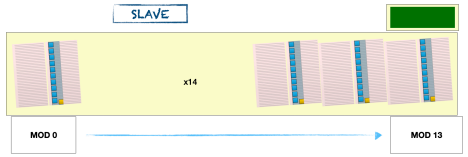
$T_{chiller}$ = 20 C, -40 C, -50 C
V_{bias} = - 400 V

- Input response for the 14 modules on the **MASTER** side
- Input noise for both rows of strips
- Bump observed in the central area (col 0 strips) due to additional noise introduced by the DC-DC converter





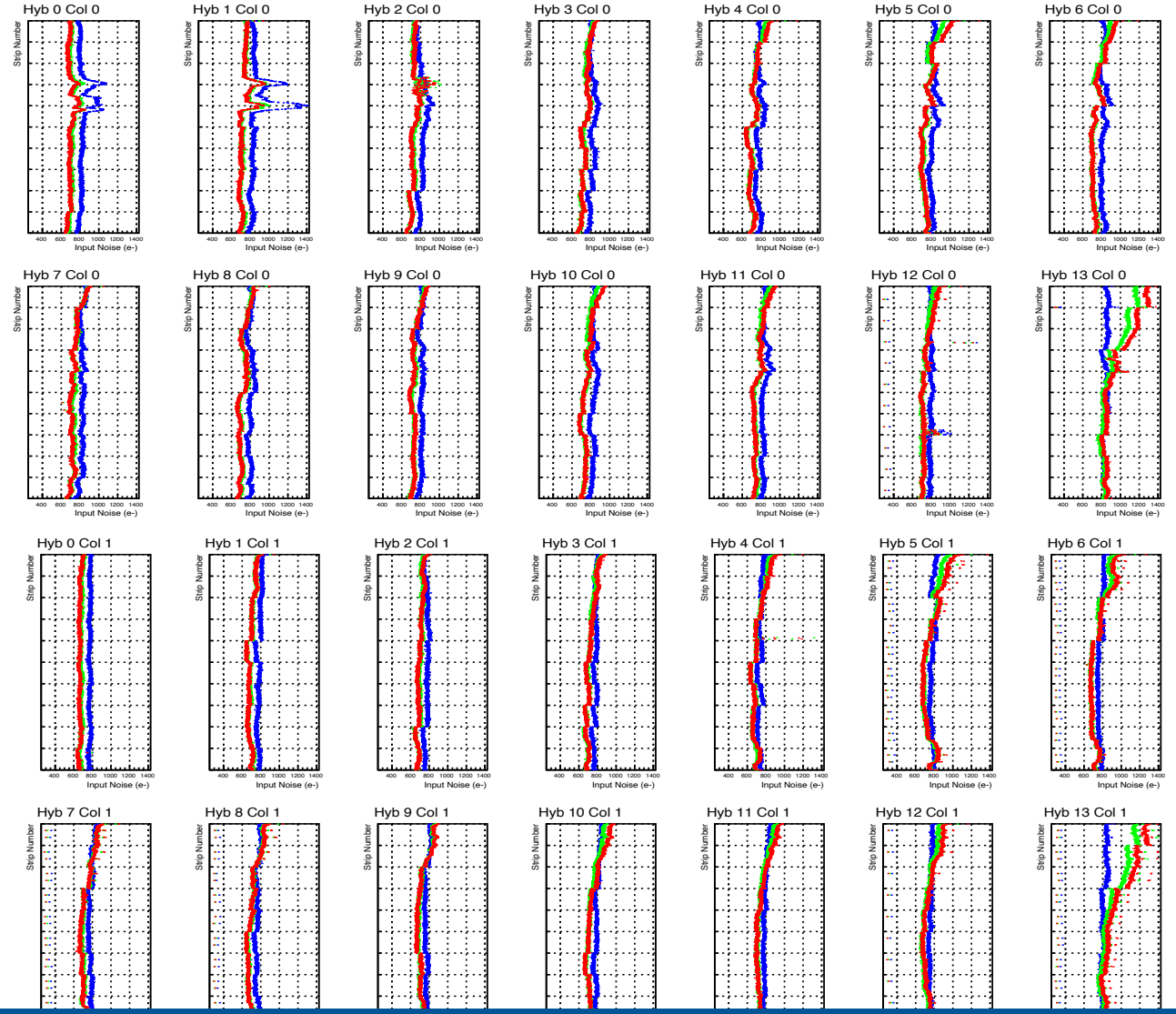
Cold Temperatures Results - Input Noise



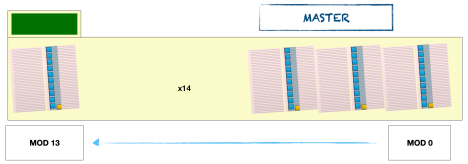
$T_{chiller}$ = 20 C, -40 C, -50 C

V_{bias} = - 400 V

- Input response for the 14 modules on the **SLAVE** side
- Input noise for both rows of strips
- DC-DC Bump observed only in the first two modules
- Other modules have a better shielding (new power board version)



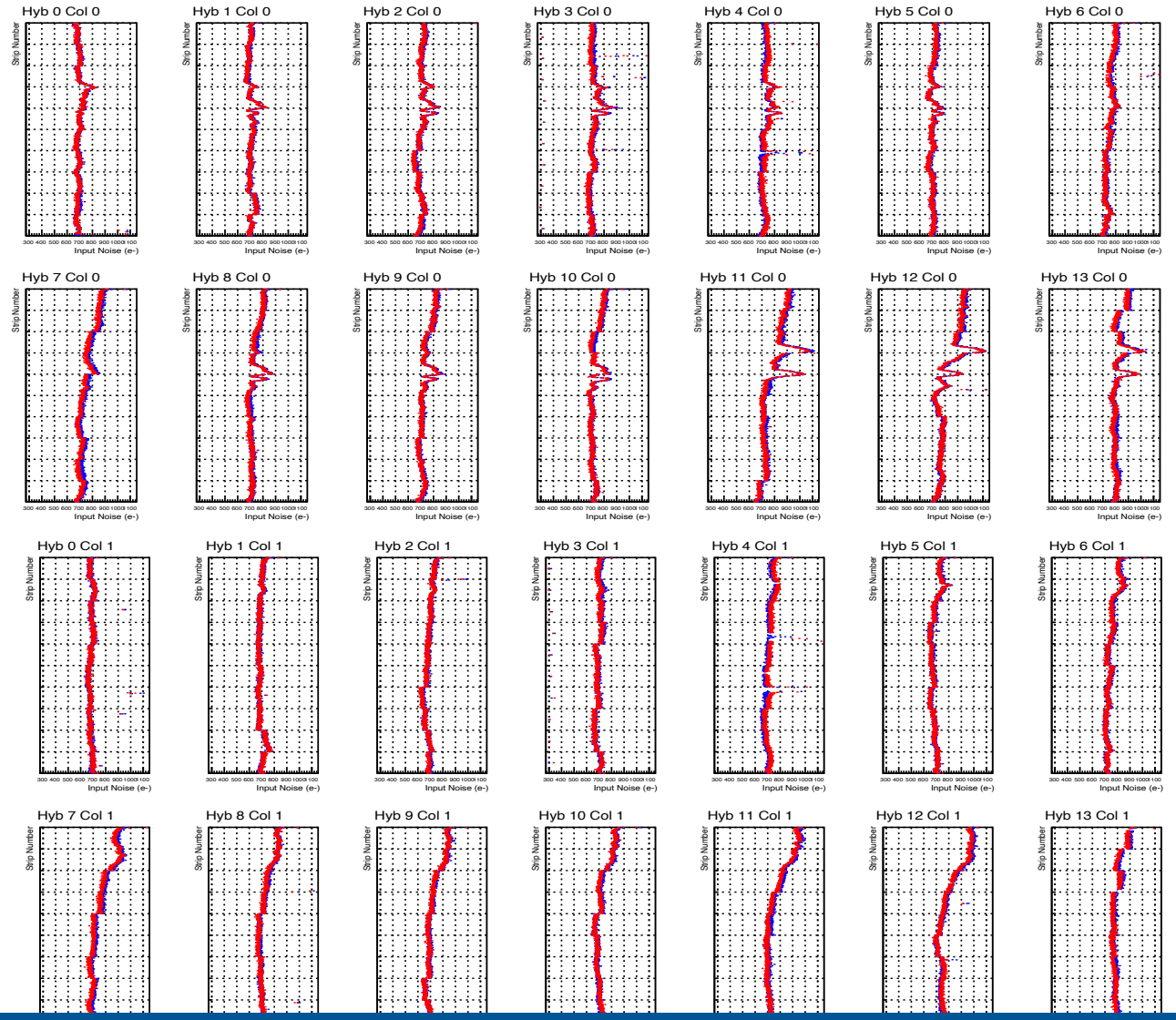
HV Scan - Input Noise



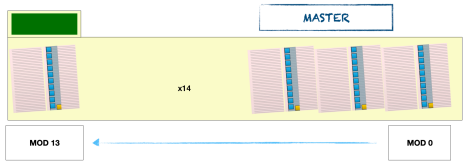
$T_{chiller}$ = -50 C

V_{bias} = - 400 V, -500 V

- First test evaluates the dependence of upon input noise upon depletion voltage
- Applied -500V to over - depleted the silicon sensors
- Input voltage for all the 14 modules on the **MASTER** side
- No difference observed in the noise response
- Same trend also for slave side (backup slides)



DC-DC Input Voltage - Input Noise



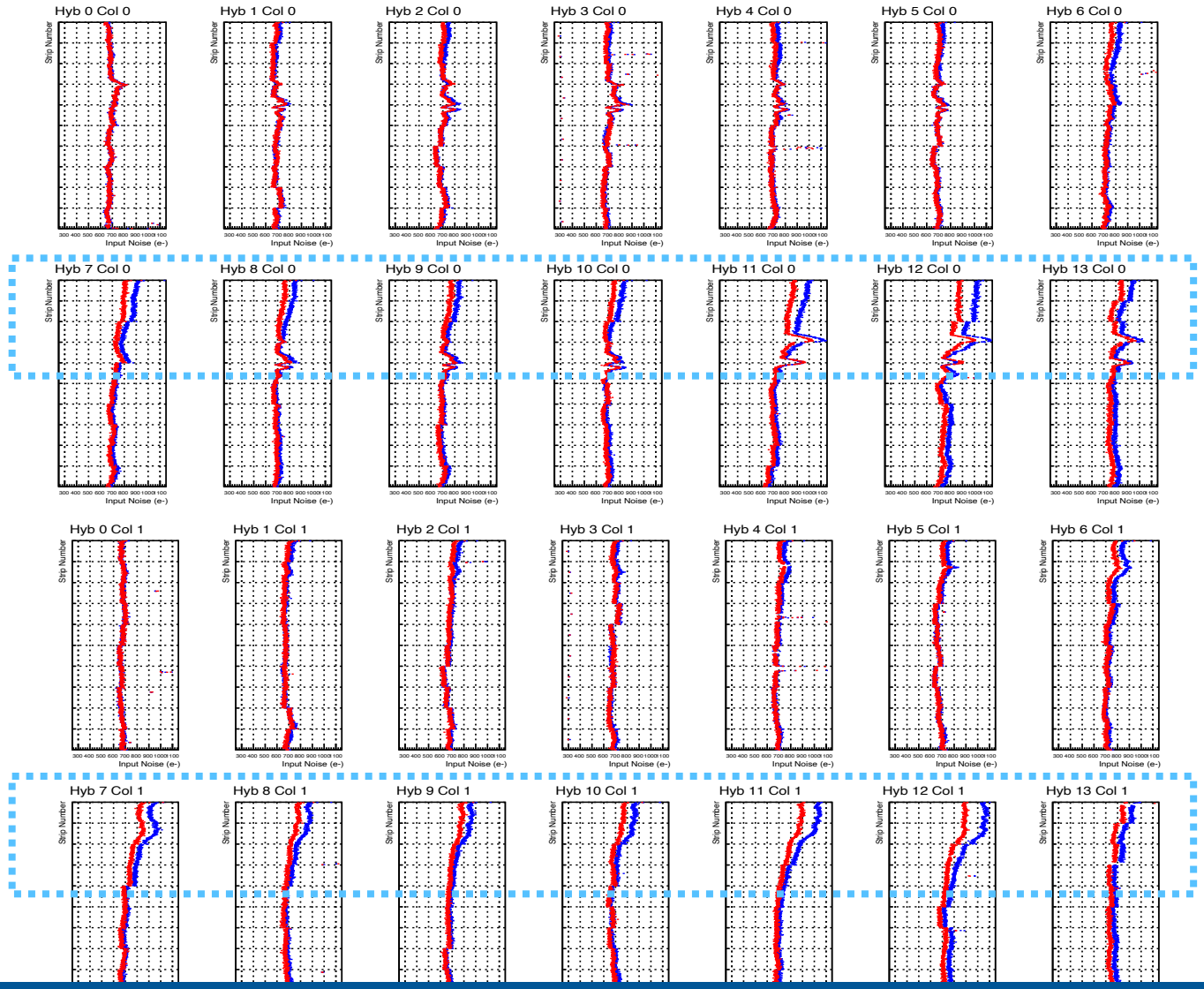
$T_{chiller}$ = -50 C

LV (DC-DC input) = 11 V, 10 V

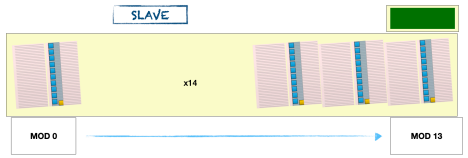
V_{bias} = - 400 V

- Investigate dependence of input noise upon LV power
- Lowered the DC-DC input voltage from 11 V to 10 V
- Input voltage for all the modules on the **MASTER** side

- Reducing input voltage to the DC-DC converter reduces noise increase in the upper half of the hybrid



DC-DC Input Voltage - Input Noise



$T_{chiller}$ = -50 C

LV (DC-DC input) = 11 V, 10 V

V_{bias} = - 400 V

- Investigate dependence of input noise upon LV power
- Lowered the DC-DC input voltage from 11 V to 10 V
- Input voltage for all the modules on the **SLAVE** side

- Reducing input voltage to the DC-DC converter reduces noise increase in the upper half of the hybrid
- Same trend also for slave side