The AMAC ASIC for the ATLAS ITk silicon strip detector

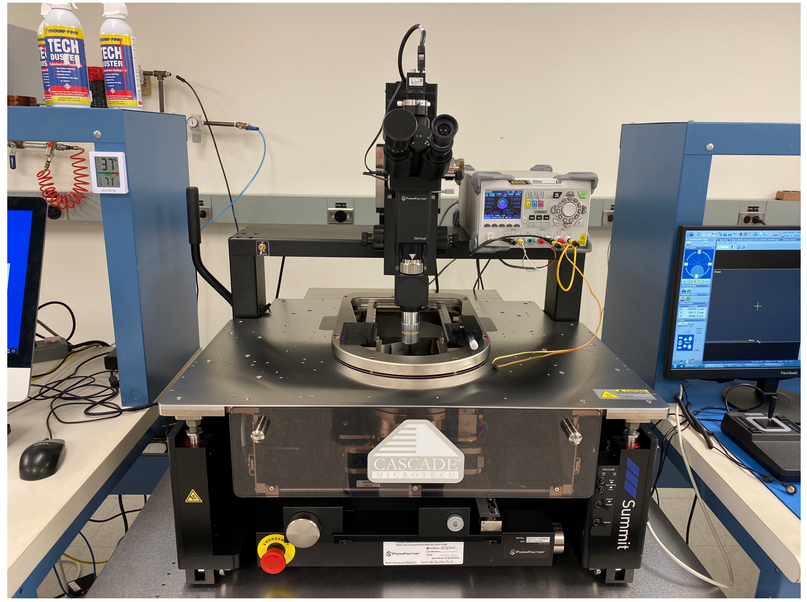
Results of prototype wafer testing

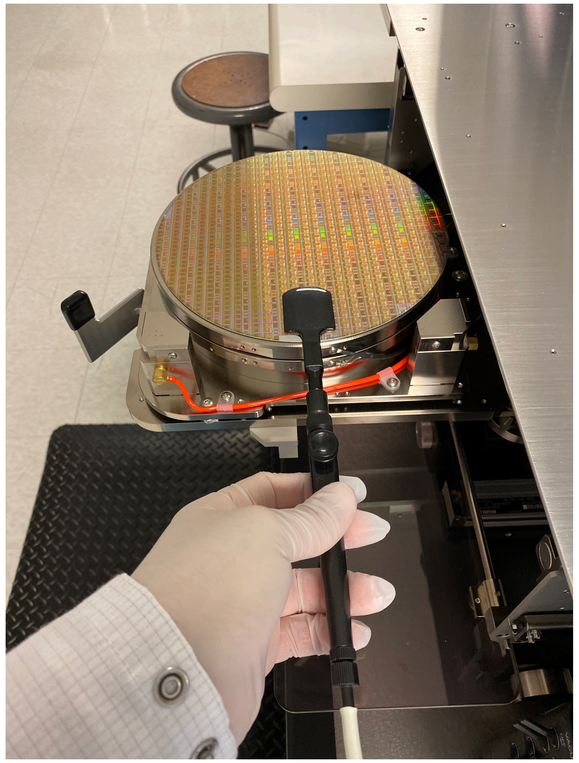
Division of Particles & Fields 2021

Luis Felipe Gutierrez

Outline

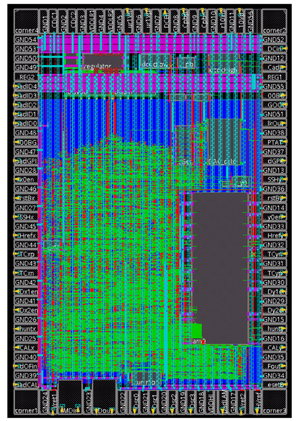
- ASICs Design and Fabrication Overview
- Wafer Testing Setup at Penn
- AMAC Functionality and Performance Characterization
- AMAC Prototype Wafer Testing Results



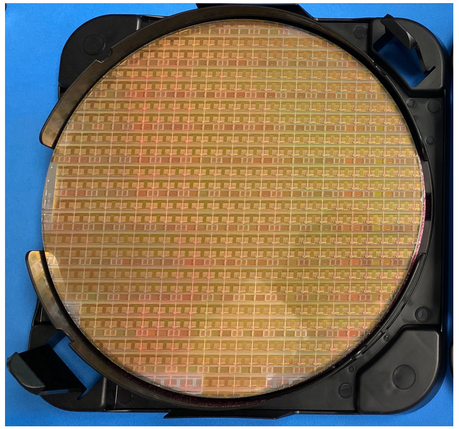


ASICs Design and Fabrication Overview

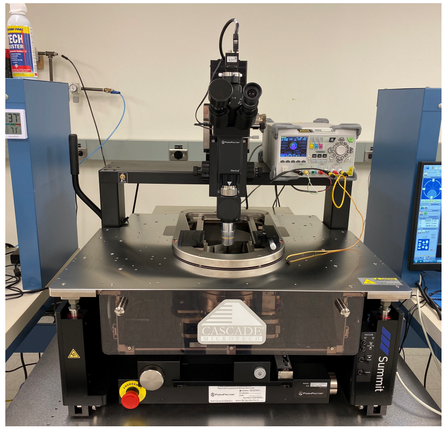
ASIC Cycle Overview



Design and Verification

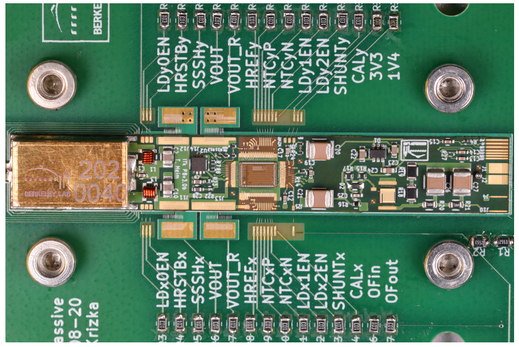


Wafer Fabrication

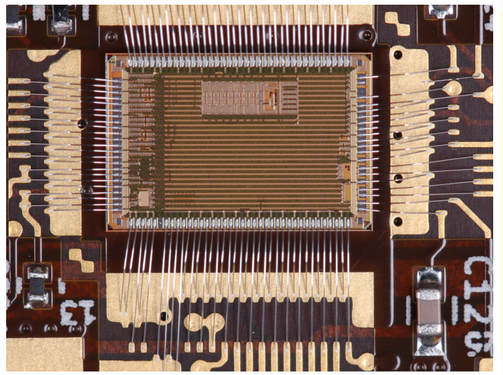


Wafer Probing

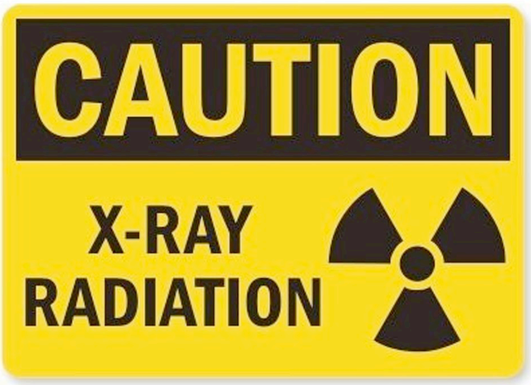
* Images from Karol Krizka



System Tests *



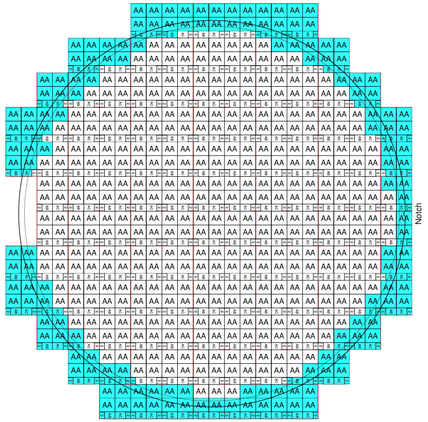
Single Chip Tests *



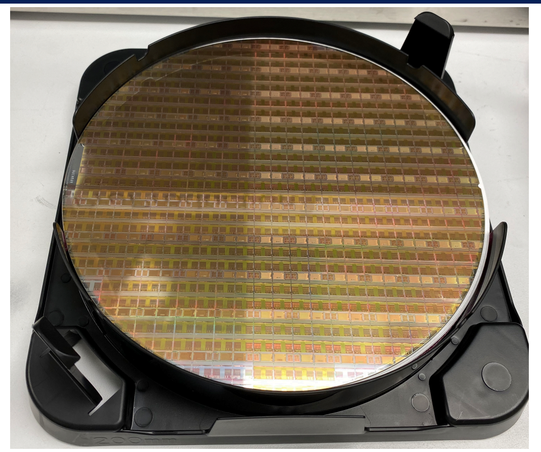
Irradiation Tests

ASIC Fabrication Overview

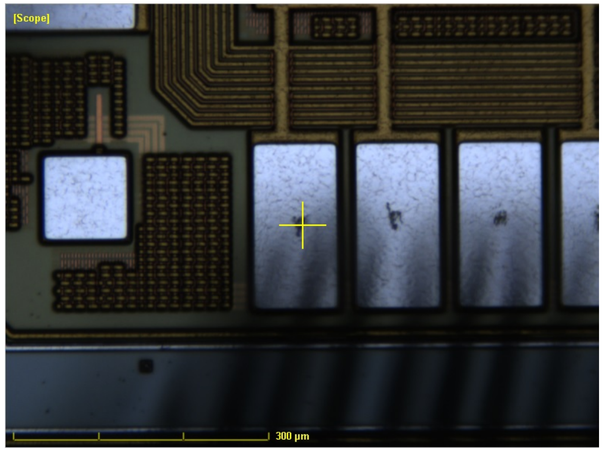
Silicon Wafer



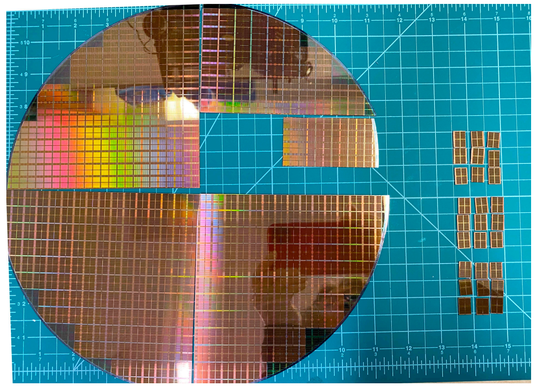
Photolithography



Wafer with dies



Wafer Testing

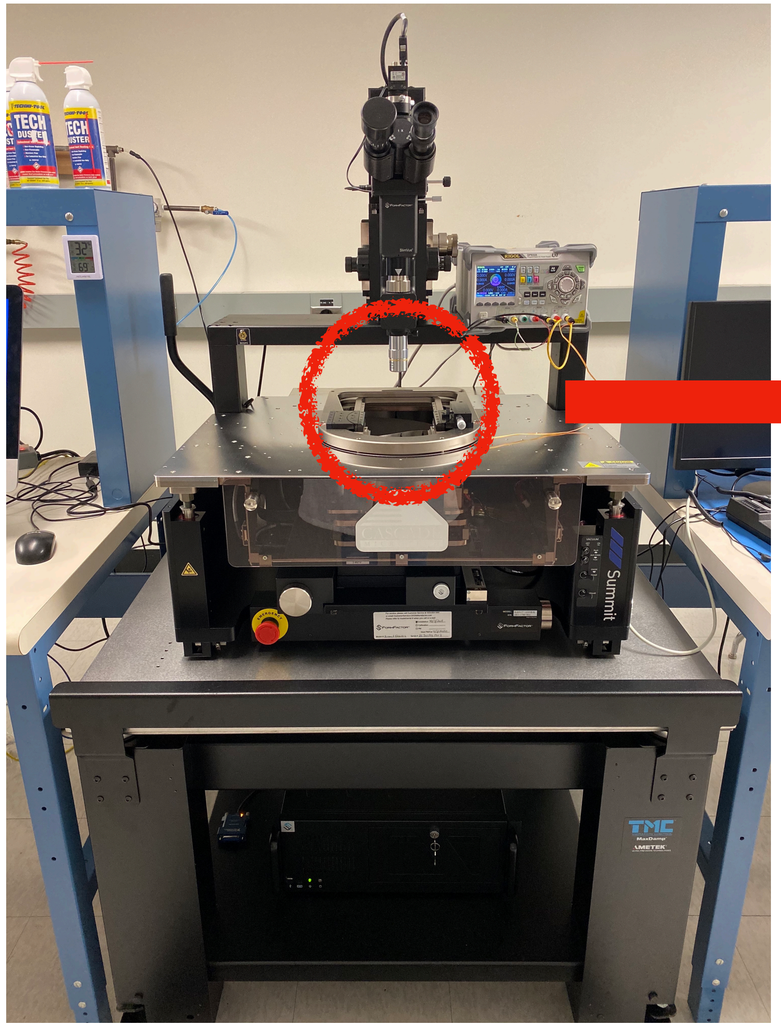


Dicing

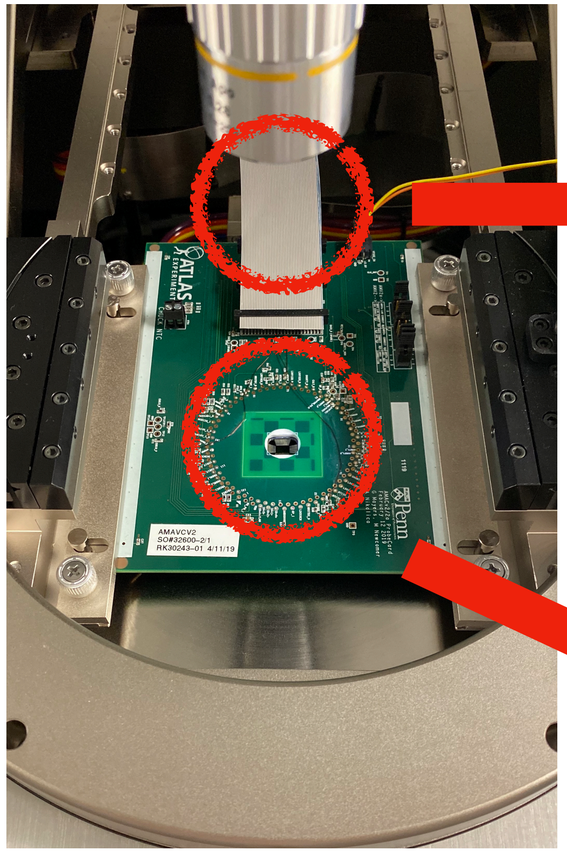
Packaged and Shipped

Wafer Testing Setup at Penn

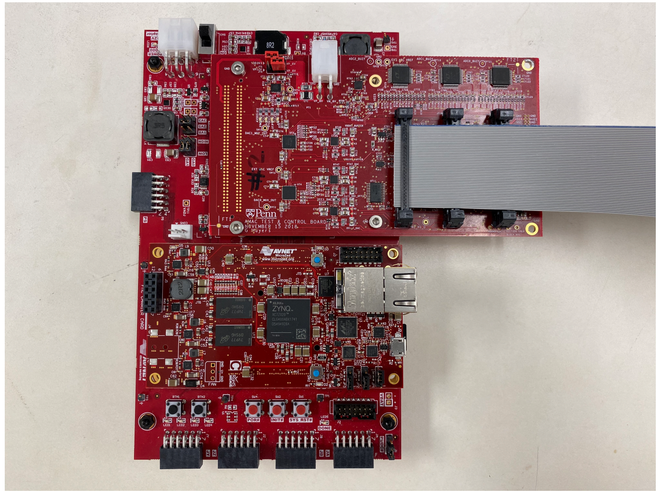
Probe Station, Probe Card and Test Board



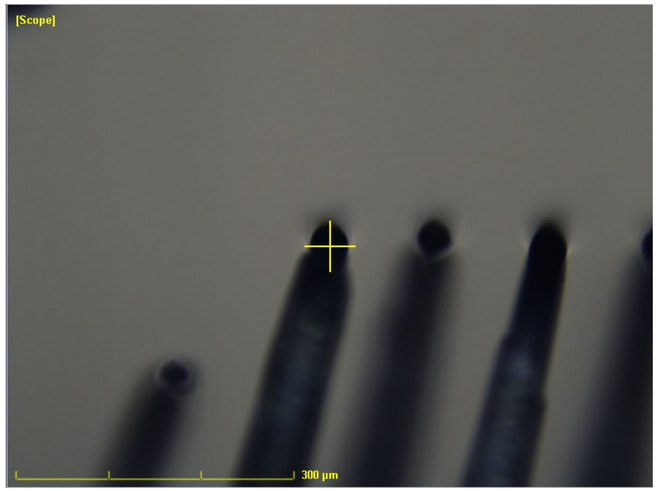
Probe Station



Probe Card

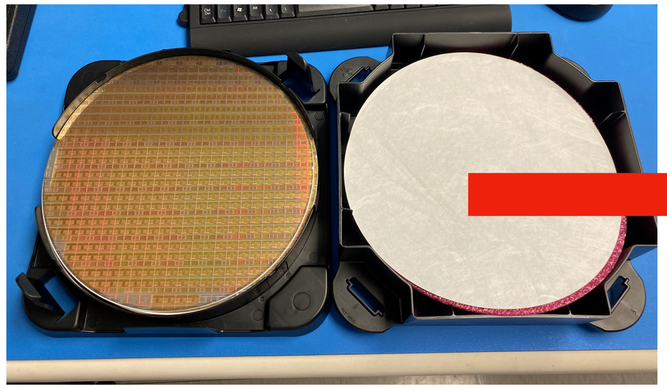


Test Board

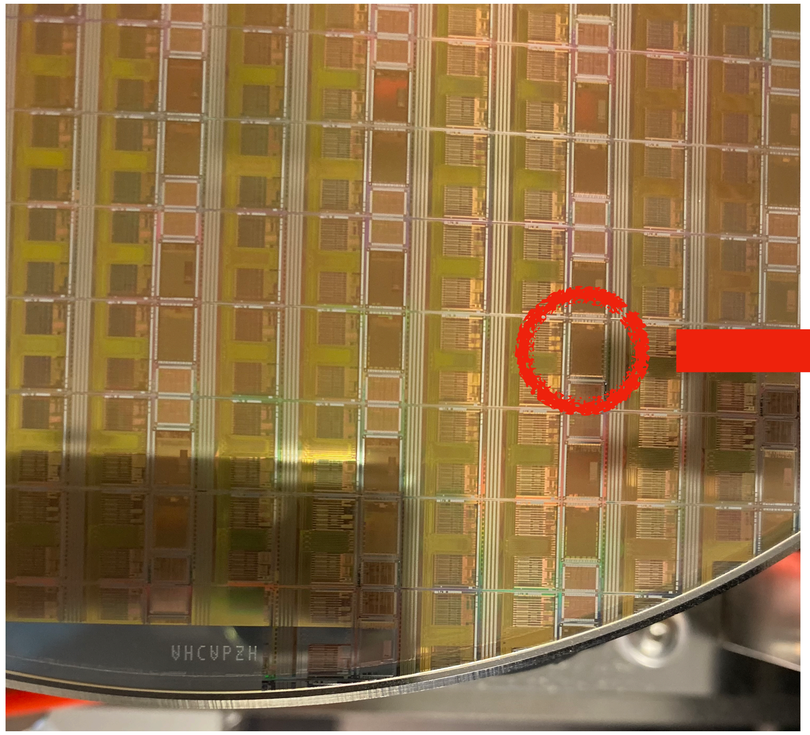


Probe Card Needles

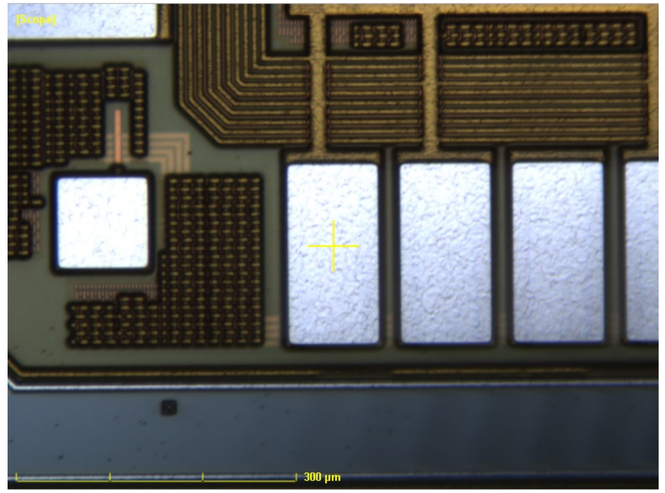
Wafer Die



Wafer

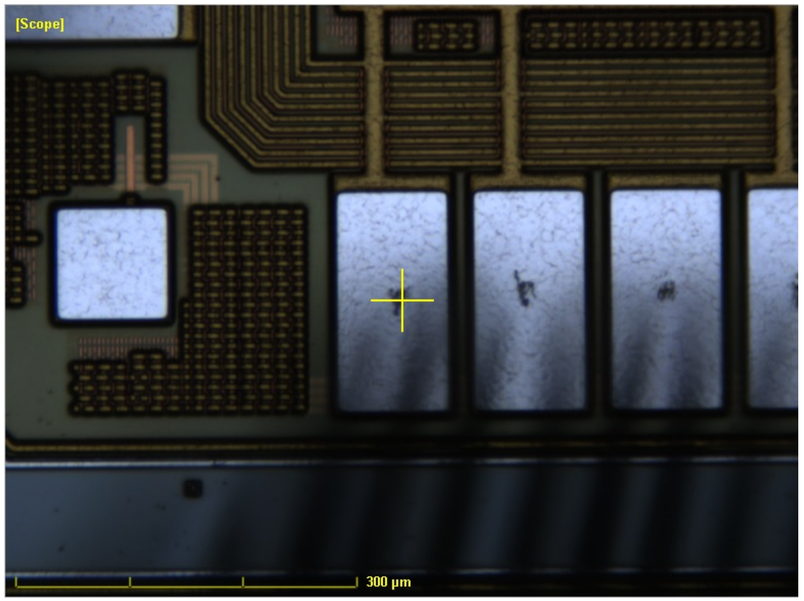


Wafer Dies

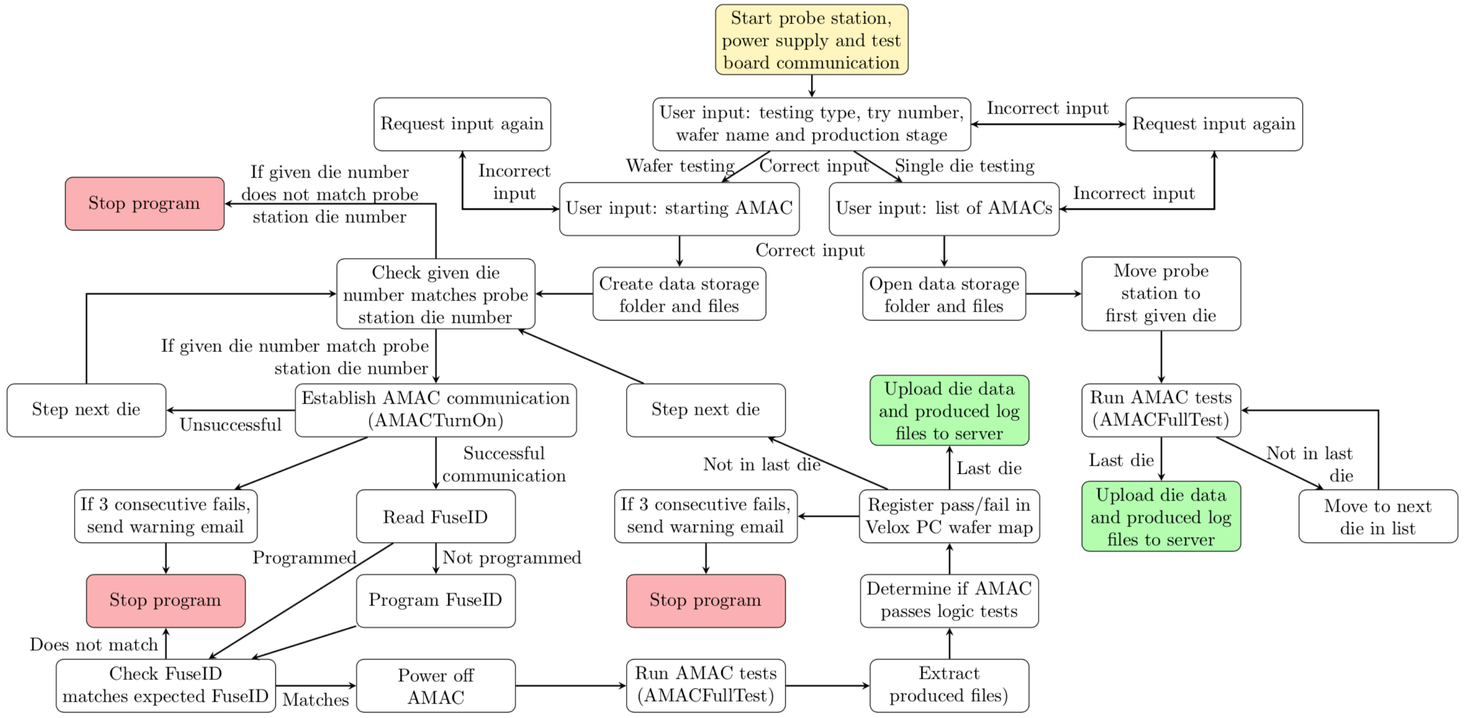


Die Pads

Contact and Software



Probe Card - Die Contact



Probe Station Controller Software

Current setup takes a bit less than 4 minutes per AMAC

AMAC Functionality

AMAC Functions

AMAC desired functionality are translated to ASIC functions:

Power Status:

- i.e. DC-DC Converter

Parameter Calibration:

- i.e. VDD/AM Bandgap

  (Adjustable reference voltage)

Logic Control:

- i.e. Hybrid reset

Analog/Digital Conversions:

- i.e. External Voltages/Currents Measurements

Design tests to check ASIC functions. Types of tests:

- AMAC can be configured
- Resets
- Autonomous feature
- Range of measurements
- Measurements accuracy

AMAC Performance Characterization

Vital and Performance Functions

To know how well an AMAC is performing, we classify the AMAC functions in two:

1. Vital Functions (Absolutely needed for AMAC to work):
   - AMAC needs to power ON
   - AMAC needs to communicate
   - AMAC needs to recover
   - AMAC needs to turn things off, etc.
2. Performance Functions:
   - Measuring external currents accurately
   - Setting desired voltages, etc.

Functions tests output parameters used to characterize AMAC performance

- More than 1000 parameters per die

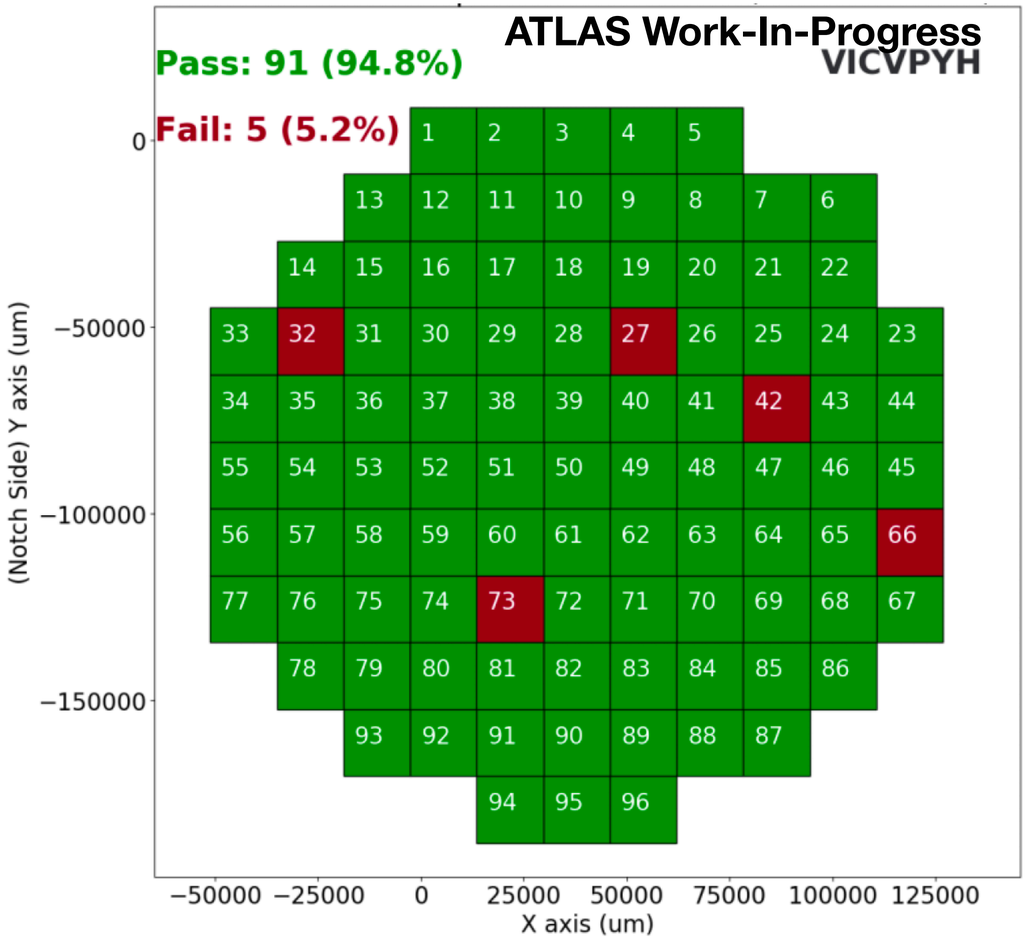
Die Grade	Vital Functions Tests	Performance Functions Tests
A	✓	✓
B	✓	✓
C	✓	✓
F	✗	-

Prototype Wafer AMAC Testing Results

Wafer Map

Green: Die passed all tests (Grade A)

Red: Die failed at least one test (Grade B, C or F)



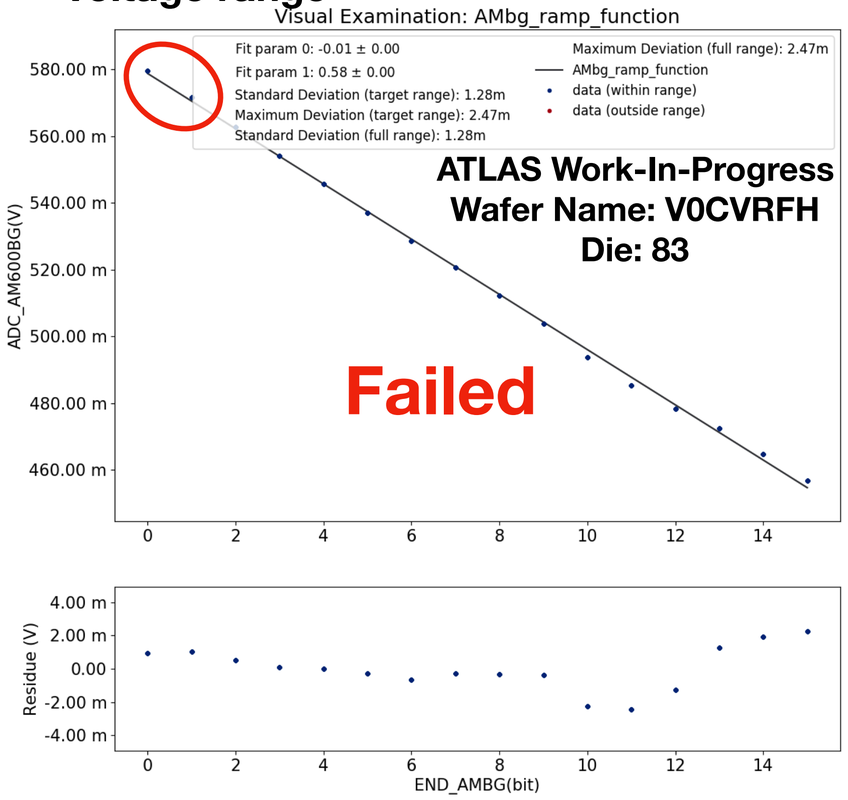
AMAC from 12 prototype wafers probed at Penn

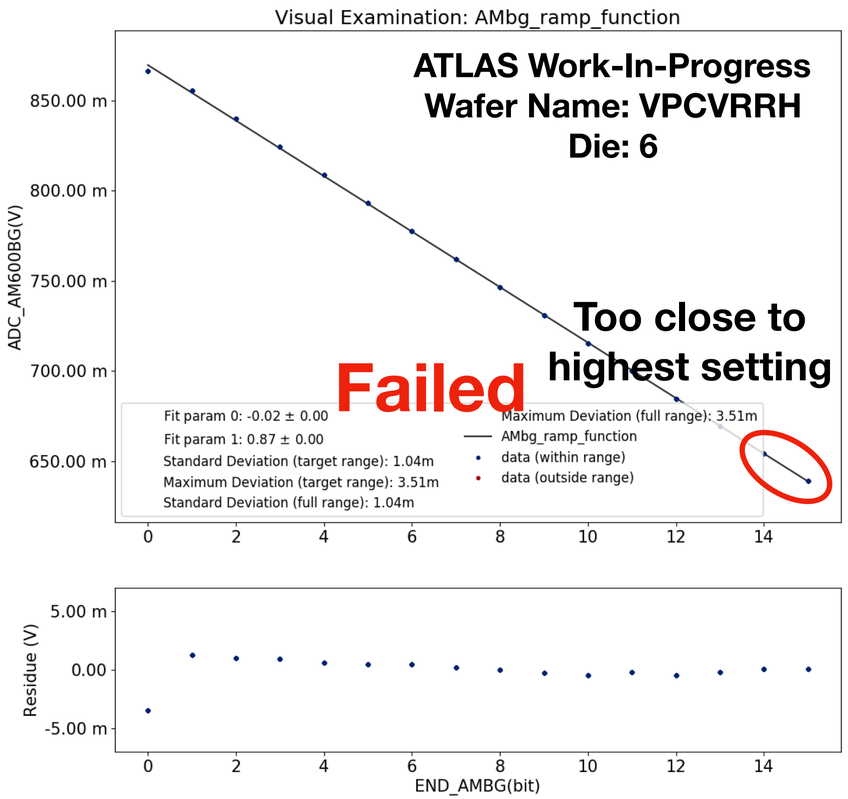
- Dies tested: 1152
- Average yield: 96%

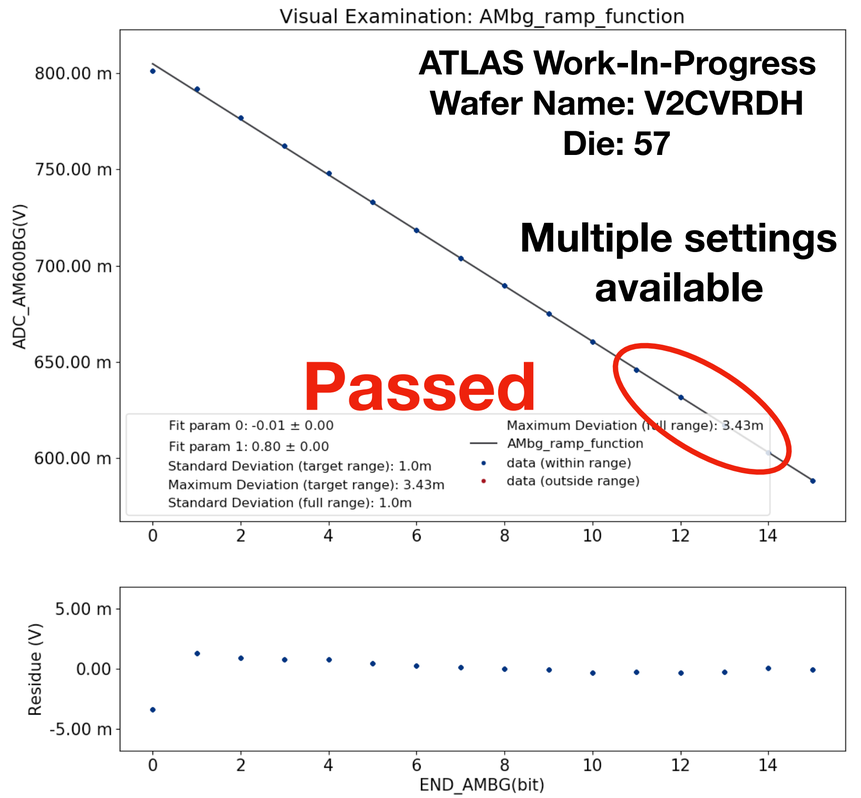
Main Failure (15): Highest Internal Voltage Reference

Below desired voltage range

Performance function parameter







Desired internal voltage reference: 0.65V-0.59V (Best is closest to 0.625V).

Highest internal voltage reference limits: 0.85V-0.78V

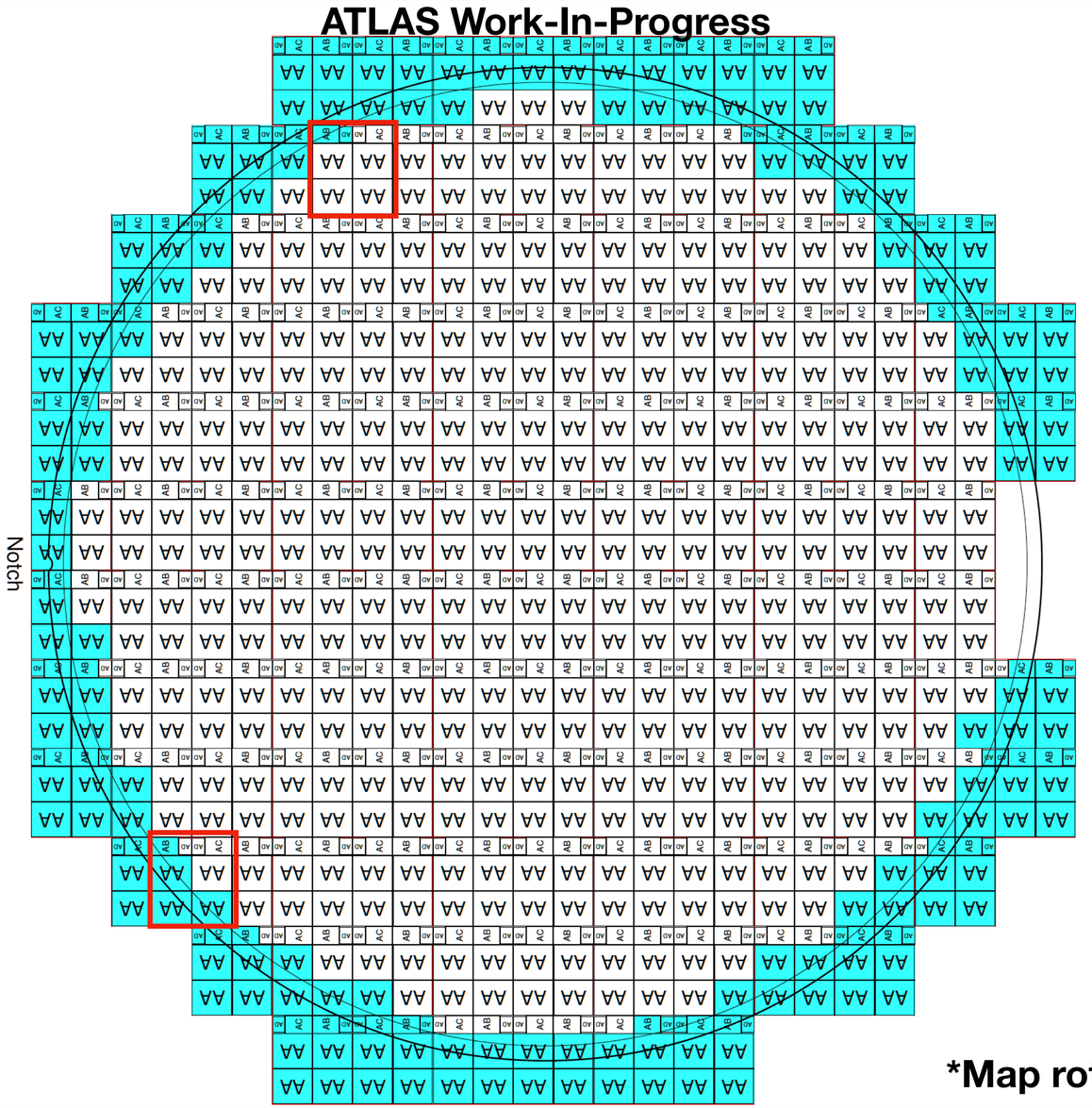
Summary

- Average yield over 12 wafers is 96% (Grade A dies).
  - More work will be done towards defining grade B and C dies.
- Main failure is a performance test parameter: Highest Internal Voltage Reference.
- Coming soon: Improved AMAC testing and probe station controlling softwares.

THANK YOU

Backup

Prototype Wafer Reticle



ATLAS Work-In-Progress

Die ID	Design Name	Estimated Max Die Size X	Estimated Max Die Size Y	Estimated Quantity on Wafer
AA	ABCSTAR	8057	7090	371
AB	HCCSTAR	3650	5450	98
AC	AMAC	3650	5450	96
AD	PATT	2577	3650	199

			Total on Wafer:	764

***Map rotated on purpose to have notch on the left (testing orientation)**

Wafer Maps

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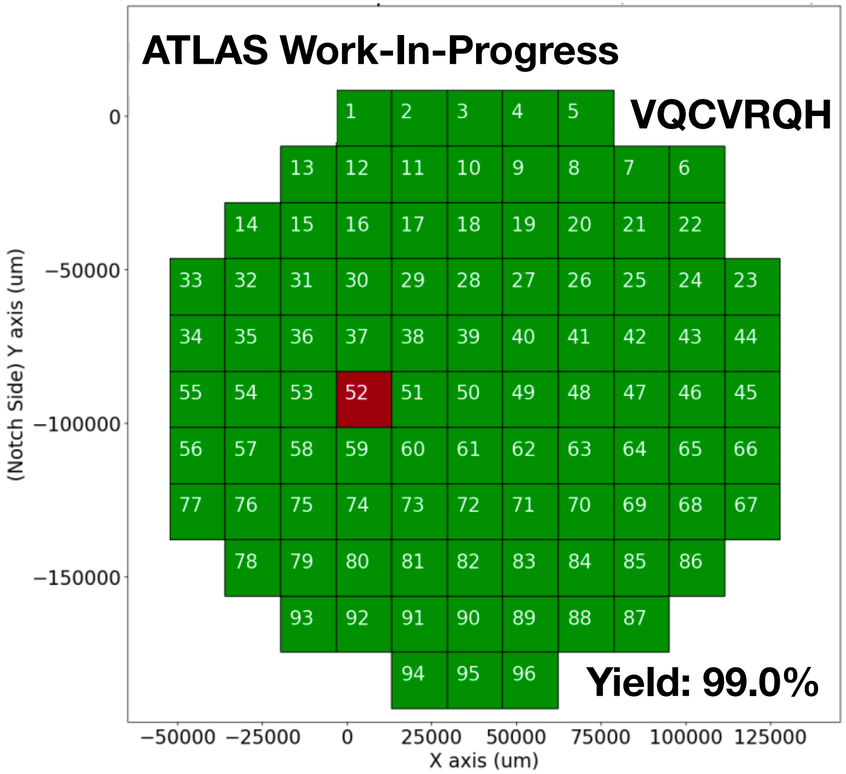
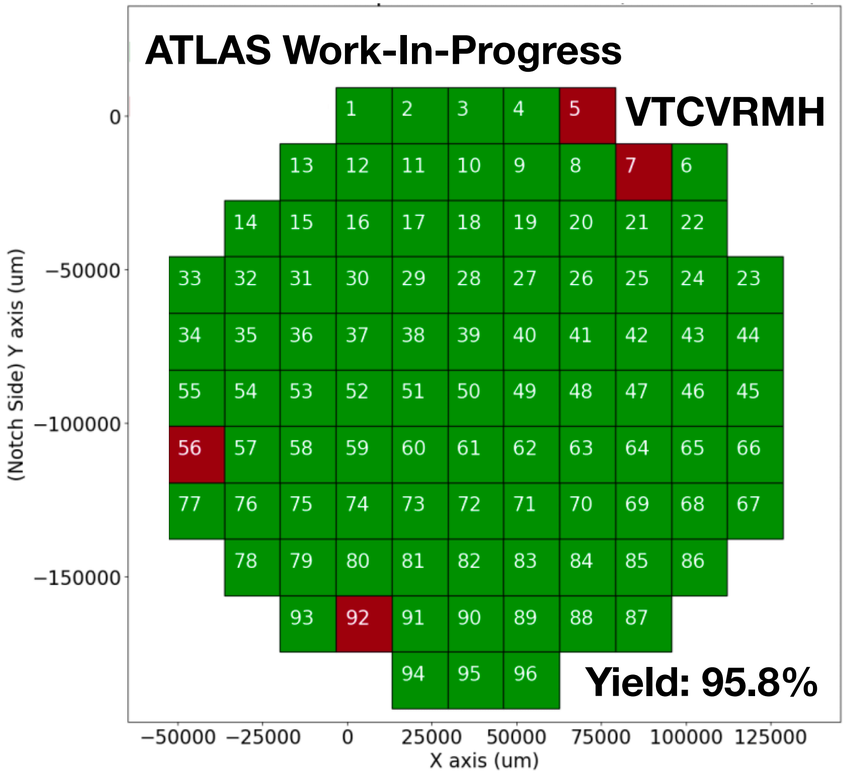
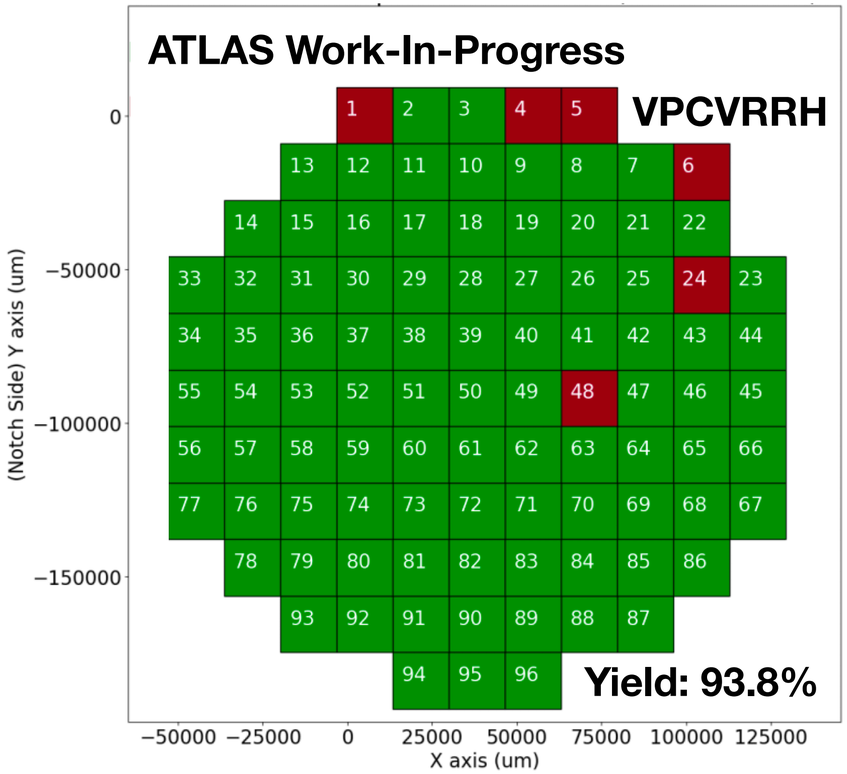
Red: Die failed at least one test (Grade B, C or F)







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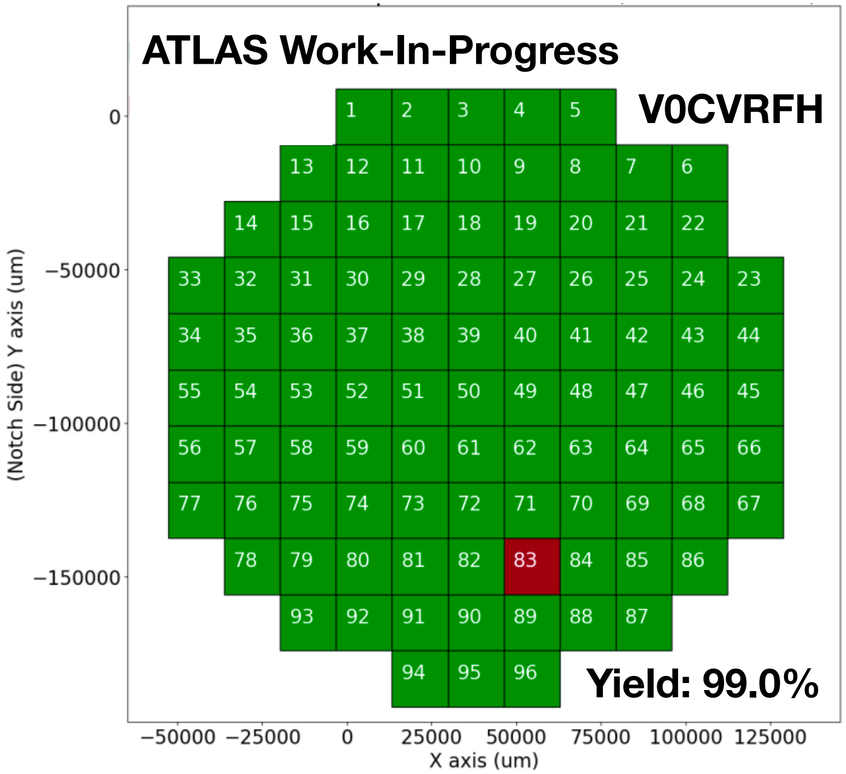

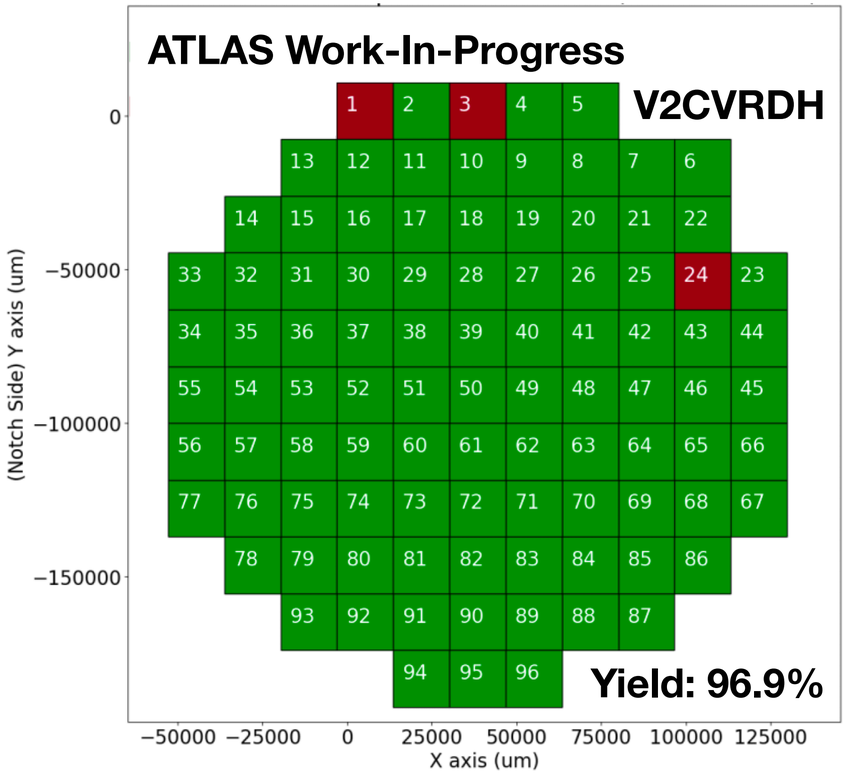

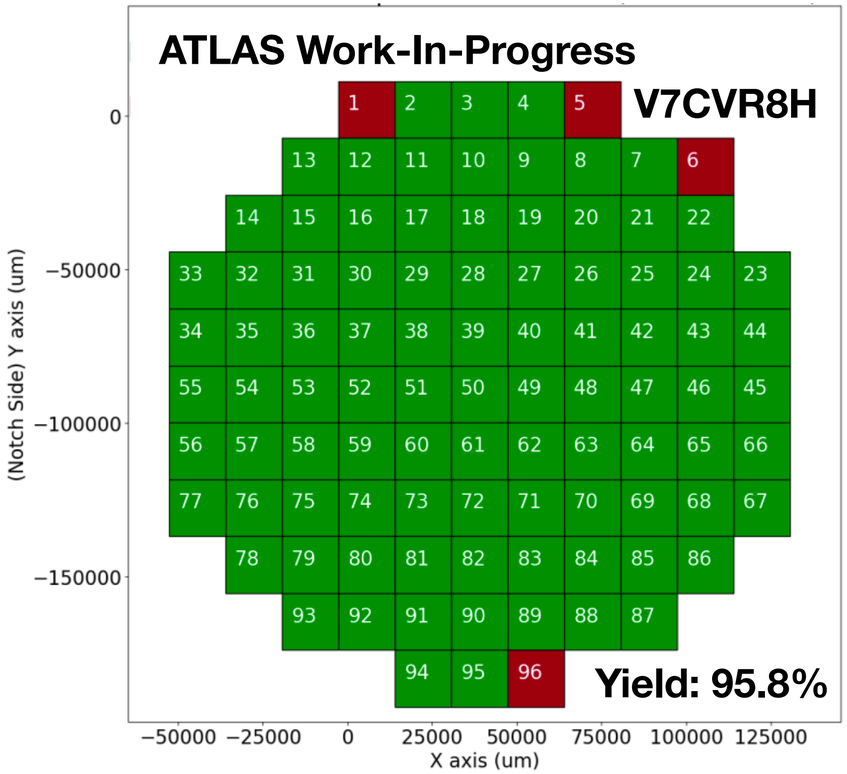

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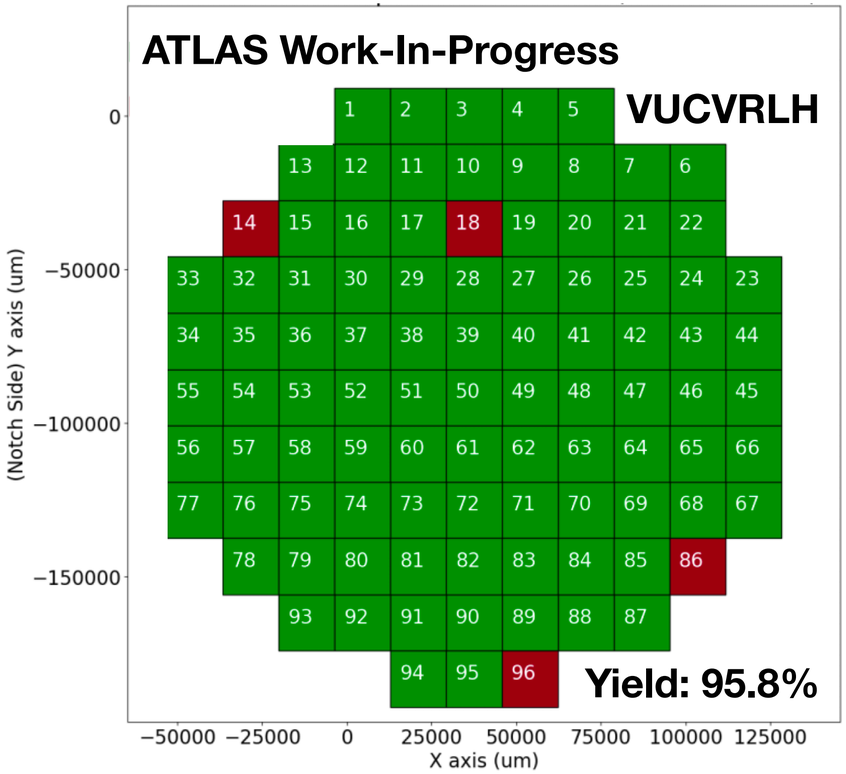

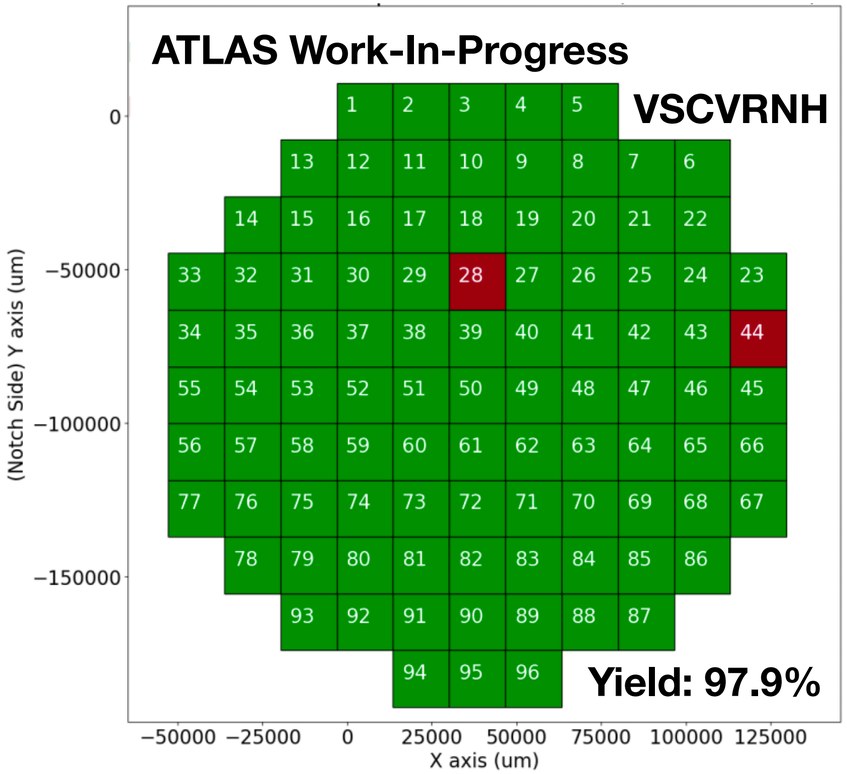

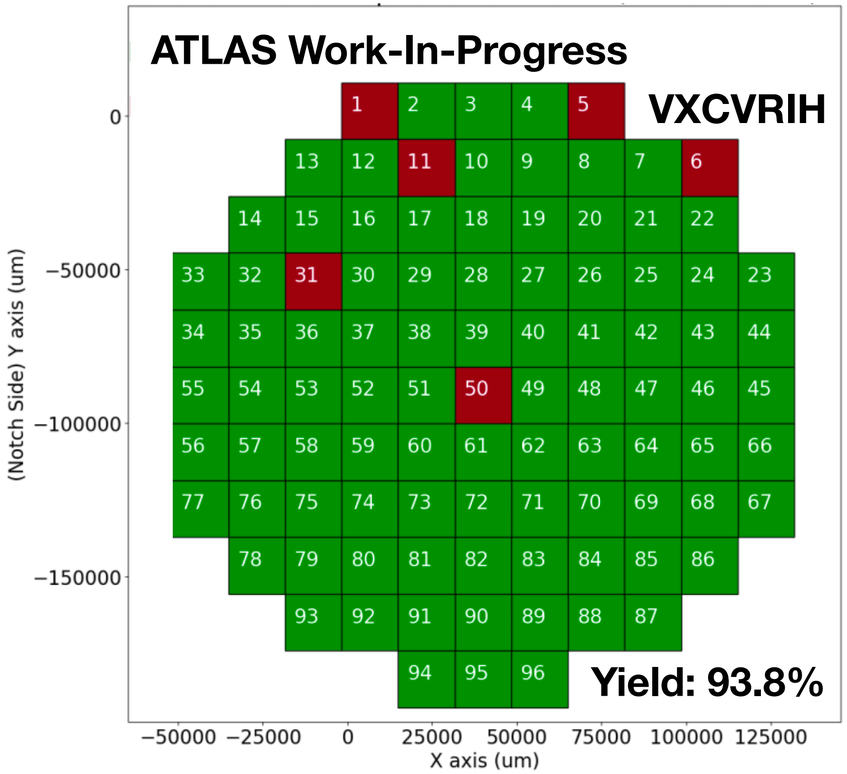

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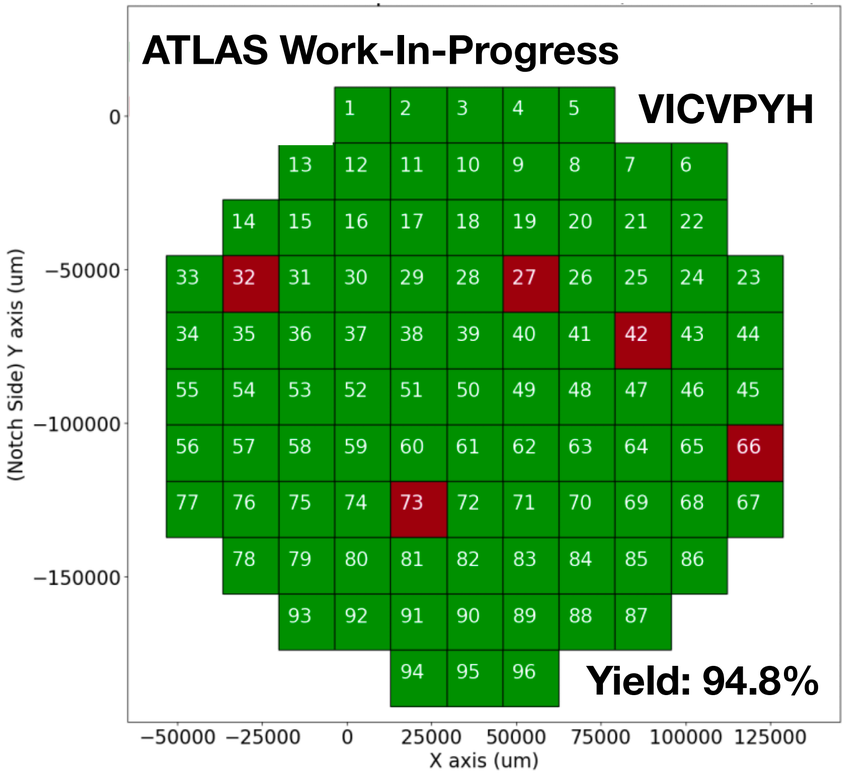
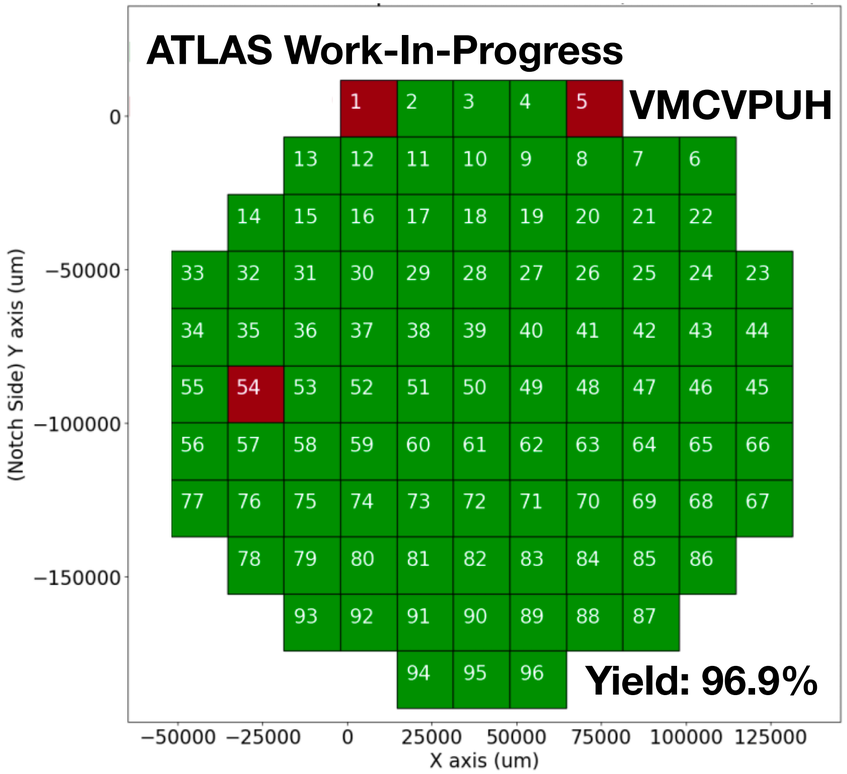
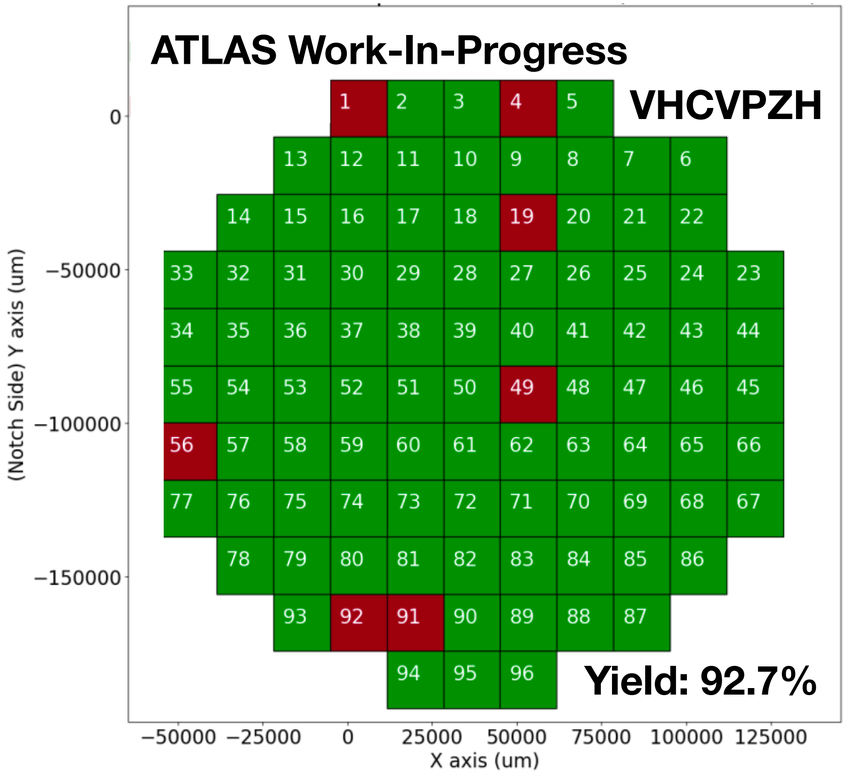






Prototype AMAC Wafer Testing Failures

ATLAS Work-In-Progress

Parameter name	Failures	Parameter name	Failures	Parameter name	Failures
AMbg ramp intercept	15	Hx Flag Logic 100	2	DCDC Flag Logic 011	2
ADC AM VDDLR A	10	Hx Flag Logic 010	2	DCDC Flag Logic 010	2
No communication	8	Hx Flag Logic 000	2	DCDC Flag Logic 001	2
Best slope	7	Hx Flag Latching	2	DCDC Flag Logic 000	2
Best AM600BG	5	HV2 Flag Logic 110	2	CH9 Zero Calib	2
VDDbg ramp ADC VDD range max	4	HV2 Flag Logic 100	2	CH8 Zero Calib	2
DCDC Flag Latching	4	HV2 Flag Logic 010	2	CH2 Zero Calib	2
CH14 Zero Calib	3	HV2 Flag Logic 000	2	CH15 Zero Calib	2
VDDbg ramp ADC VDD range min	2	HV2 Flag Latching	2	CH13 Zero Calib	2
Hy Flag Validation Val3	2	HV0 Flag Logic 110	2	CH11 Zero Calib	2
Hy Flag Validation Val2	2	HV0 Flag Logic 100	2	CH10 Zero Calib	2
Hy Flag Validation Val1	2	HV0 Flag Logic 010	2	Best VDD	2
Hy Flag Logic 110	2	HV0 Flag Logic 000	2	CH6 Zero Calib	1
Hy Flag Logic 100	2	HV0 Flag Latching	2	CH3 Zero Calib	1
Hy Flag Logic 010	2	DCDC Flag Logic 111	2	CH1 Zero Calib	1
Hy Flag Logic 000	2	DCDC Flag Logic 110	2	CH12 Zero Calib	1
Hy Flag Latching	2	DCDC Flag Logic 101	2	CH0 Zero Calib	1
Hx Flag Logic 110	2	DCDC Flag Logic 100	2		

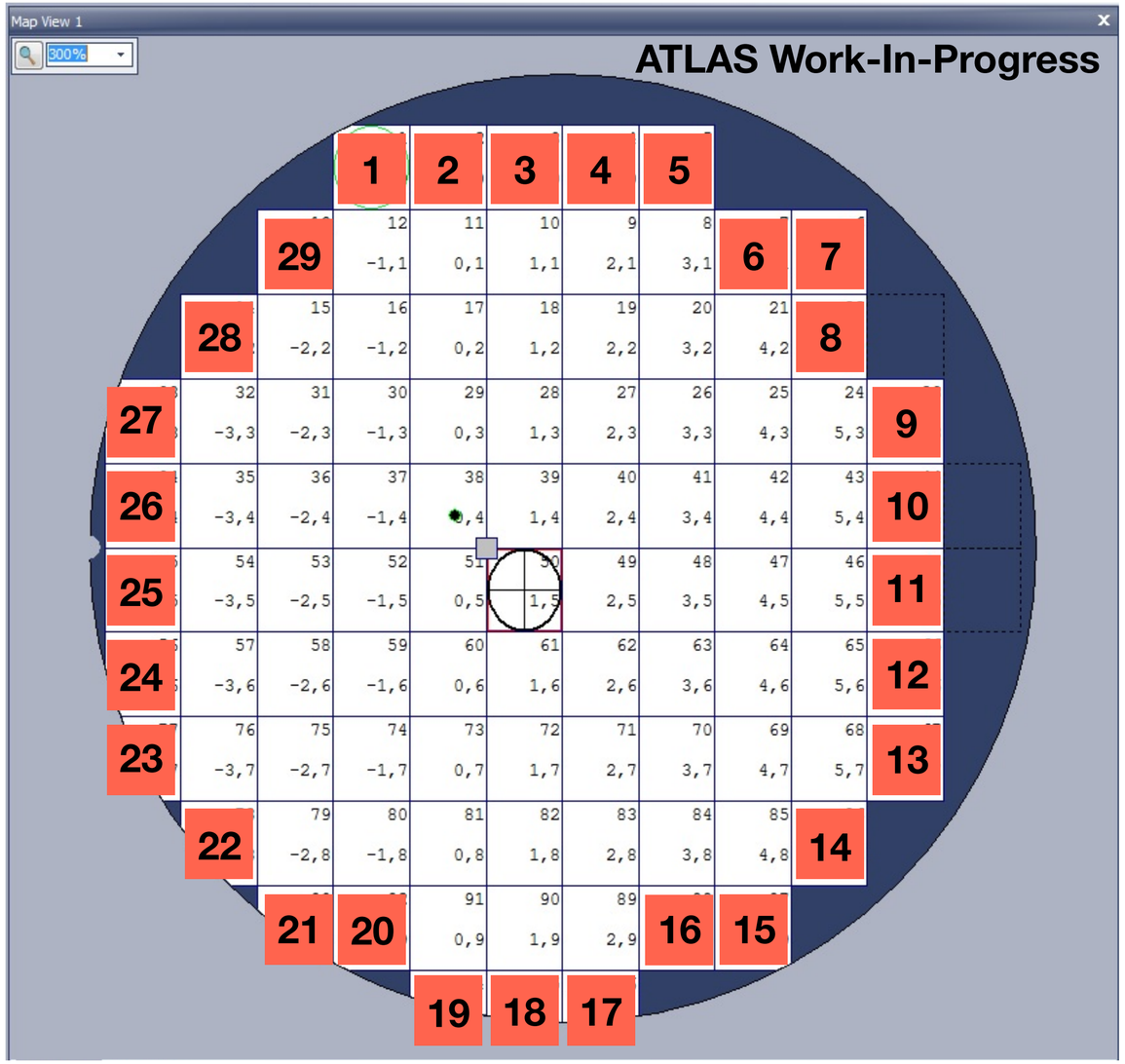
Topological analysis

Edge dies: 29 per wafer (30.2%).

- Total edge dies tested: 348
- Total edge dies failures: 28
- Edge dies yield: 92.0%

Core dies: 67 per wafer (69.8%)

- Total core dies tested: 804
- Total core dies failures: 18
- Core dies yield: 97.8%

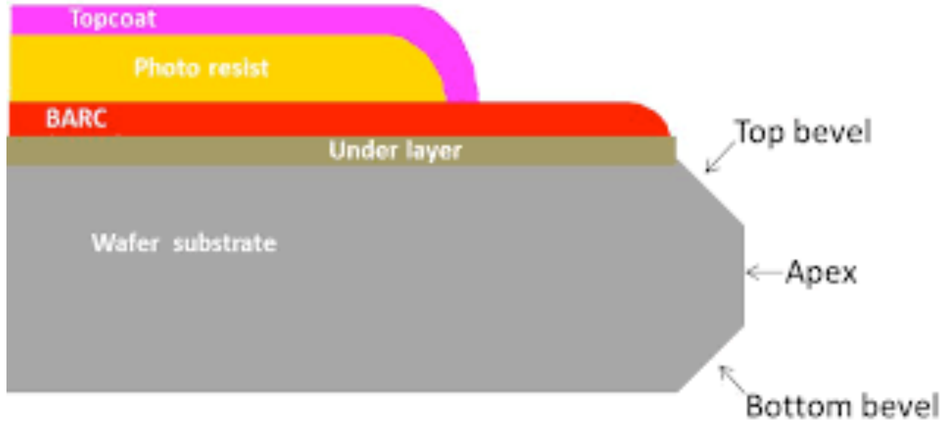


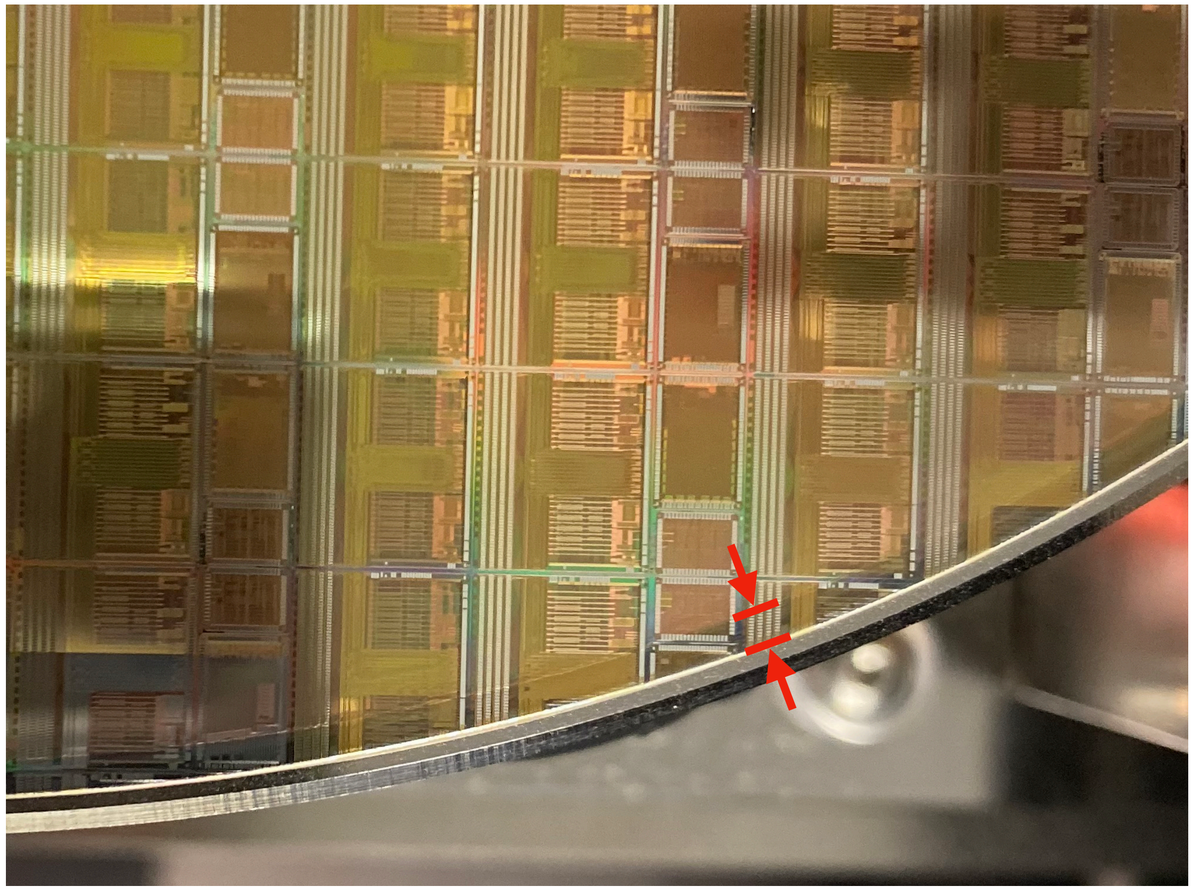
Some reticles are cut because it is a multidie project wafer

Wafer Edge Exclusion Zone

Burkeen, Vedula, Meeks - “Transition from a planar surface to the wafer bevel creates a high-stress area”

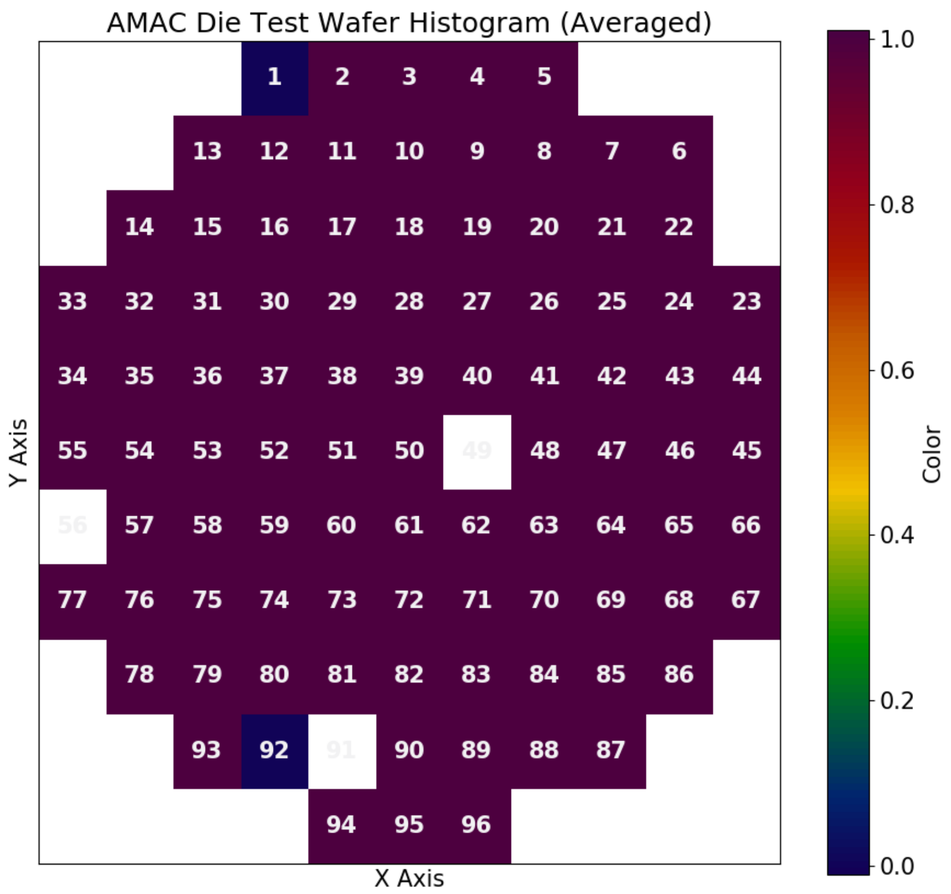
- Film does not adhere properly
- Film delamination





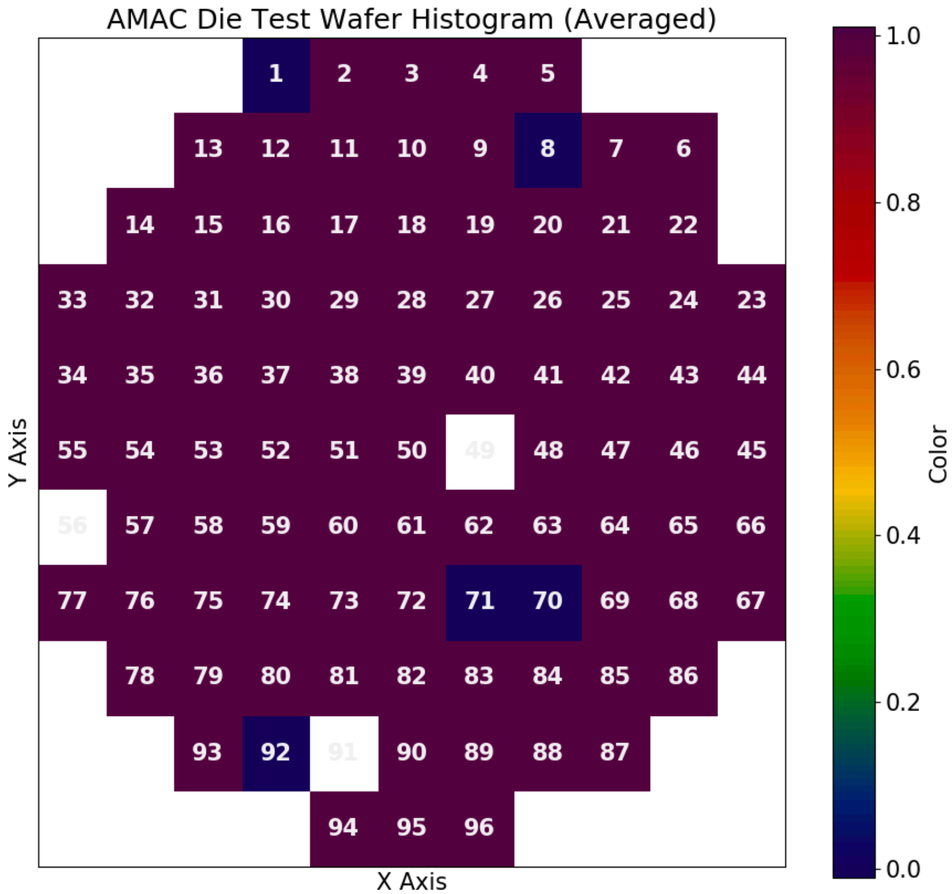
AMAC Probe Cards Comparison

Probe Card 1



ATLAS Work-In-Progress

Probe Card 2



ATLAS Work-In-Progress

AMAC Probe Cards Comparison

ATLAS Work-In-Progress

Wafer Name: VHCVPZH
Die Number: 2

Row 2: ADC_AM_VDCDC_V is supposed to be zero. 60% difference is pure noise.

Row 9: VDDbg_ramp_function_ADC_VDD_range_max is mostly affected by contact. With the second probe card we had better contact on this die, that is why we see 9.2% difference

Overall: Wafer results from both probe cards were consistent

	diff_percent	key	val_card_1	val_card_2
0	0.169319	ADC_AM_VDDLR_V	1.482410	1.479900
1	1.626120	ADC_AM_VDDLR_A	0.037537	0.038148
2	60.000105	ADC_AM_VDCDC_V	0.000381	0.000153
3	0.000000	ADC_AM_VDCDC_A	0.000153	0.000153
4	0.000000	ADC_VDD_HI_A_OFF	0.000015	0.000015
5	7.479922	ADC_VDD_HI_A_R07_4HV00	0.004175	0.003863
6	4.464236	ADC_VDD_HI_A_R07_4HV03	0.005006	0.004782
7	0.243329	ADC_AM_LVDS_CM1	0.690013	0.691692
8	1.106191	VDDbg_ramp_function_ADC_VDD_range_min	1.165260	1.178150
9	9.185040	VDDbg_ramp_function_ADC_VDD_range_max	1.246810	1.361330
10	0.273296	AMbg_ramp_function_intercept	0.820452	0.818210
11	0.385548	Best_AM600BG	0.613413	0.611048
12	0.236353	Best_slope	0.960850	0.958579
13	0.806888	Best_VDD	1.219500	1.229340
14	0.000000	CH0_Zero_Calib	36.000000	36.000000
15	0.000000	CH1_Zero_Calib	34.000000	34.000000
16	0.000000	CH2_Zero_Calib	25.000000	25.000000
17	3.703704	CH3_Zero_Calib	27.000000	28.000000
18	0.000000	CH4_Zero_Calib	30.000000	30.000000
19	0.000000	CH5_Zero_Calib	26.000000	26.000000
20	0.000000	CH6_Zero_Calib	30.000000	30.000000
21	3.333333	CH7_Zero_Calib	30.000000	31.000000
22	0.000000	CH8_Zero_Calib	28.000000	28.000000
23	0.000000	CH9_Zero_Calib	27.000000	27.000000
24	0.000000	CH10_Zero_Calib	35.000000	35.000000
25	0.000000	CH11_Zero_Calib	35.000000	35.000000
26	6.250000	CH12_Zero_Calib	16.000000	17.000000
27	0.000000	CH13_Zero_Calib	31.000000	31.000000
28	0.000000	CH15_Zero_Calib	35.000000	35.000000
29	0.000000	CH14_Zero_Calib	127.000000	127.000000

AMAC Power Consumption vs. RO Frequency

One of the ideas was to reduce current consumption by slowing down the AMAC ring oscillator frequency

ATLAS Work-In-Progress

Die 1 (ZeroCalib ON, AMen OFF)								
RO Frequency Setting	0	1	2	3	4	5	6	7
RO Frequency (MHz)	29.3	29.9	31.2	31.9	34.1	34.7	36.7	37.5
Current Consumption (mA)	36.8	36.8	37.5	37.7	38.3	38.9	40.7	39.8

ATLAS Work-In-Progress

Die 1 (ZeroCalib OFF, AMen OFF)								
RO Frequency Setting	0	1	2	3	4	5	6	7
RO Frequency (MHz)	29.3	29.9	31.2	31.9	34.1	34.8	36.7	37.5
Current Consumption (mA)	36.8	36.8	36.8	37.7	38.3	38.3	39.8	39.7

ATLAS Work-In-Progress

Die 2 (ZeroCalib ON, AMen OFF)								
RO Frequency Setting	0	1	2	3	4	5	6	7
RO Frequency (MHz)	29.6	30.2	31.5	32.2	34.3	35.0	37.0	37.8
Current Consumption (mA)	36.0	36.8	37.4	36.8	39.1	39.8	40.0	39.8

ATLAS Work-In-Progress

Die 2 (ZeroCalib OFF, AMen OFF)								
RO Frequency Setting	0	1	2	3	4	5	6	7
RO Frequency (MHz)	29.6	30.1	31.5	32.1	34.4	35.0	36.9	37.8
Current Consumption (mA)	35.9	36.0	37.7	37.4	38.3	39.1	40.6	40.7

Conclusion: Lower RO Frequency results in lower power consumption