AMAC ASIC for the ATLAS ITk silicon strip detector
Design and Verification

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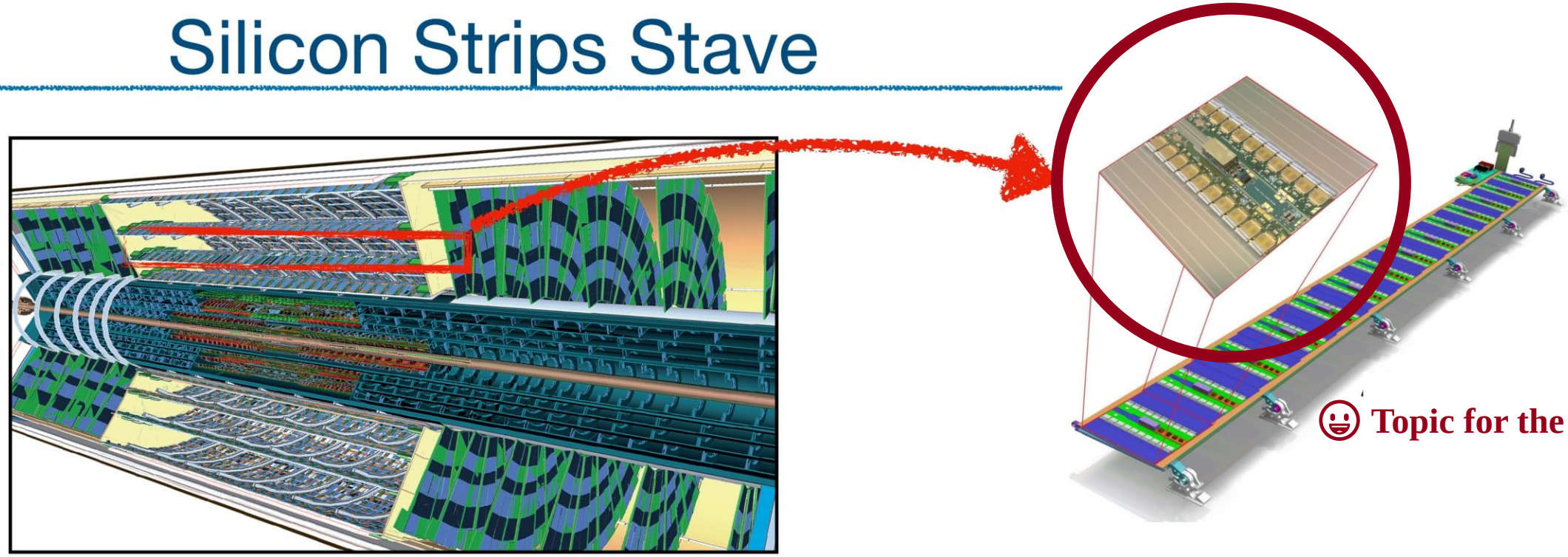
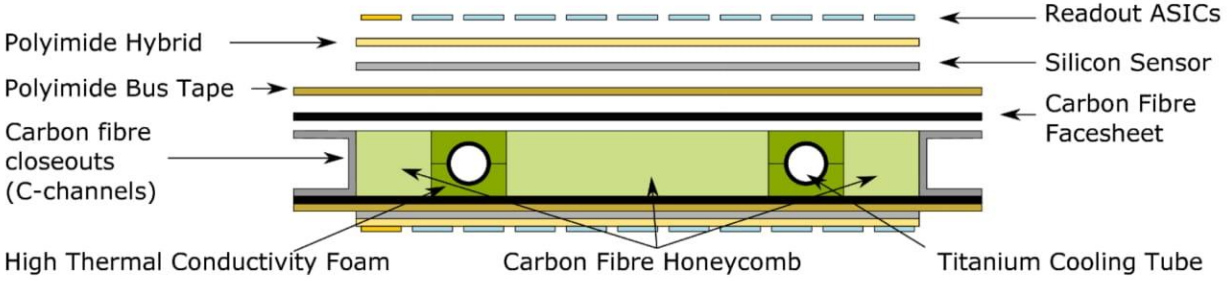
Silicon Strips Stave



Topic for the next hour!

- Staves are the basic units of the ITk Strip Barrel detector
- It is made of a 1.4 m long support structure
  - provides **mechanical rigidity and support** by using high stiffness and high thermal conductivity carbon fiber
  - Provides **cooling** to modules
  - Polyimide bus-tape is co cured on both faces to channel power and data from and to the modules .
- 14 silicon modules are directly glued on both sides of the stave support structure



ATLAS Binary Chip - Star:

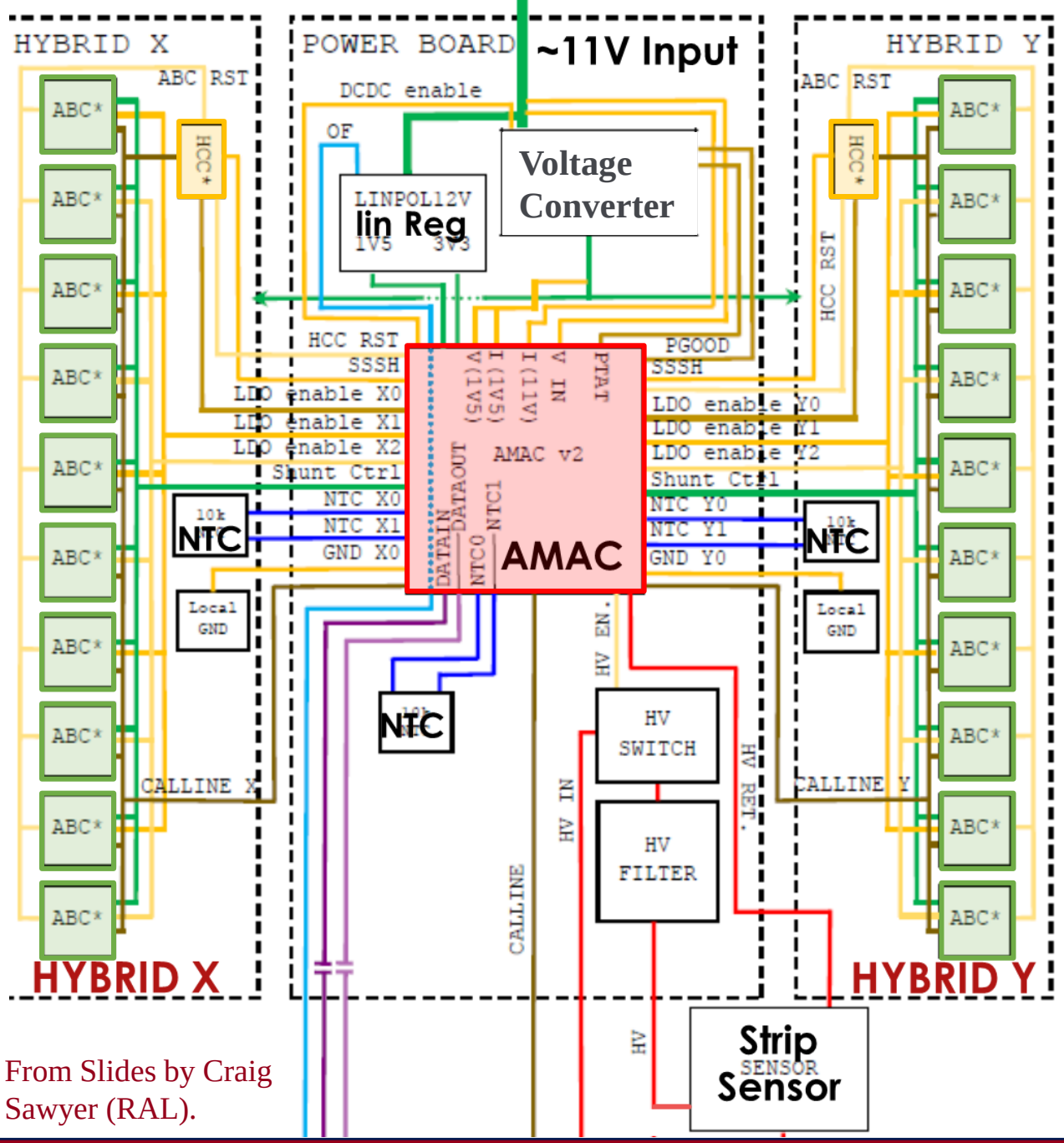
"Charged particles passing through the silicon strip sensor will create a signal. Each ABCStar is responsible for 256 strip channel, and signals from each strip are amplified, shaped, and discriminated to provide binary output."

-- ATLAS ITk TDR

Hybrid Controller Chip - Star:

"Each HCCStar receives the signals from up to 12 ABCStar, builds packets and moves them on.
It also receives the clock and control signals and distributes those to the ABCStar."

20× ABCStar ✓ ✓2× HCCStar



From Slides by Craig Sawyer (RAL).

Autonomous Monitor And Control

Why we need the AMAC & How does it help

- Hazards in detector modules
  - Abnormal Temperature:
    - E.g., local high temperature
    - ⇒ bent/damage sensor
    - ⇒ loss of positioning accuracy
  - Abnormal Current:
    - E.g., individual components short
    - ⇒ takes too much power
    - ⇒ high temperature/insufficient supply
  - Abnormal Voltages:
    - All ASICs and Sensor needs proper voltage to work!
    - Low Voltage ~ 1.5V
    - High Voltage ~ 500V

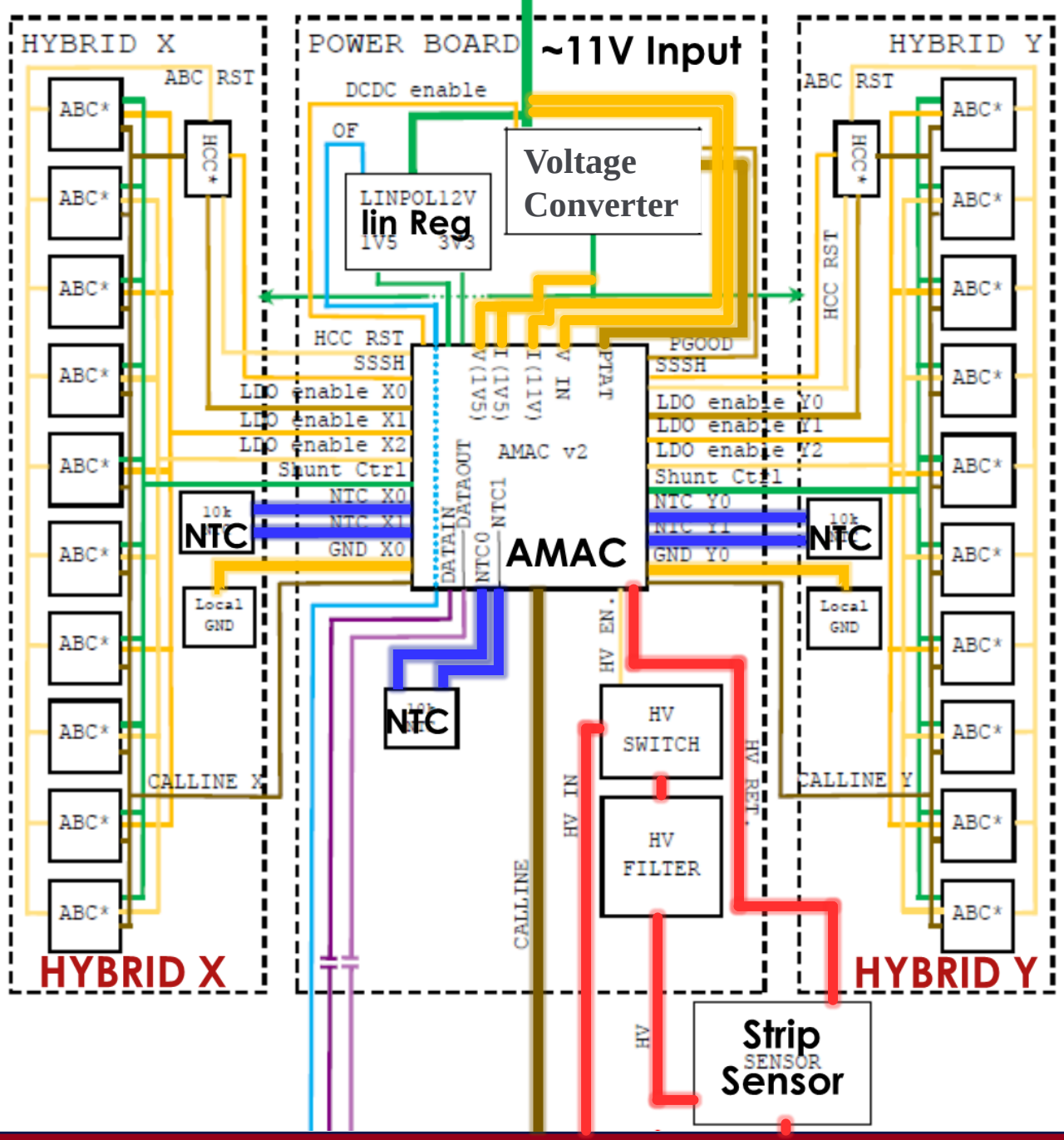
- How does AMAC help?
  - **Monitor!**
    - "Spotting" the issues in the first place,
    - With continuous analog monitoring every 0.5 millisecond.
  - **Control!**
    - "Handle" the defective components without dismantling the detector,
    - With 5 switches to different components.
  - **Autonomous!**
    - Quickly isolate the issue & Stop it from spreading,
    - By autonomous interlock logic channels.

OUTLINE

Autonomous Monitoring And Control

- **What is AMAC & Why we need it**
- Design of AMAC
  - Monitor
  - Control
  - Autonomous
  - Radiation Hard
- Verification of AMAC
  - Digital Verification
  - Analog Verification

Analog Monitoring



Temperature

- **Hybrid X/Y** Temperature & **Power Board** Temperature
- **Power Supply** Temperature
- **AMAC** Internal Temperature

Current

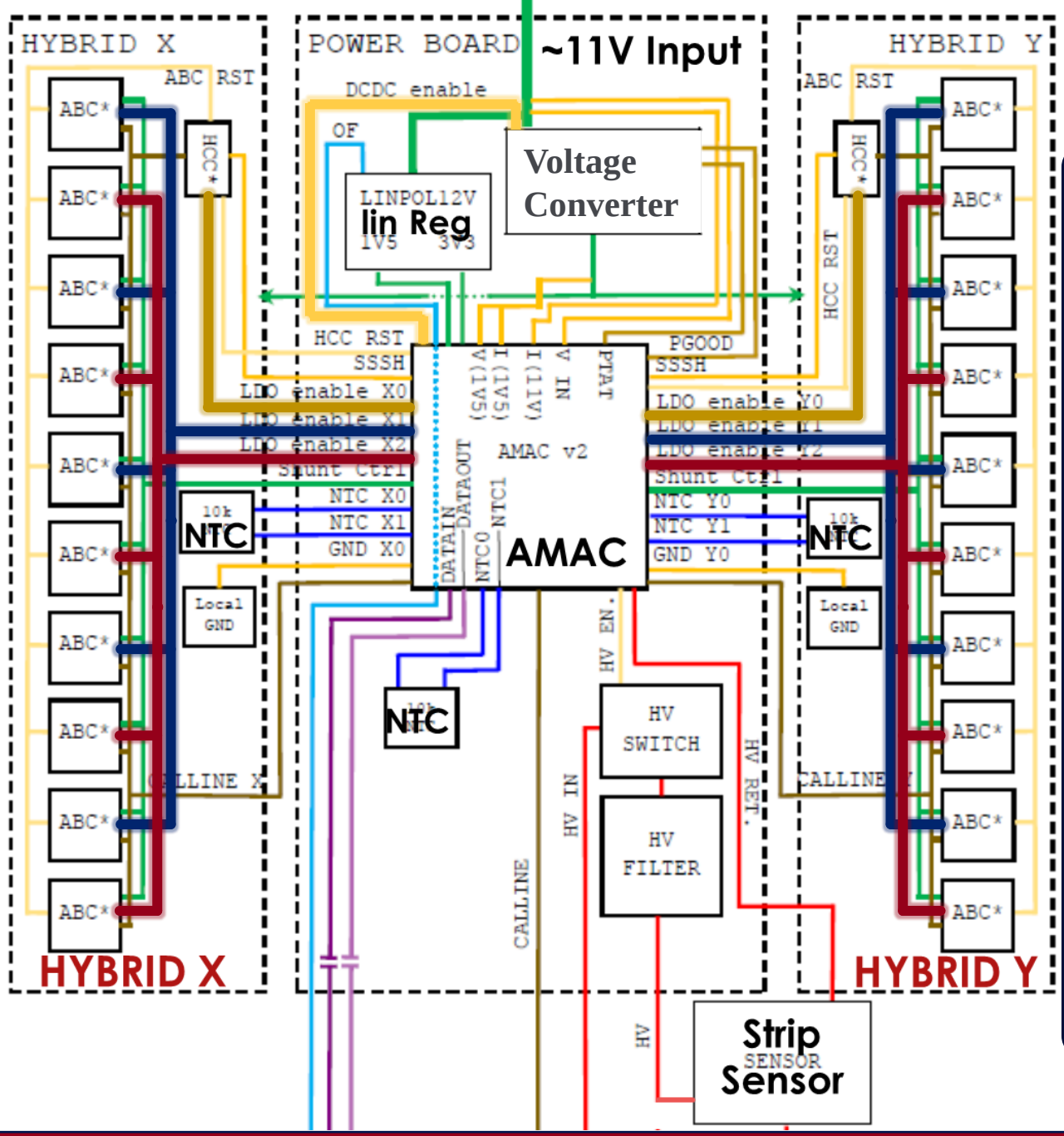
- **Silicon Sensor** Bias Current (High Voltage Return)
- **Voltage Converter** Input
- **Voltage Converter** Output

Voltage

- Ground Voltage Calibration (**Hybrid X/Y** & **End-of-Stave**)
- **Voltage Converter** Input
- **Voltage Converter** Output

Analog to Digital Converter
(16 Multiplexer Channel)

Powering Control



Interlock Switch Output

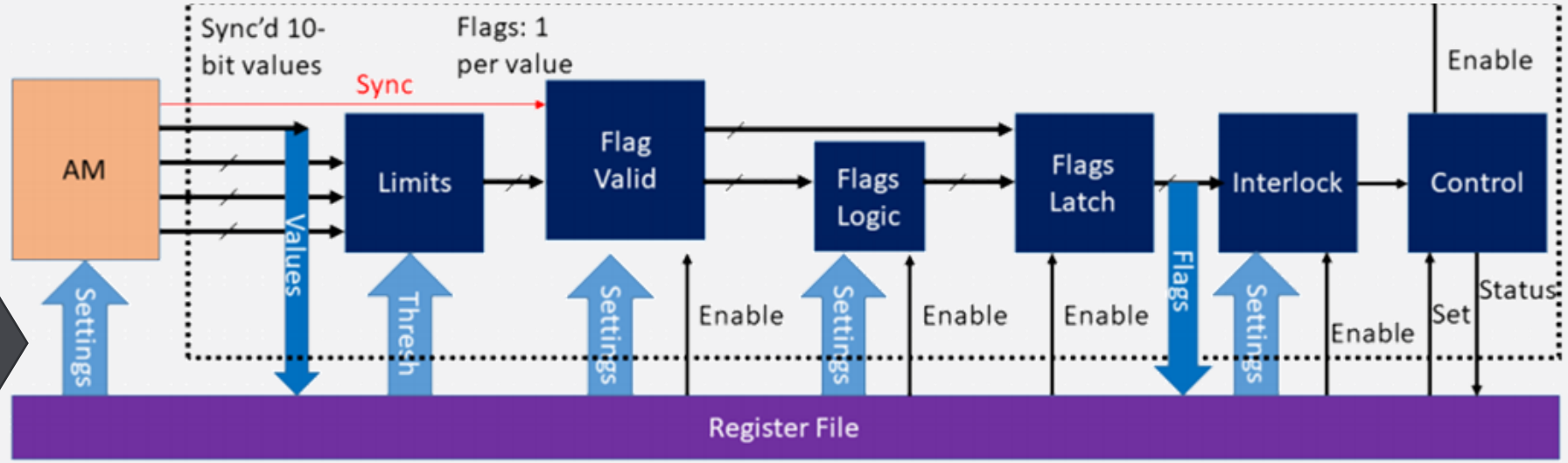
Hybrid X Low Power	X0: HCCStar X1: 5×ABCStar X2: 5×ABCStar
Hybrid Y Low Power	Y0: HCCStar Y1: 5×ABCStar Y2: 5×ABCStar
Power Enable	Voltage Converter On/Off
High Voltage Switch 0 & 1	HV 0 On/Off HV 1 On/Off
High Voltage Switch 0 & 1	HV 2 On/Off HV 3 On/Off

AMAC Internal

Autonomous Monitor And Control (AMAC)

Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Channel



Interlock Switch Output

Example workflow:

Channel:	**Value.**	**Check?**	**Flag!**
Hybrid X:	10°C	≤ −10°C?	**High** Flag!
Hybrid Y:	−20°C	≤ −10°C?	No Flag.
Power-board:	−20°C	≤ −10°C?	No Flag.
Total Current:	200mA	≤ 150mA?	**High** Flag!
…	…	…	…

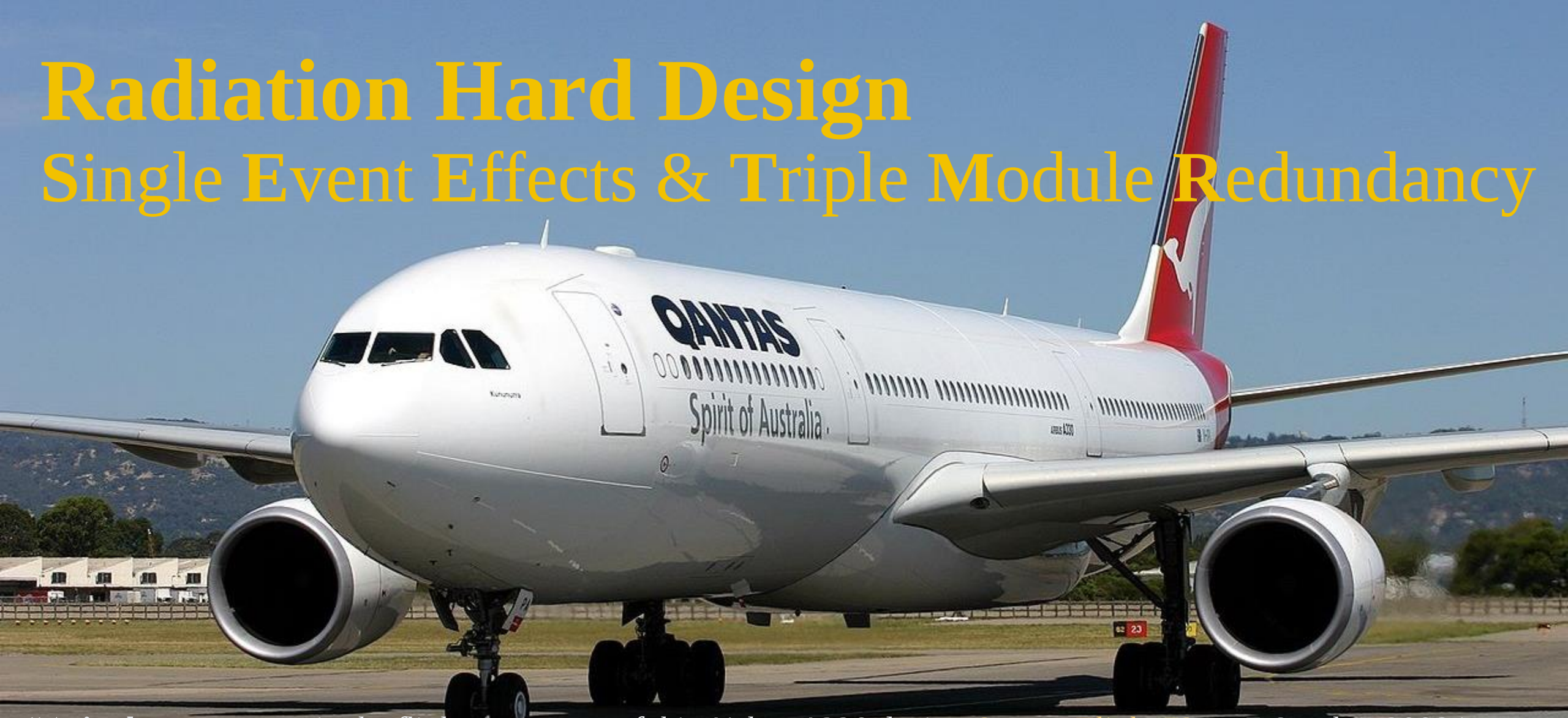
Latch flag to **register** for debugging and analysis…

Move the **interlock state** from **ON** to **LOCK**

Turn All **Hybrid X ASICs** to Low-Power Mode!

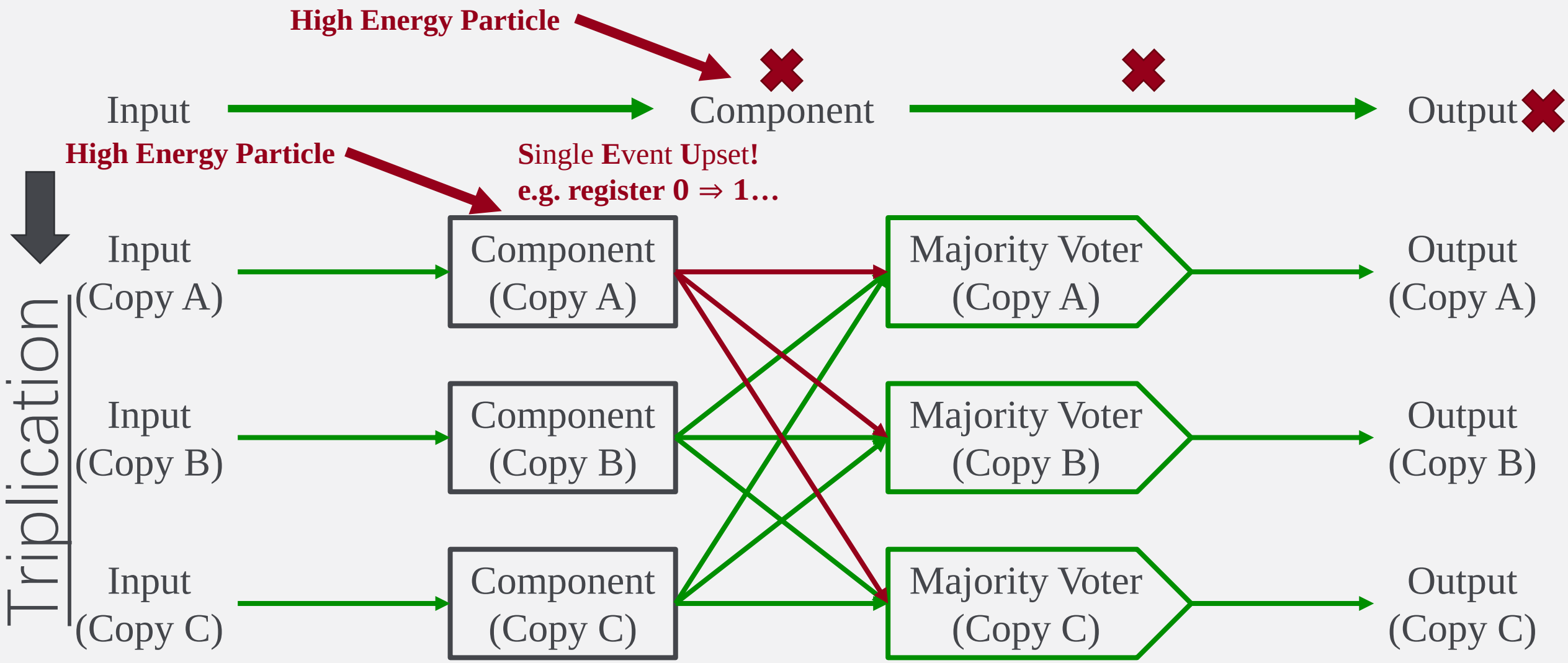
Radiation Hard Design

Single Event Effects & Triple Module Redundancy



*"A **single event upset** in the flight computers of this Airbus A330 during Qantas Flight 72 on 7 October 2008 is suspected to have resulted in an aircraft upset that nearly ended in a crash after the computers experienced several malfunctions."* *Rare event in aviation and daily life, but extremely common in particle collider!*

Triple Module Redundancy against SEU & SET



Design Verification: Digital vs Analog

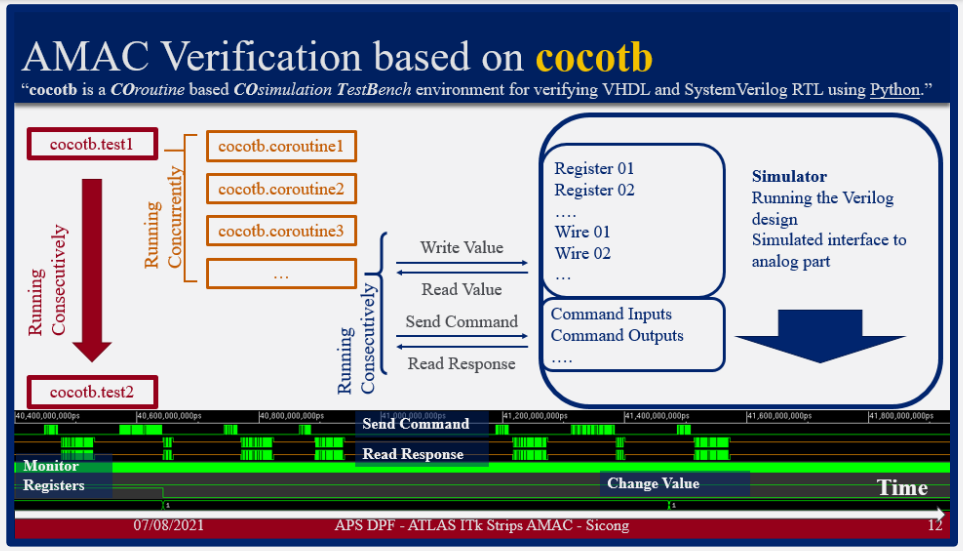
- Digital Logic Block:
  - i) Many revision and updated design version;
  - ii) Relatively independent of the manufacturing;
  - iii) Functions mostly internal;
  - iv) Many scenarios/combinations to be considered!

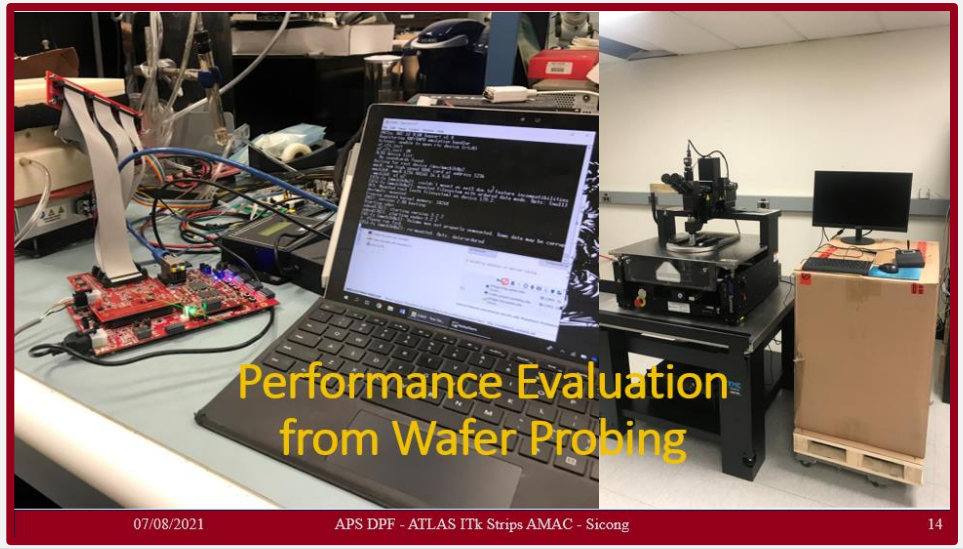
1010
1010

Simulate

- Analog Block:
  - i) Design relatively fixed;
  - ii) Parameters heavily dependent on manufacturing;
  - iii) Needs a real set-up with external devices;
  - iv) Data needed for each chip!

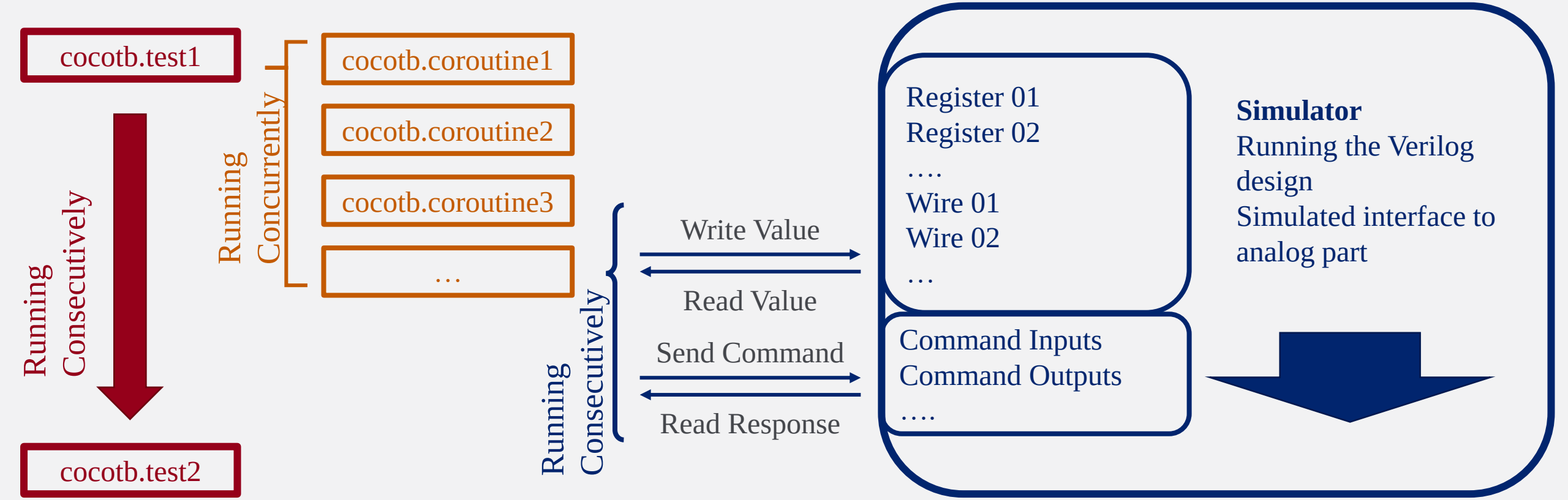
Probe & Fit

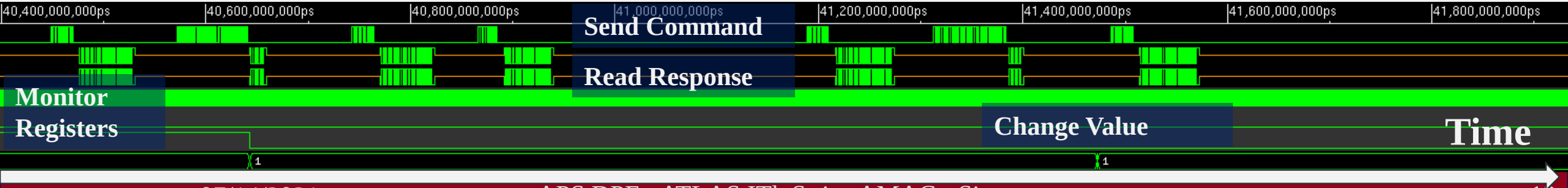




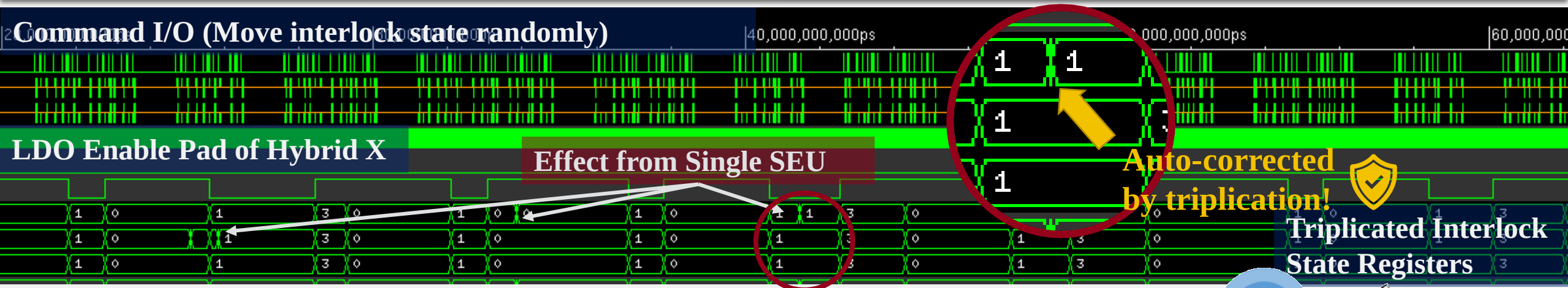
AMAC Verification based on **cocotb**

"**cocotb** is a ***CO**routine* based ***CO**simulation **Test**Bench* environment for verifying VHDL and SystemVerilog RTL using Python."

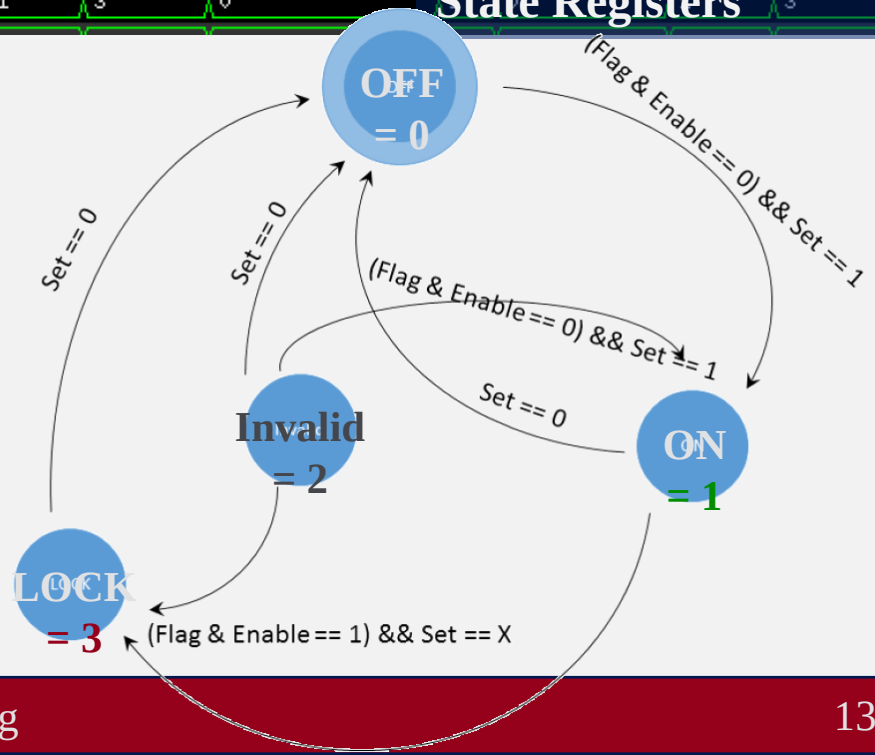




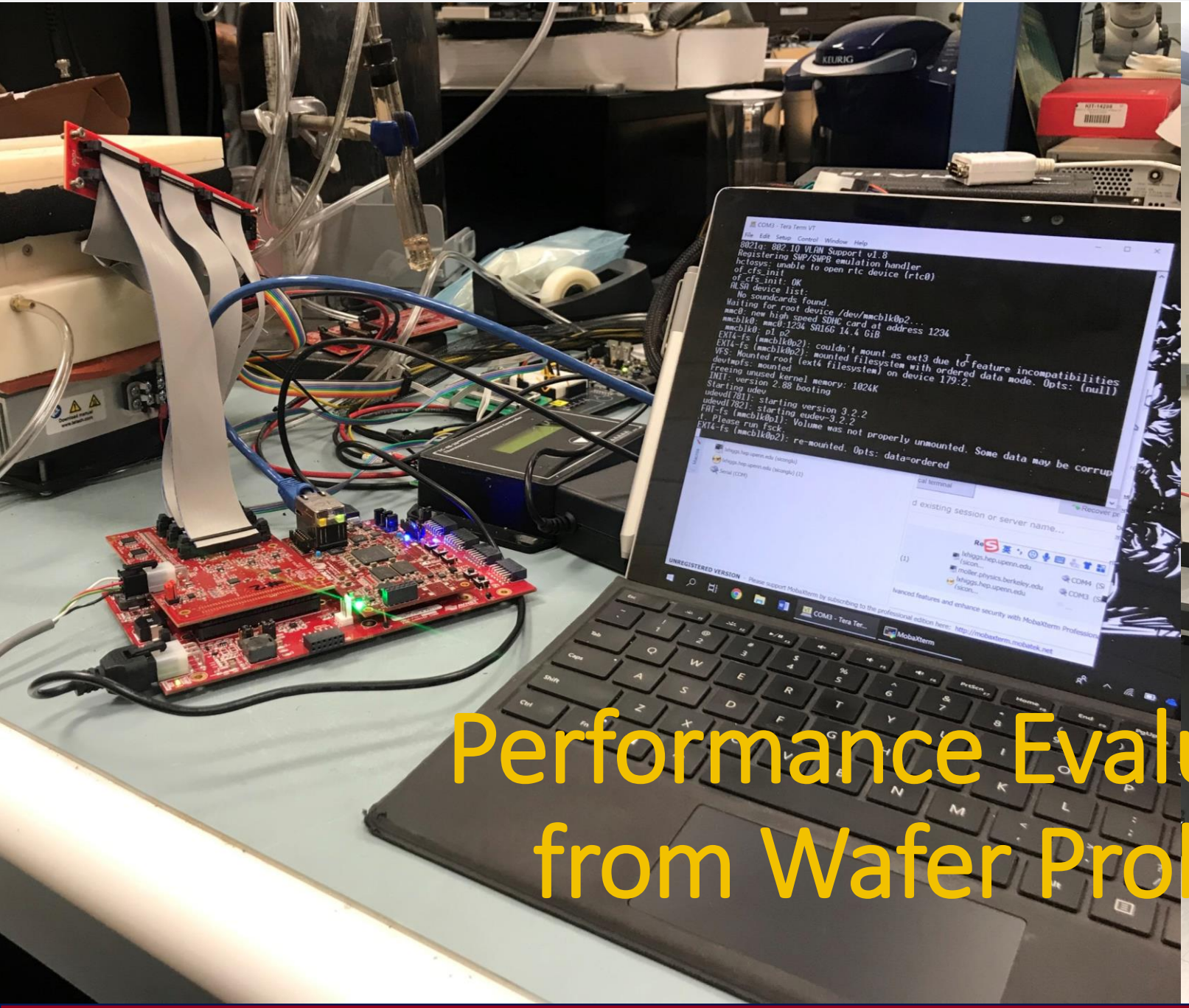
Example Test Routine (Interlock Toggling under single SEU blast)



- **Coroutine #1:**
  - Simulate the interlock move conditions by commands
  - Verify that the resulting interlock states are correct
- **Coroutine #2:**
  - Continuously inflict random **S**ingle **E**vent **U**pset on any register in related interlock channel
- Note that the **triplicated** register correct themselves!



Performance Evaluation from Wafer Probing



Numerical AMAC Performance Evaluation

Voltage Measurement

Current Measurement

Temperature Measurement

Digital-to-Analog Output

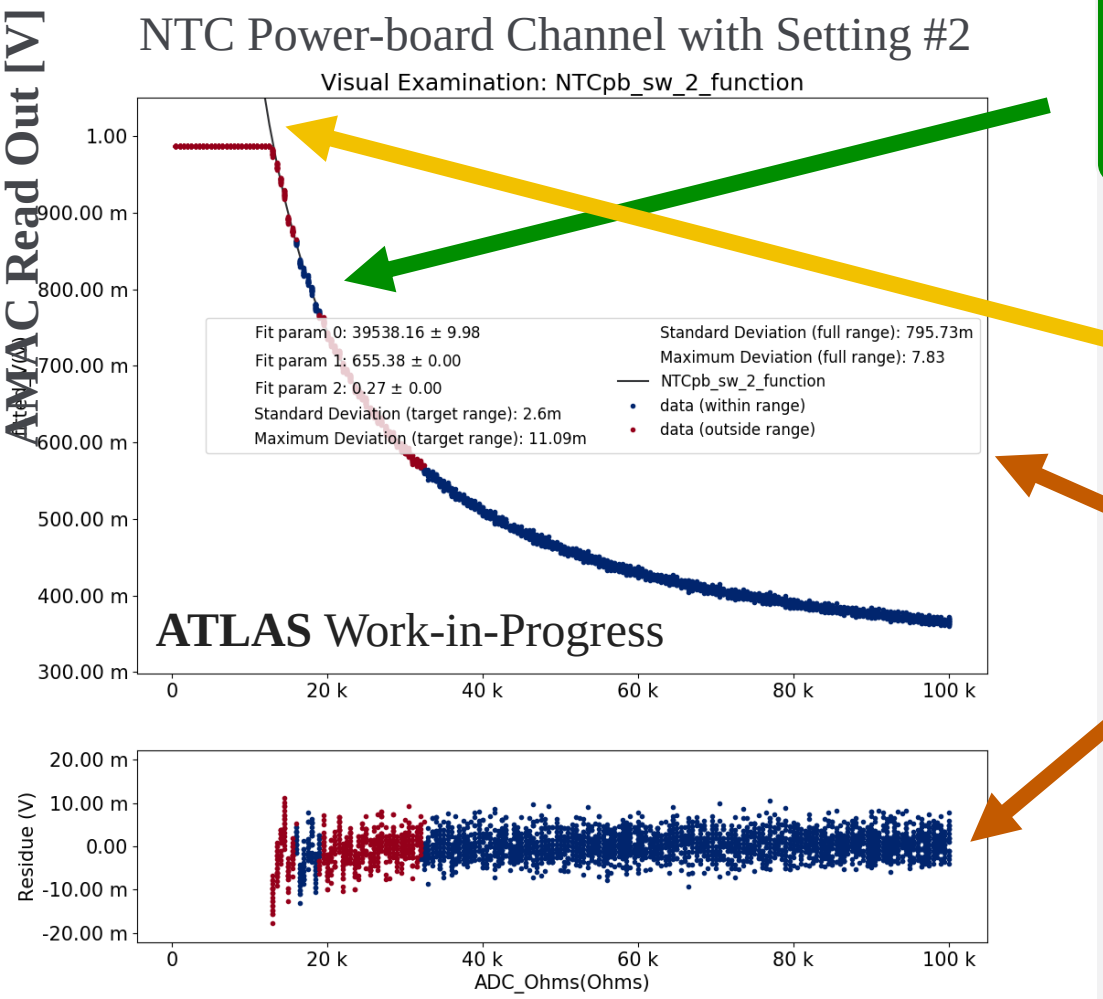
- ✓ Use external digital device to scan the measurement
- ✓ Use AMAC to read the value multiple times
- ✓ Compare input and readout to check that it follows the design
- ✓ Fit to evaluate accuracy & precision

Only NTC measurement will be discussed here as an example of analysis procedure.

Analysis of Individual Tests

e.g. Fit to a simplified circuit model:

$$V_{\text{measure}} = 250\text{mV}\frac{R_{\text{sw}}}{R_{\text{NTC}} + R_{\text{internal}}} + V_{\text{zero}}$$



Collect Data Array

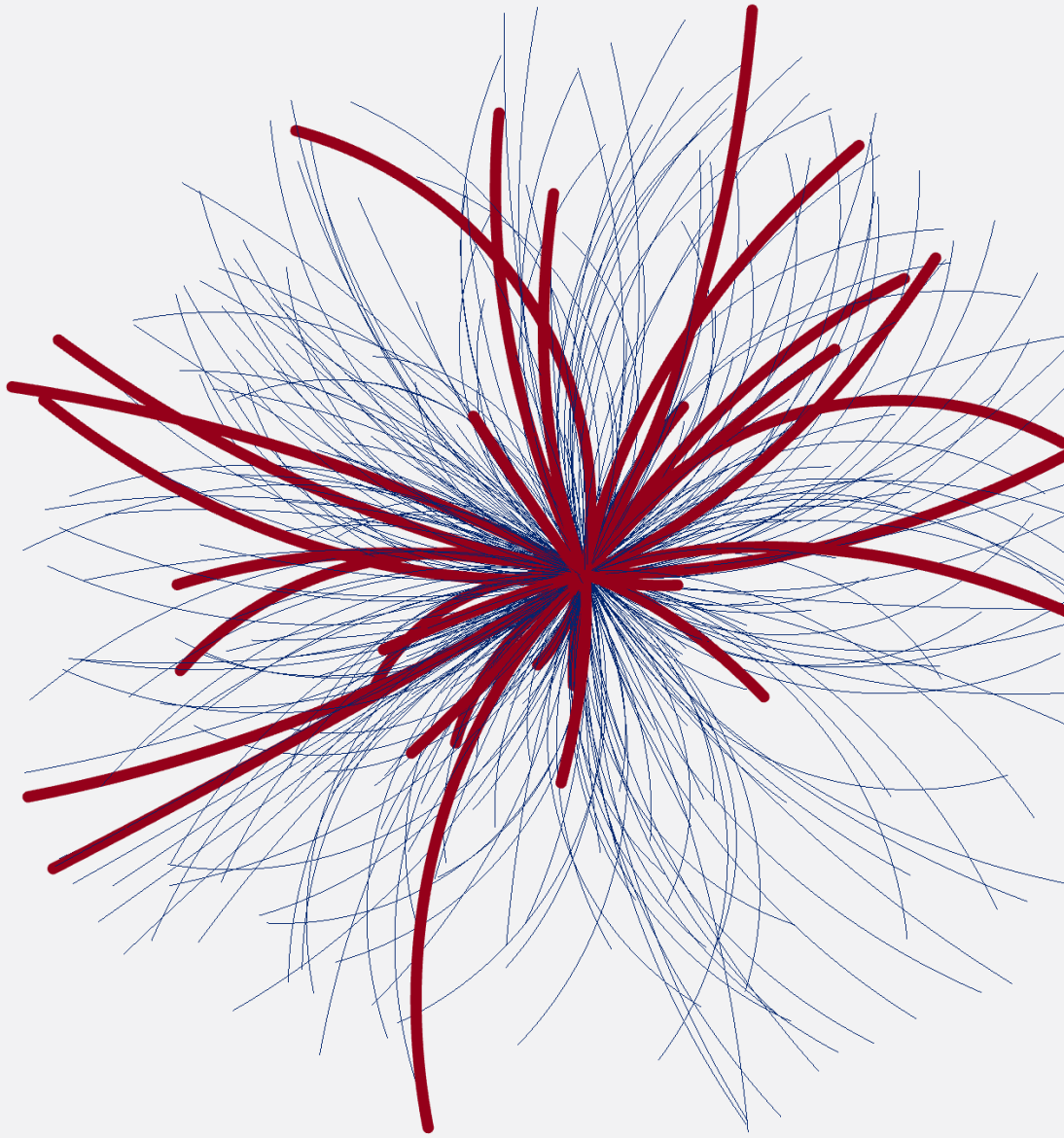
Fit to Designed Function

Numerical Fit Parameter & Residual Parameters

Save Result to Local and Online Database ⟹

The prototype has been exceptionally successful!
Luis will tell you more about it in the next presentation!

Thank you for your attention!!!



OUTLINE

- Autonomous Monitoring And Control
  - What is AMAC & Why we need it
  - Design of AMAC
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    - Control
    - Autonomous
    - Radiation Hard
  - Verification of AMAC
    - Digital Verification
    - Analog Verification

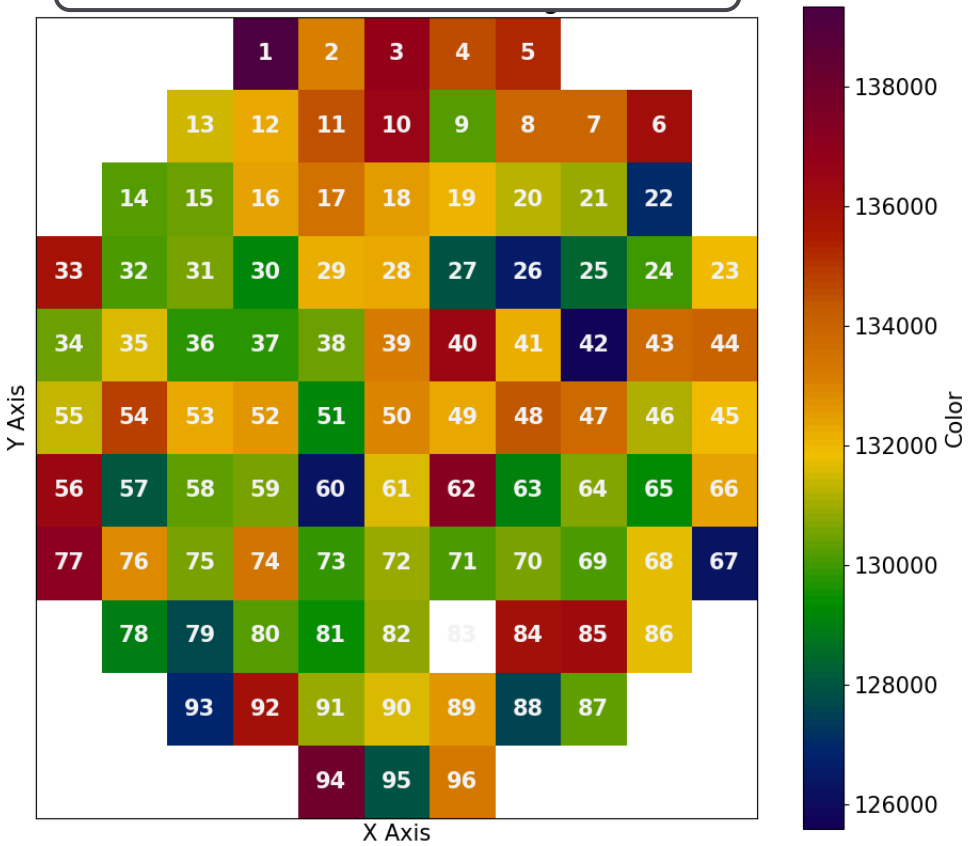
Back-Up

Numerically Fitted Chip Parameter
NTC Power-board Resistance - R_0

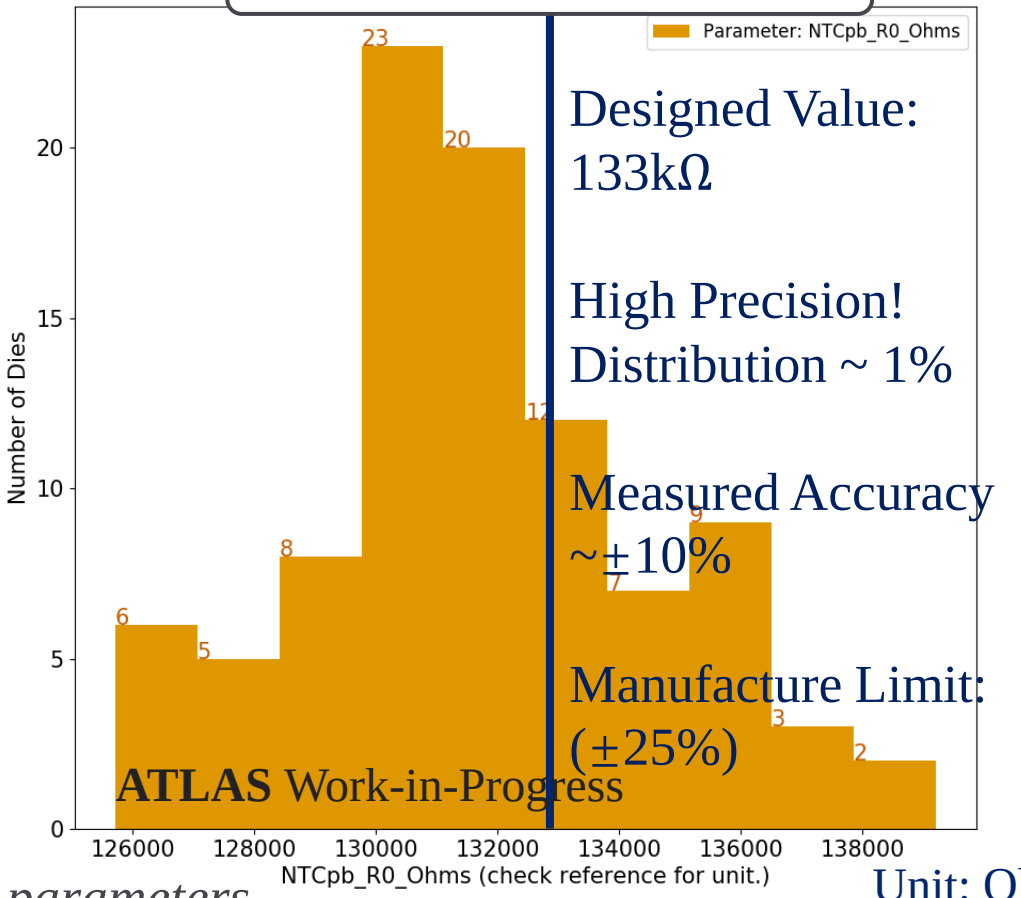
Wafer : **V0CVRFH**
Dice: 95/96 passed

Distribution by Chip on Wafer

Unit: Ohms



Parameter Value Histogram



Unit: Ohms

Like this one above, we have:

>1000 collected parameters

>200 analog diagnostic parameters

>50 analog pass/fail parameters

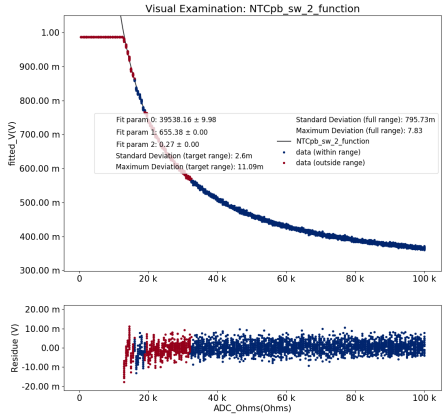
Data Flow from **Wafer Probing** to **Dicing** & **Database**

*All results except Raw Data are **available online!***

Raw Data (.csv)

ADC_Ohms	END_NTC_SW	END_Count
65000	0	935.312 5.90253
65500	0	931.5 4.38748
66000	0	929.688 3.09675
66500	0	922.688 5.13224
67000	0	923 4.48609
67500	0	915.312 4.1791
68000	0	913.125 3.78938
68500	0	905 3.96863
69000	0	899.188 3.72858
69500	0	898.438 5.52233
70000	0	891.75 3.78319
70500	0	887.125 4.25551
71000	0	883.688 4.7791
71500	0	880.188 3.20583
72000	0	872.125 6.34306
72500	0	872.875 4.09077
73000	0	869.938 4.87941
73500	0	860.688 5.76323
74000	0	858.125 4.48435
74500	0	854.562 4.21261
75000	0	854.375 5.01093
75500	0	847.375 4.21122
76000	0	846.625 5.23062
76500	0	842.625 3.56853

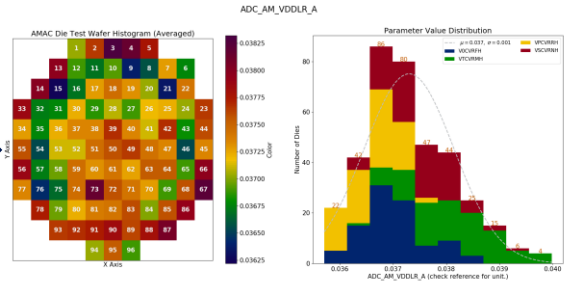
Numerical Fit & Grading (.py)



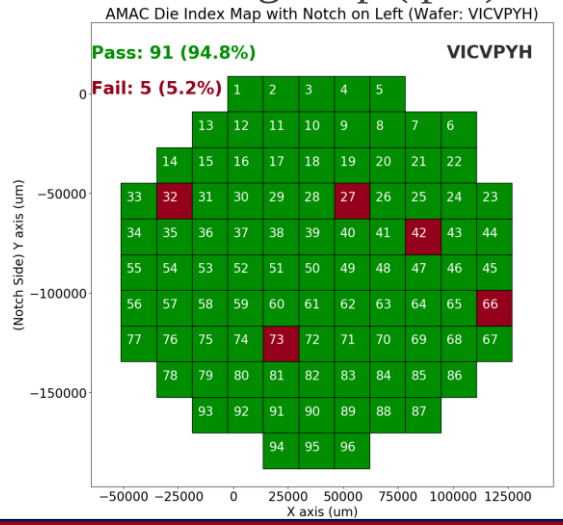
Parameterized Record (.csv)

NTCx_sw_1_function_fitted_V_residue_std_full_range	2.47422921
NTCx_sw_1_function_xName	ADC_Ohms
NTCx_sw_1_function_ADC_Ohms_range_max	100000
NTCx_sw_1_function_suffix	NTCx_sw_1_function
NTCx_sw_1_function_fitted_V_range_min	0.411553934
NTCx_sw_1_function_mask_str	(END_Counts > 100 & END_
NTCx_sw_1_function_fitted_V_residue_std_target_range	0.007169923
NTCx_sw_1_function_fitted_V_residue_max_dev_target_range	0.043140791
NTCx_sw_1_function_yUnit	V
NTCx_sw_1_function_fitted_V_range_max	0.873929299
NTCx_sw_1_function_fitted_V_residue_max_dev_full_range	27.0844731
NTCx_sw_1_function_xUnit	Ohms
NTCx_sw_1_function_ADC_Ohms_range_min	29000
NTCx_sw_1_function_yName	fitted_V
HVRET_3_ramp_function_slope	0
HVRET_3_ramp_function_xName	ADC_uA_Expected
HVRET_3_ramp_function_END_Counts_residue_std_full_range	0
HVRET_3_ramp_function_END_Counts_range_max	1023
HVRET_3_ramp_function_suffix	HVRET_3_ramp_function
HVRET_3_ramp_function_intercept	0
HVRET_3_ramp_function_END_Counts_residue_std_target_rang	0
HVRET_3_ramp_function_mask_str	(END_Counts > 300 & END_
HVRET_3_ramp_function_yUnit	count
HVRET_3_ramp_function_ADC_uA_Expected_range_min	99.9725

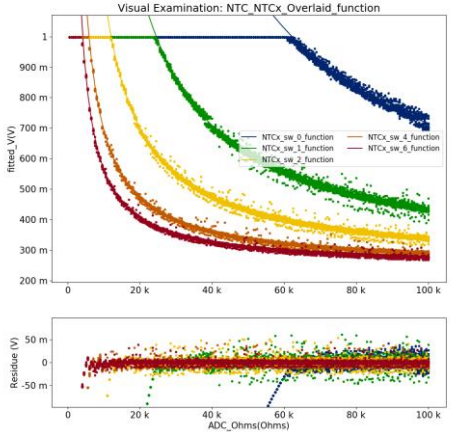
Wafer Statistics Distribution (.csv)



Dicing Map (.pdf)



Visual Examination (.png/.html)



Component Property& Test Run (.json)

Parent Directory

- AMACv2a_0x0000200a_try2_AMAC_DAC_CALX_RAMP_FUNCTION.json
- AMACv2a_0x0000200a_try2_AMAC_DAC_CALY_RAMP_FUNCTION.json
- AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALX_RAMP_FUNCTION.json
- AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALY_RAMP_FUNCTION.json
- AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_SHUNTX_RAMP_FUNCTION.json


```
{"component": "20USG000500876", "problems": false, "results": {}, "defects": [], "testTypeState":
"active", "date": "29.05.2020", "testType": "POWER_FUNCTIONS", "institution": "UPENN", "runNumber":
"try2", "comments": [], "properties": {"ADC_VDD_HI_V_OFF": 0.00030518, "BEST_WORKING_VDD": 1.23804,
"ADC_VDDLR": 1.47433, "ADC_AM_VDDLR_V": 1.4831, "ADC_AM_VDDLR_A": 0.0369268, "BEST_AM600BG": 0.620813,
"BEST_AMBG": 13, "ADC_VDD_HI_A_RO7_4HVO0": 0.00421381, "ADC_VDD_HI_A_RO7_4HVO1": 0.00493768,
"ADC_VDD_HI_A_RO7_4HVO2": 0.0048784, "ADC_VDD_HI_A_RO7_4HVO3": 0.0047892, "ADC_AM_VDD_HI_A": 1.49598e-05,
"ADC_VDD_HI_V_RO7_4HVO3": 3.14046, "ADC_VDD_HI_V_RO7_4HVO2": 3.14046, "ADC_VDD_HI_V_RO7_4HVO1": 3.14046,
"ADC_VDD_HI_V_RO7_4HVO0": 3.17639, "BEST_VDD": 1.23804, "ADC_AM_VDD_HI_V": 0.000228885, "BEST_RAMP": 0,
"BEST_SLOPE": 1.00578, "ADC_AM_LVDS_CM1": 0.69482, "ADC_AM_LVDS_CM0": 0.680705, "BEST_WORKING_VDDBG": 11,
"BEST_VDDBG": 11, "ADC_AM_VDCDC_V": 0.00015259, "ADC_VDD_HI_A_STD_RO7_4HVO2": 0.00104764,
"ADC_VDD_HI_A_STD_RO7_4HVO3": 0.00105412, "ADC_VDD_HI_A_STD_RO7_4HVO0": 0.000883412,
"ADC_VDD_HI_A_STD_RO7_4HVO1": 0.00105266, "ADC_VDD_HI_A_OFF": 0, "ADC_AM_VDCDC_A": 0.00015259}, "passed":
true}
```


ITk Production Database

ITk Production Database

https://itkpd-test.unicorncollege.cz/

Component Details

Show details of selected Component of the Inner Tracker.

20USG000501034

AMAC Chip - AMACv2a

Basic Properties

ATLAS SERIAL NUMBER
20USG000501034

COMPONENT TYPE
AMAC Chip AMAC

TYPE
AMACv2a

CURRENT STAGE
Probed at University of Pennsylvania

CURRENT LOCATION
University of Pennsylvania UPENN

PROJECT
Strips

SUBPROJECT
Strip general

REGISTRATION
03.06.2020 11:44
Sicong Lu

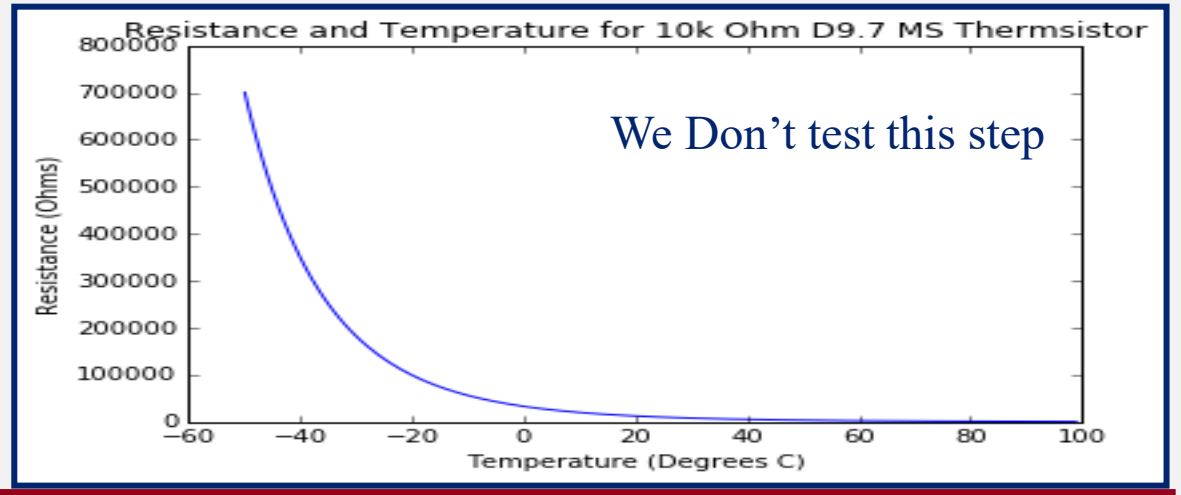
OWNER INSTITUTE
University of Pennsylvania UPENN

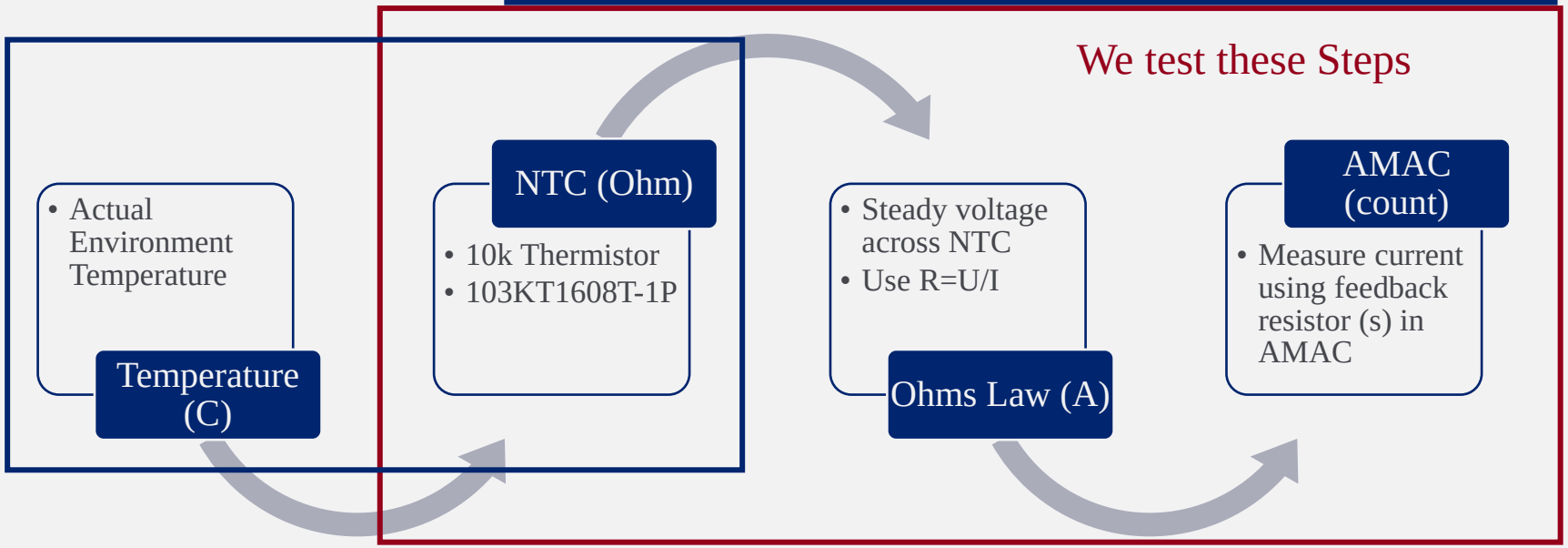
SHIPMENT DESTINATION
No current shipment destination

a73982646f2503de102f1bbe27254ca9

Example Temperature Measurement

- The way we measure the temperature:
  - Use industrial NTC
  - Measure Resistance through current
  - Measure Current (through resistor to voltage) by AMAC
- Simple Circuit:
  - Simple amplifier
  - Can measure resistance



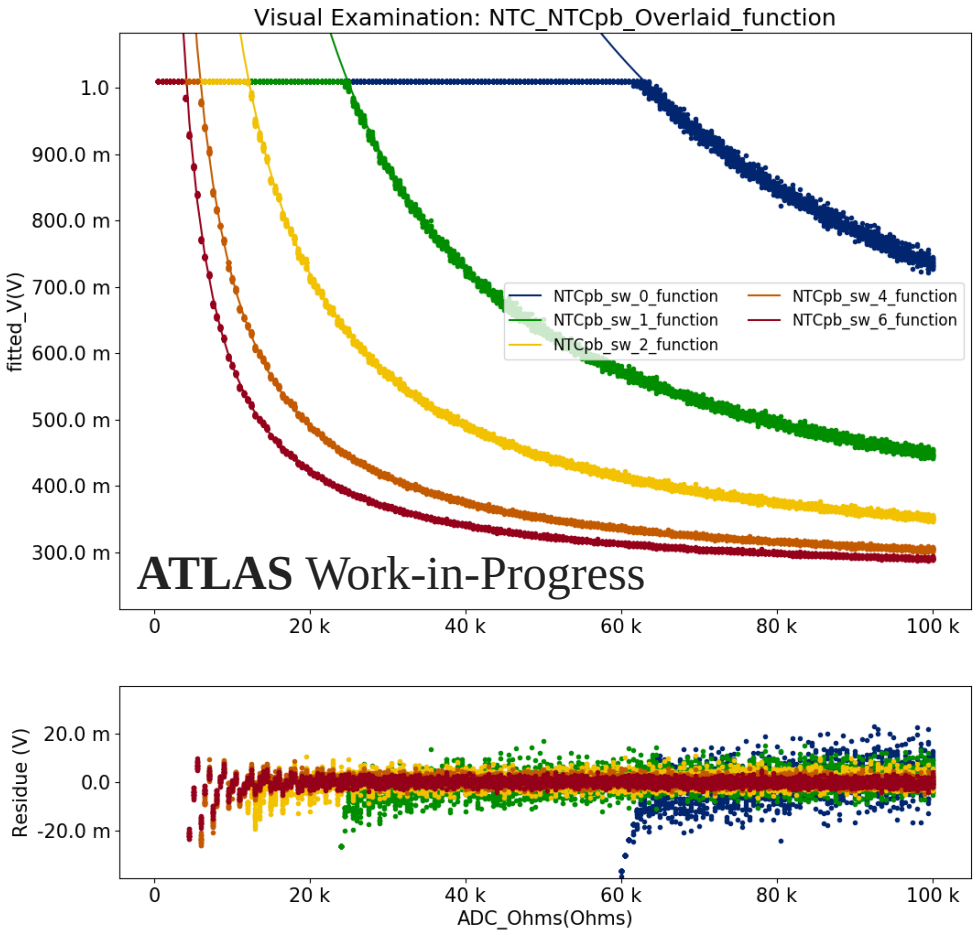


We also measure:
BPol12V by PTAT
(proportional to absolute temperature)
AMAC by CTAT
(complementary to absolute temperature)

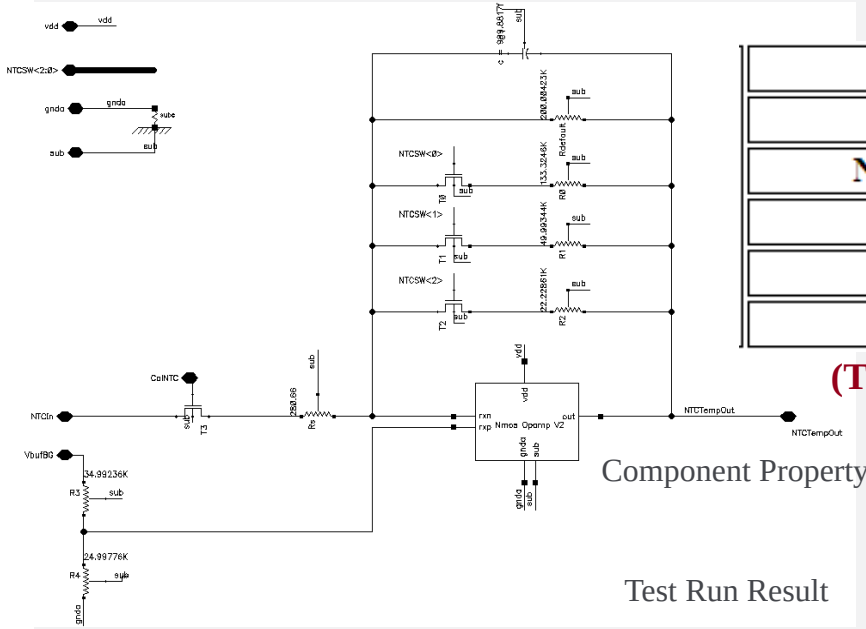
Example: Validation & Fit

Plot Fit by Simplified Circiuit Model:

$$V_{\text{measure}} = 250\text{mV}\frac{R_{\text{sw}}}{\boldsymbol{R}_{\text{NTC}} + R_{\text{internal}}} + V_{\text{zero}}$$



- Given the simple design, we can perform numerical fit for the individual resistance
- We could also use this to verify the how well is the manufacturer on producing resistors



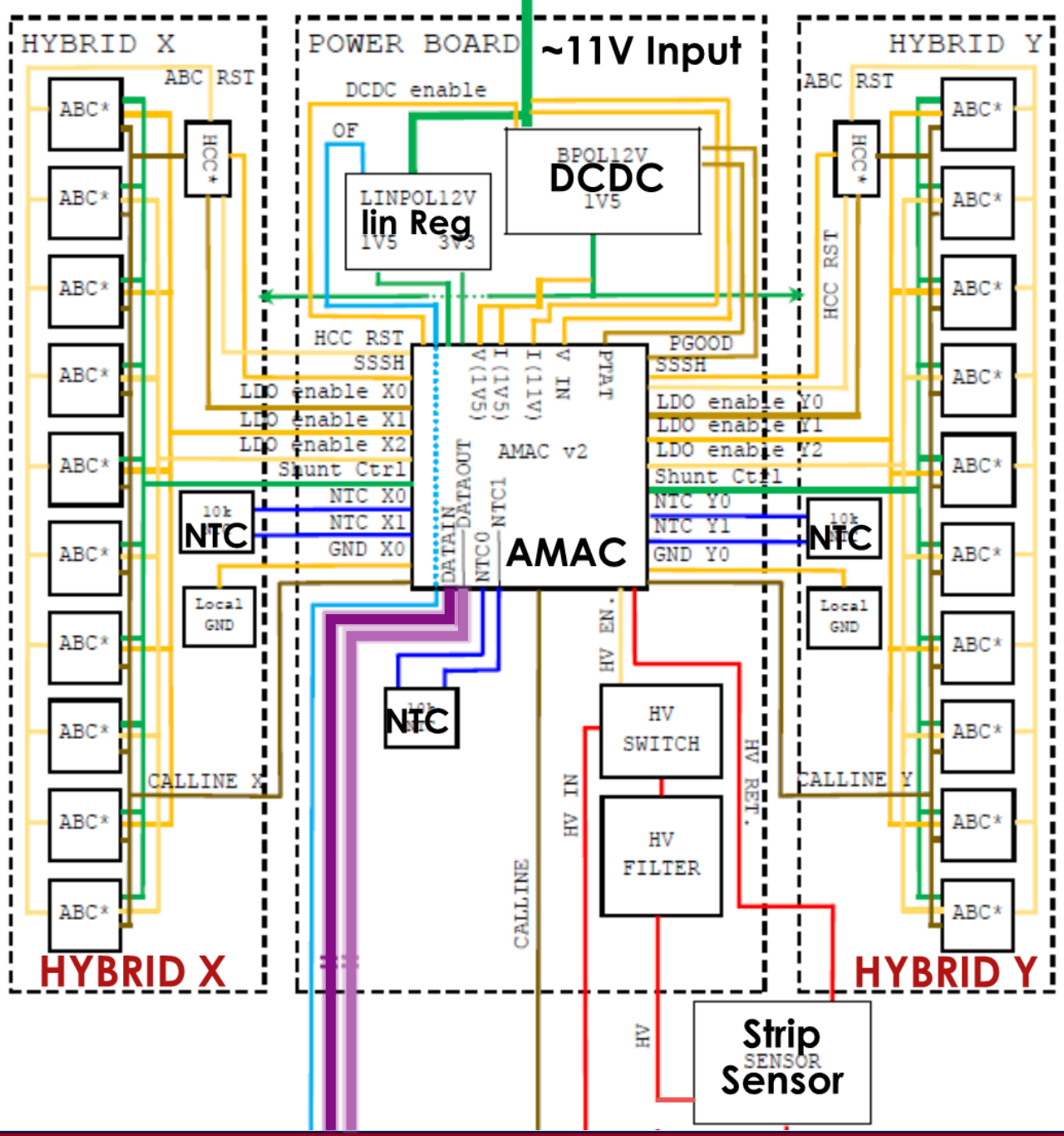
NTCx_R_internal	171.65
NTCx_V_zero	243.85m
NTCx_Rdefault_Ohms	188.77k
NTCx_R0_Ohms	123.86k
NTCx_R1_Ohms	45.87k
NTCx_R2_Ohms	20.31k

(They agree with the designed value!)

Component Property

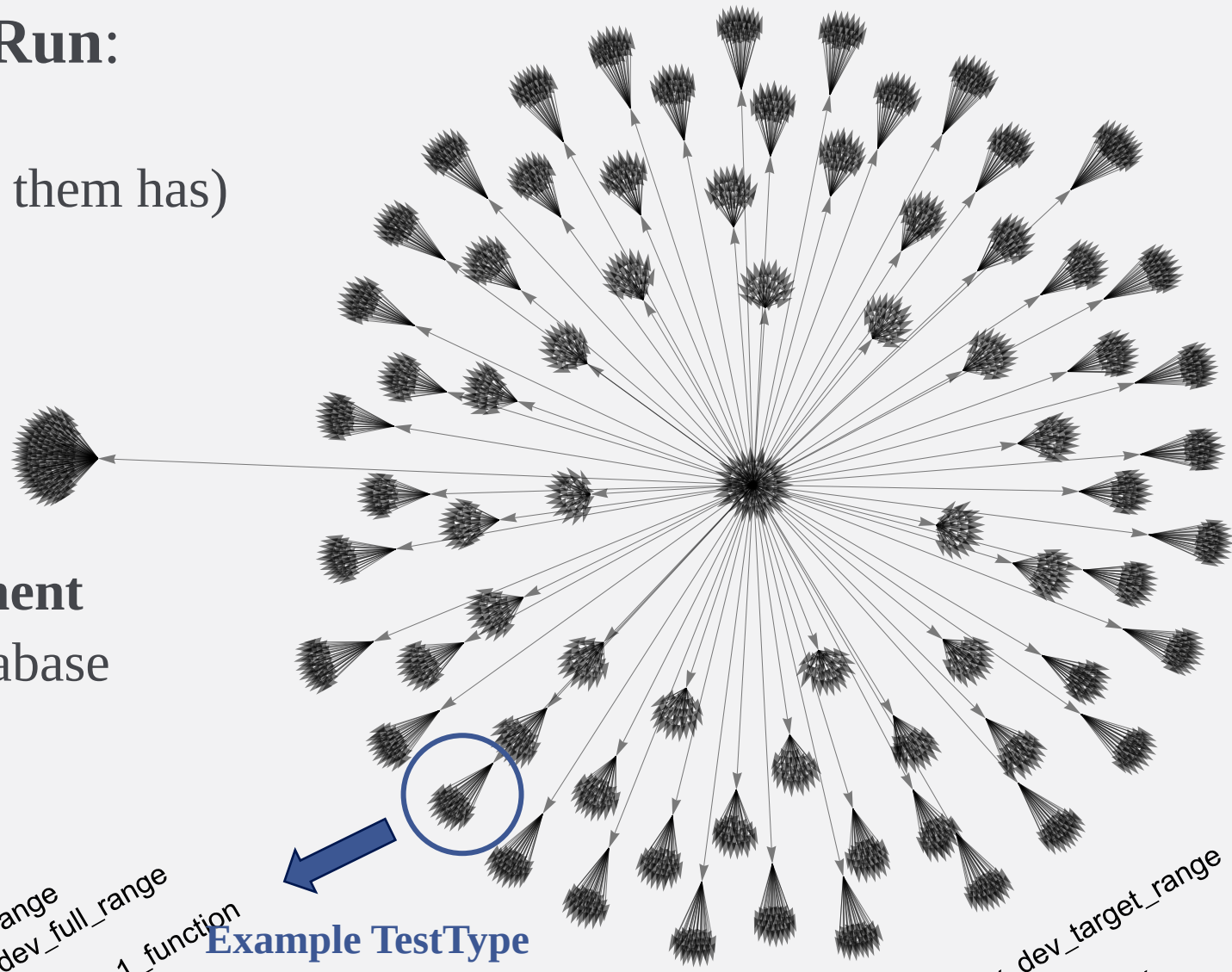
Test Run Result

NTCpb_sw_6_Ohms	14555.58796931094
NTCpb_sw_6_function	
29.05.2020 try1	✓



Reset in:
→SSSHx
→SSSHy
→ OFIn;
Resets Out
2 HCC Reset→
OFOut→
Voltage DAC:
Calx/y →;
Shuntx/y →;
Communications lines:
→ **Command Data In**;
Command Data Response →

- For each successful **AMAC - Test Run**:
  - 60 characterization **properties**
  - 72 **test** with fits and analysis (most of them has)
    - 8 **test parameters** per **test**
      - Each is an array of some type
    - 18 **test properties** per **test**
    - See next slides for example
- Database Structure Visualization ⇒
  - The center represent AMAC **Component**
  - Each arrow represent an object in database
    - Parameters, properties, tests, etc
  - Each cluster is a **TestType**



Example TestType