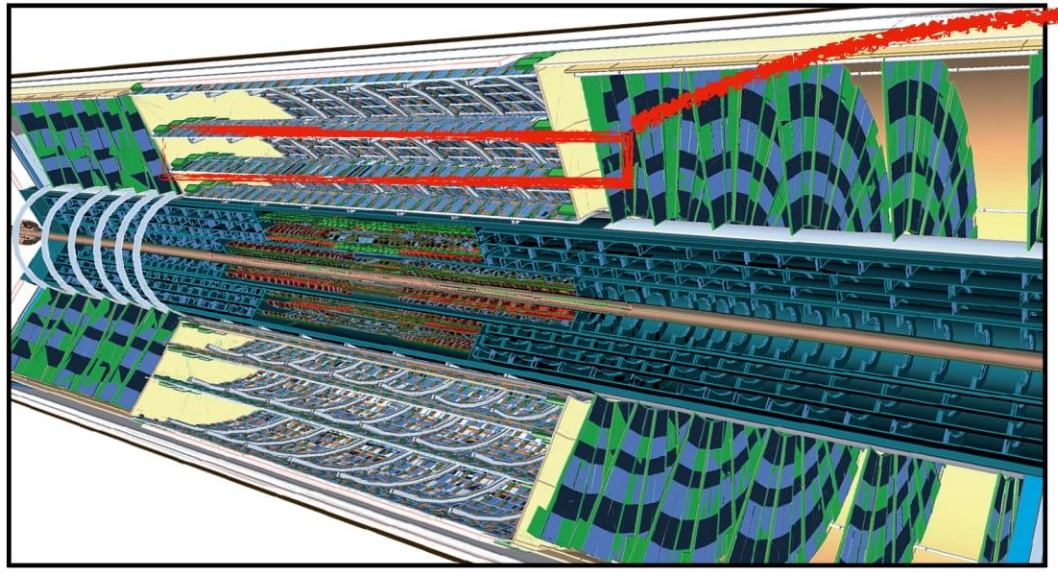
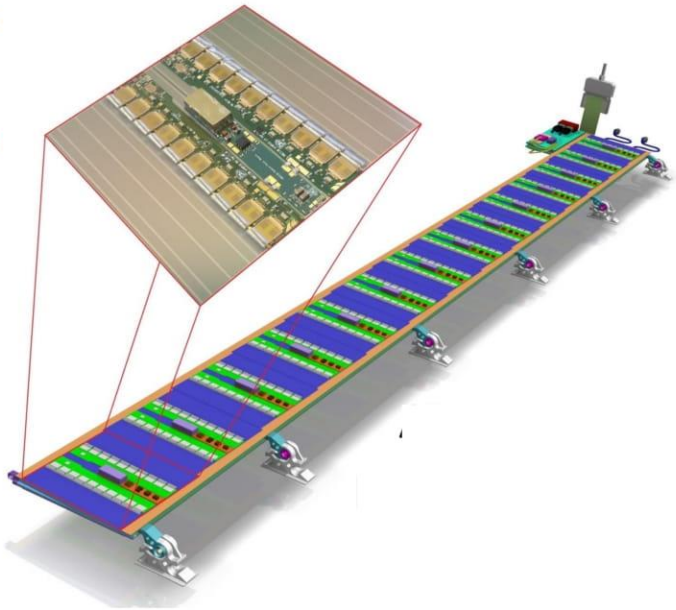
AMAC ASIC for the ATLAS ITk silicon strip detector
Design and Verification

Sicong Lu

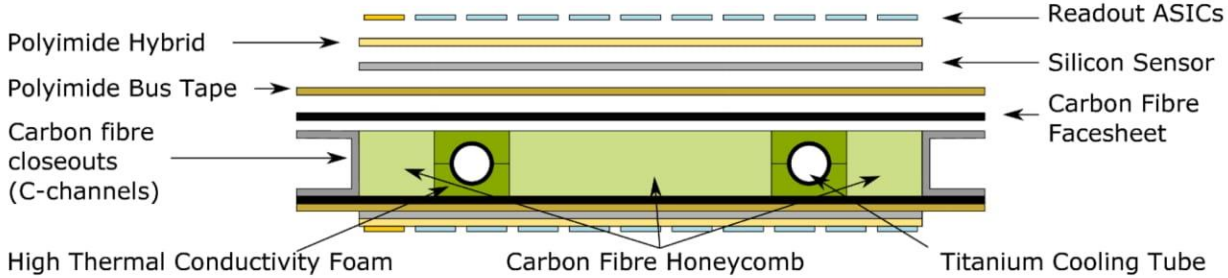
University of Pennsylvania
sicong.lu@cern.ch

Silicon Strips Stave





- Staves are the basic units of the ITk Strip Barrel detector
- It is made of a 1.4 m long support structure
  - provides **mechanical rigidity and support** by using high stiffness and high thermal conductivity carbon fiber
  - Provides **cooling** to modules
  - Polyimide bus-tape is co cured on both faces to channel power and data from and to the modules .
- 14 silicon modules are directly glued on both sides of the stave support structure



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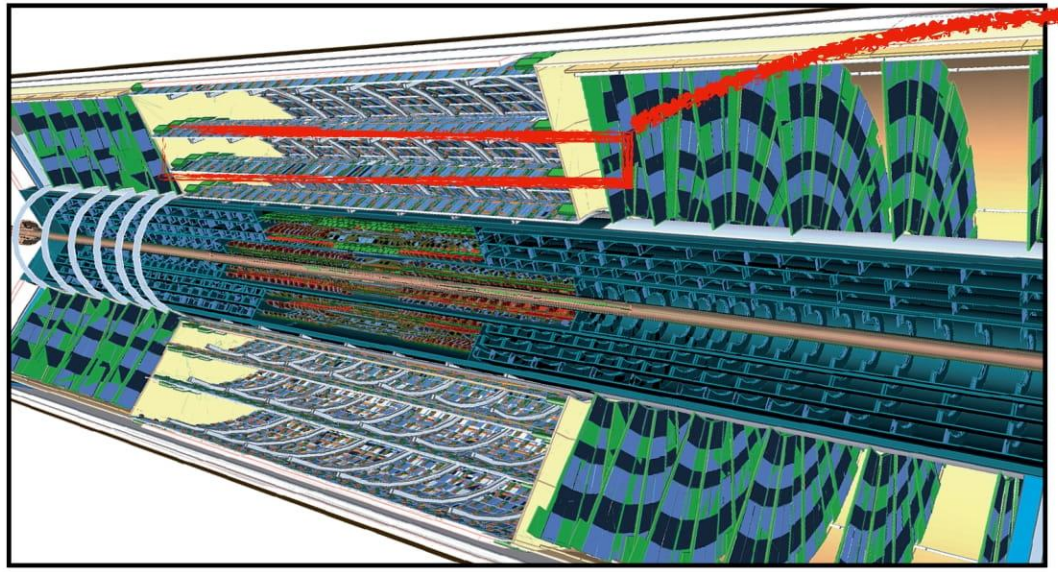

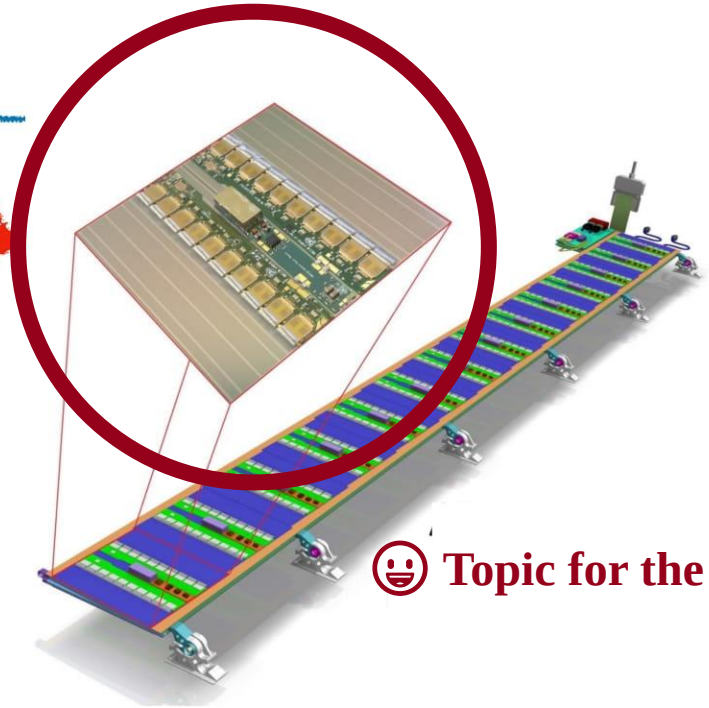

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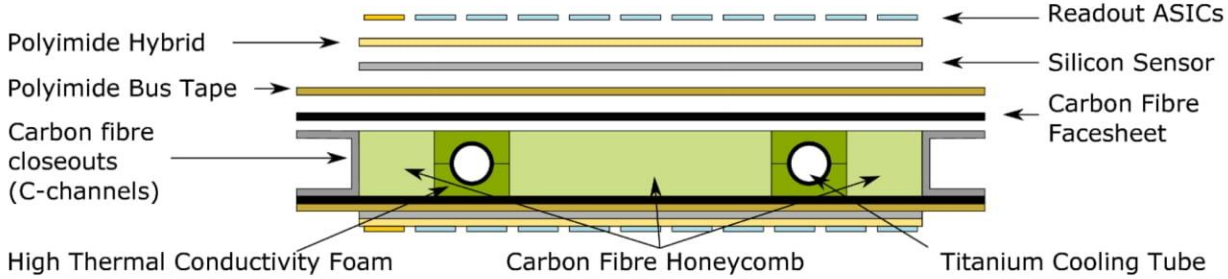

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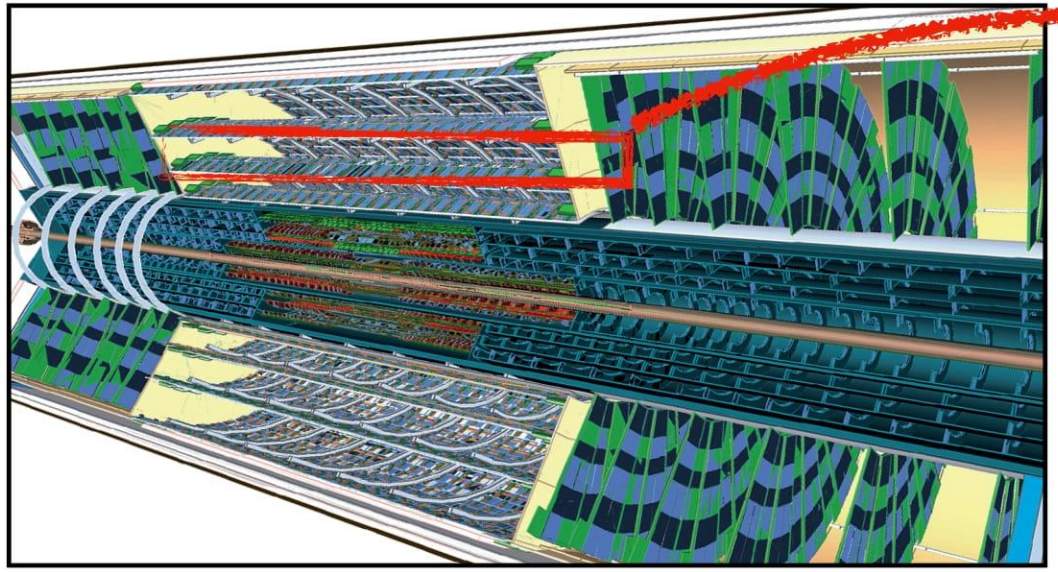

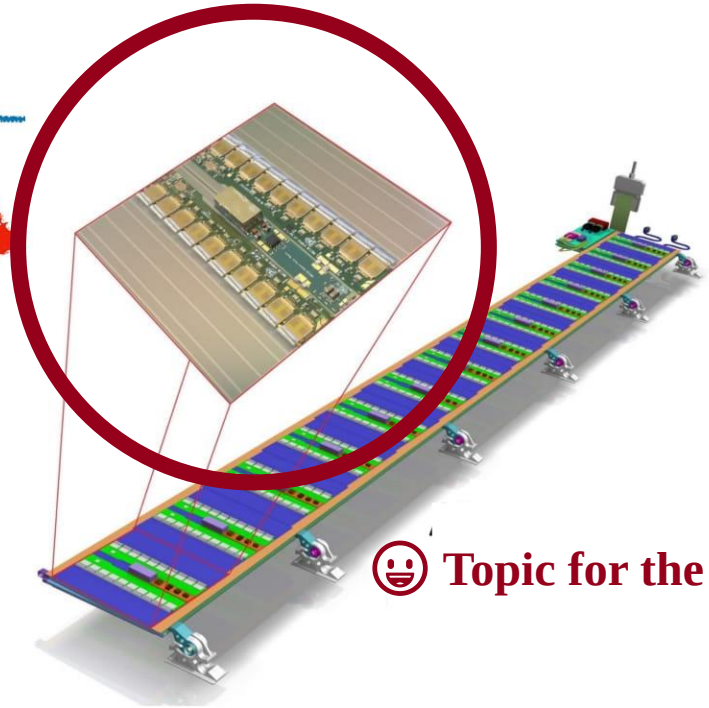

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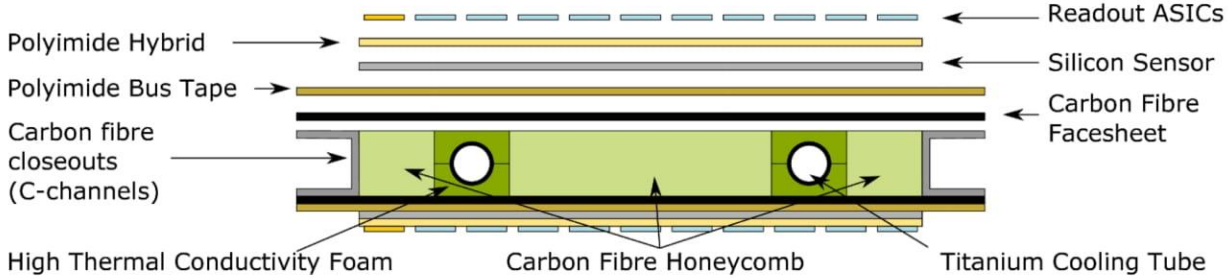

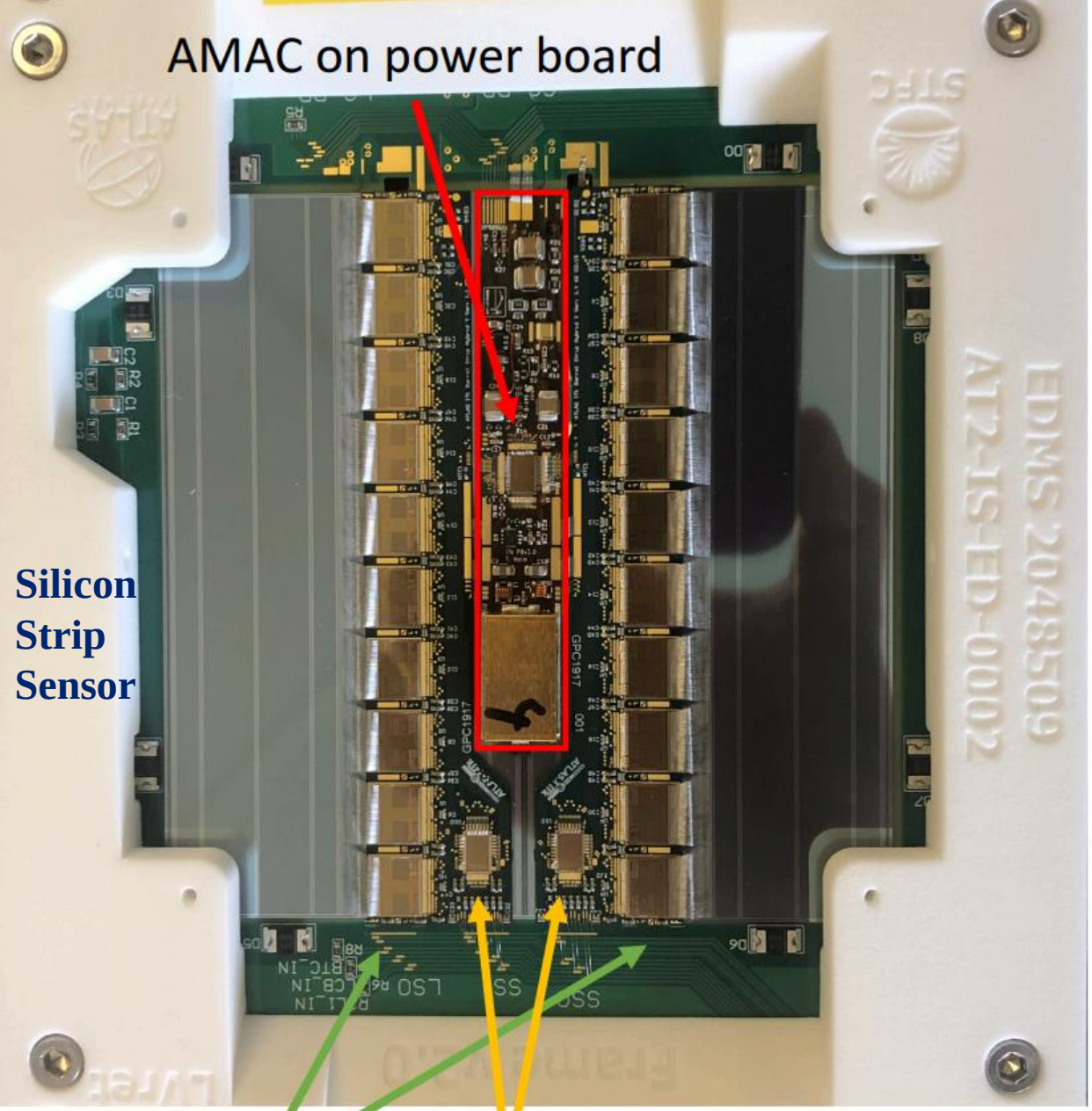

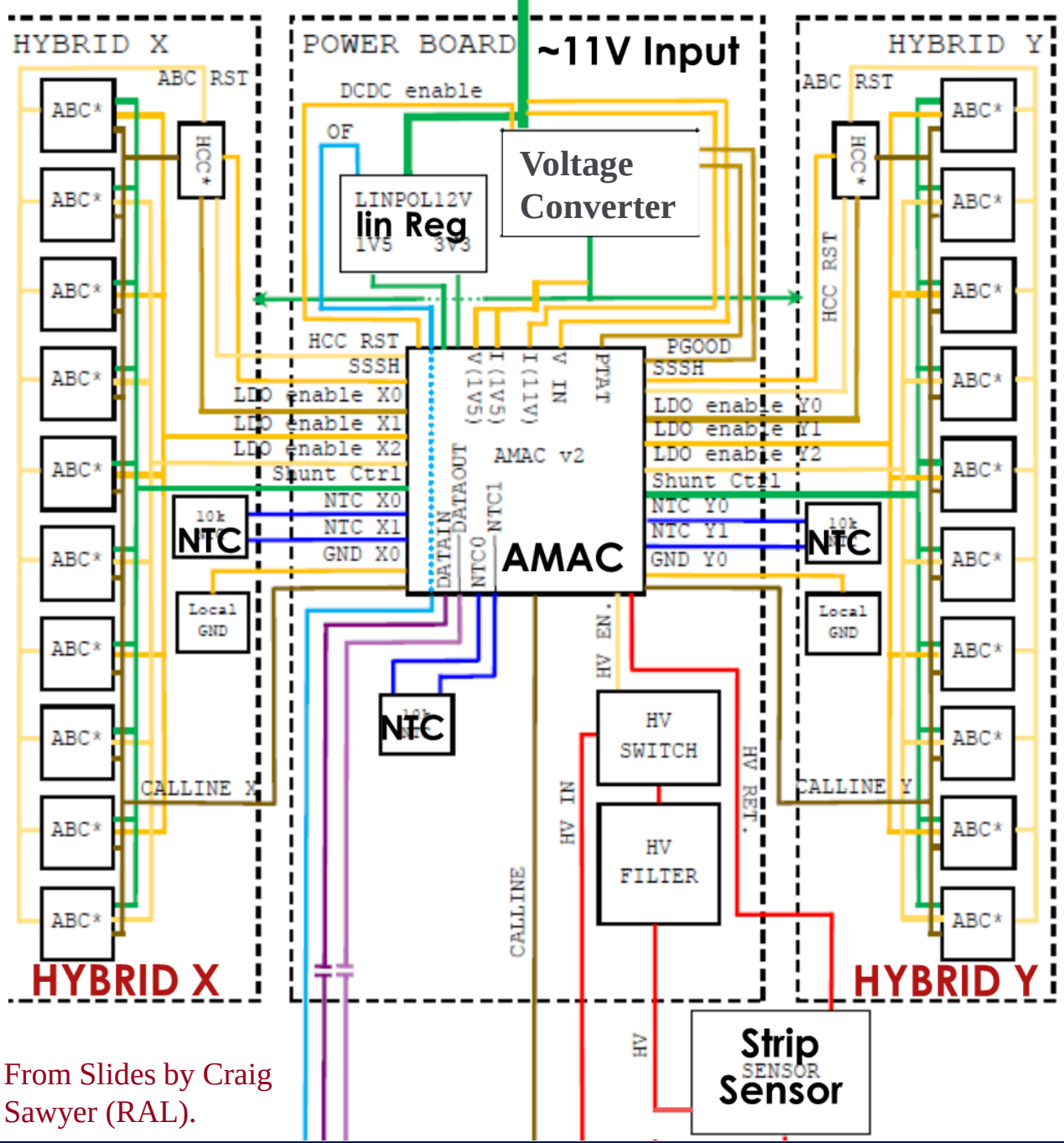

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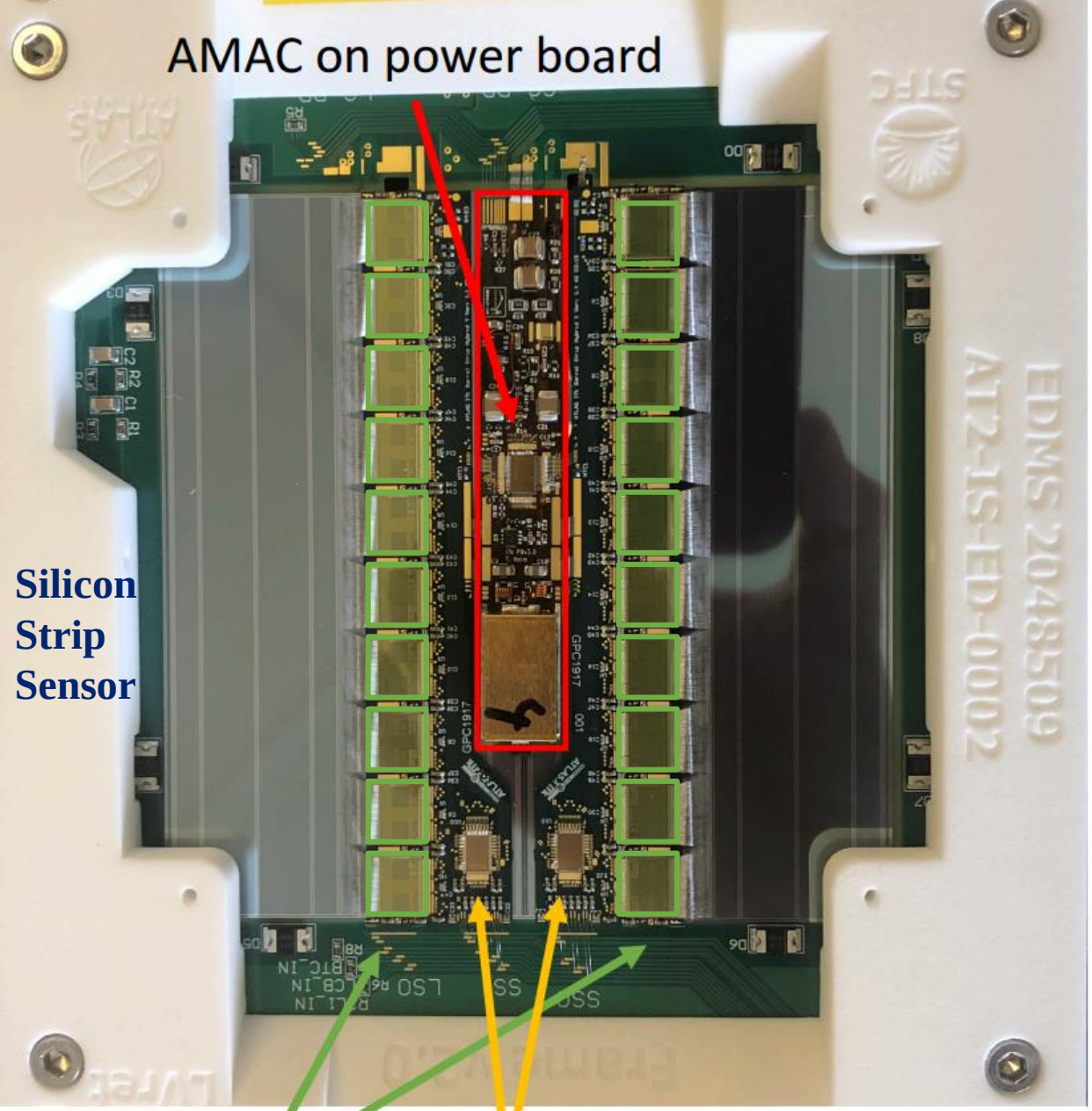

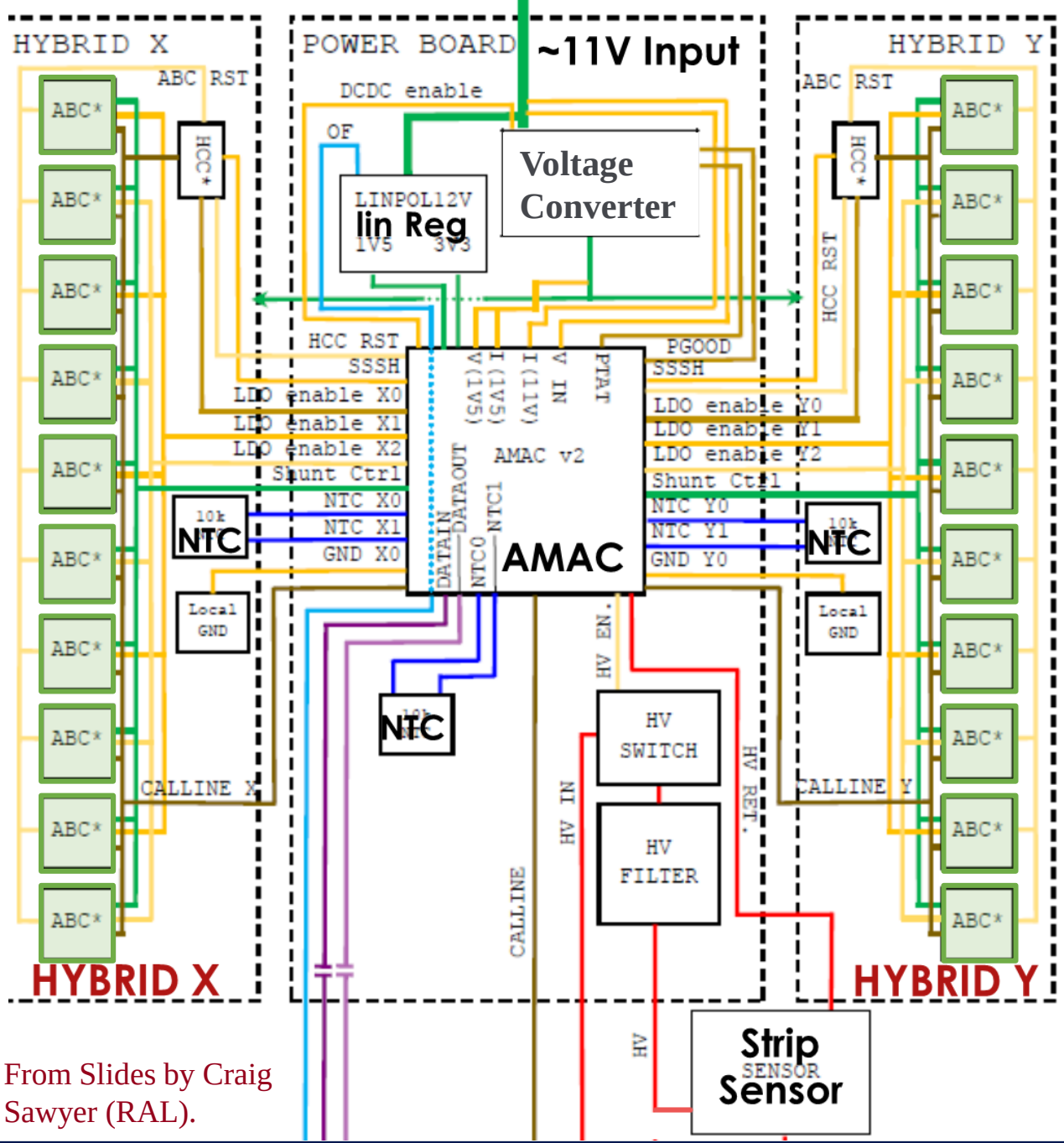

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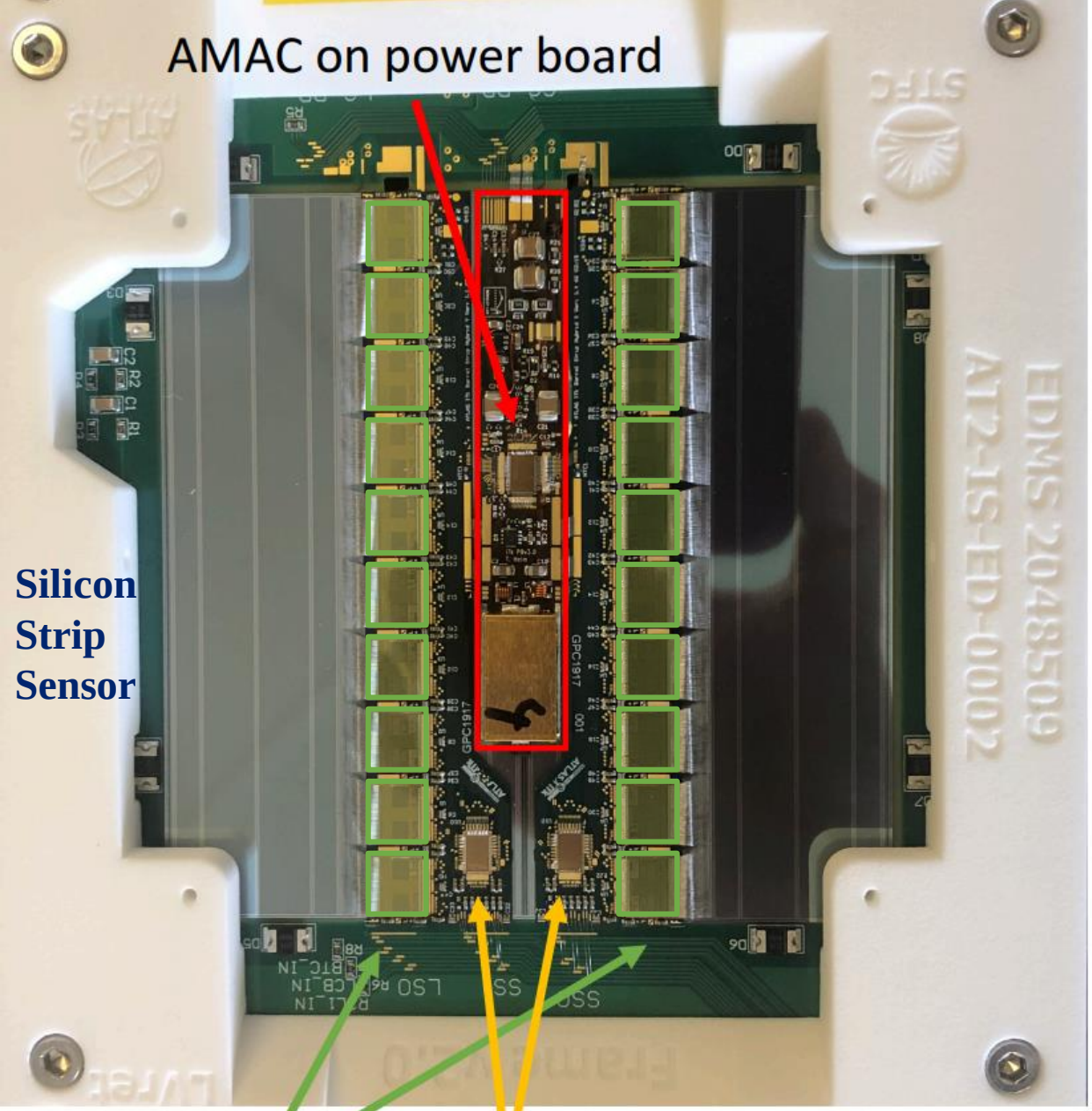

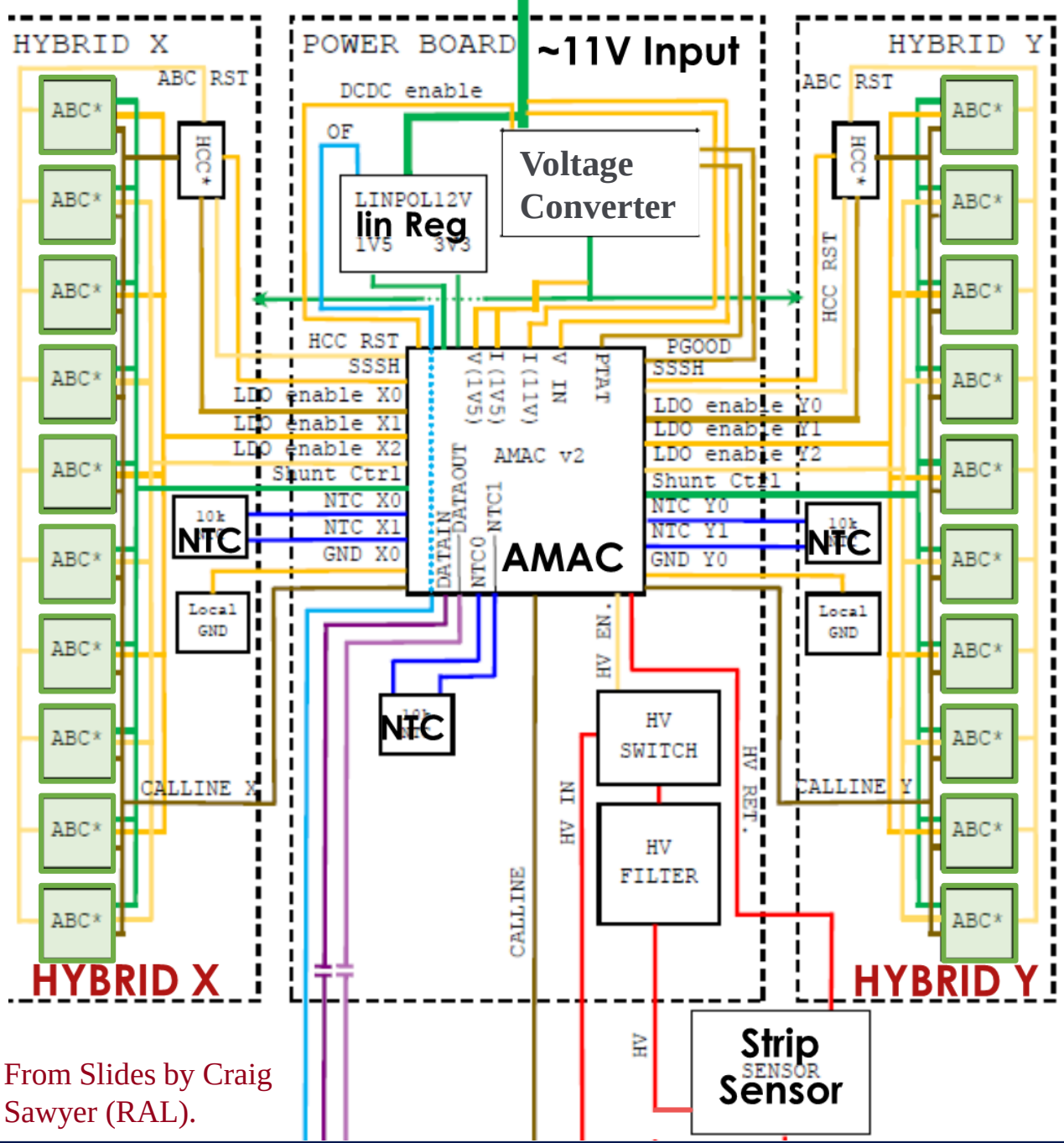

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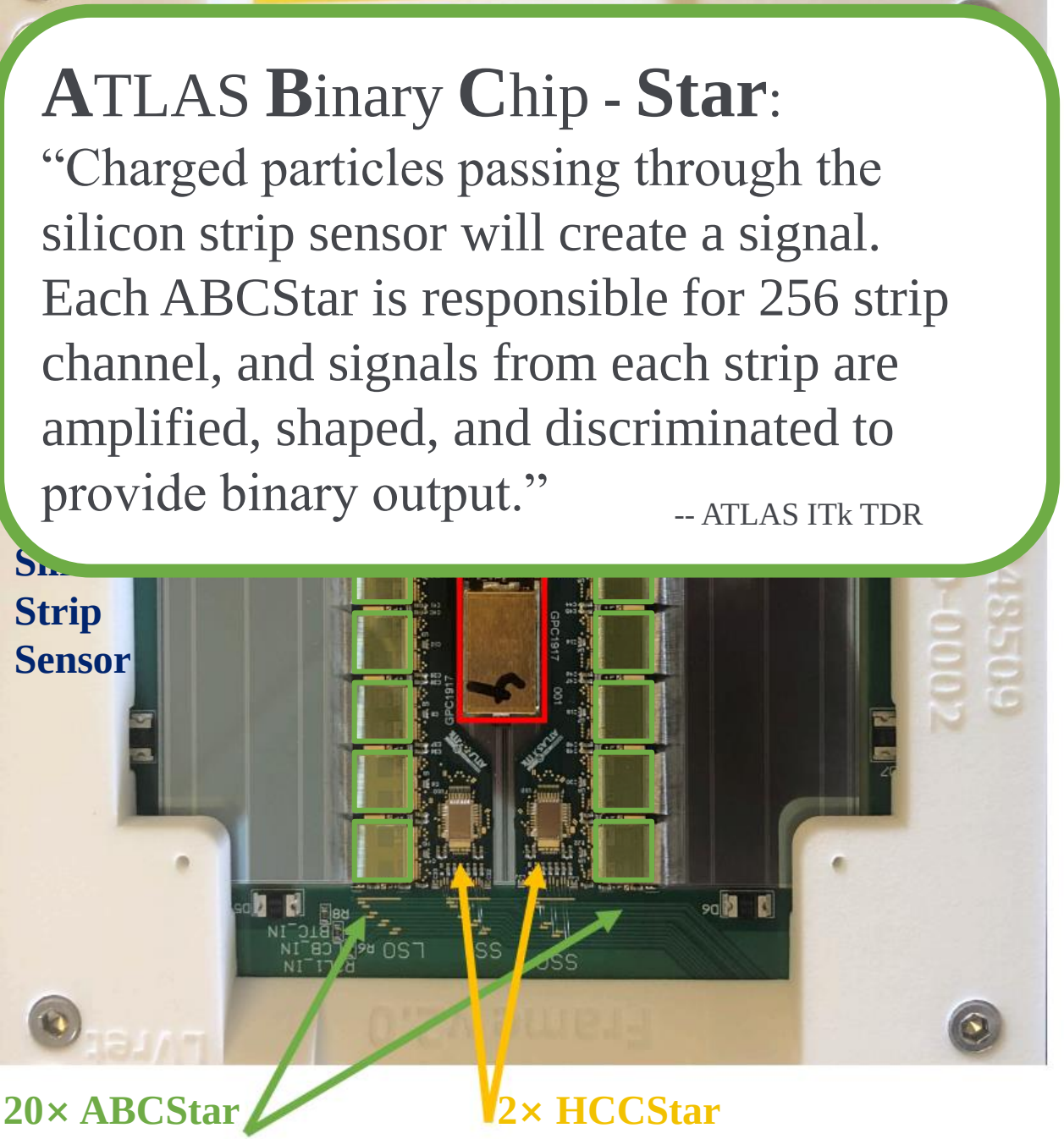
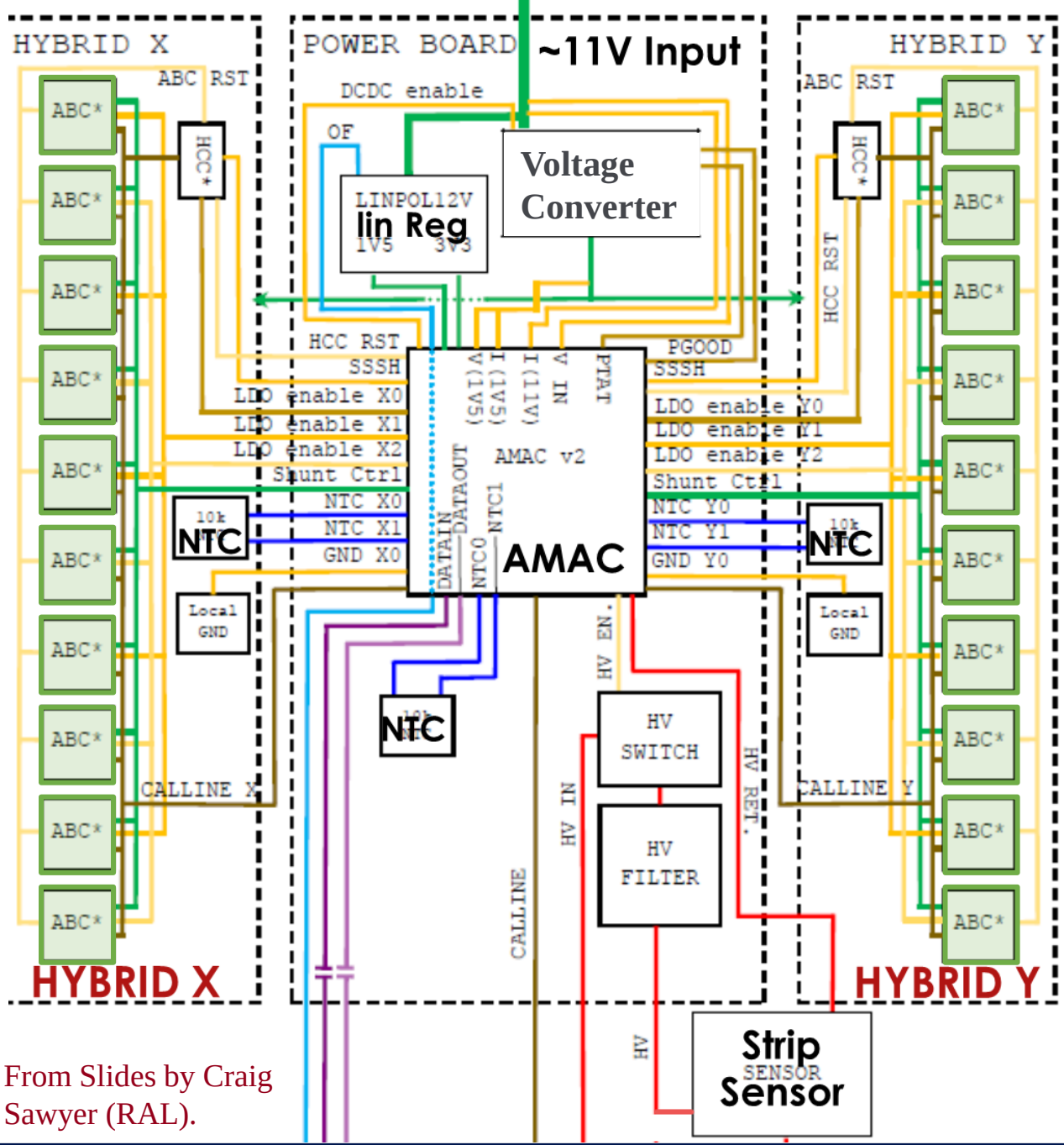
-- ATLAS ITk TDR





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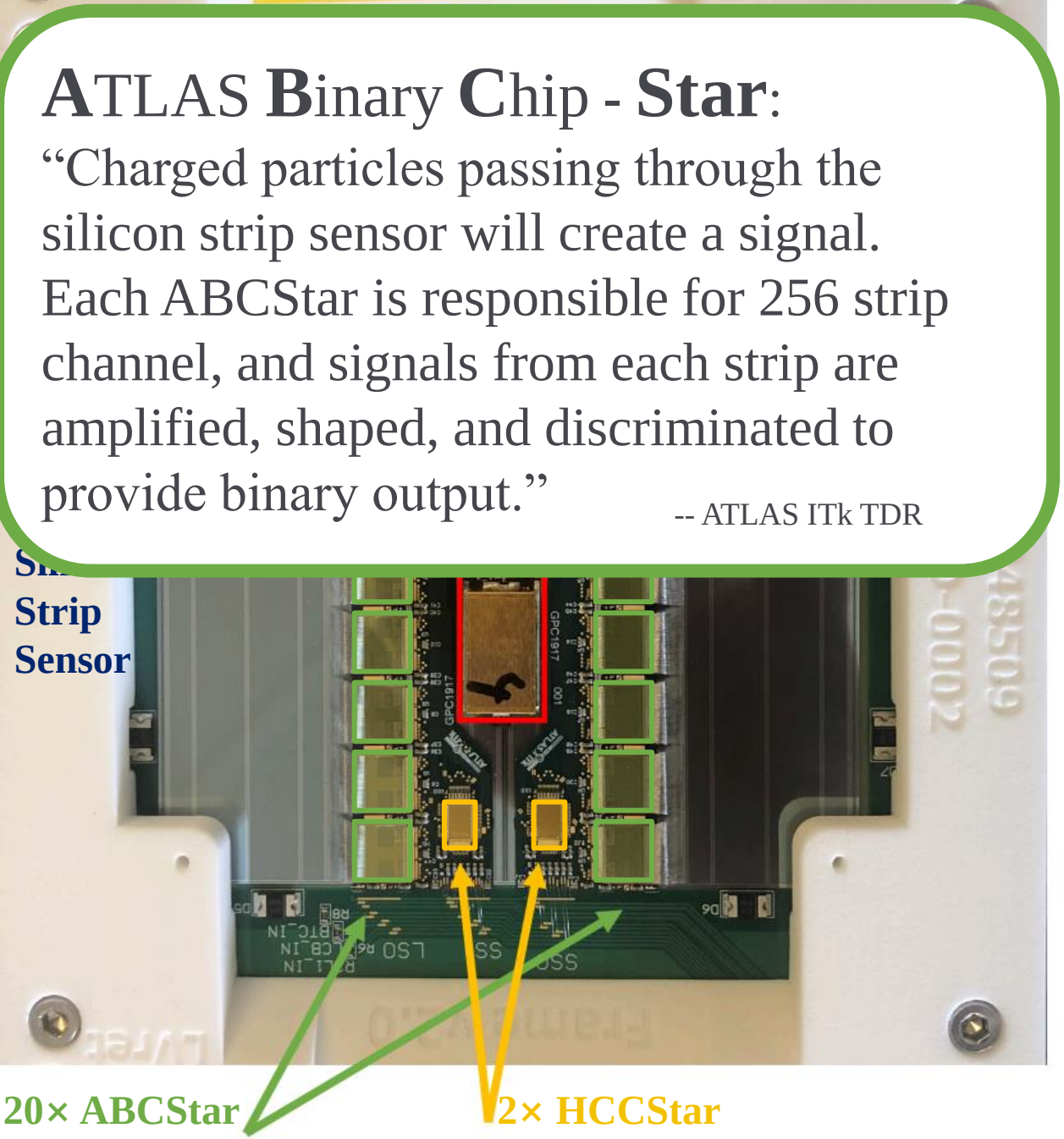

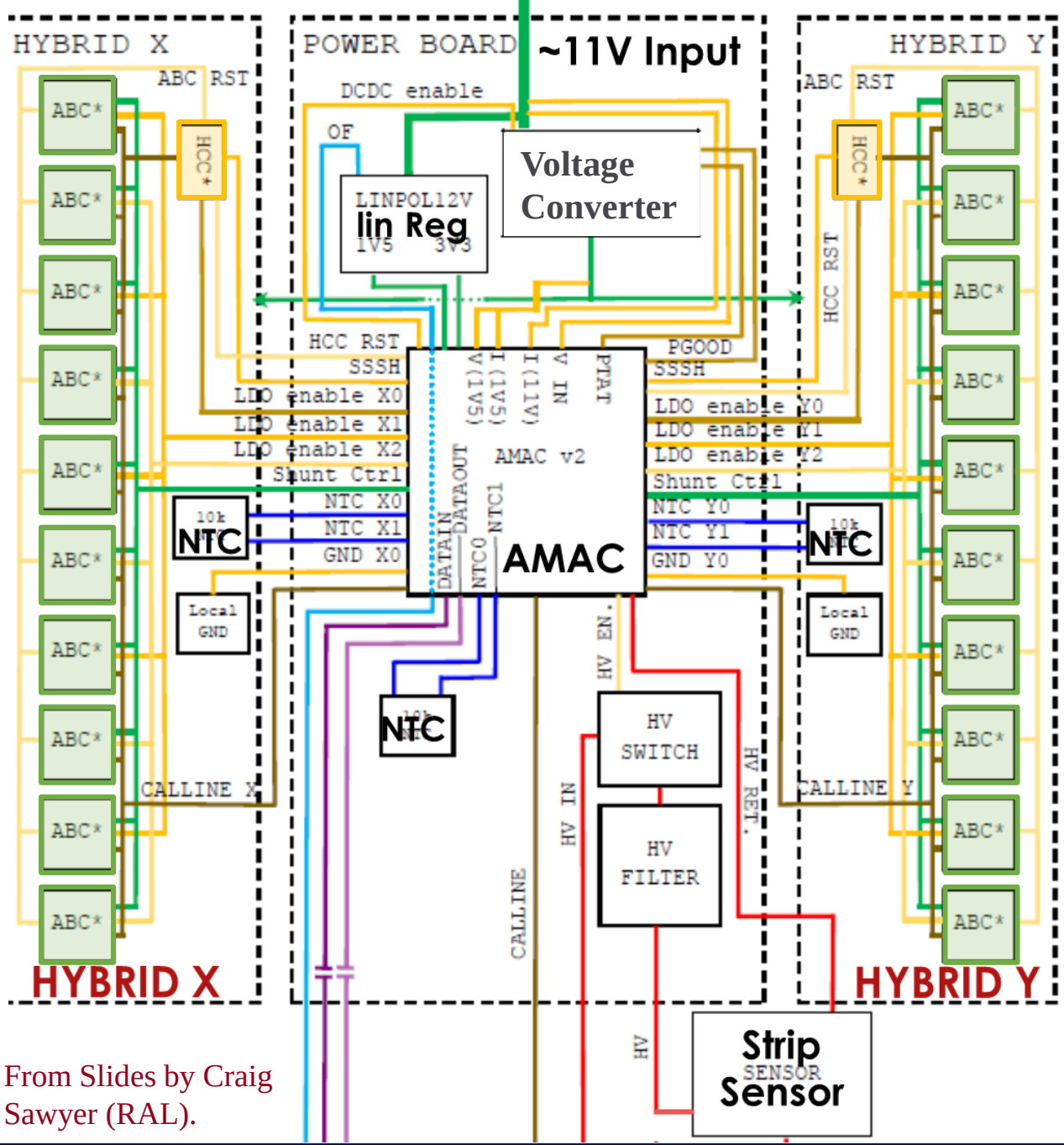

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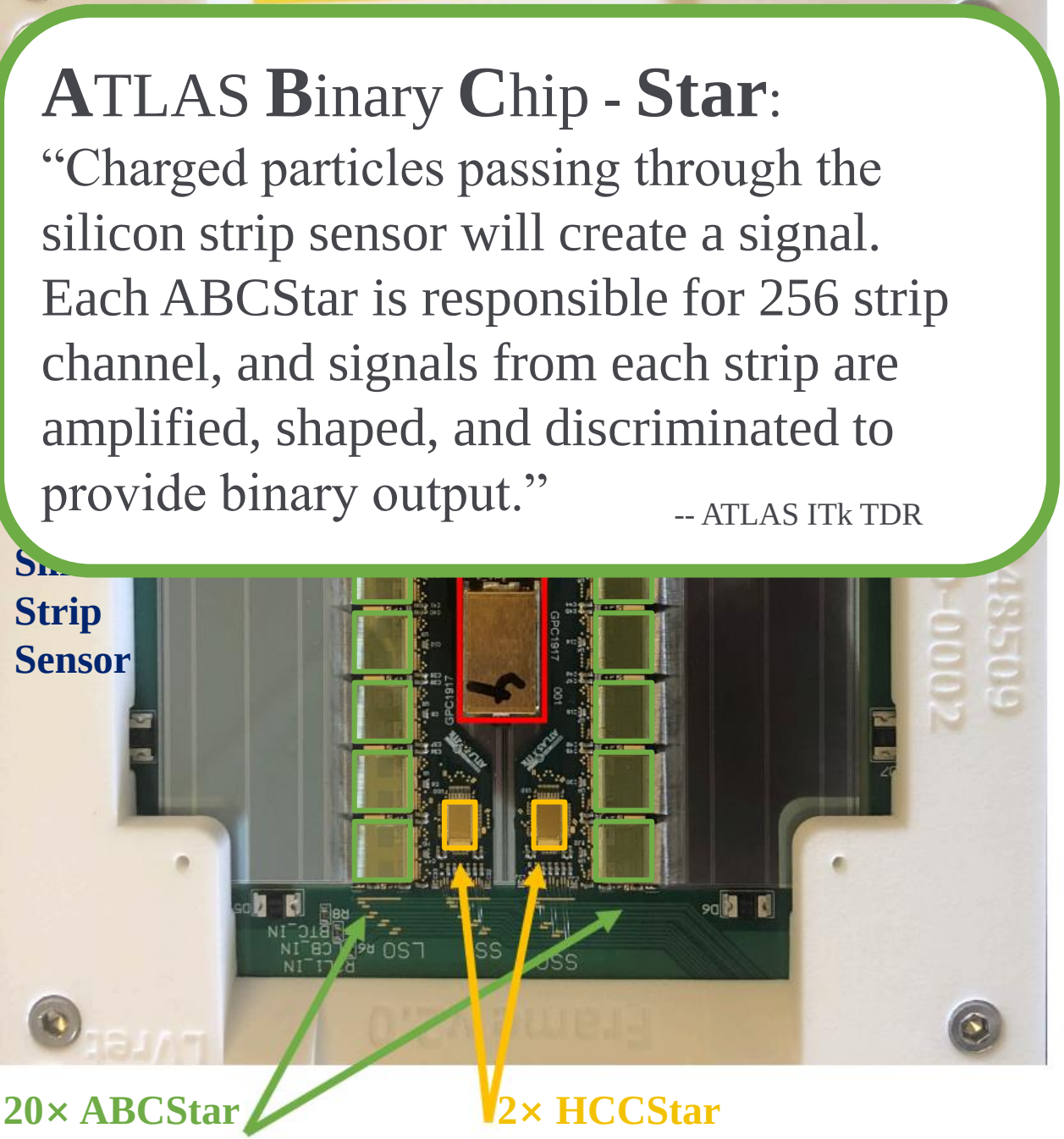

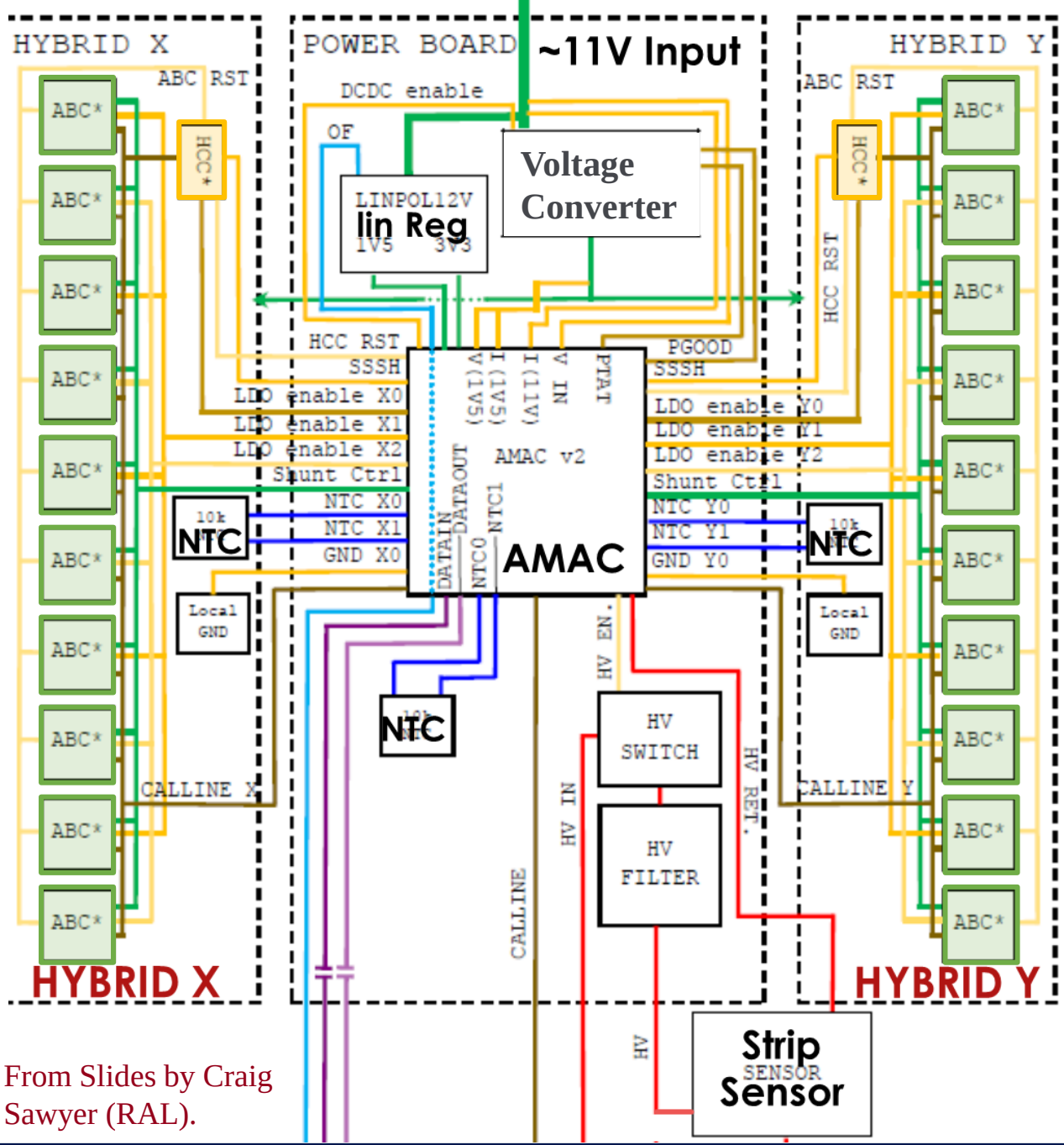

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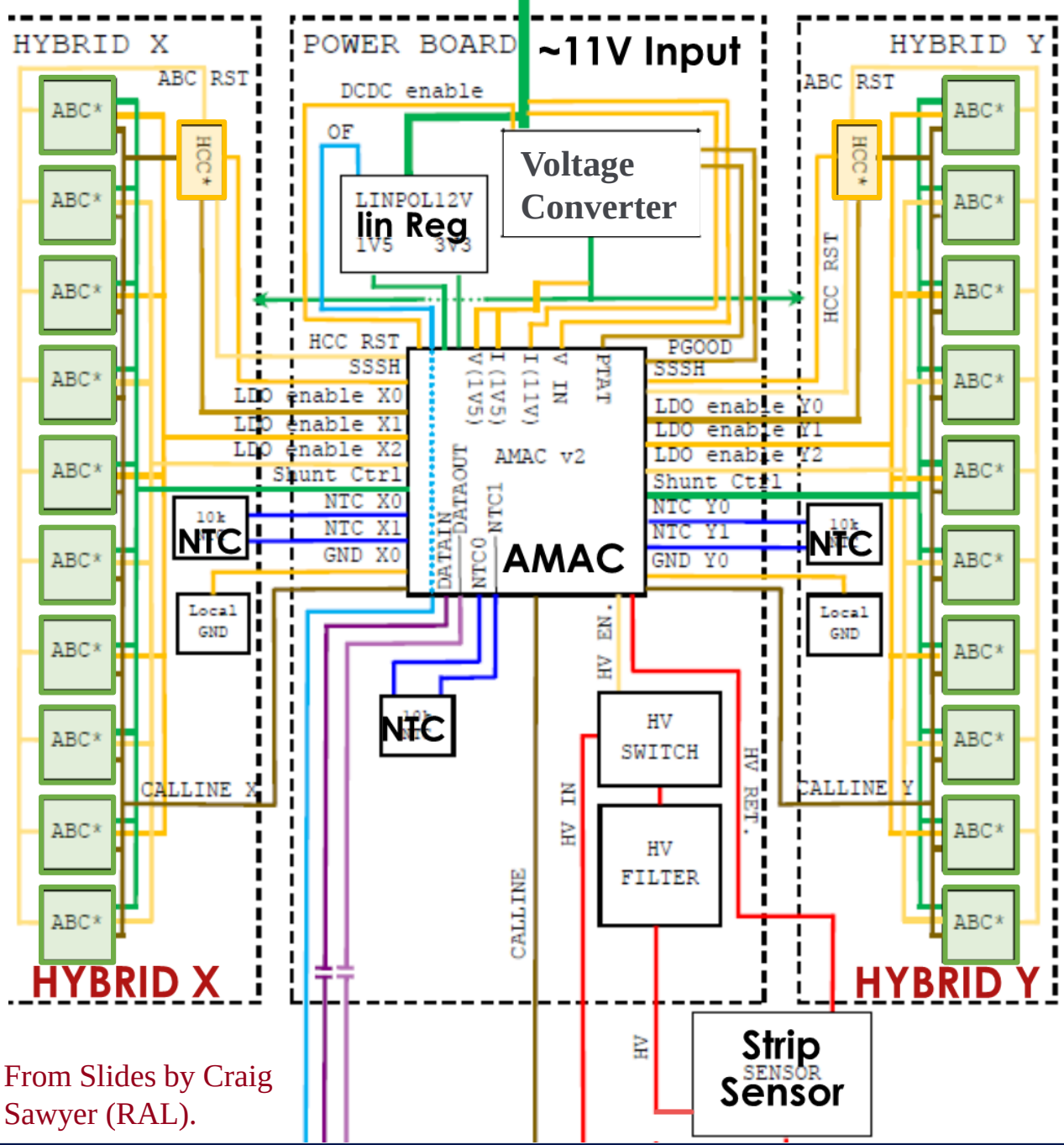
Hybrid Controller Chip - Star:

"Each HCCStar receives the signals from up to 12 ABCStar, builds packets and moves them on.
It also receives the clock and control signals and distributes those to the ABCStar."

20× ABCStar

2× HCCStar



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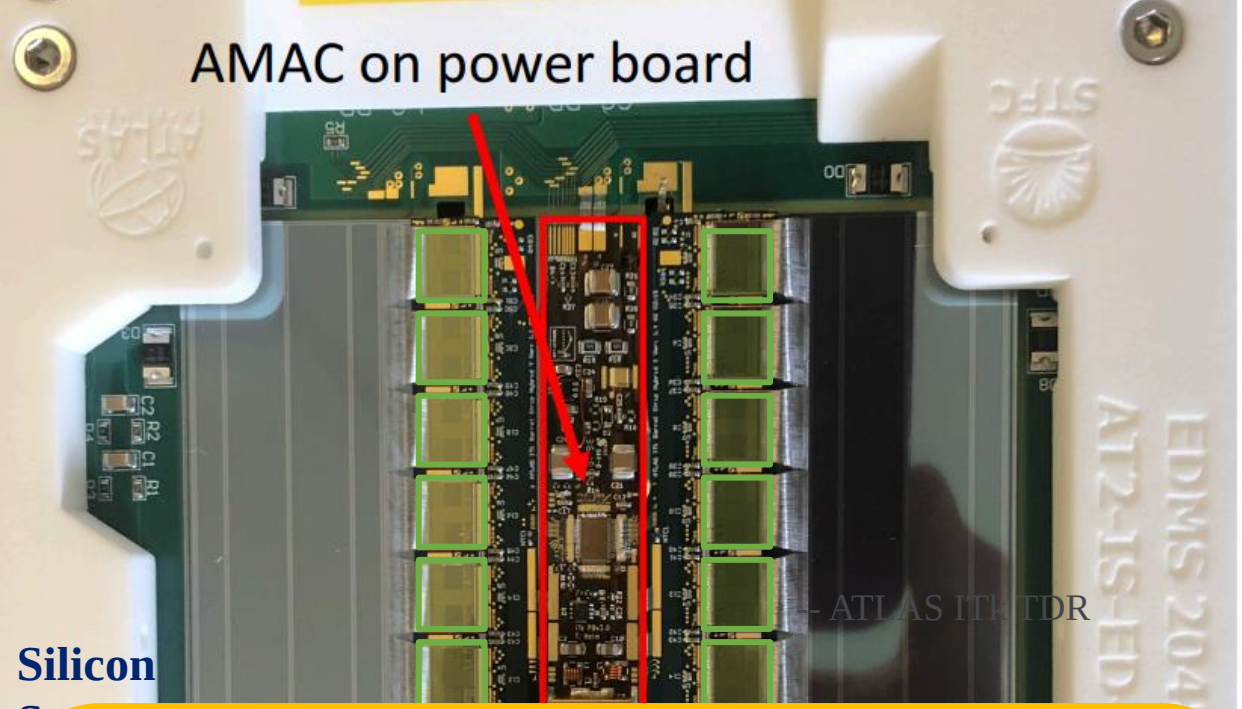

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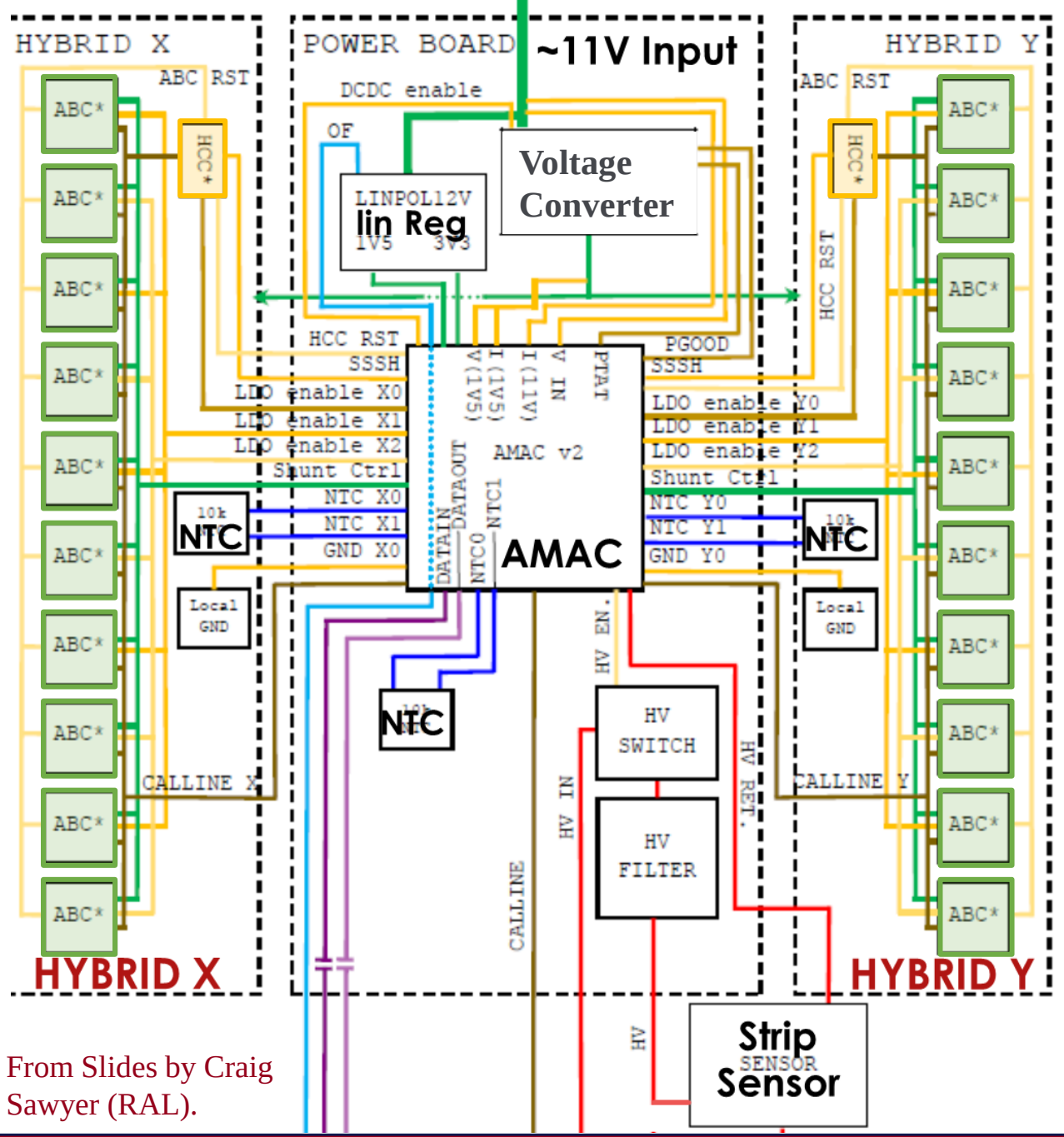

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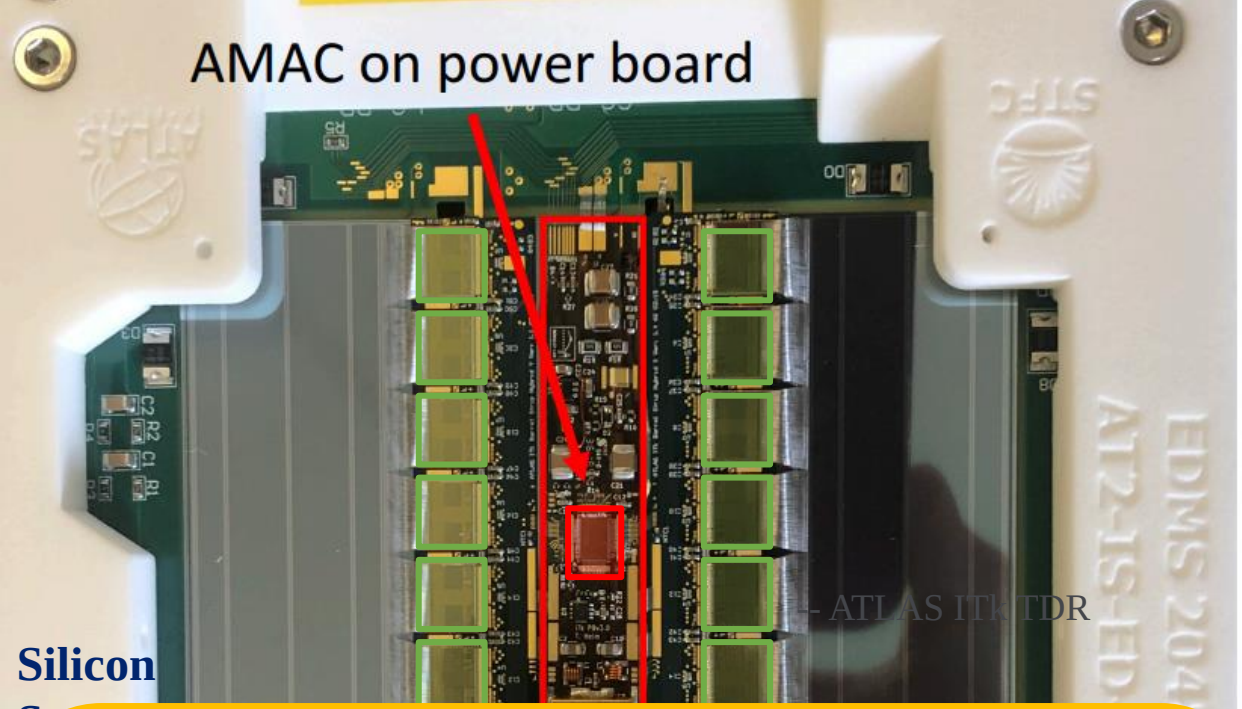

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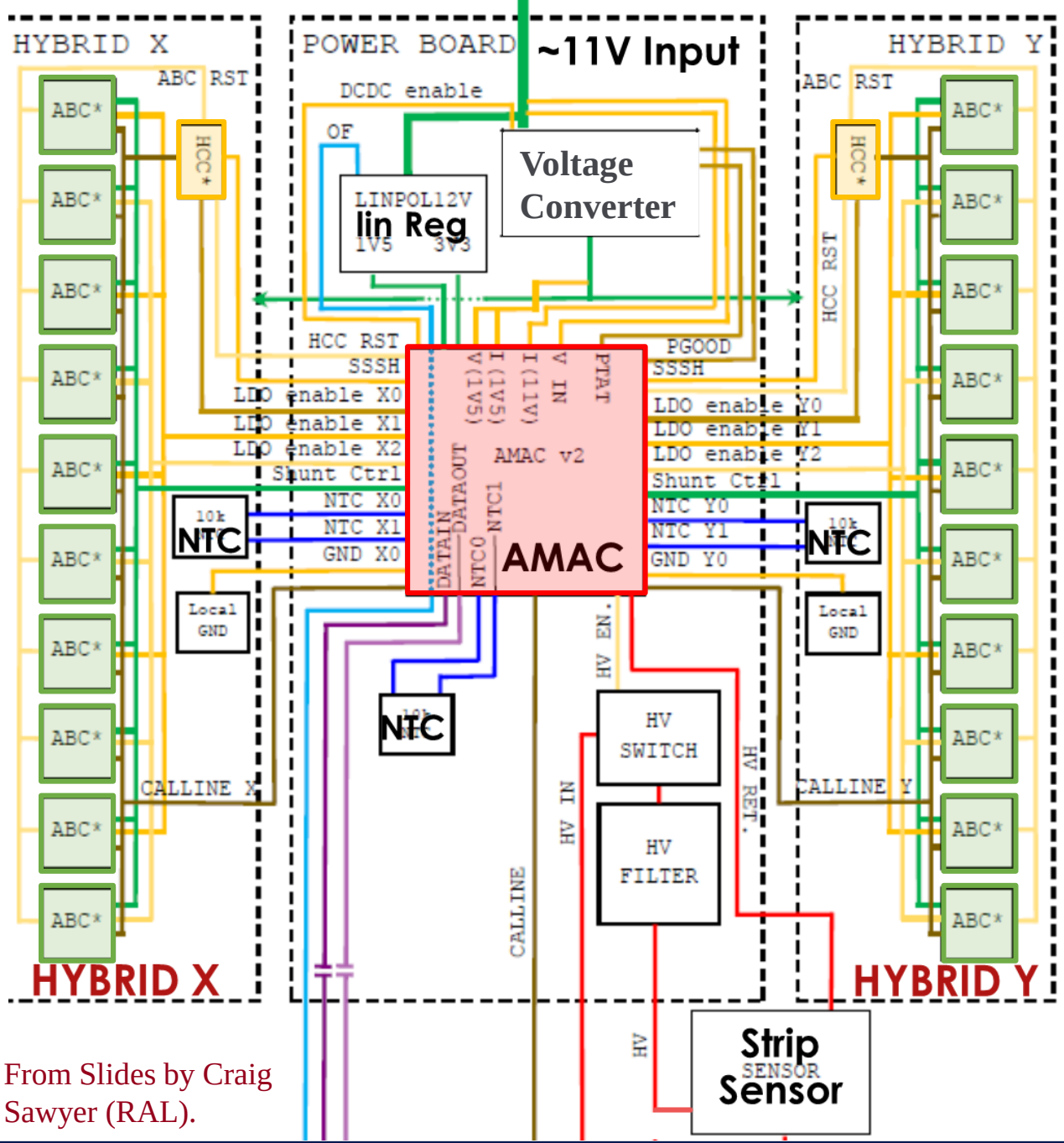

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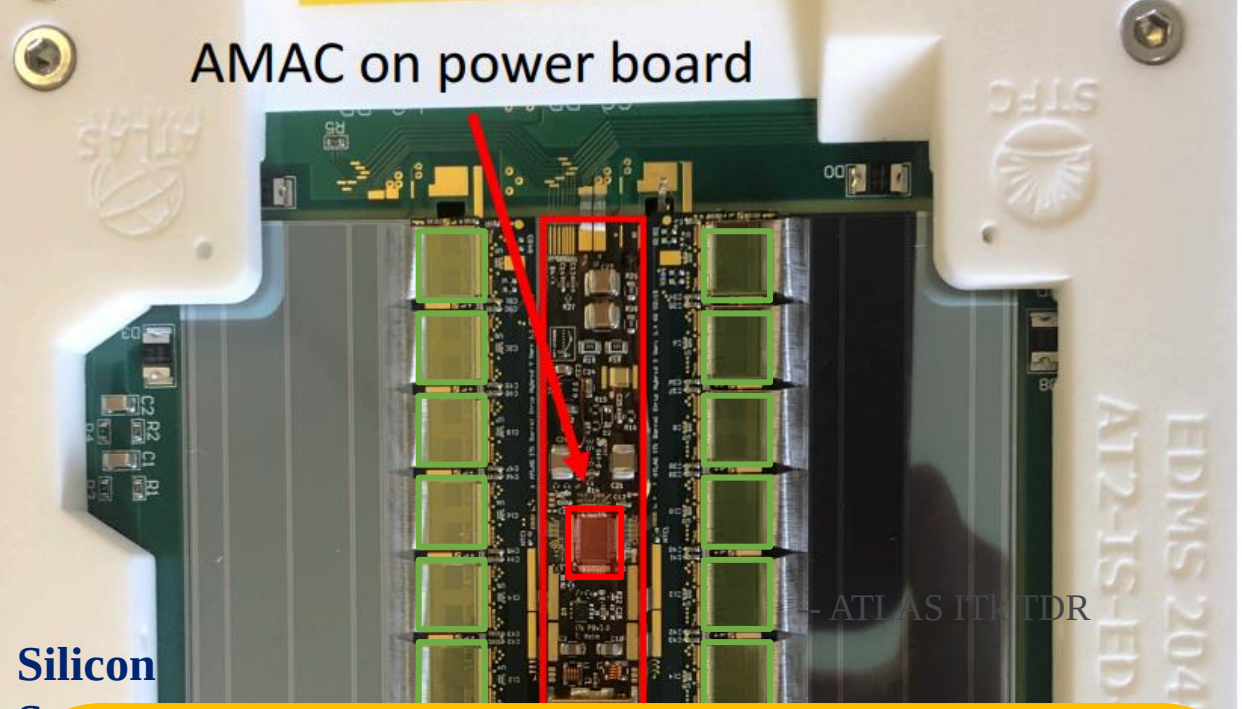

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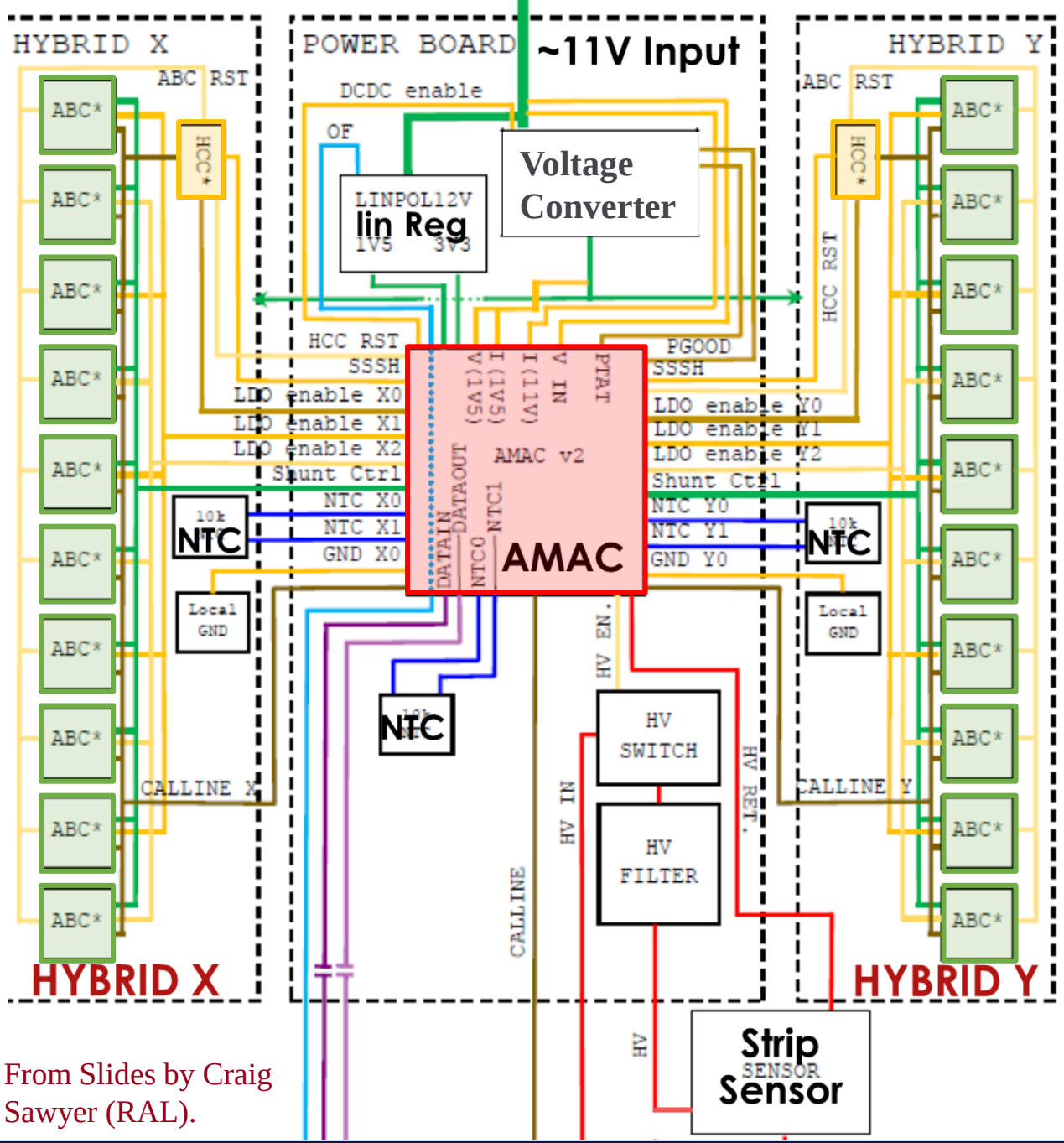

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Autonomous Monitor And Control

Why we need the AMAC & How does it help

- Hazards in detector modules
  - Abnormal Temperature:
    - E.g., local high temperature
    - ⇒ bent/damage sensor
    - ⇒ loss of positioning accuracy
  - Abnormal Current:
    - E.g., individual components short
    - ⇒ takes too much power
    - ⇒ high temperature/insufficient supply
  - Abnormal Voltages:
    - All ASICs and Sensor needs proper voltage to work!
    - Low Voltage ~ 1.5V
    - High Voltage ~ 500V

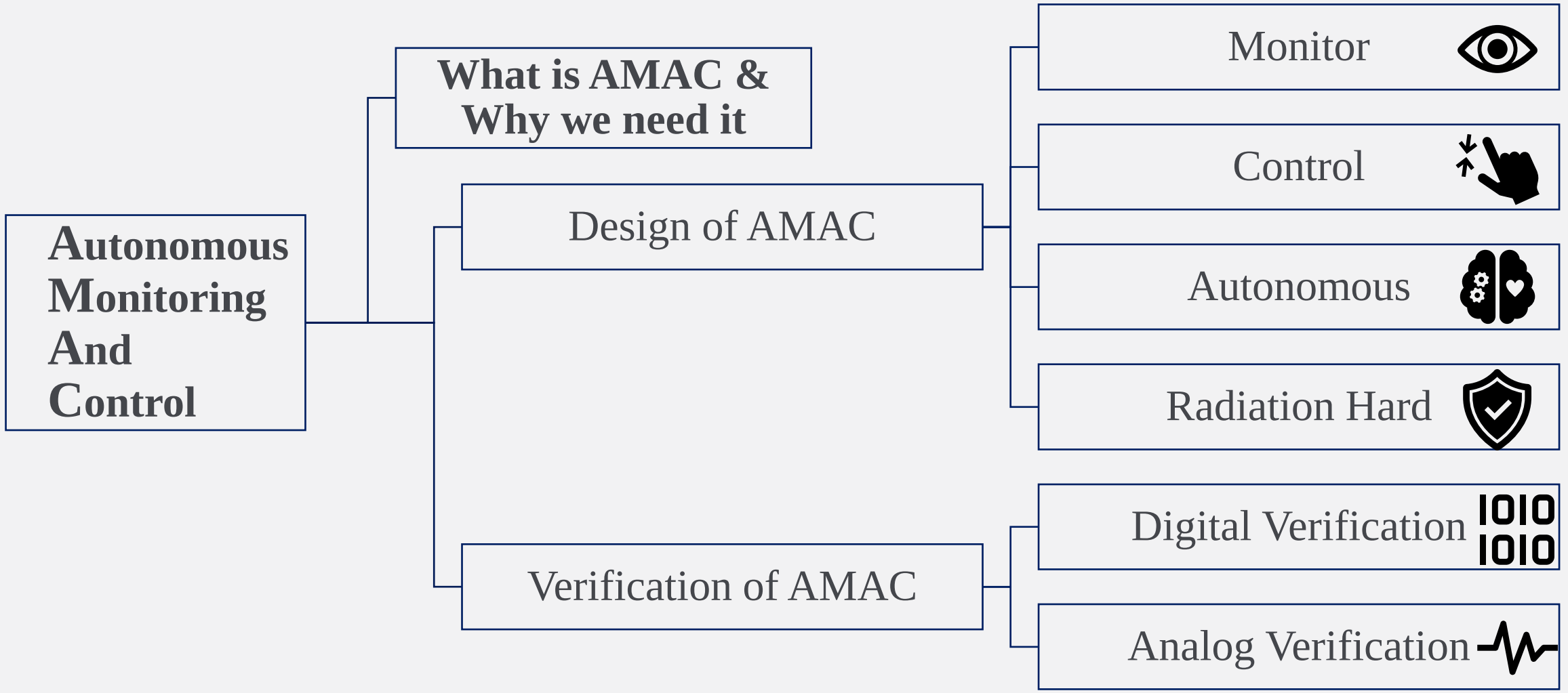
- How does AMAC help?

- **Monitor!**
  - "Spotting" the issues in the first place,
  - With continuous analog monitoring every 0.5 millisecond.

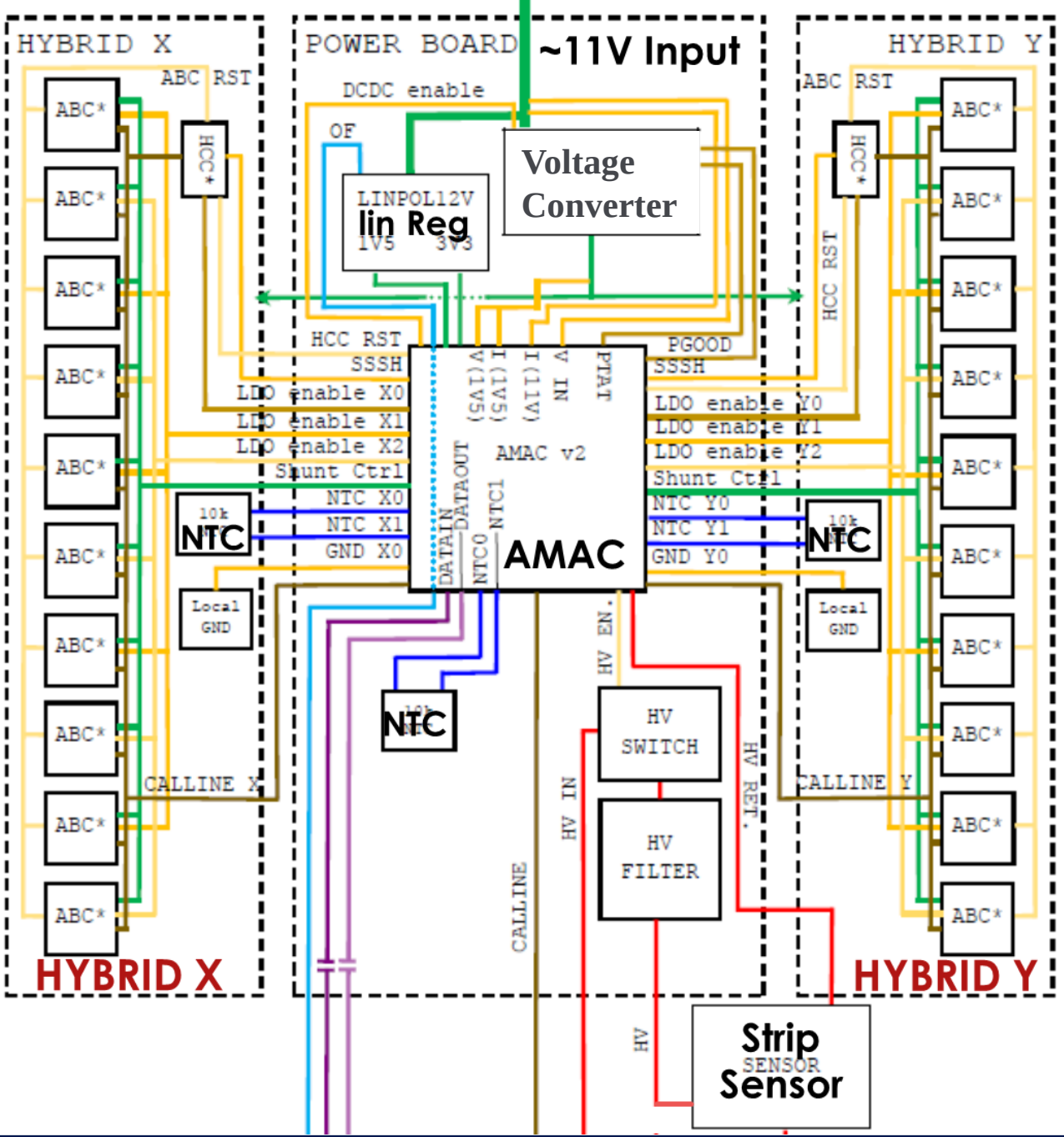
- **Control!**
  - "Handle" the defective components without dismantling the detector,
  - With 5 switches to different components.

- **Autonomous!**
  - Quickly isolate the issue & Stop it from spreading,
  - By autonomous interlock logic channels.

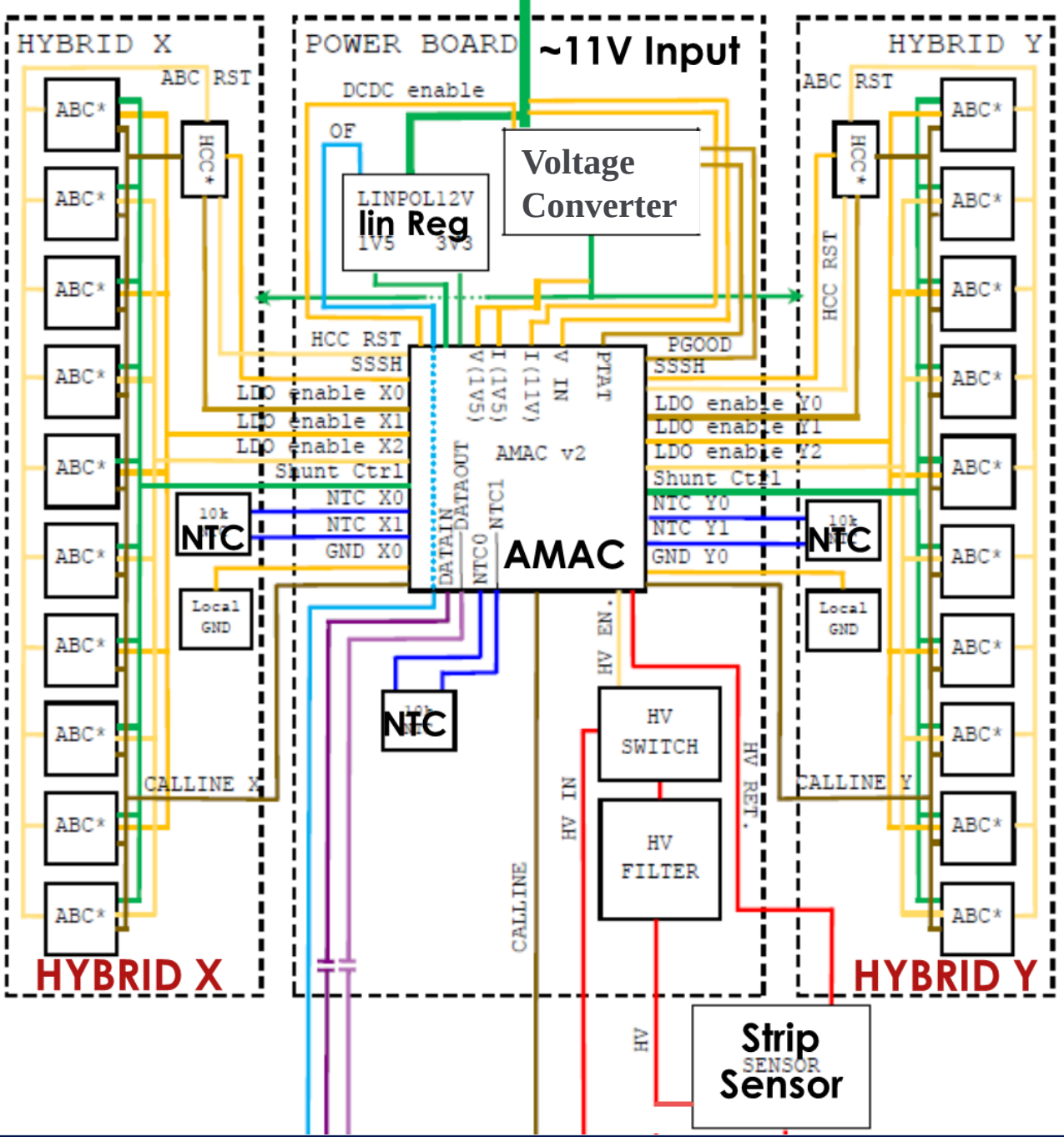
OUTLINE


Autonomous Monitoring And Control
What is AMAC & Why we need it
Design of AMAC
Monitor
Control
Autonomous
Radiation Hard
Verification of AMAC
Digital Verification
1010
1010
Analog Verification

Analog Monitoring



Analog Monitoring

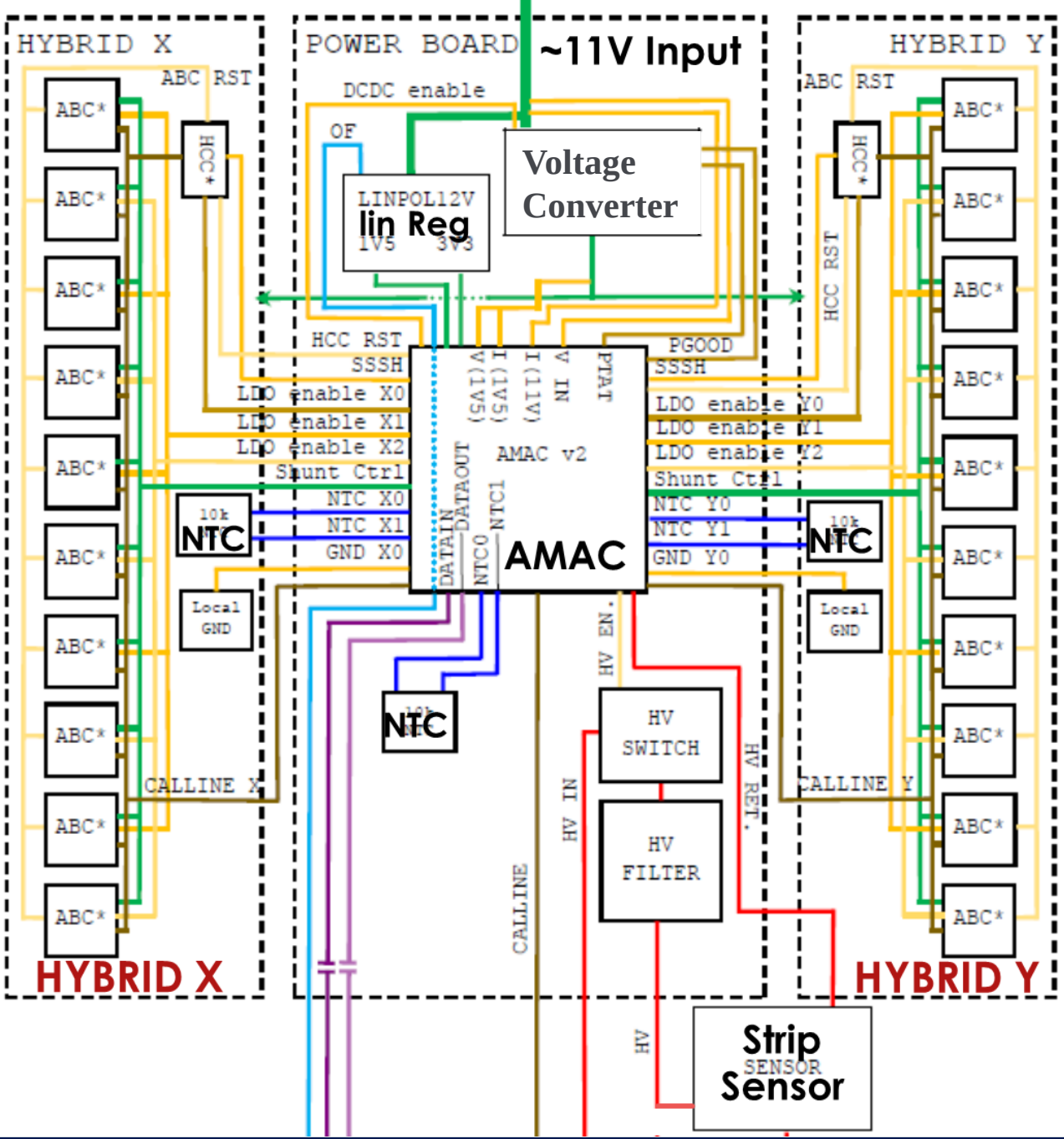


Temperature

Current

Voltage

Analog Monitoring



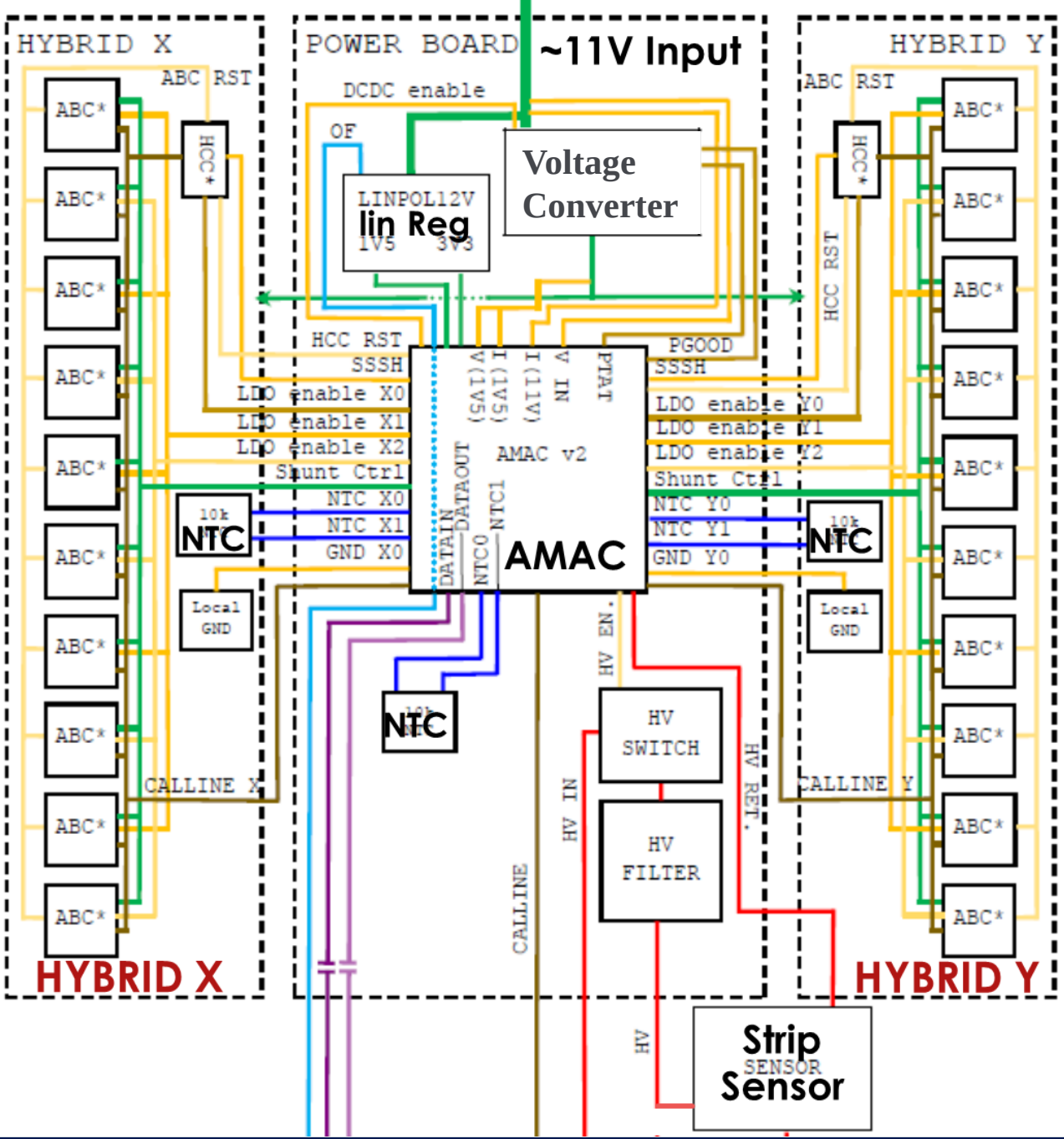
Temperature

Current

Voltage

Analog to Digital Converter
(16 Multiplexer Channel)

Analog Monitoring



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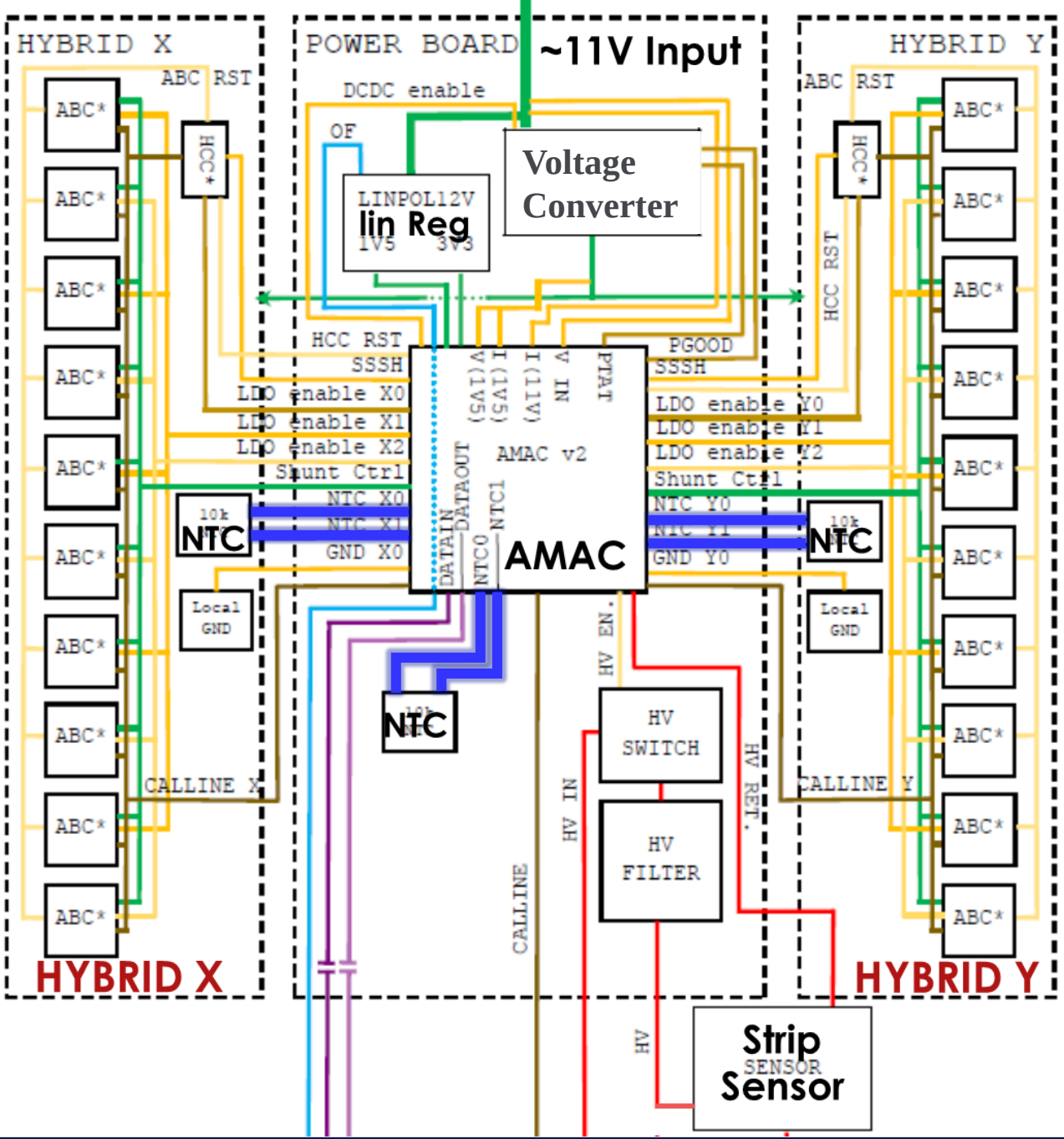

Temperature

Hybrid X/Y Temperature
& **Power Board** Temperature

Current

Voltage

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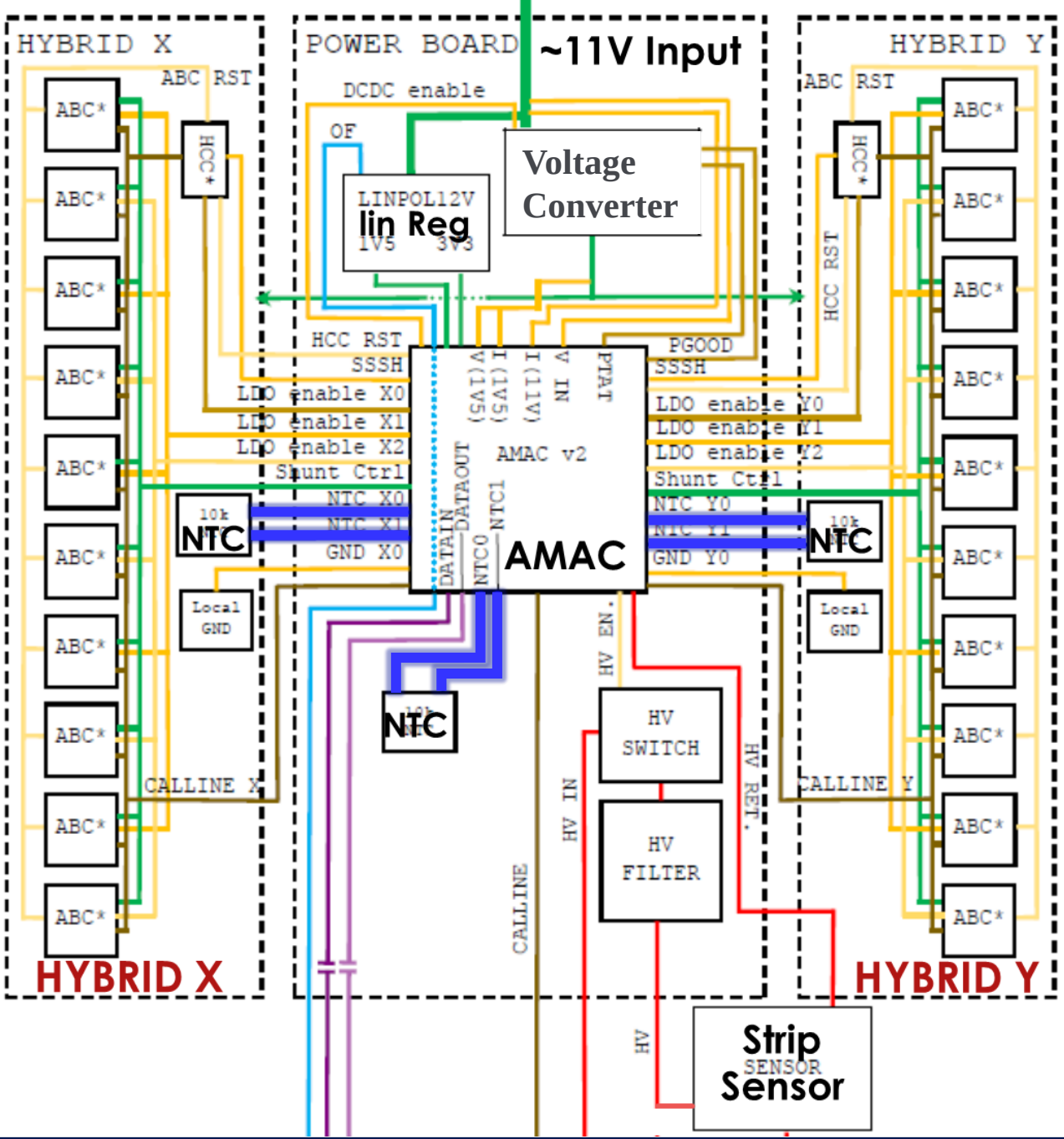
Analog Monitoring



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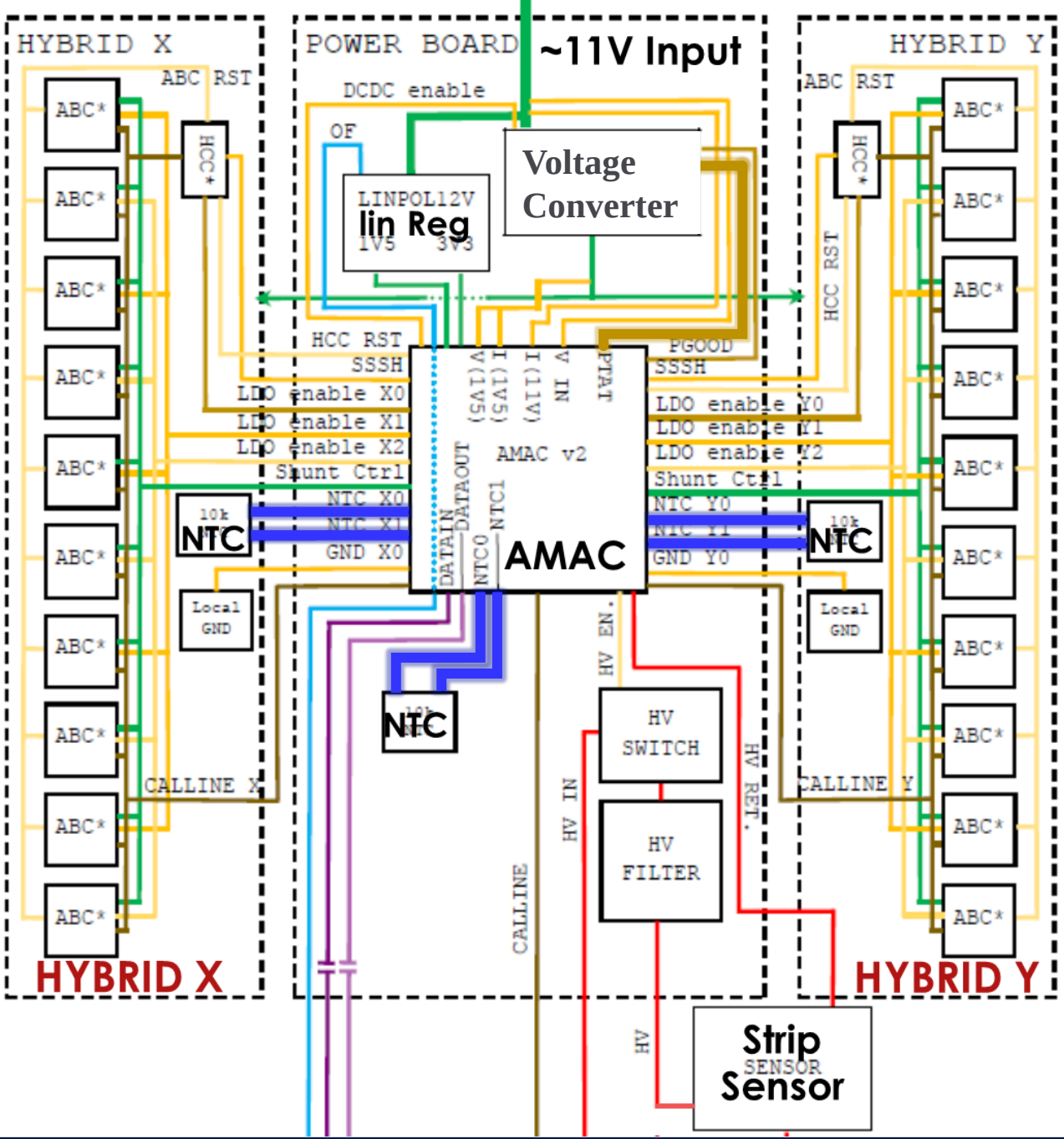

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Power Supply Temperature

Current

Voltage

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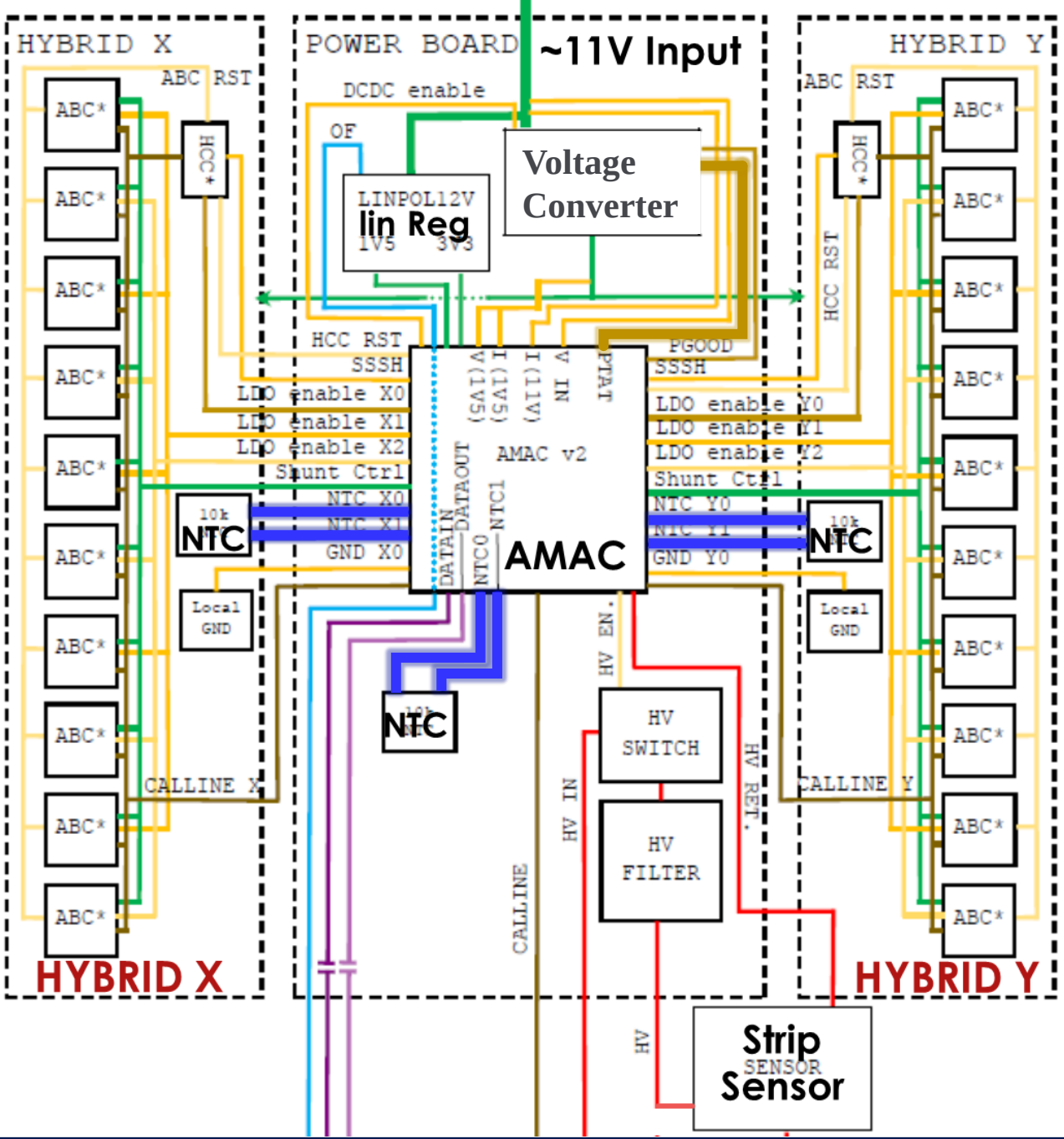

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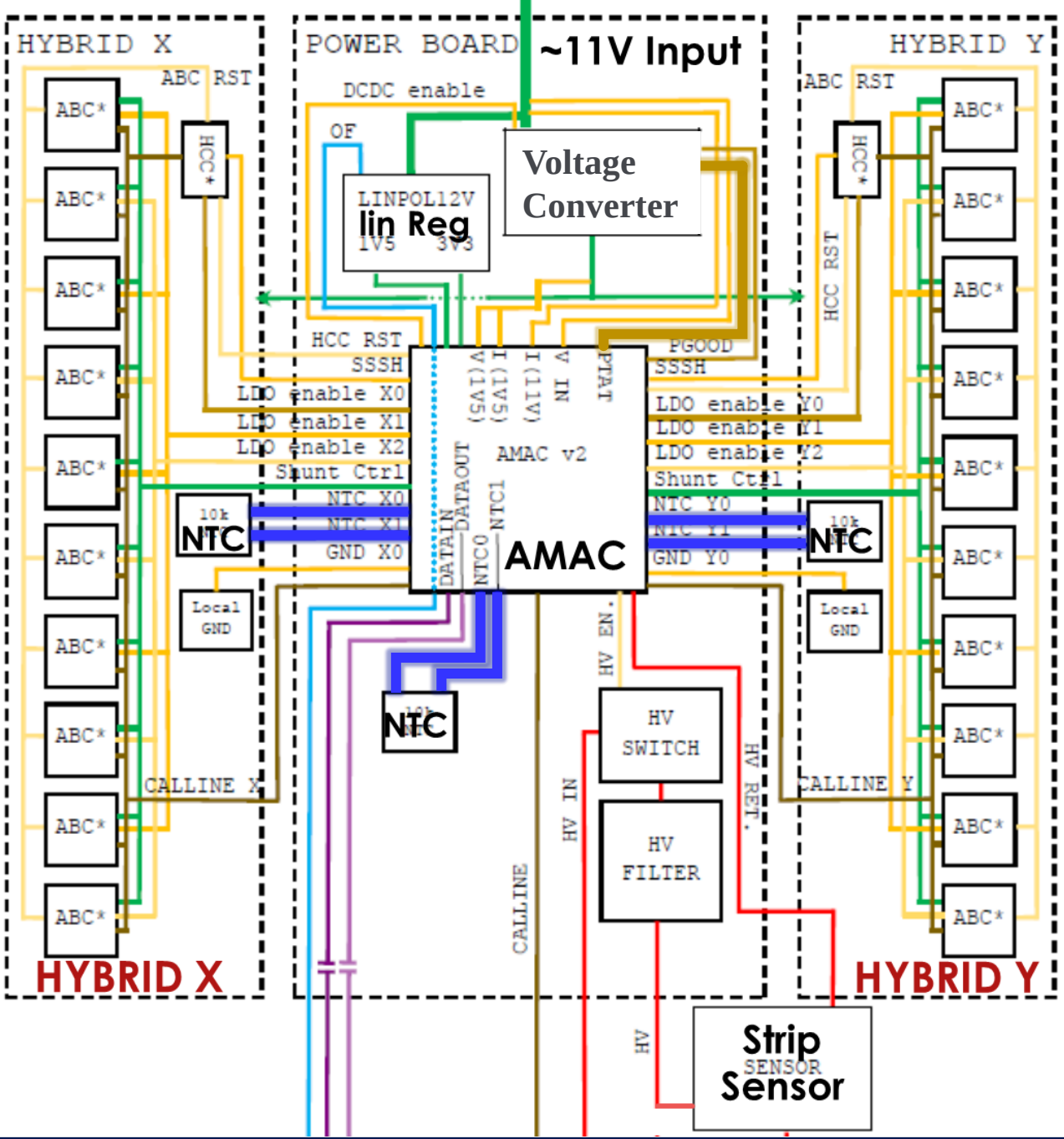

Temperature

- **Hybrid X/Y** Temperature & **Power Board** Temperature
- **Power Supply** Temperature
- **AMAC** Internal Temperature

Current

Voltage

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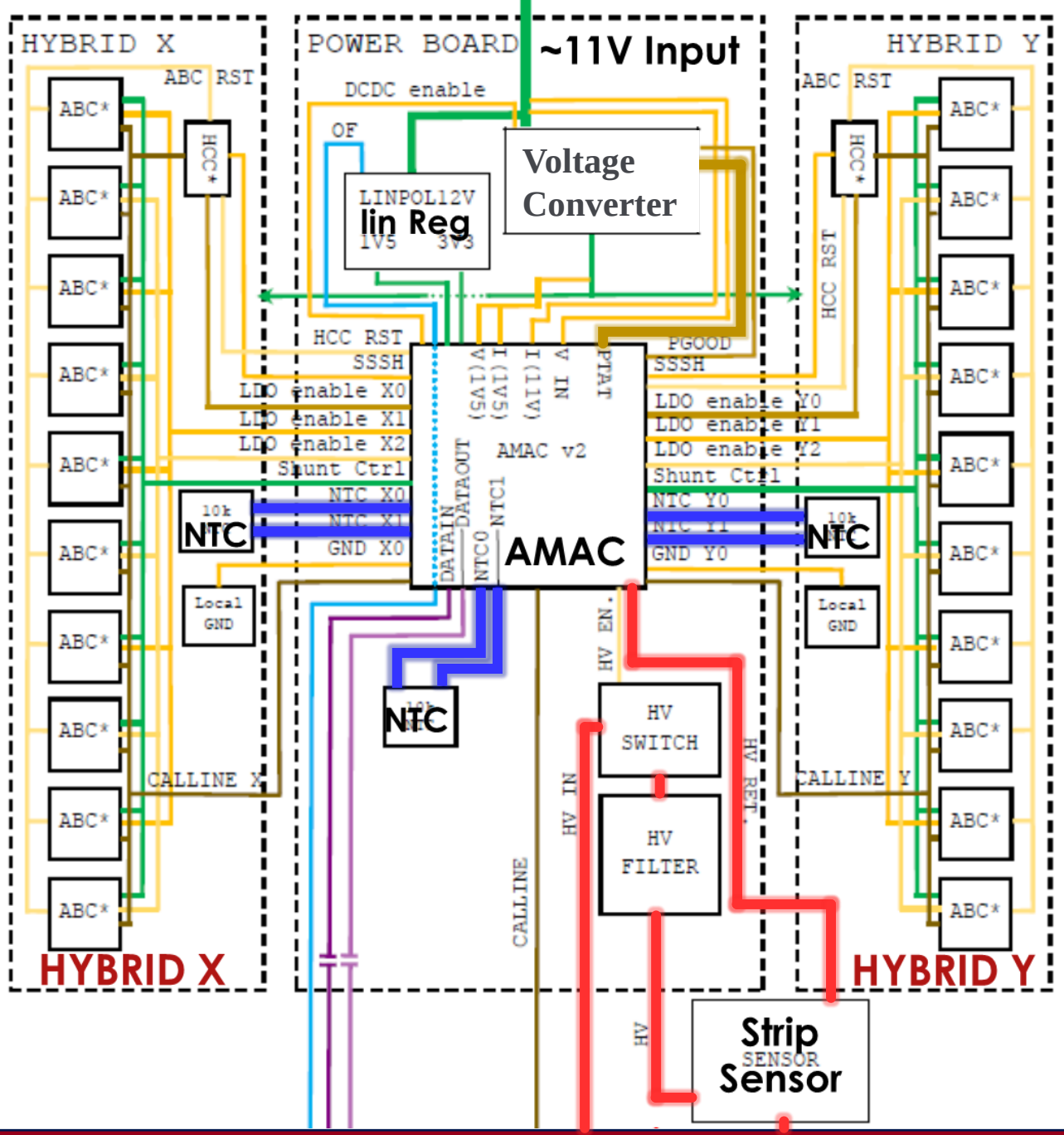
Analog Monitoring



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Current

- **Silicon Sensor** Bias Current (High Voltage Return)

Voltage

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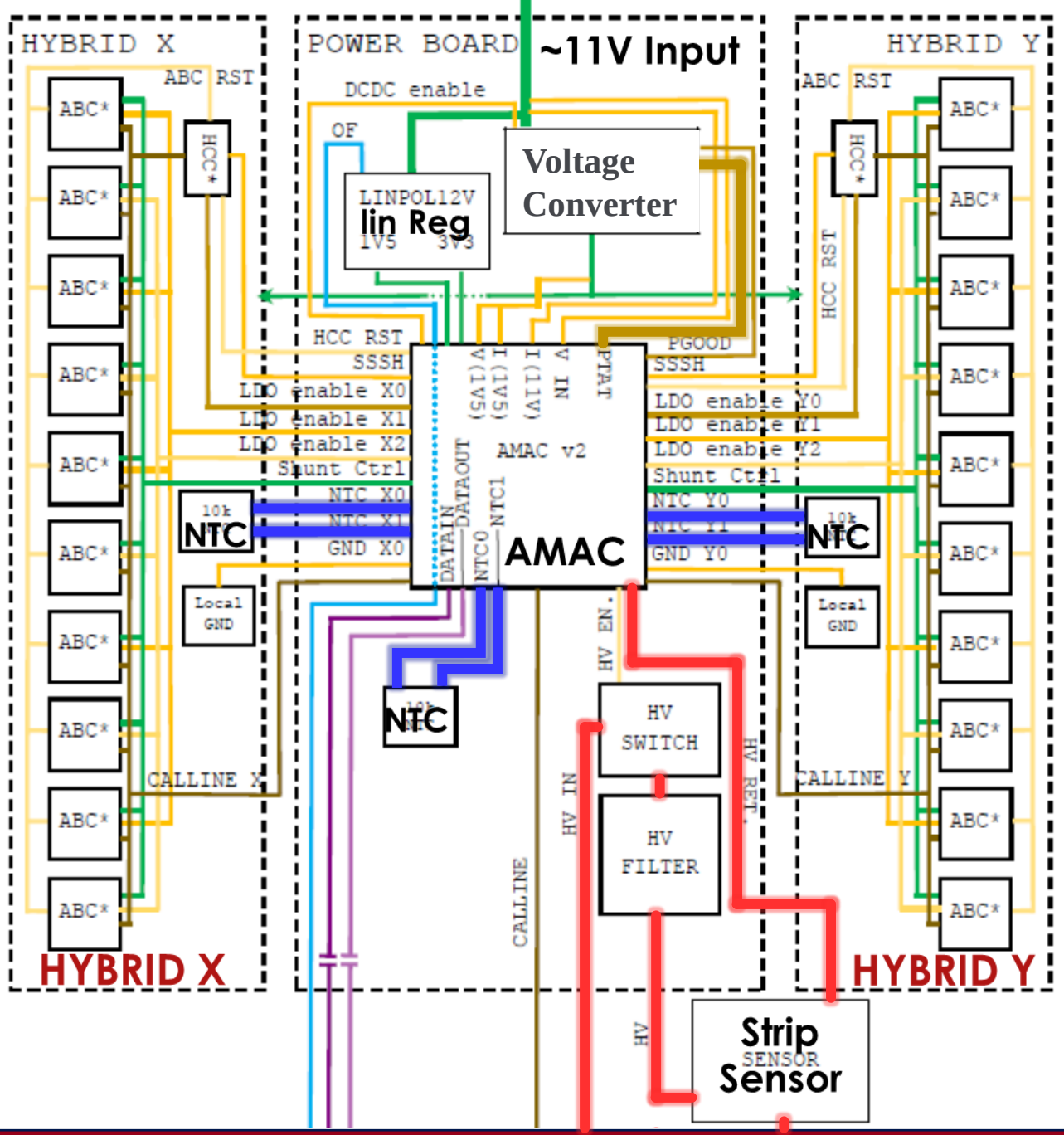

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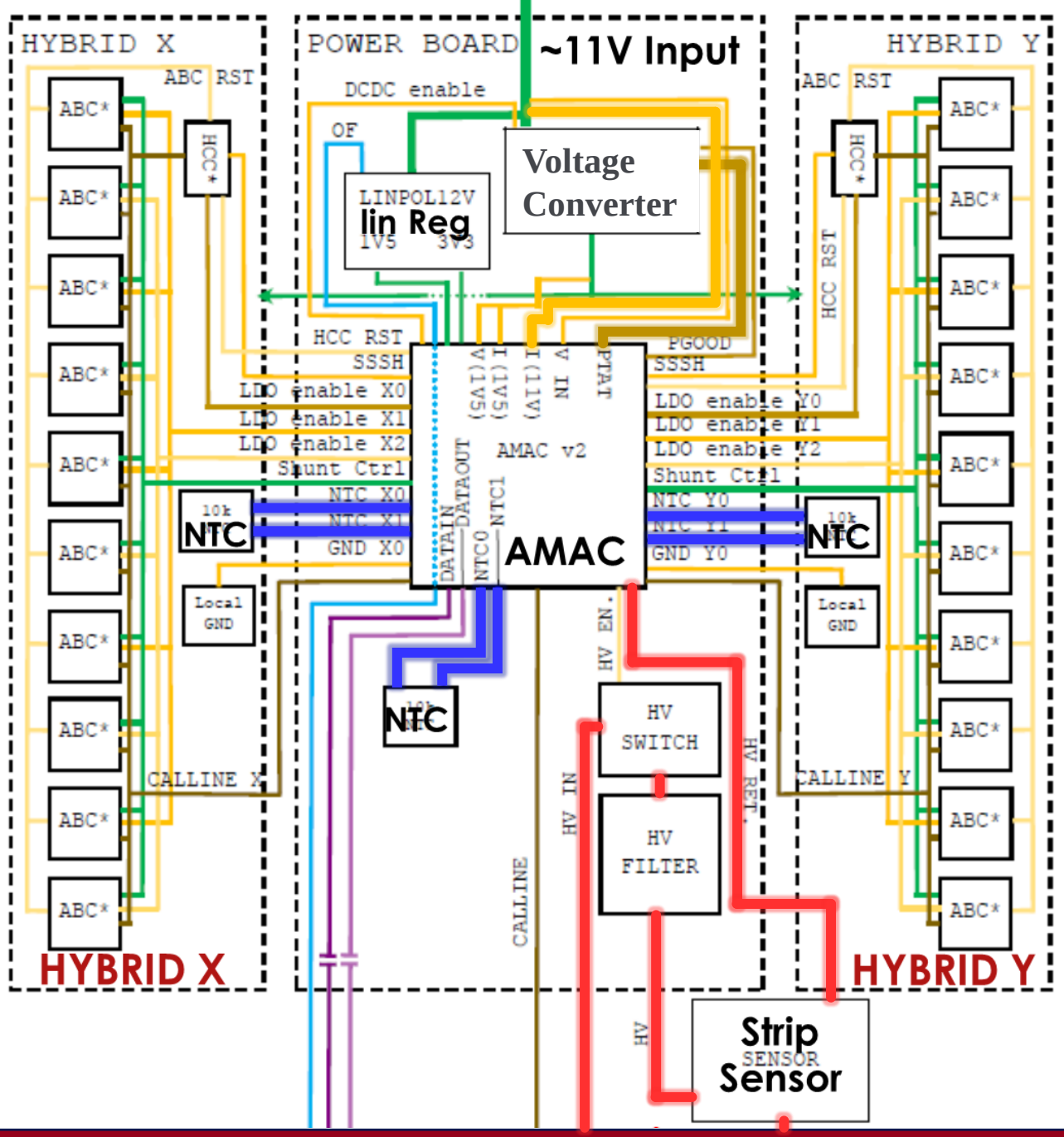

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Current

- **Silicon Sensor** Bias Current (High Voltage Return)
- **Voltage Converter** Input

Voltage

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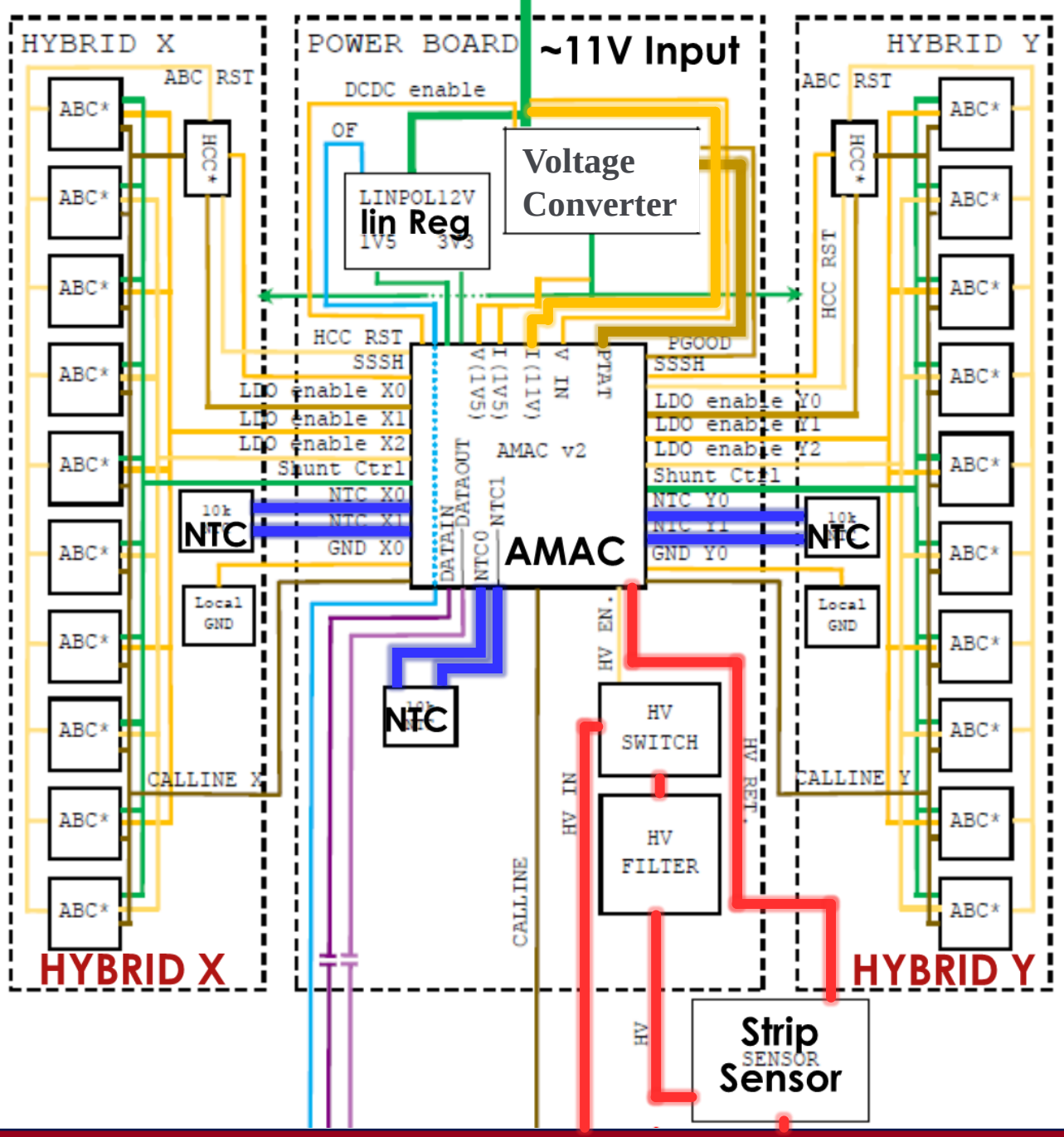

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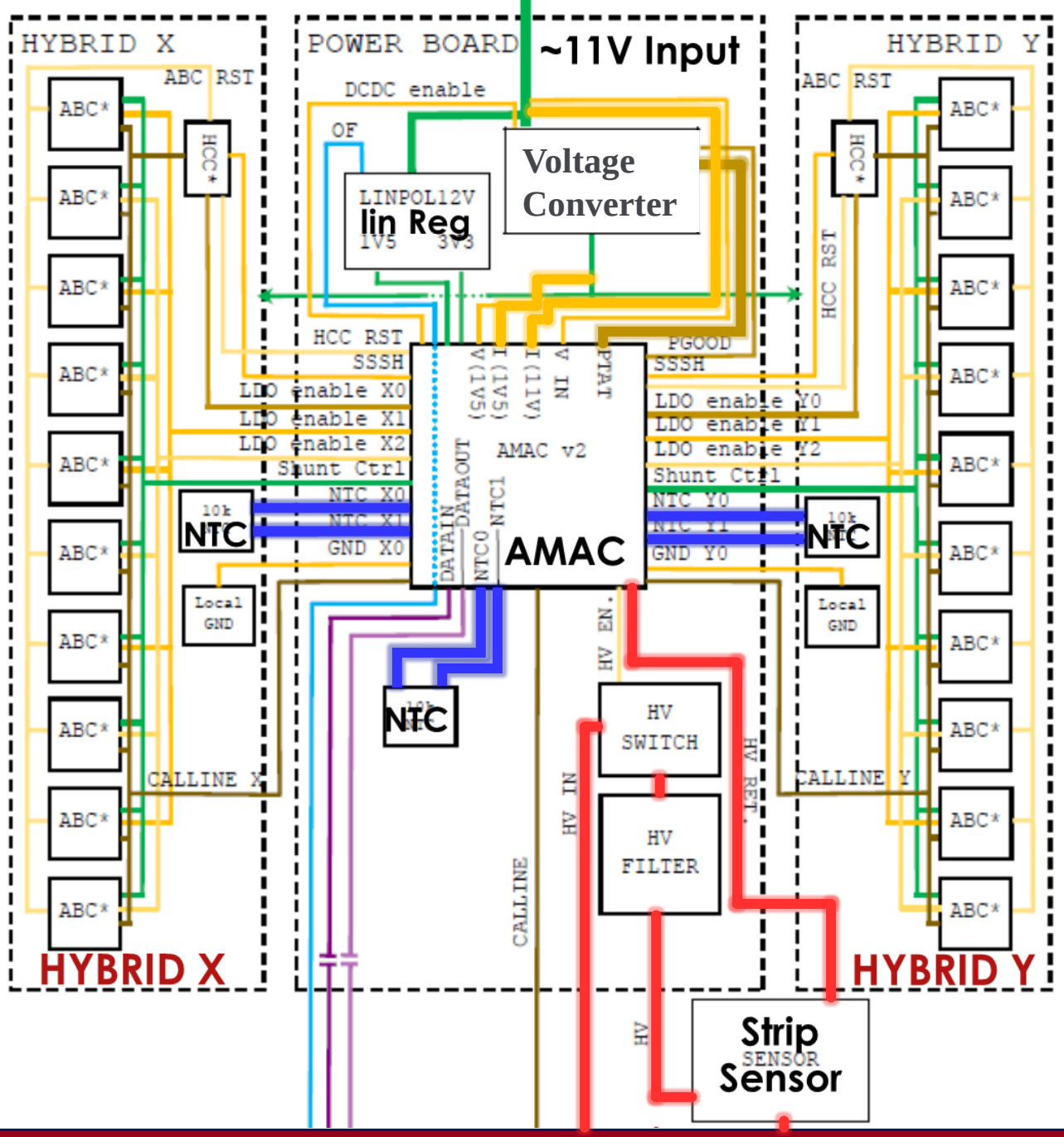

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- **Voltage Converter** Output

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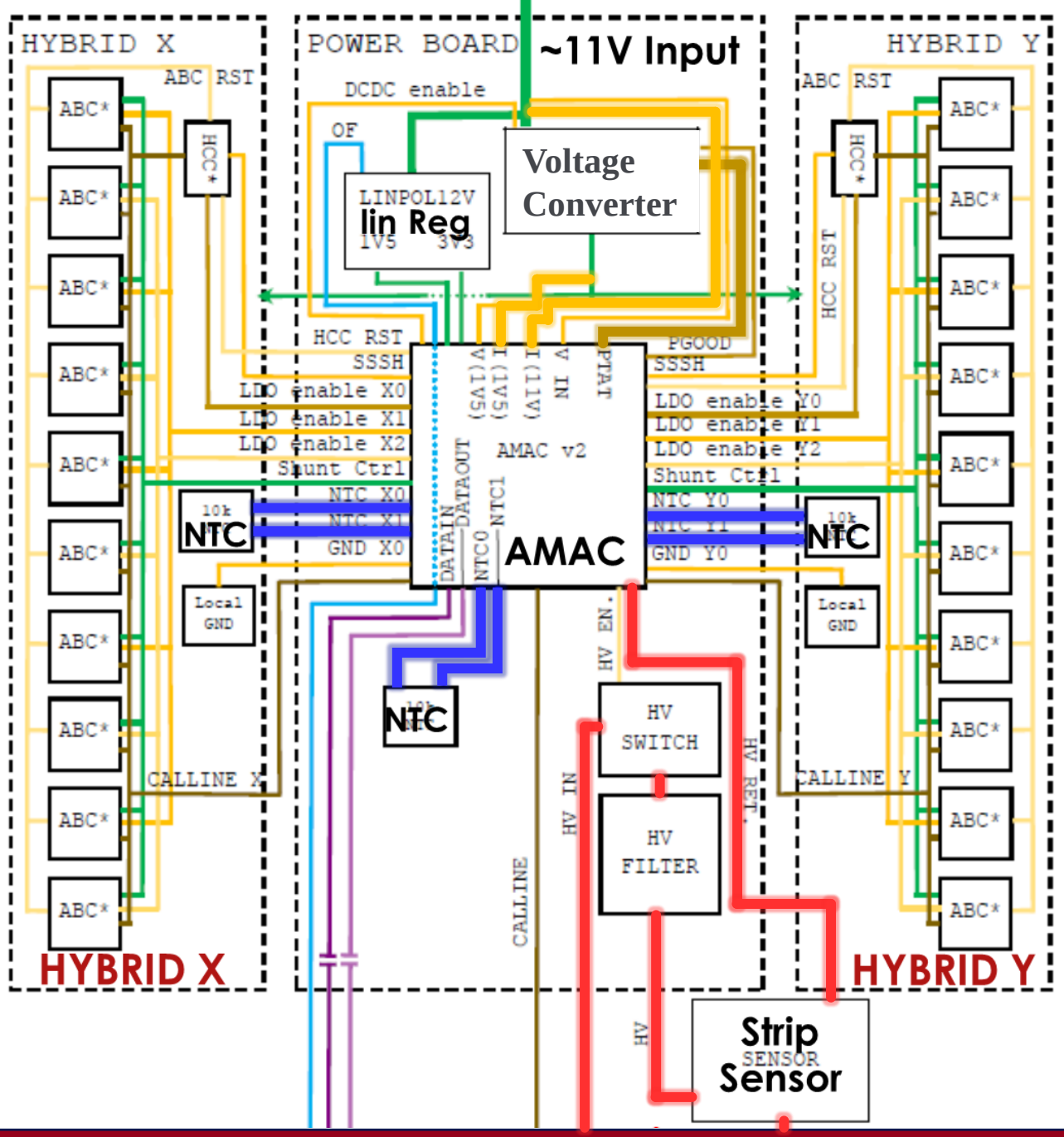

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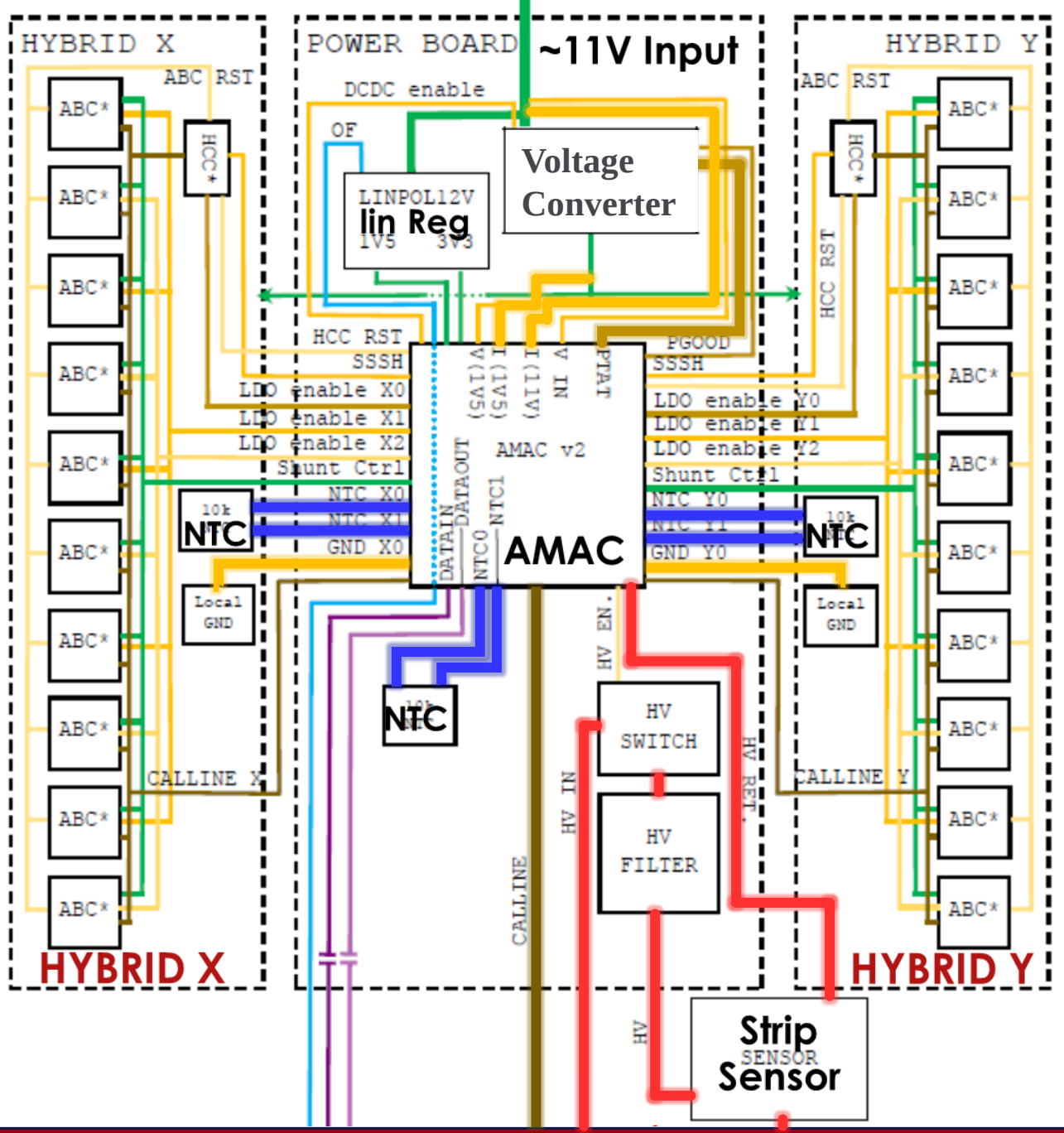


Analog Monitoring

Temperature

- **Hybrid X/Y** Temperature & **Power Board** Temperature
- **Power Supply** Temperature
- **AMAC** Internal Temperature

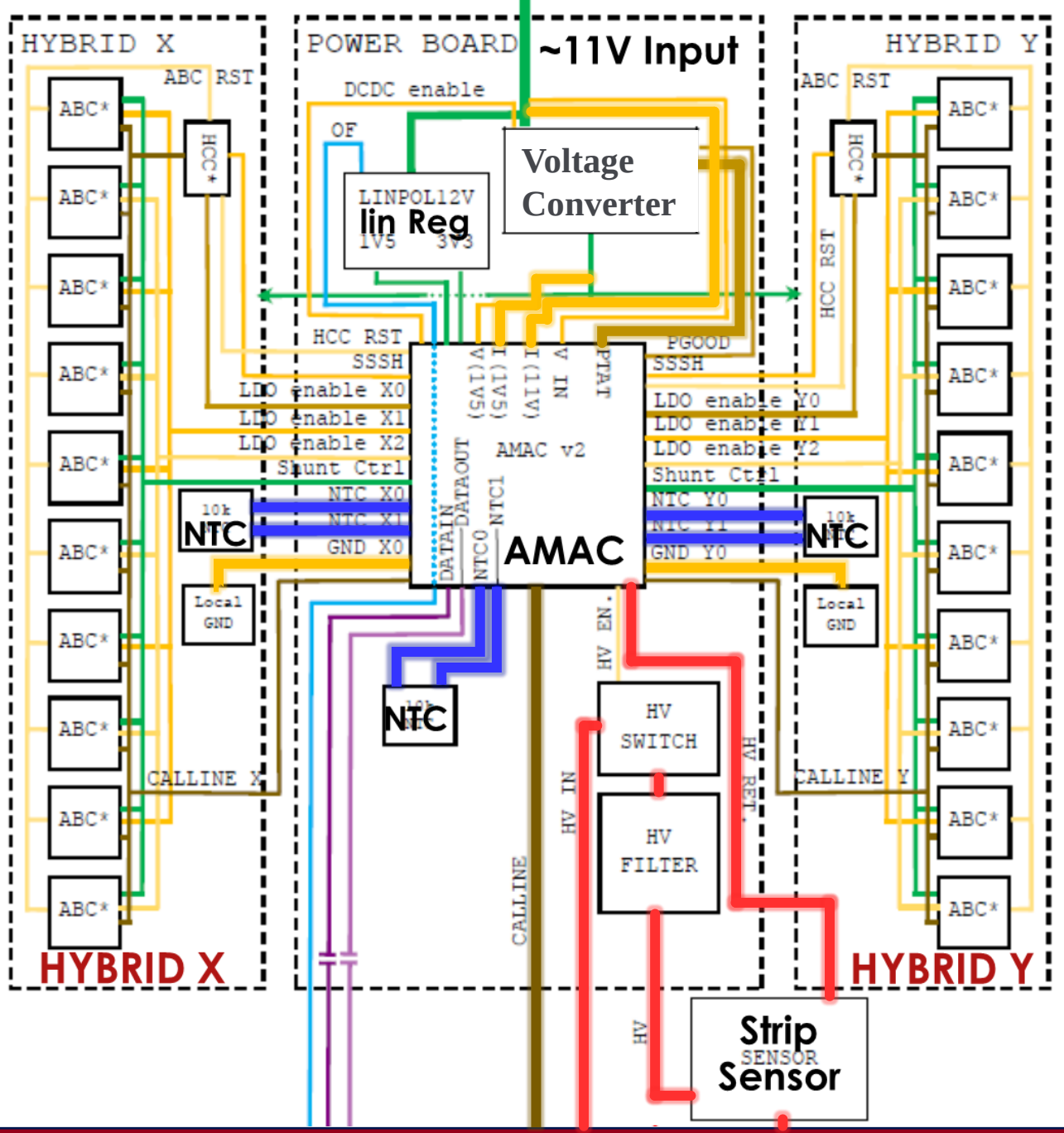
Current

- **Silicon Sensor** Bias Current (High Voltage Return)
- **Voltage Converter** Input
- **Voltage Converter** Output

Voltage

- Ground Voltage Calibration (**Hybrid X/Y** & **End-of-Stave**)

Analog to Digital Converter
(16 Multiplexer Channel)



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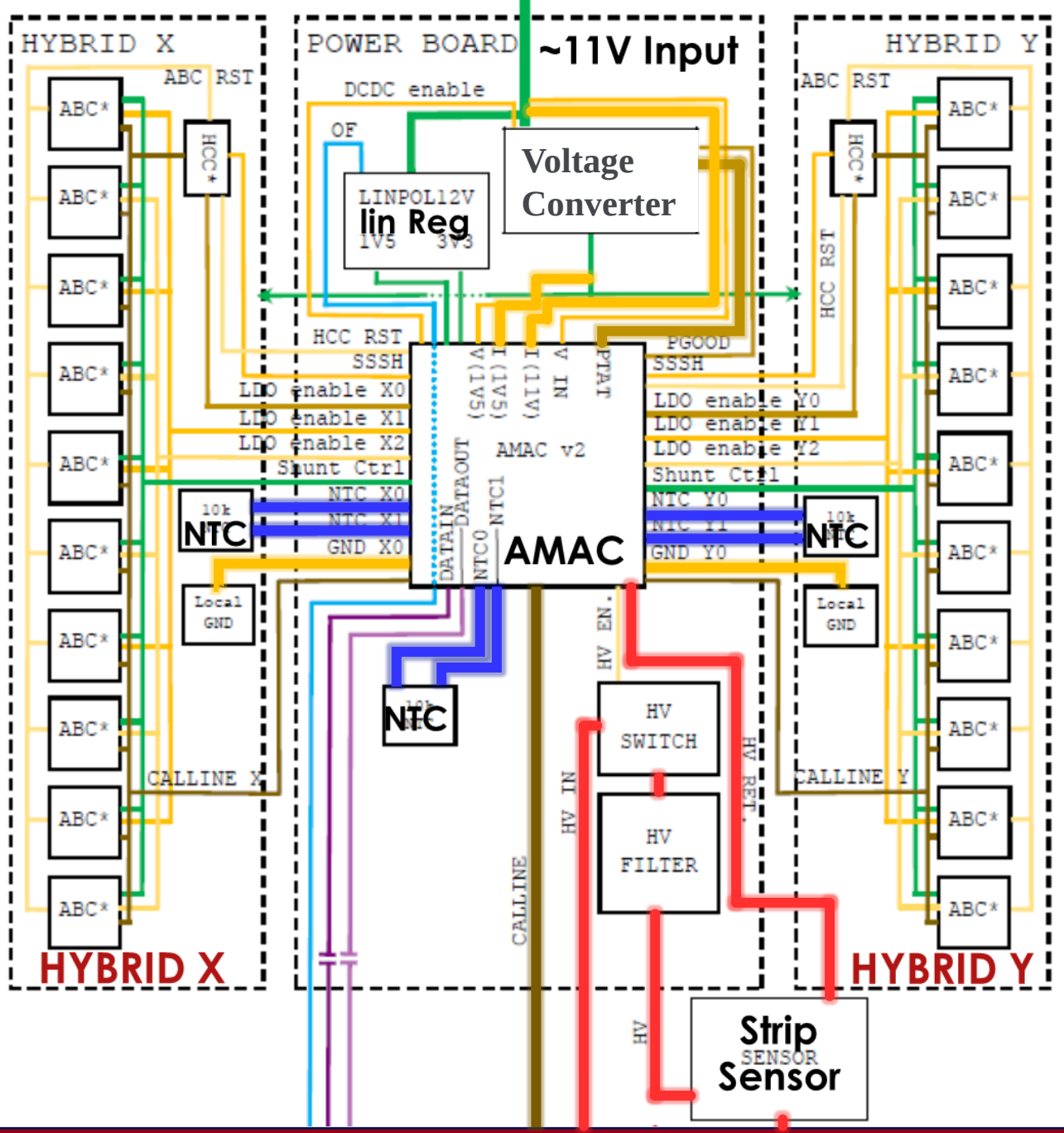
(16 Multiplexer Channel)



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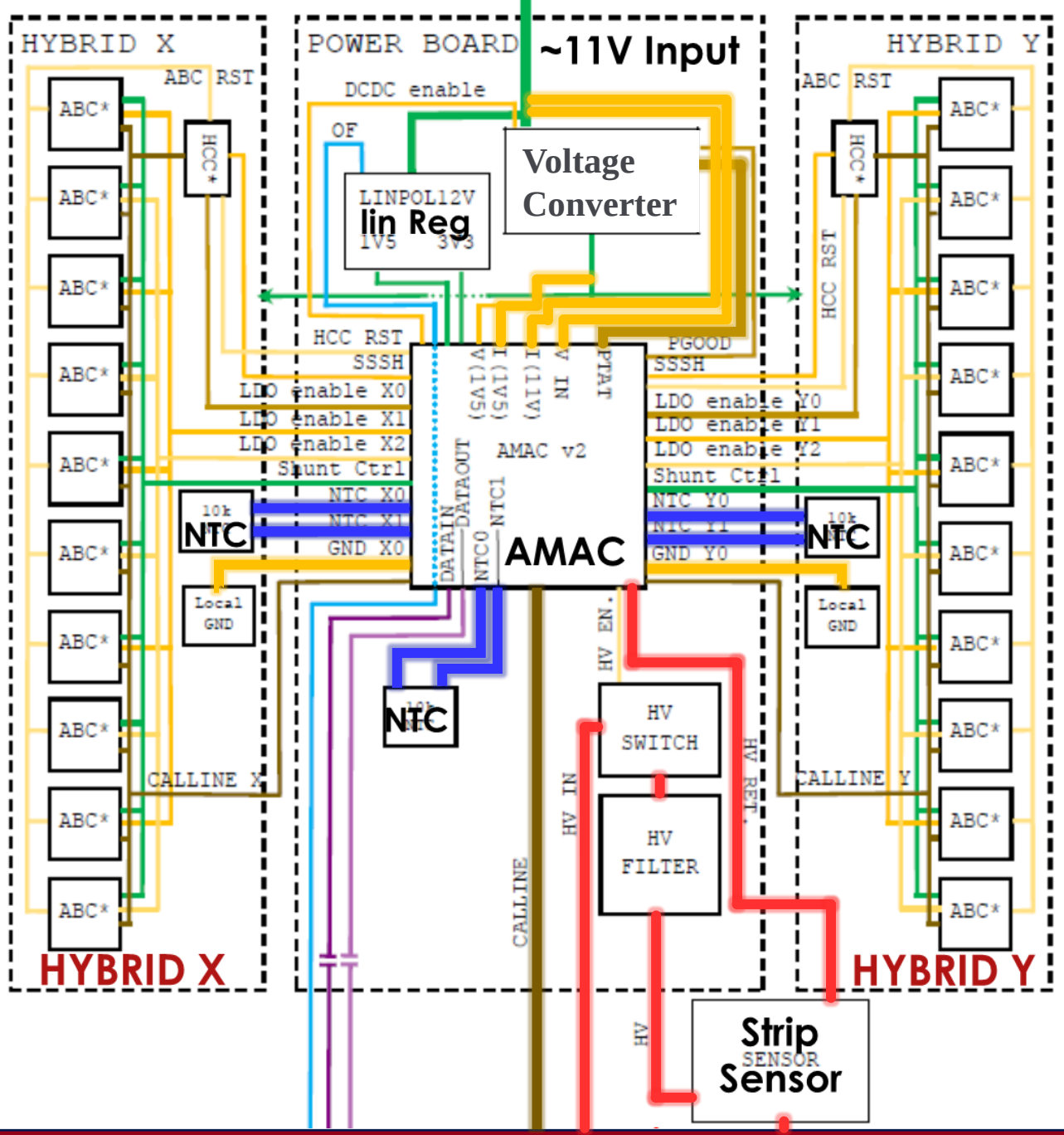

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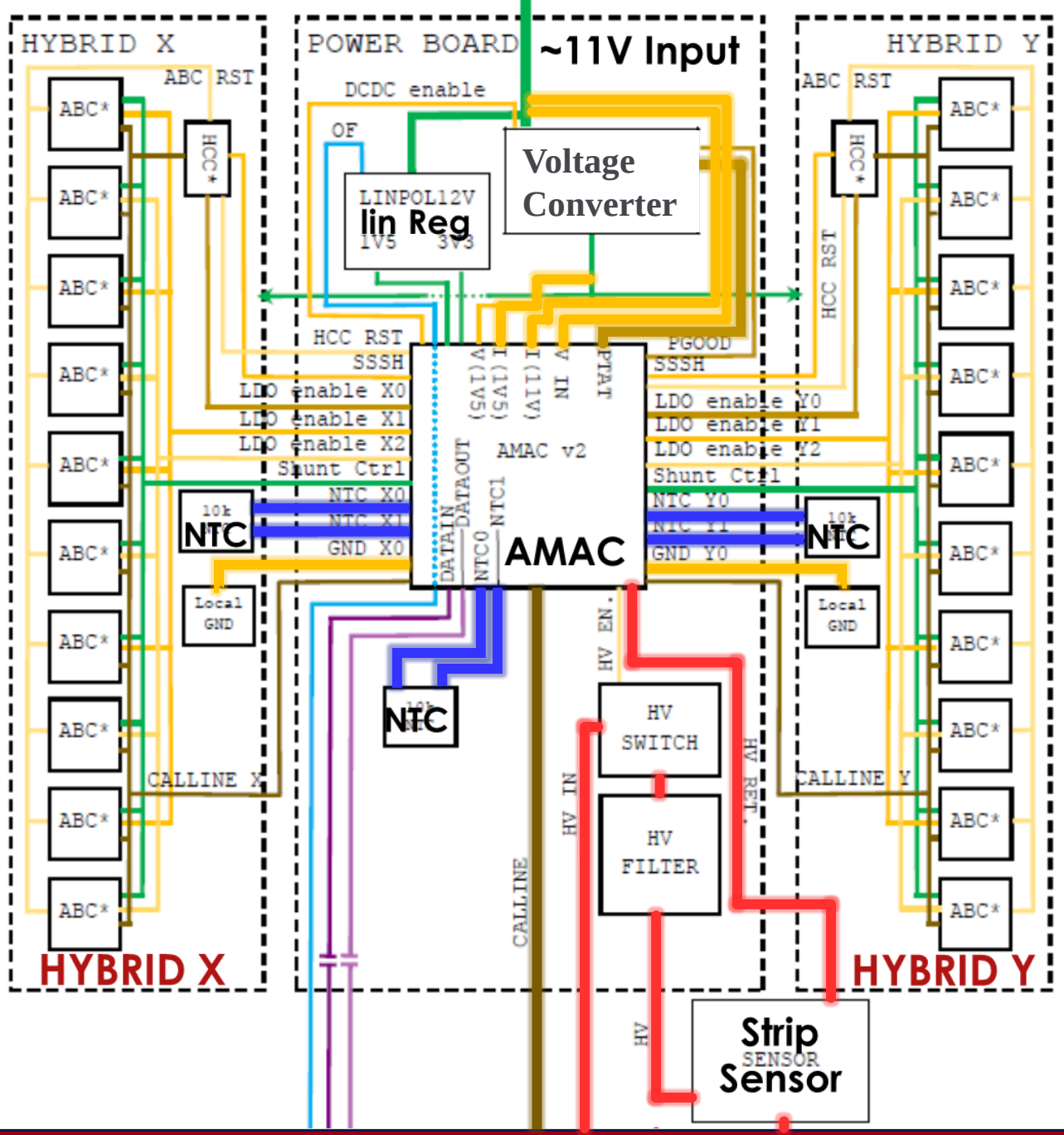

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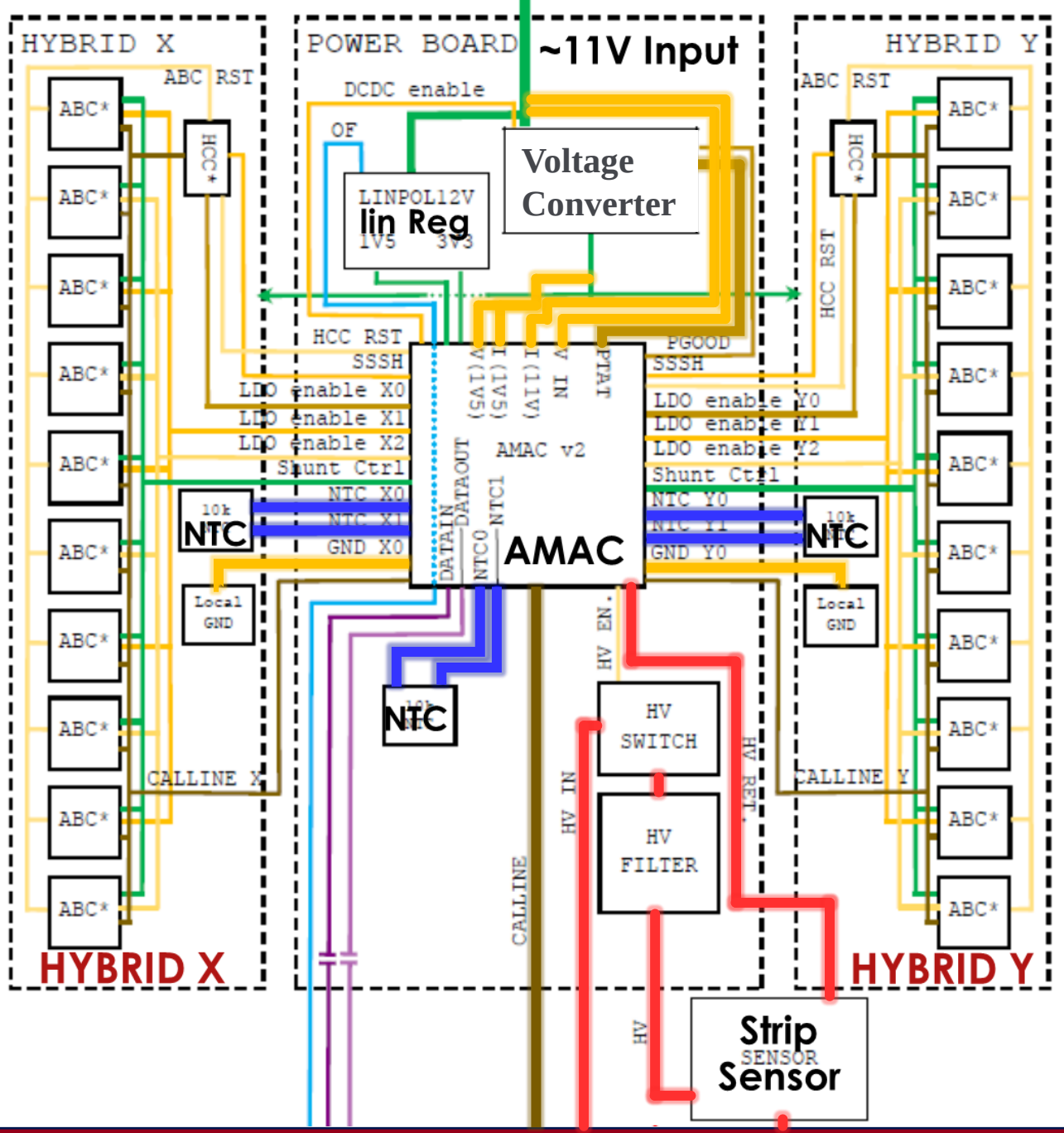

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- **AMAC** Internal Temperature

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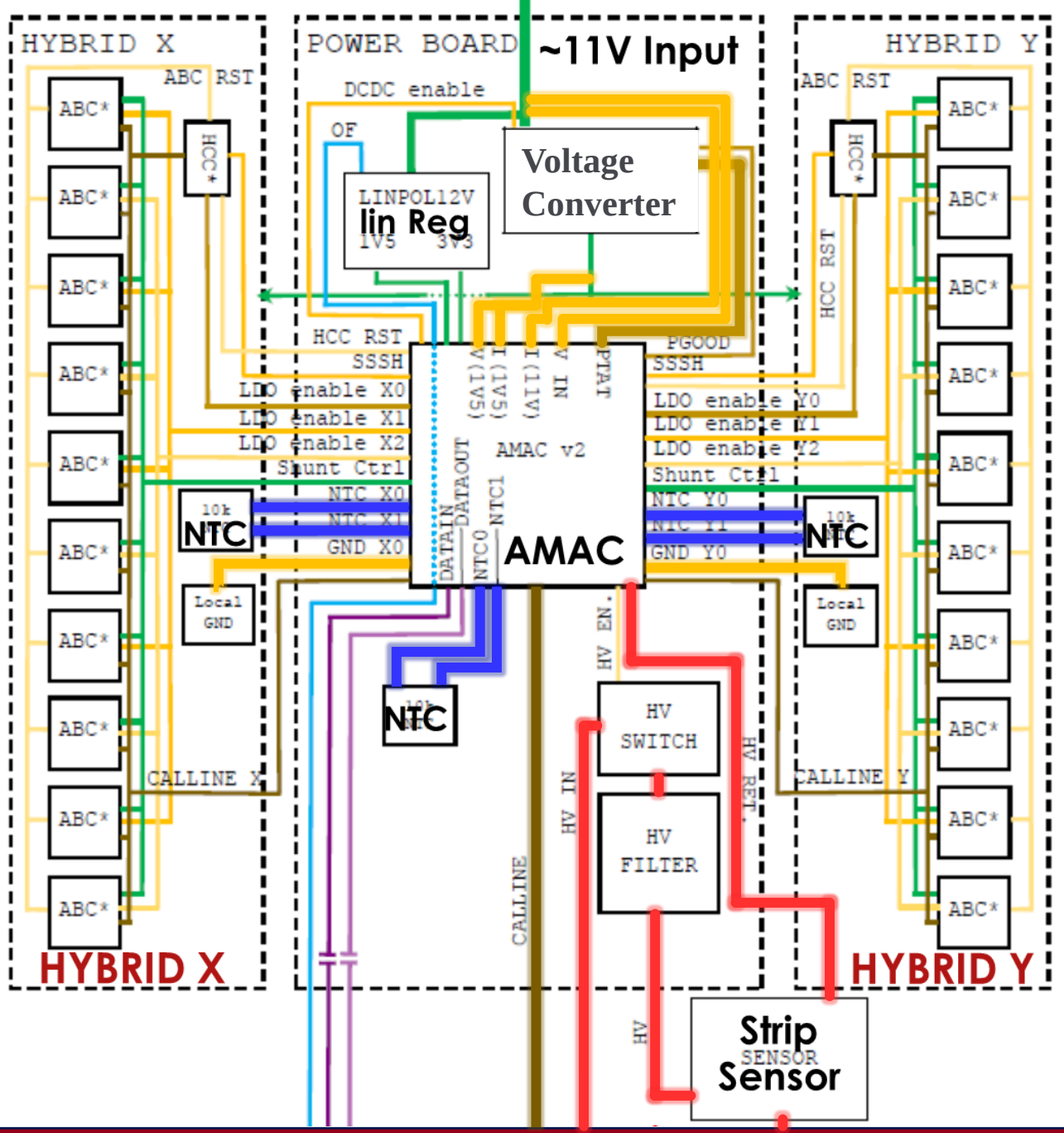
Analog to Digital Converter
(16 Multiplexer Channel)



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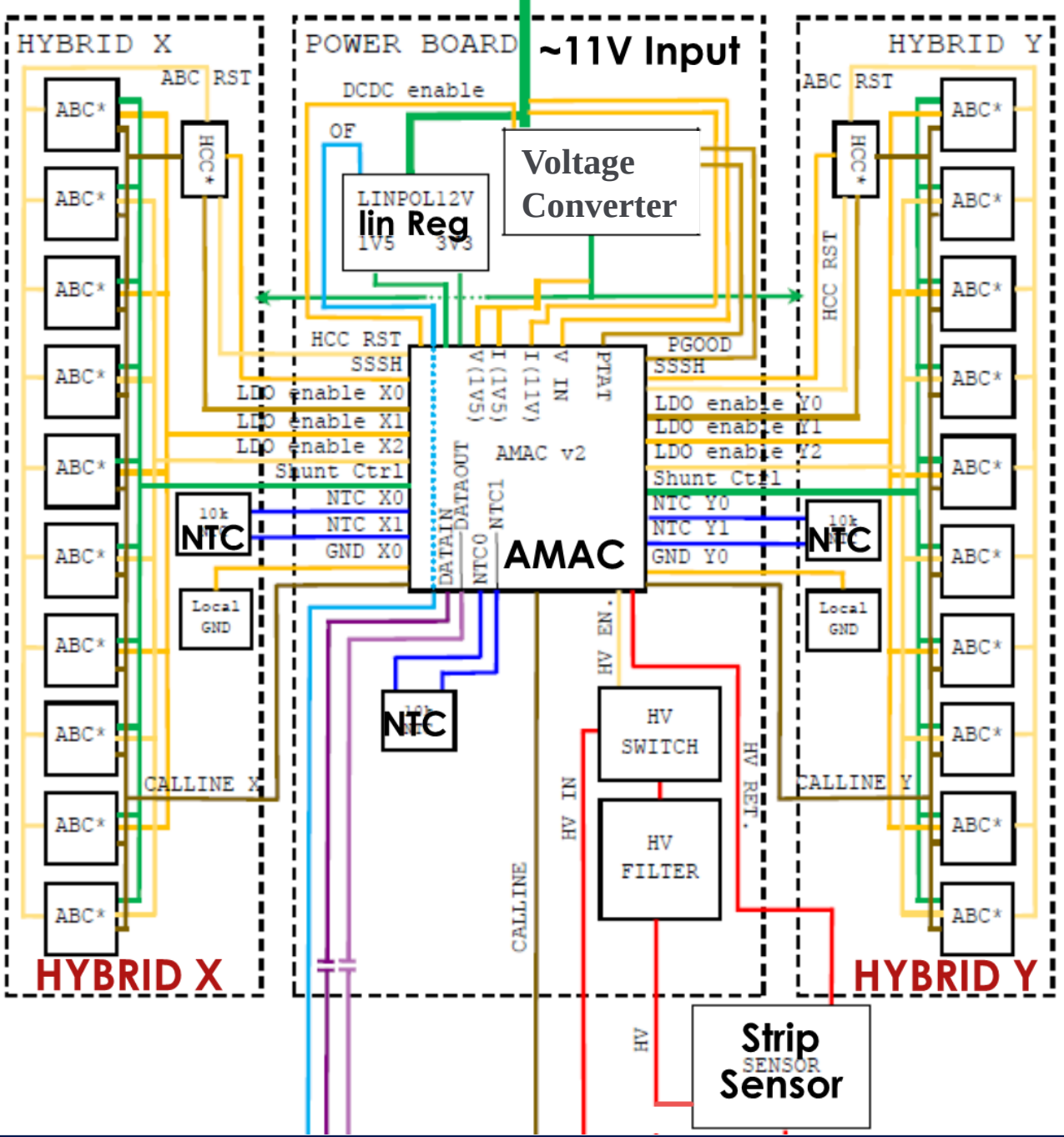
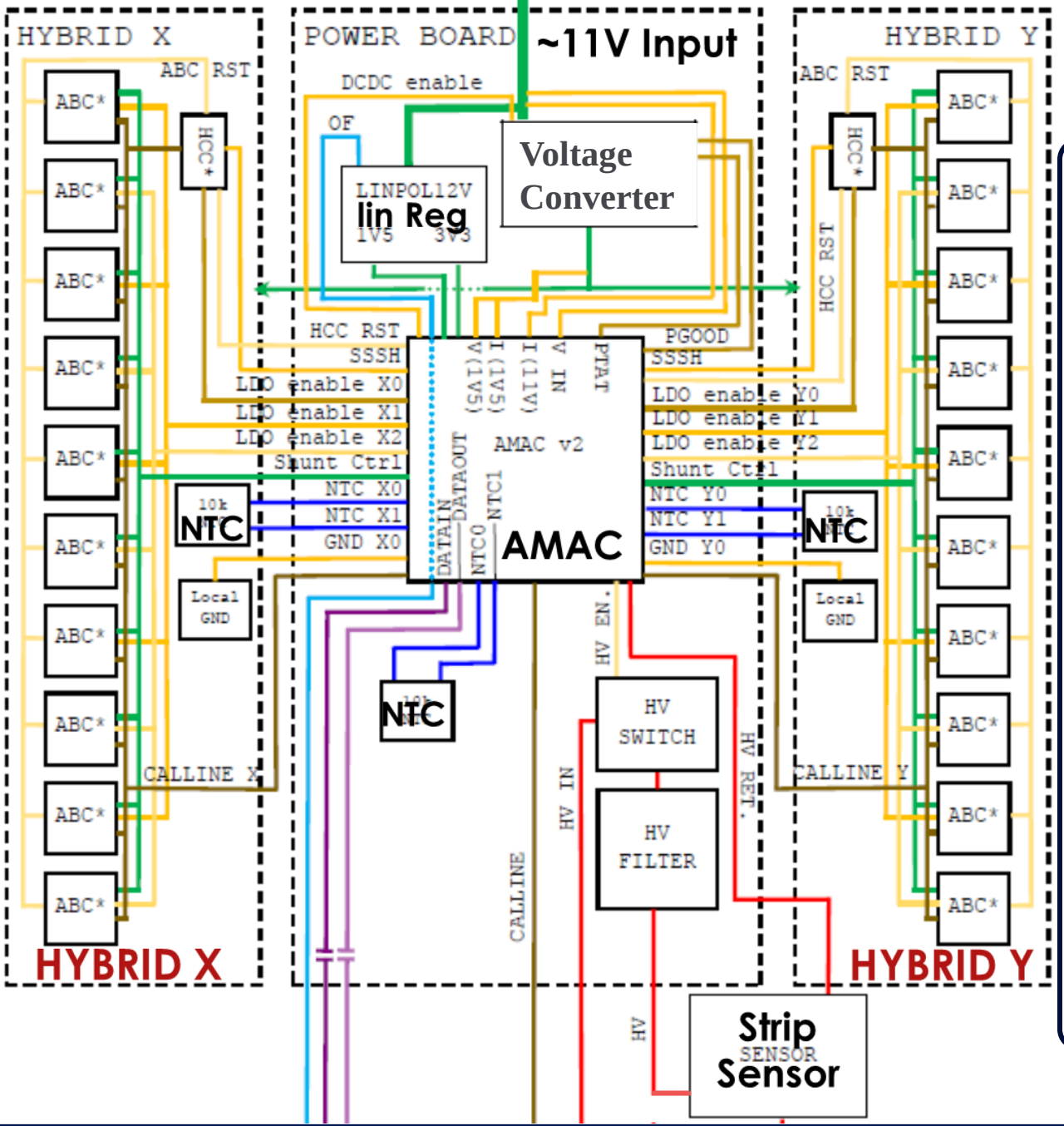
- **Voltage Converter** Output

Analog to Digital Converter
(16 Multiplexer Channel)

Powering Control

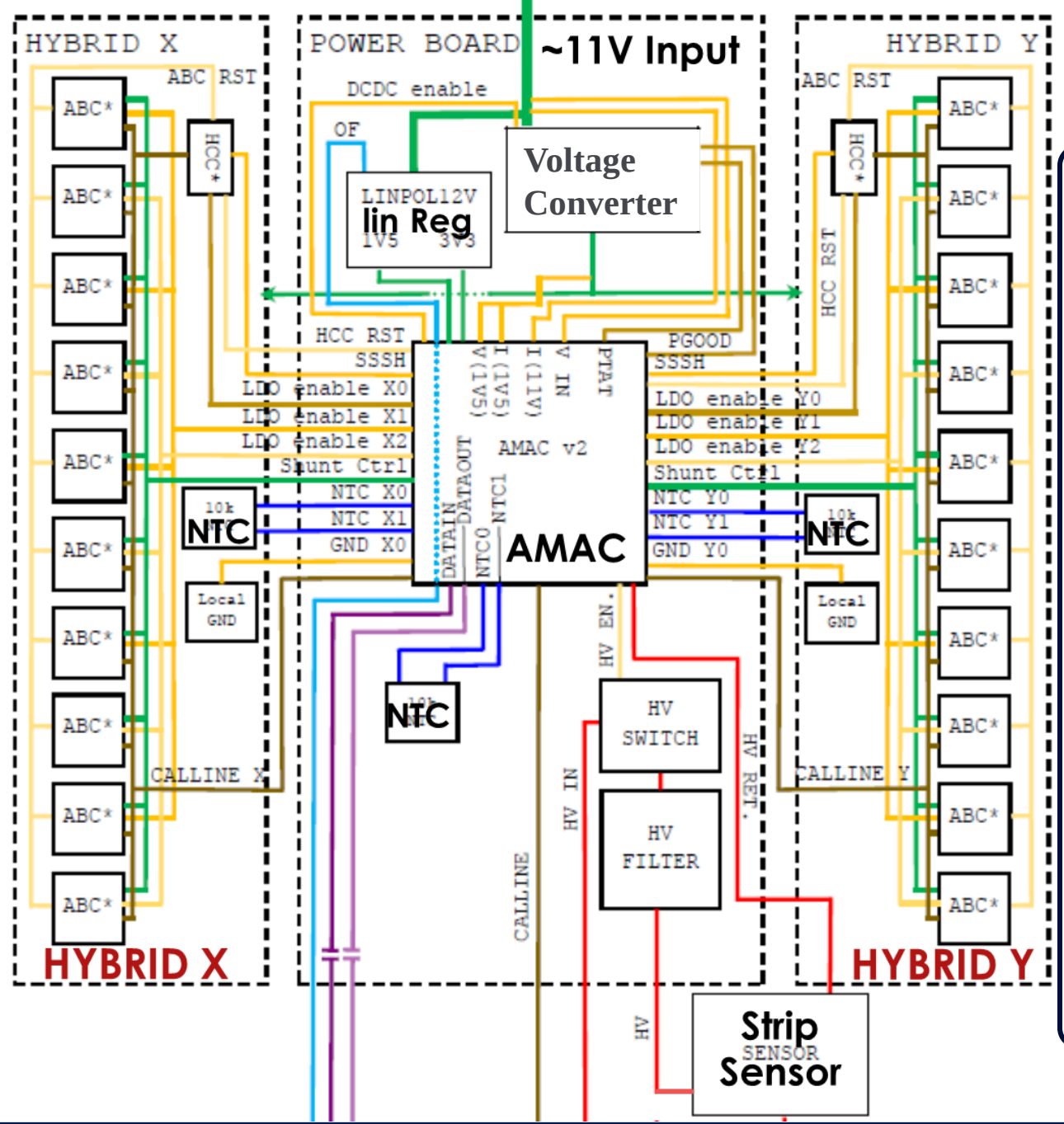


Powering Control



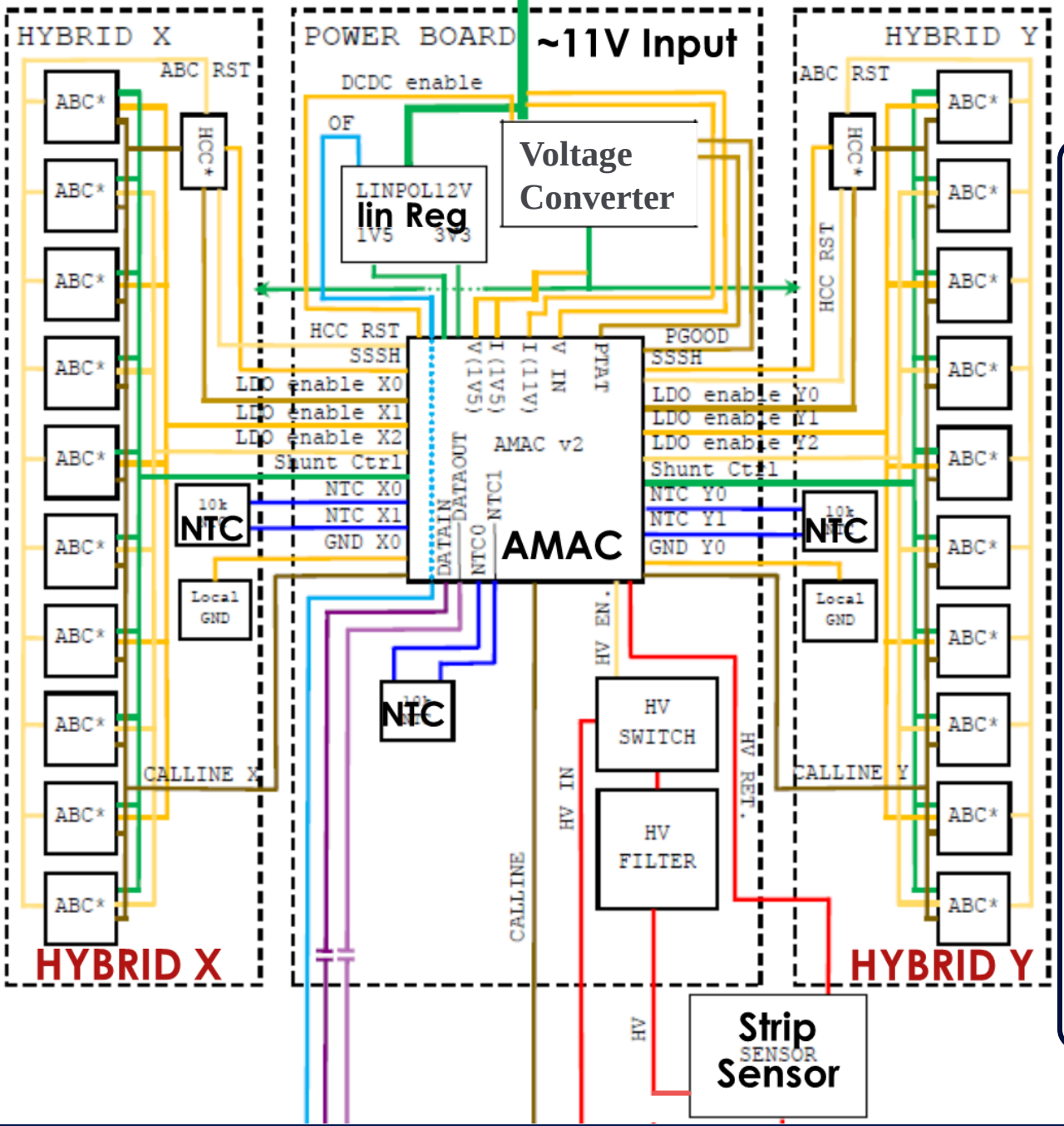
Interlock Switch Output

Powering Control



Interlock Switch Output

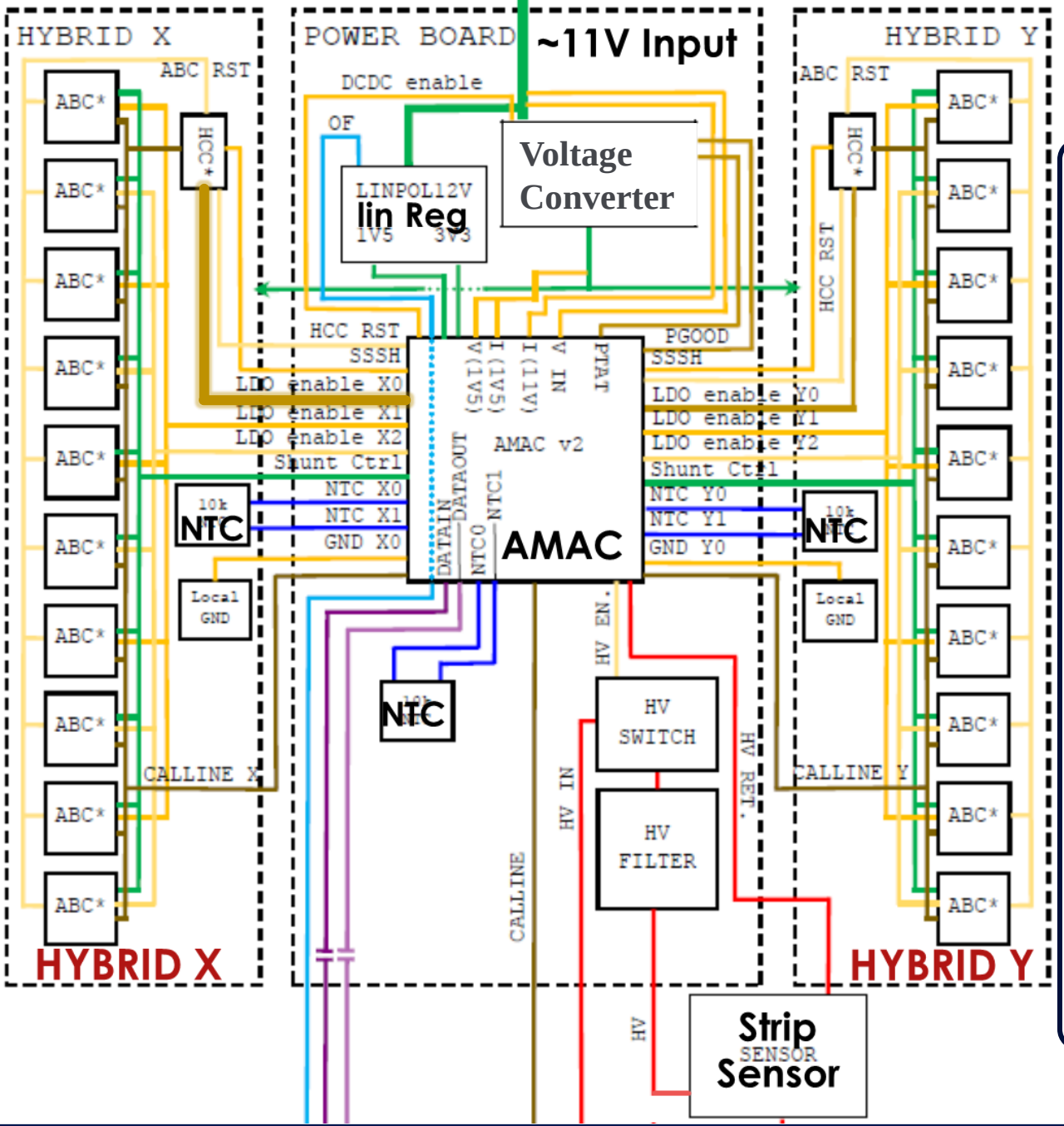
Powering Control



Interlock Switch Output

Hybrid X
Low Power

Powering Control

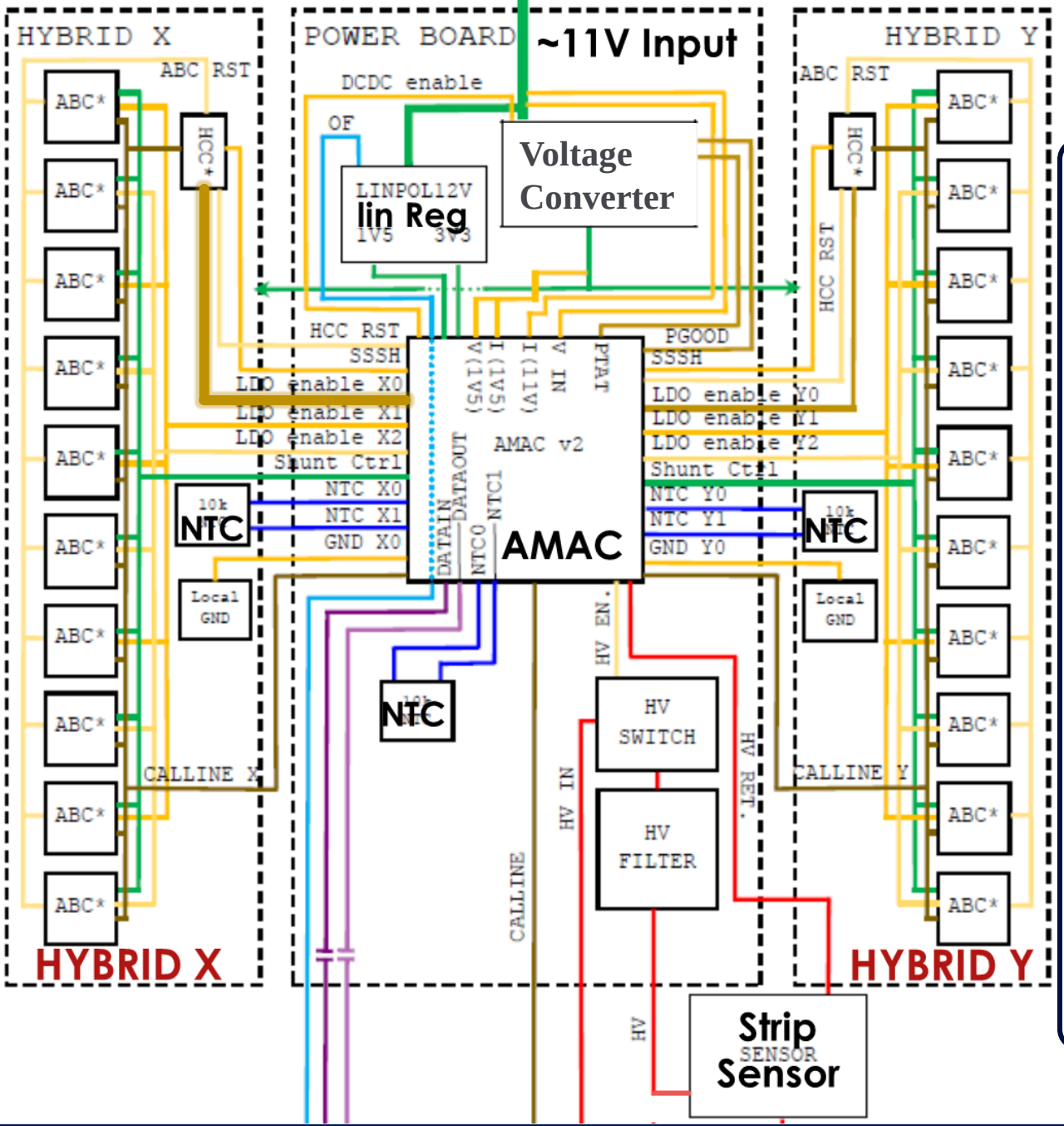


Interlock Switch Output

X0: HCCStar

Hybrid X
Low Power

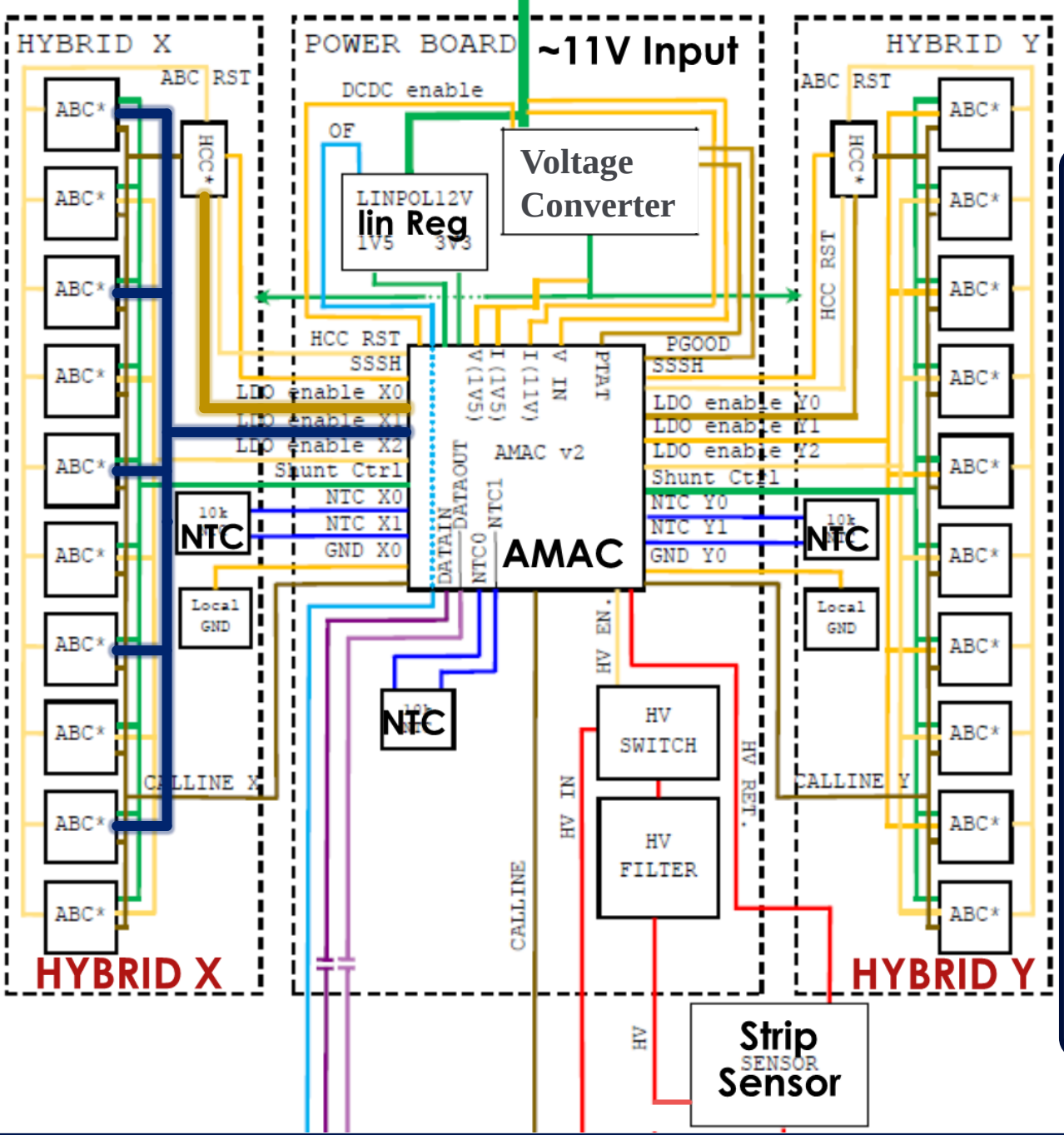
Powering Control



Interlock Switch Output

X0: HCCStar

Hybrid X
Low Power

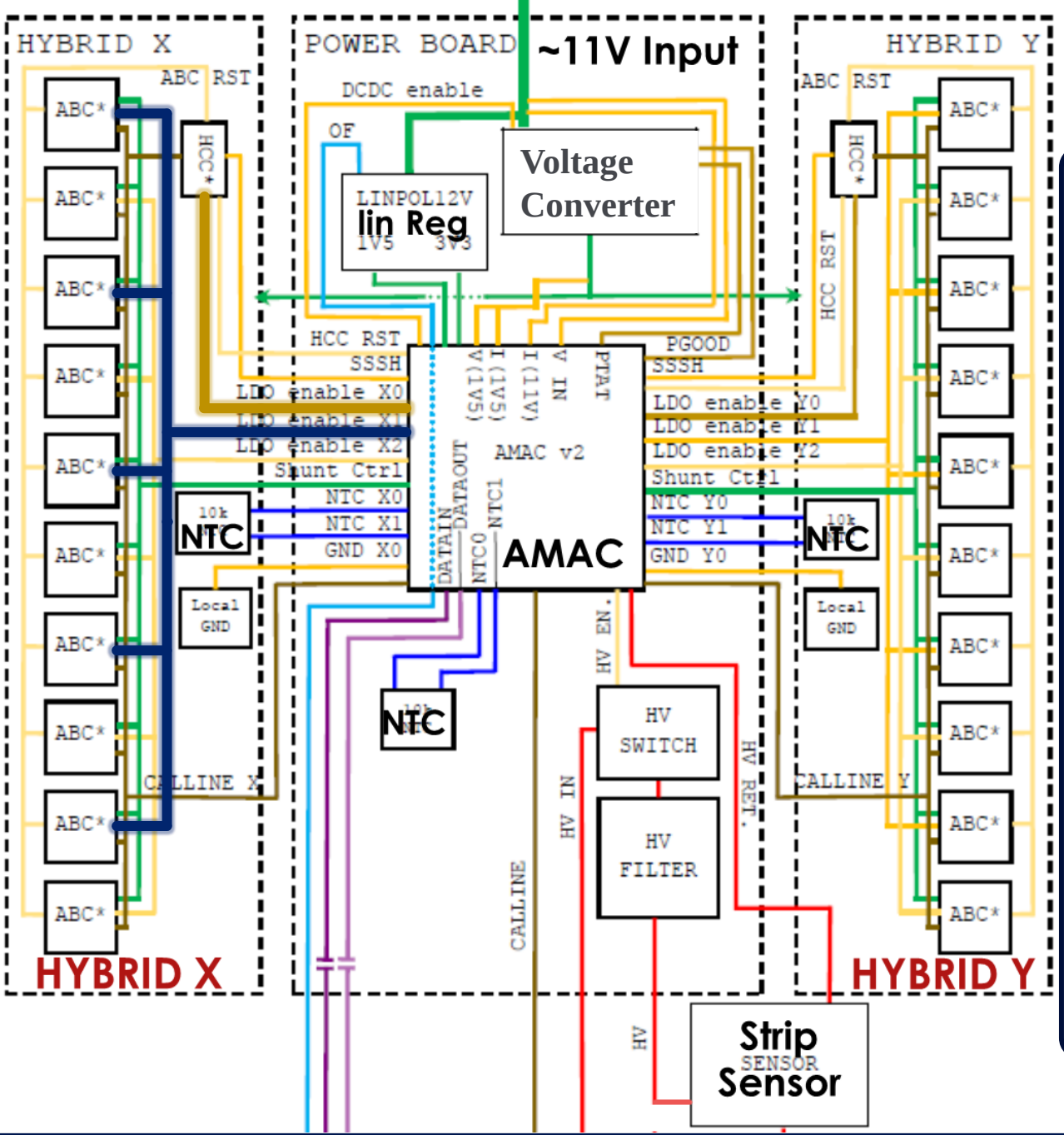


Powering Control

Interlock Switch Output

Hybrid X
Low Power

- X0: HCCStar
- X1: 5×ABCStar



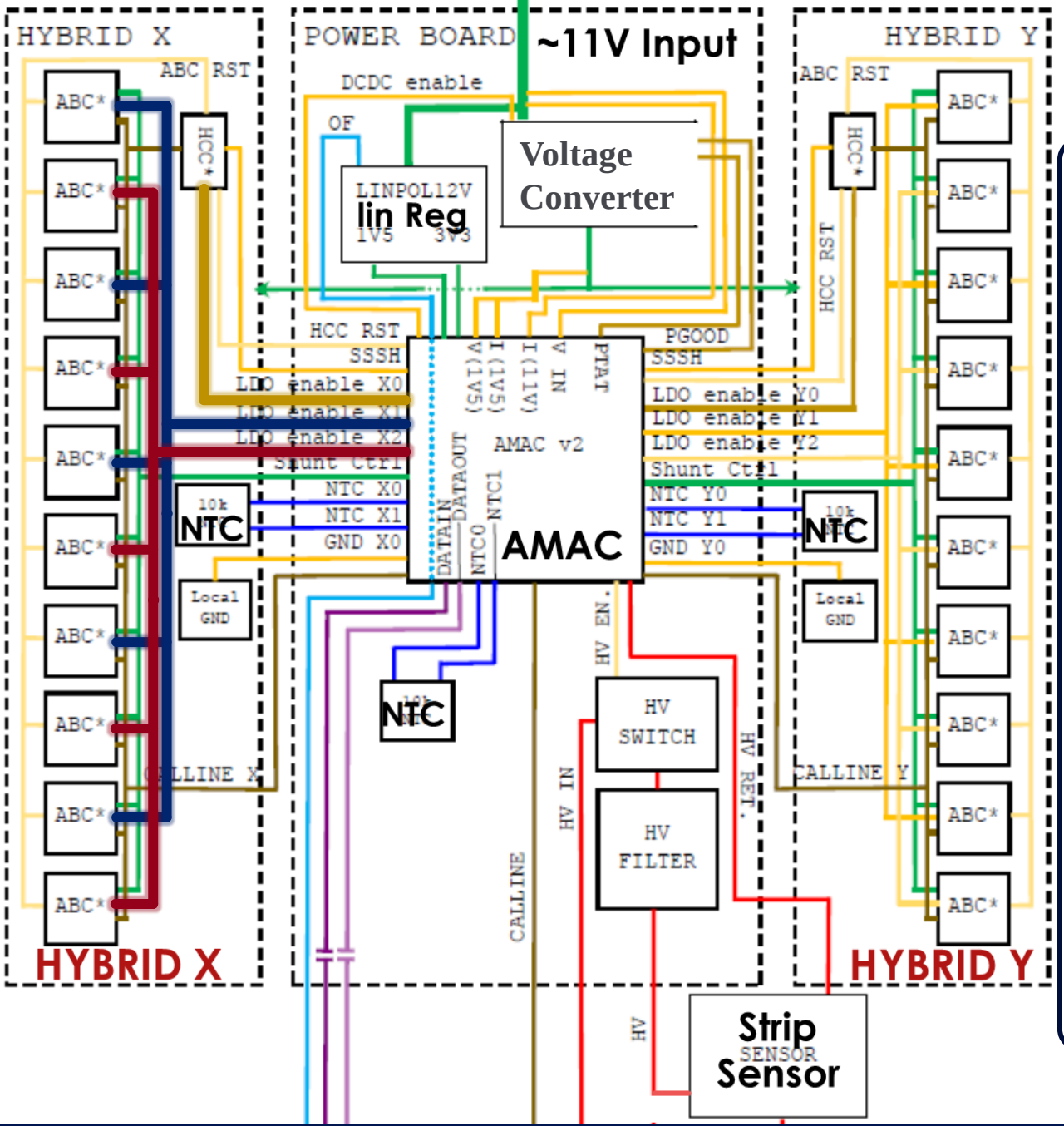
Powering Control

Interlock Switch Output

Hybrid X
Low Power

- X0: HCCStar
- X1: 5×ABCStar

Powering Control

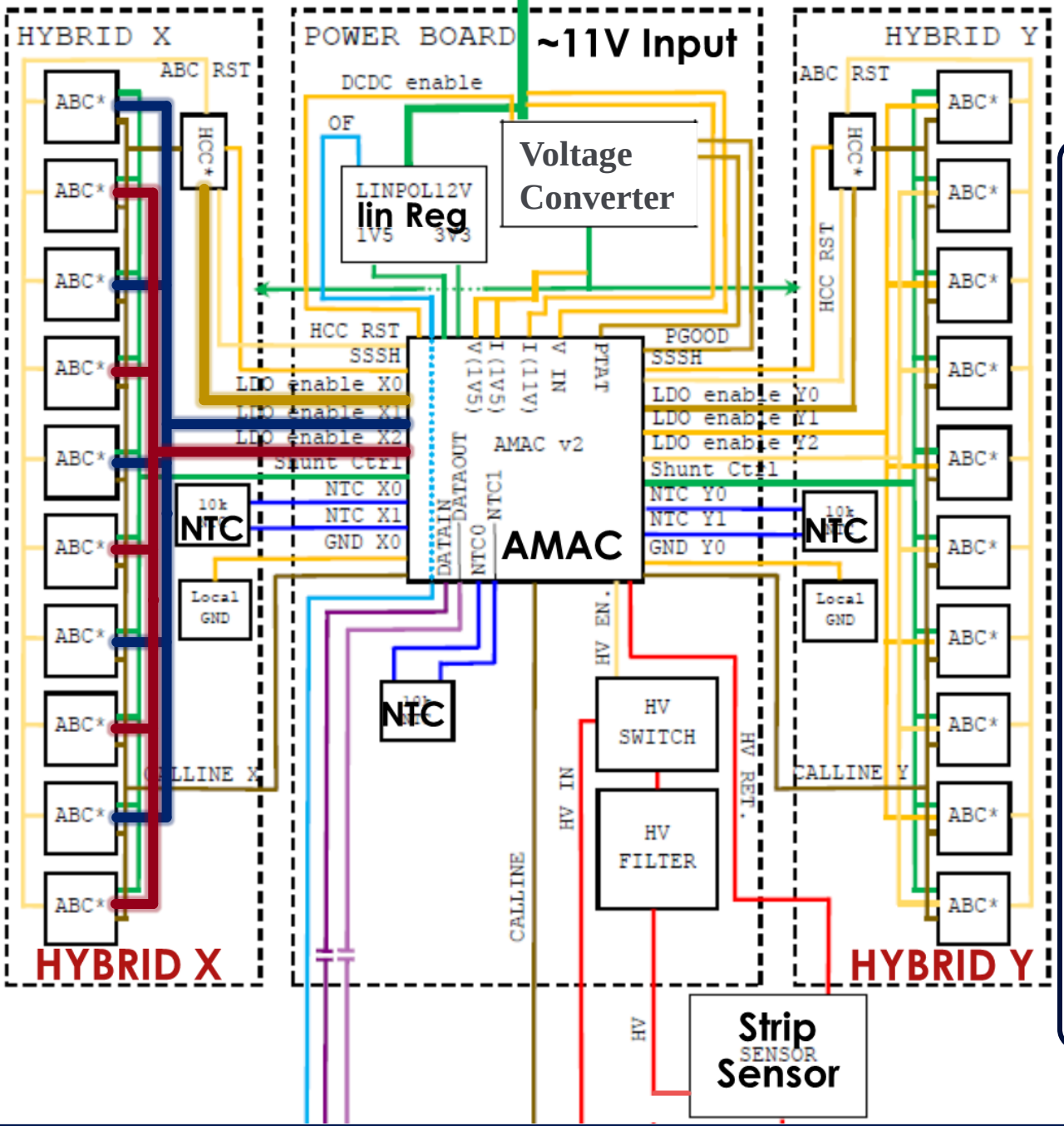


Interlock Switch Output

Hybrid X Low Power

- X0: HCCStar
- X1: 5×ABCStar
- X2: 5×ABCStar

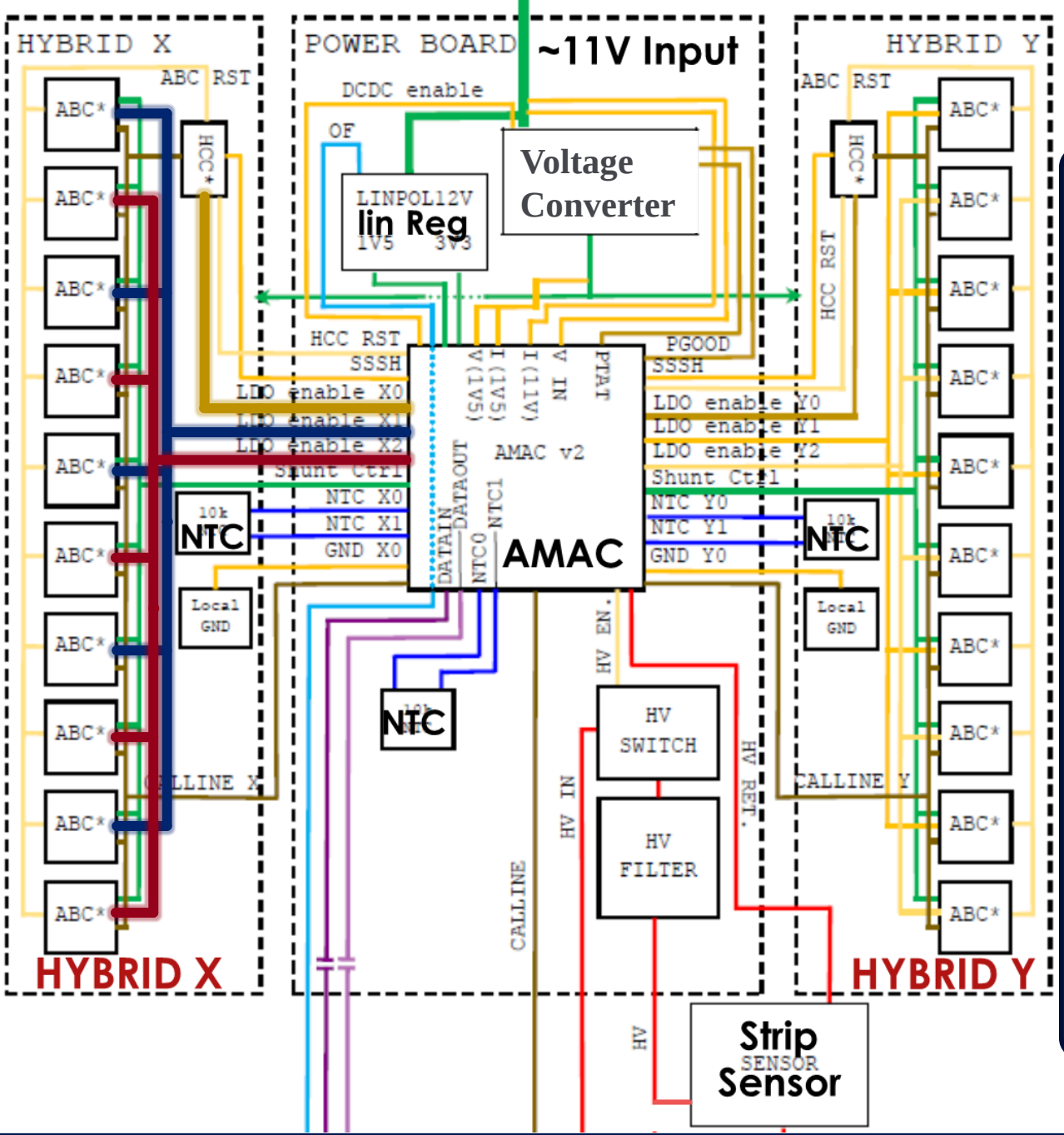
Powering Control



Interlock Switch Output

Hybrid X Low Power

- X0: HCCStar
- X1: 5×ABCStar
- X2: 5×ABCStar



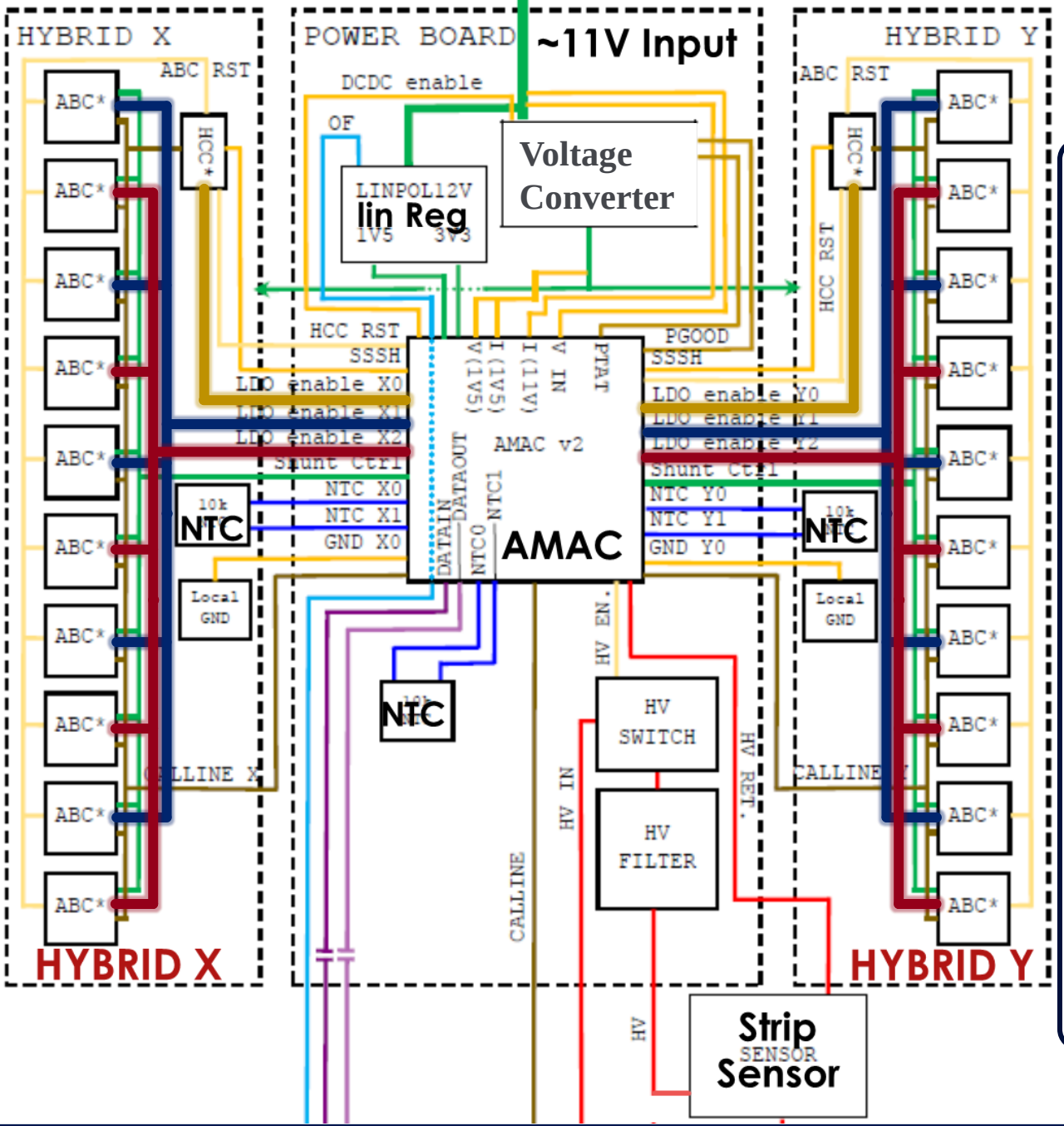
Powering Control

Interlock Switch Output

Hybrid X Low Power
- X0: HCCStar
- X1: 5×ABCStar
- X2: 5×ABCStar

Hybrid Y Low Power
- Y0: HCCStar
- Y1: 5×ABCStar
- Y2: 5×ABCStar

Powering Control

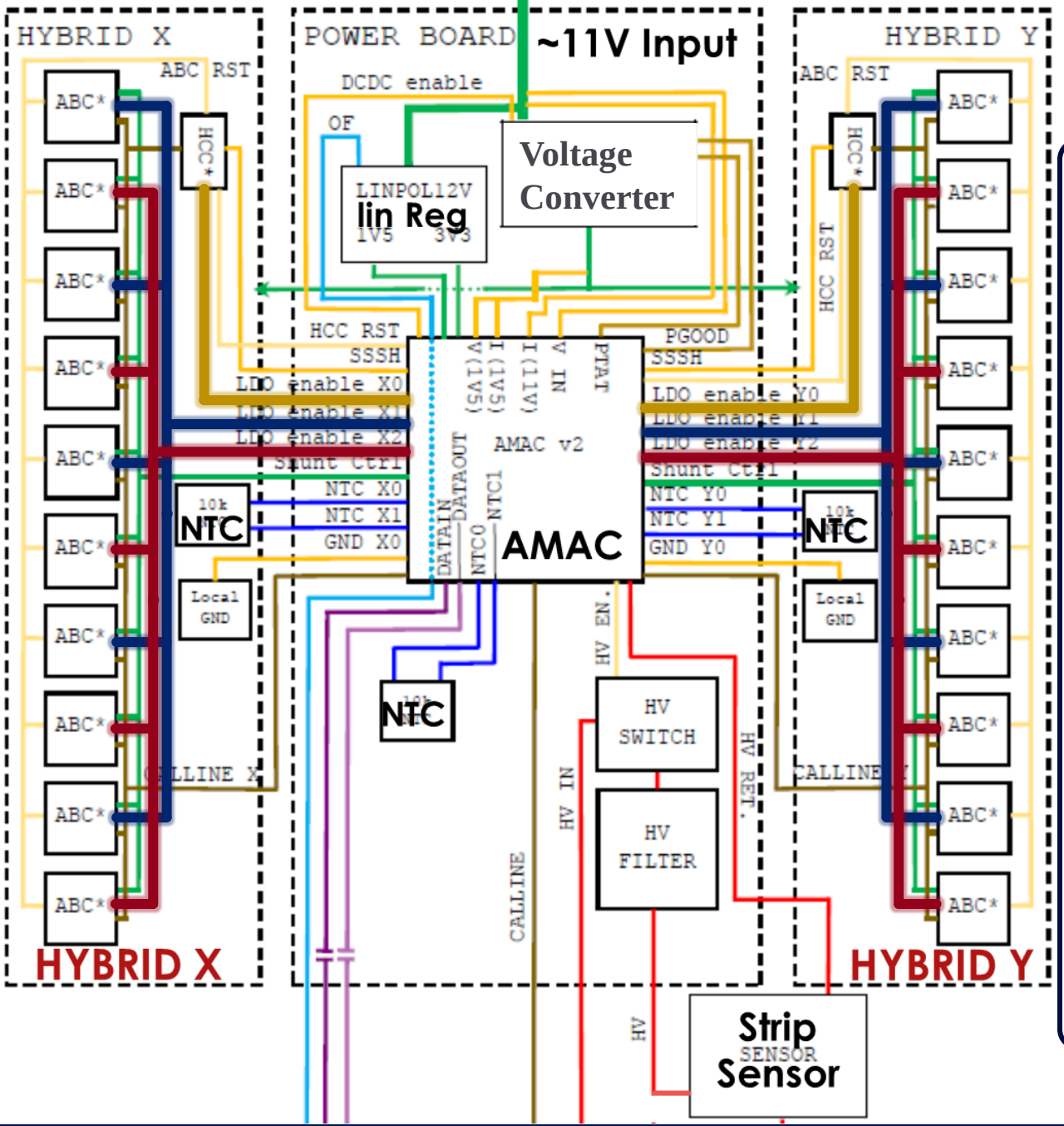


Interlock Switch Output

Hybrid X Low Power
- X0: HCCStar
- X1: 5×ABCStar
- X2: 5×ABCStar

Hybrid Y Low Power
- Y0: HCCStar
- Y1: 5×ABCStar
- Y2: 5×ABCStar

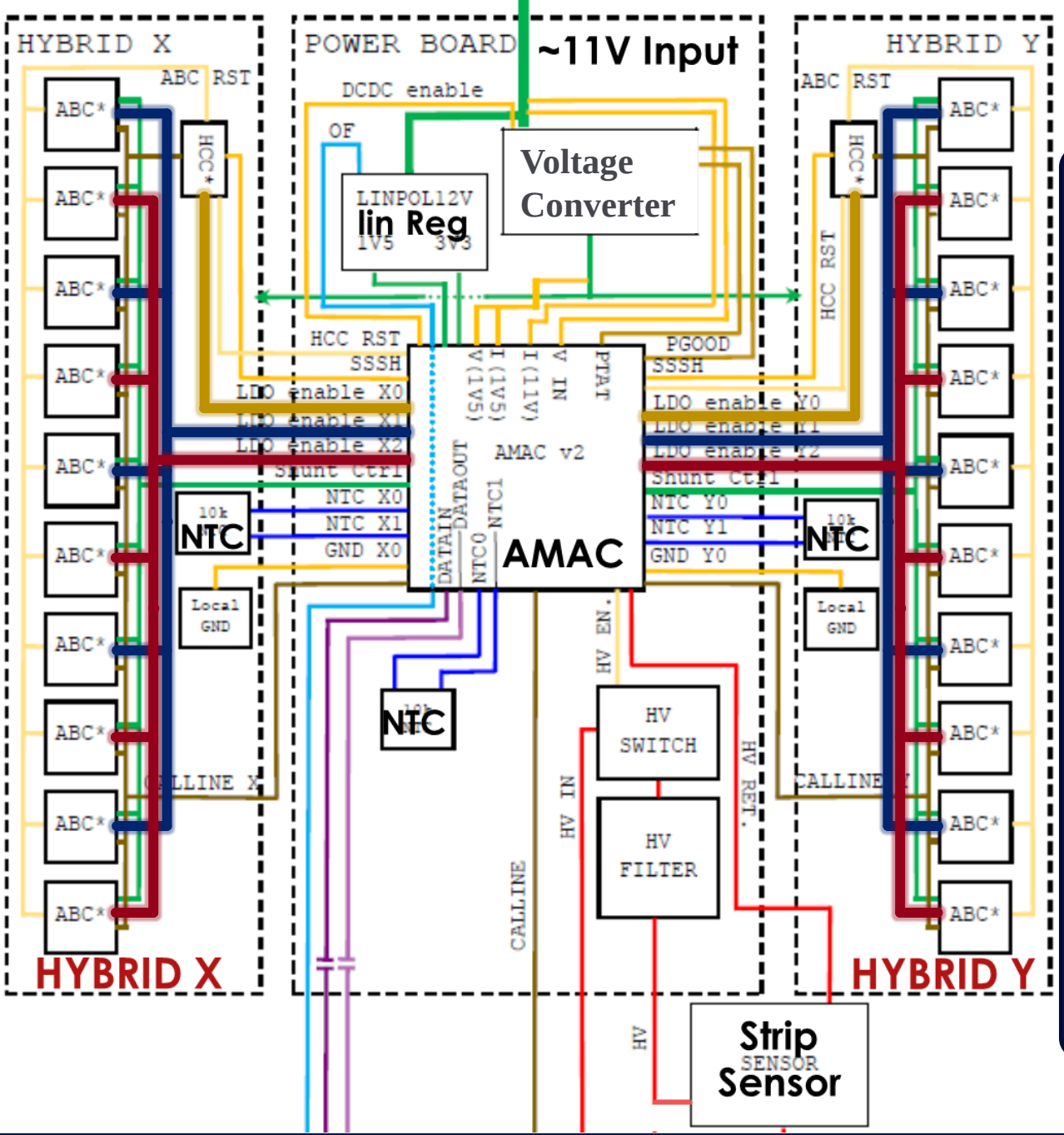
Powering Control



Interlock Switch Output

Hybrid X Low Power
- X0: HCCStar
- X1: 5×ABCStar
- X2: 5×ABCStar

Hybrid Y Low Power
- Y0: HCCStar
- Y1: 5×ABCStar
- Y2: 5×ABCStar

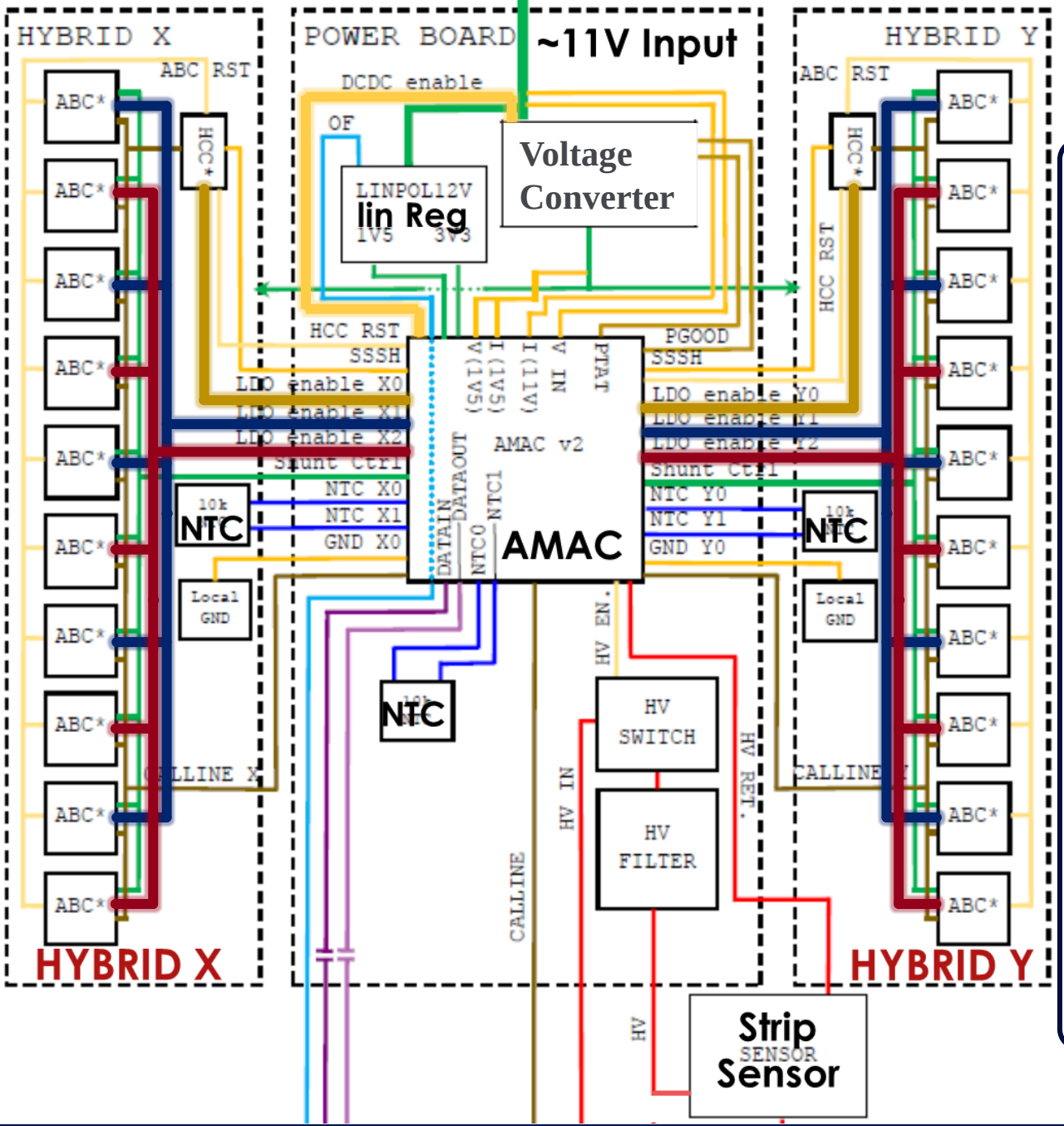


Interlock Switch Output

Powering Control

Hybrid X Low Power	X0: HCCStar X1: 5×ABCStar X2: 5×ABCStar
Hybrid Y Low Power	Y0: HCCStar Y1: 5×ABCStar Y2: 5×ABCStar
Power Enable	Voltage Converter On/Off

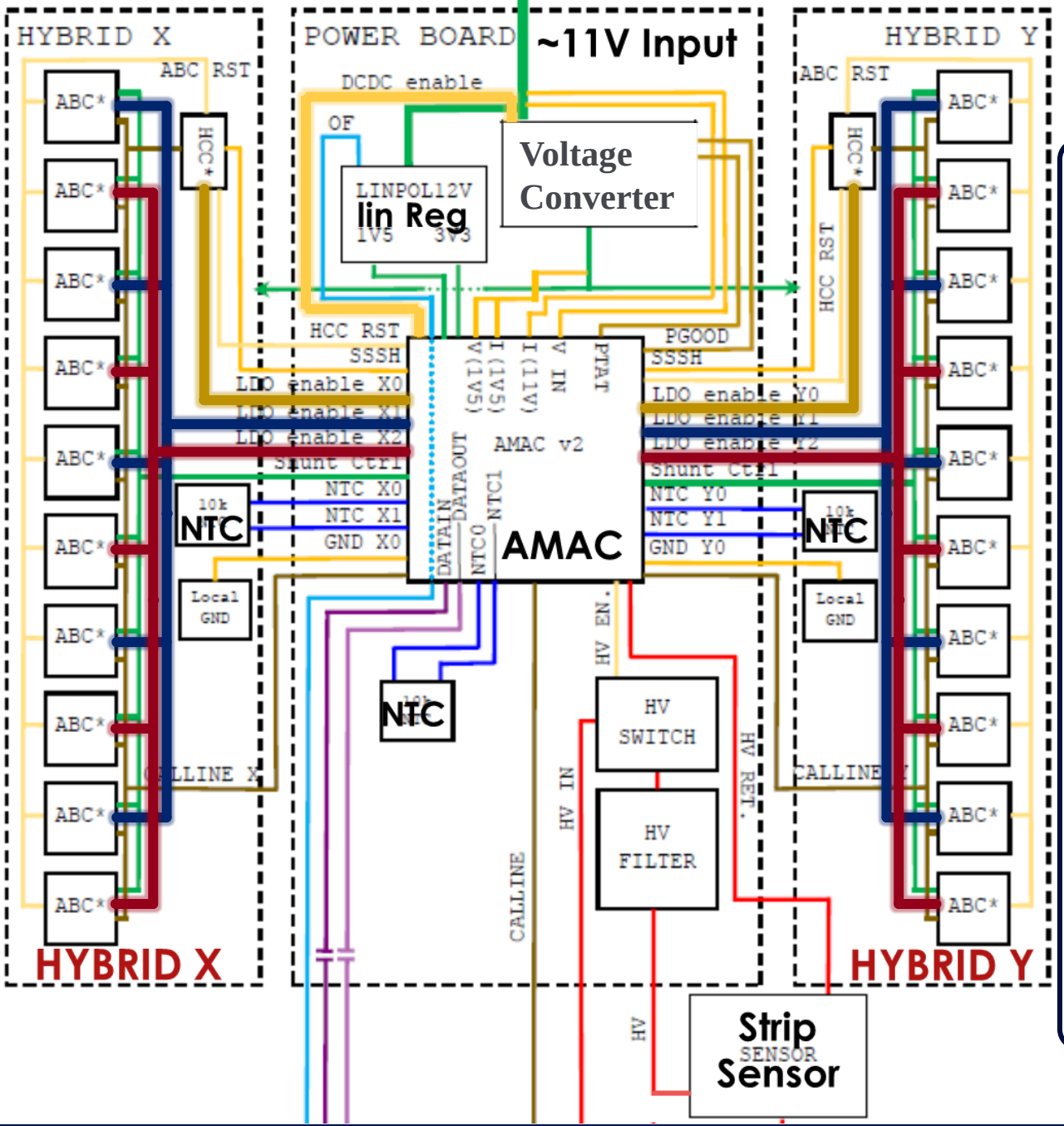
Powering Control



Interlock Switch Output

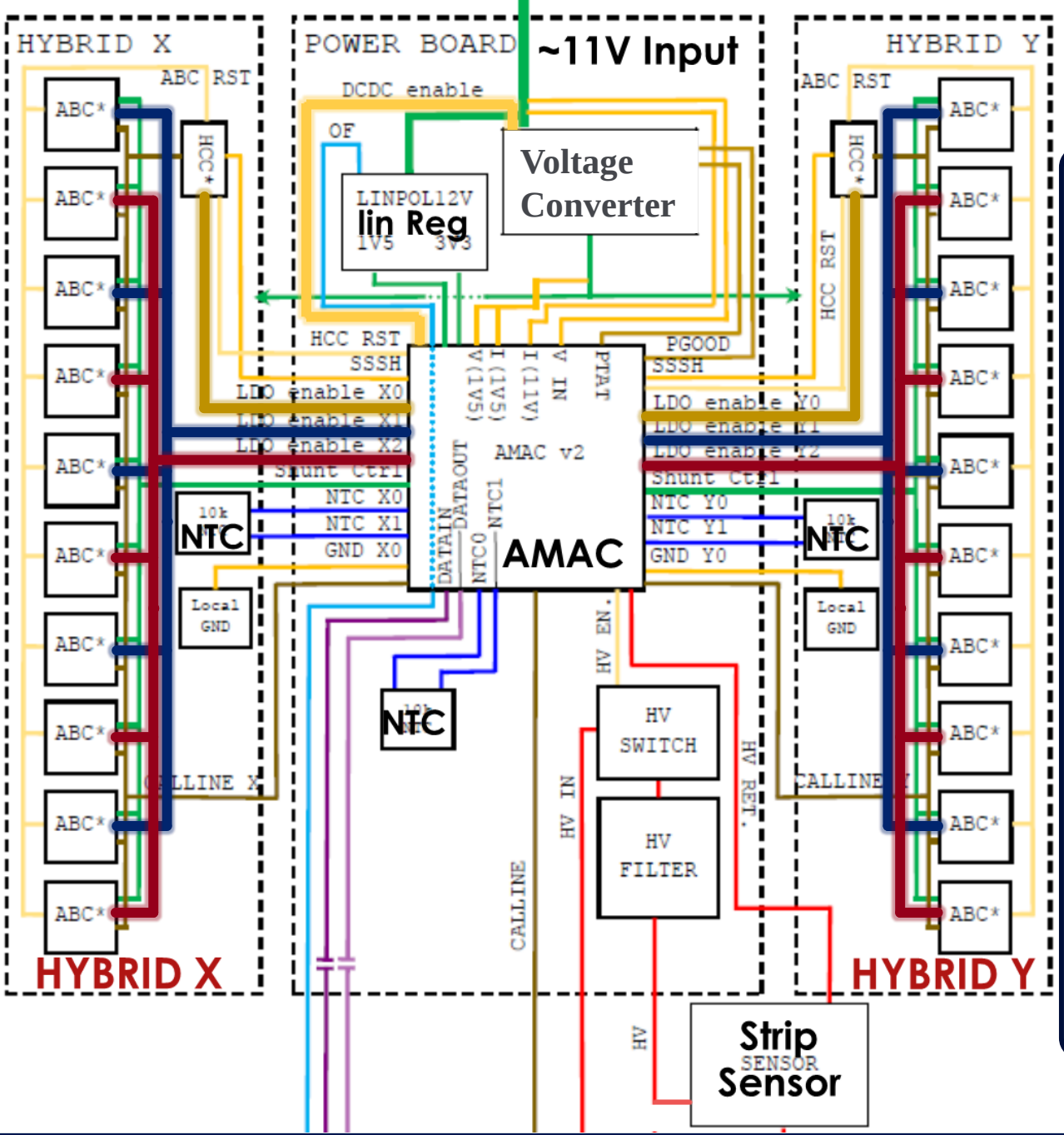
- Hybrid X Low Power
  - X0: HCCStar
  - X1: 5×ABCStar
  - X2: 5×ABCStar
- Hybrid Y Low Power
  - Y0: HCCStar
  - Y1: 5×ABCStar
  - Y2: 5×ABCStar
- Power Enable
  - Voltage Converter On/Off

Powering Control



Interlock Switch Output

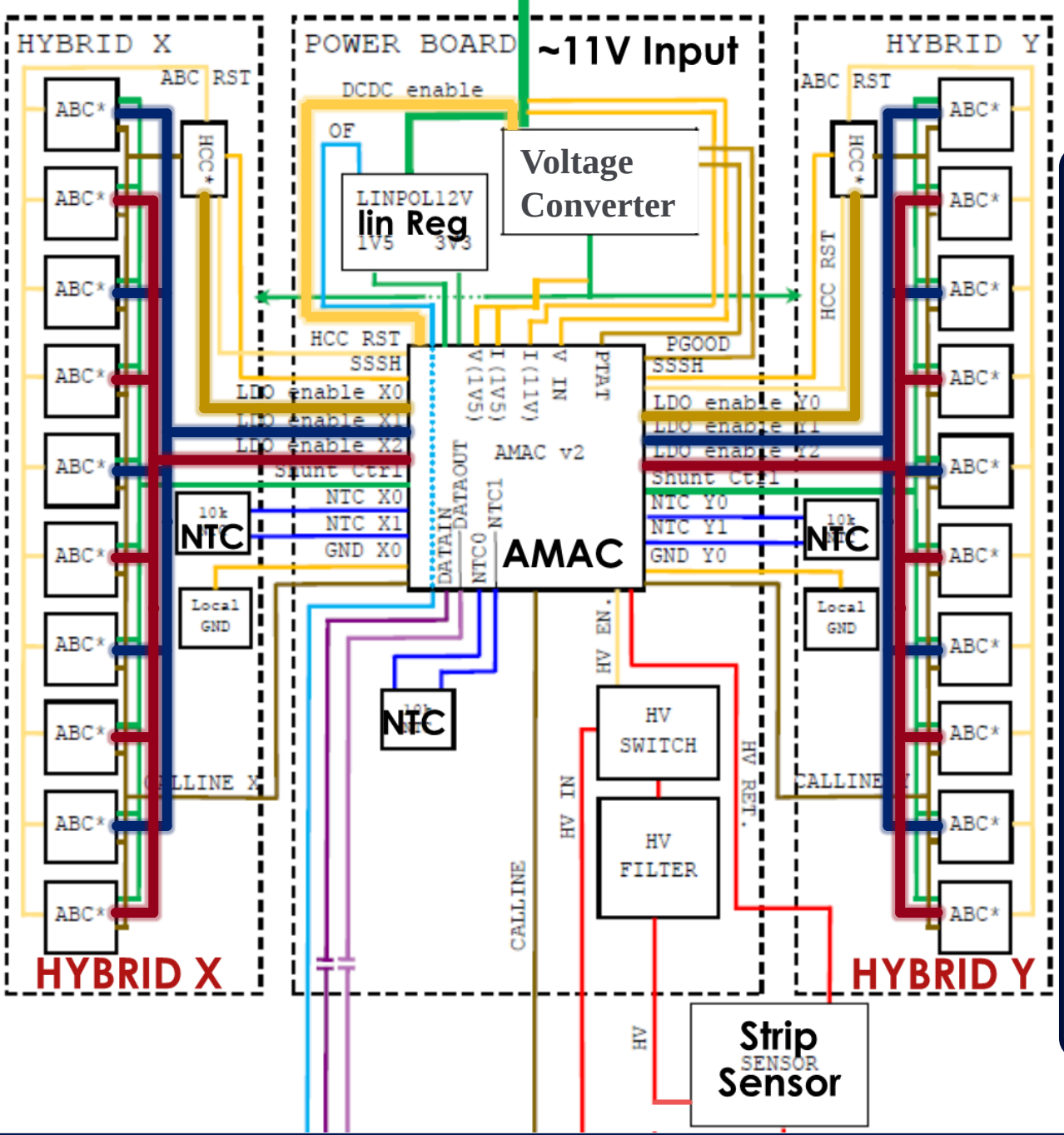
- Hybrid X Low Power
  - X0: HCCStar
  - X1: 5×ABCStar
  - X2: 5×ABCStar
- Hybrid Y Low Power
  - Y0: HCCStar
  - Y1: 5×ABCStar
  - Y2: 5×ABCStar
- Power Enable
  - Voltage Converter On/Off



Powering Control

Interlock Switch Output

Hybrid X Low Power	X0: HCCStar X1: 5×ABCStar X2: 5×ABCStar
Hybrid Y Low Power	Y0: HCCStar Y1: 5×ABCStar Y2: 5×ABCStar
Power Enable	Voltage Converter On/Off
High Voltage Switch 0 & 1	HV 0 On/Off HV 1 On/Off
High Voltage Switch 0 & 1	HV 2 On/Off HV 3 On/Off



Powering Control

Interlock Switch Output

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Power Enable	Voltage Converter On/Off
High Voltage Switch 0 & 1	HV 0 On/Off HV 1 On/Off
High Voltage Switch 0 & 1	HV 2 On/Off HV 3 On/Off

AMAC Internal

Autonomous Monitor And Control (AMAC)

Autonomous Monitor And Control (AMAC)

Analog to Digital Converter
(16 Multiplexer Channel)

Autonomous Monitor And Control (AMAC)

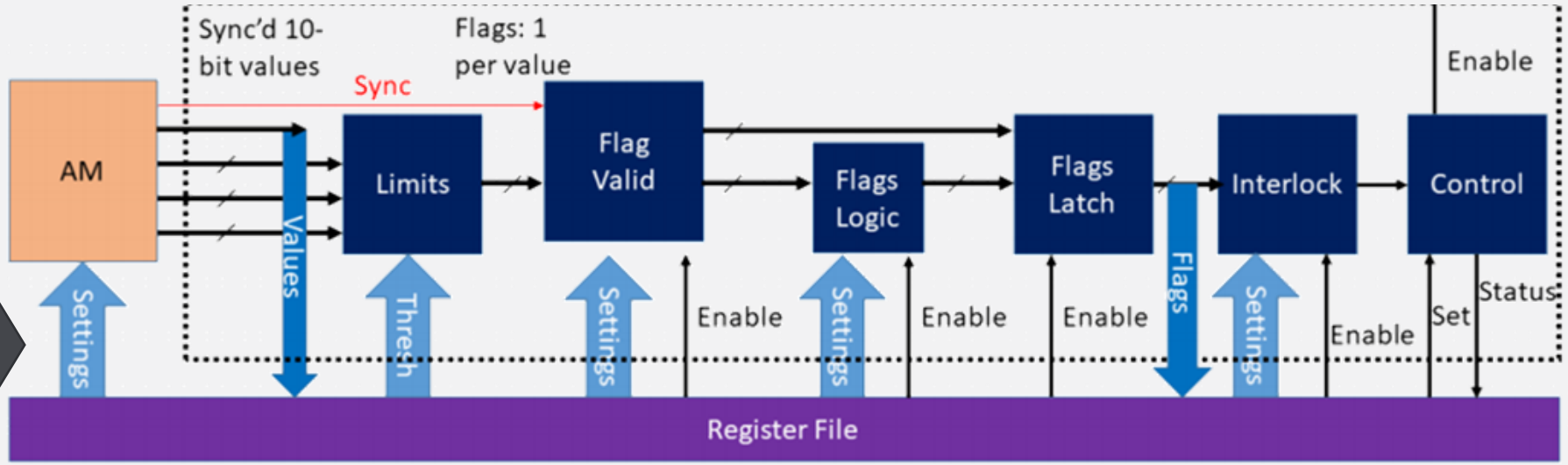
Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Switch Output

Autonomous Monitor And Control (AMAC)

Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Channel



Interlock Switch Output

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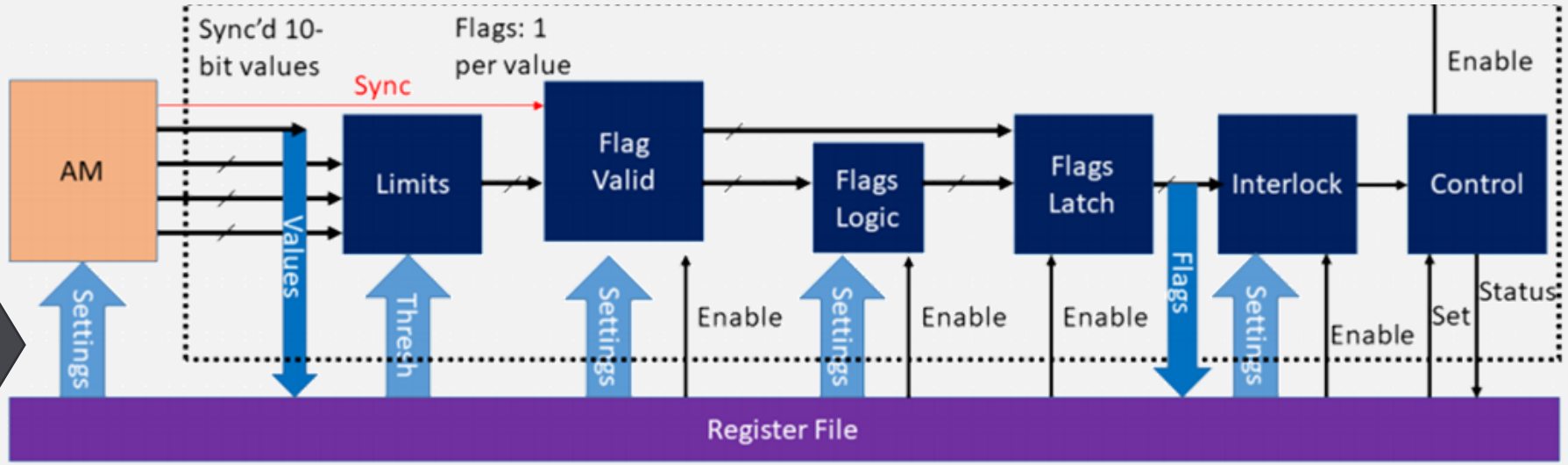
Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Channel



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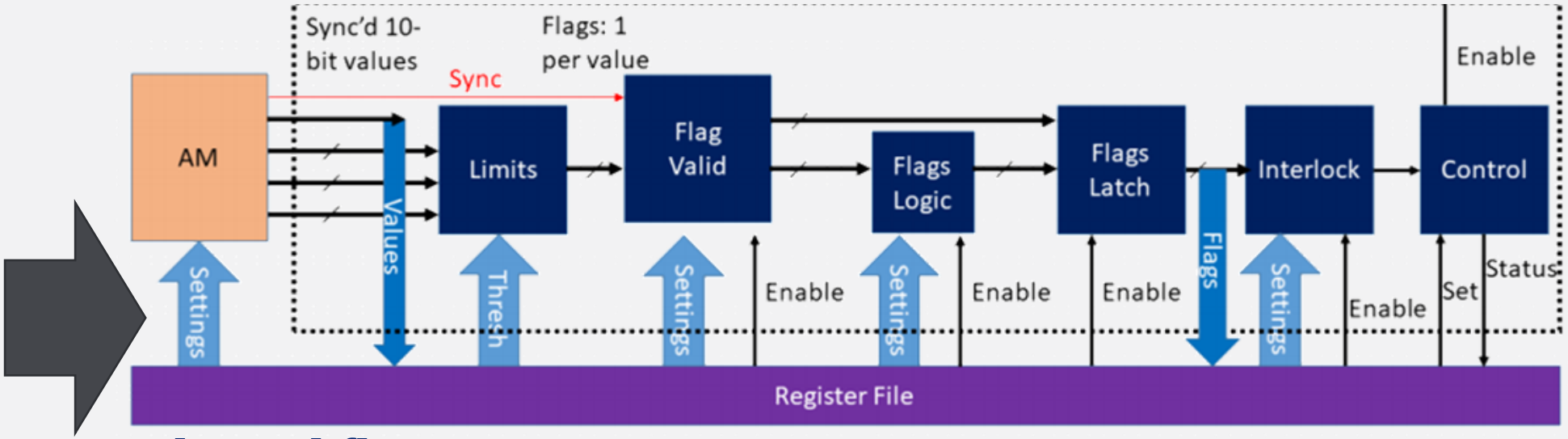


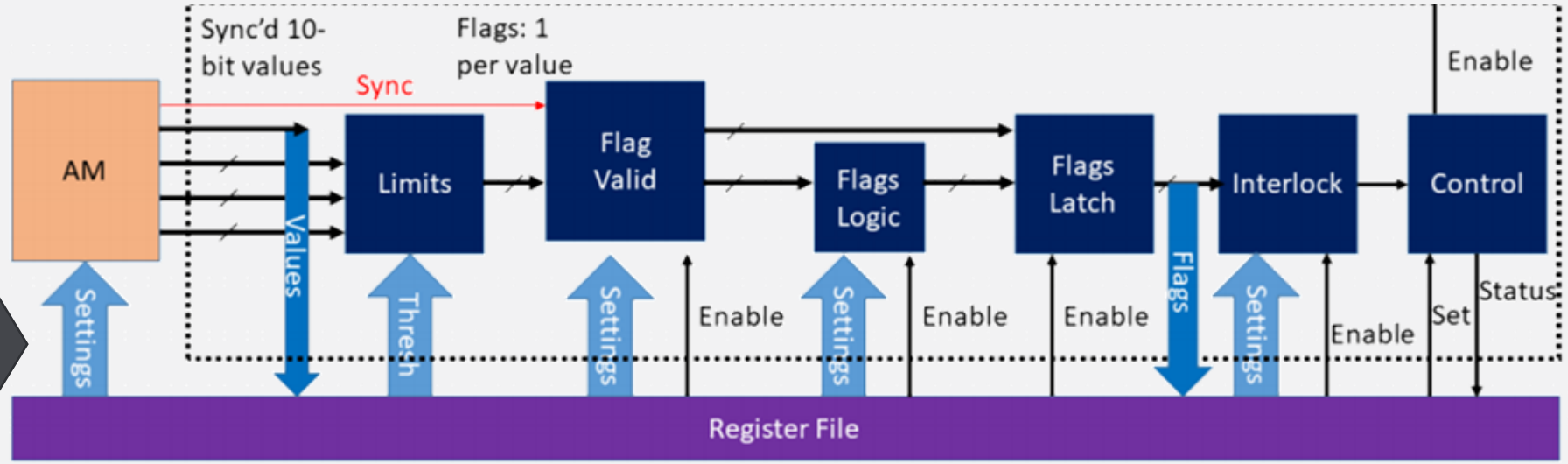
Example workflow:

Interlock Switch Output

Autonomous Monitor And Control (AMAC)

Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Channel



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Interlock Switch Output

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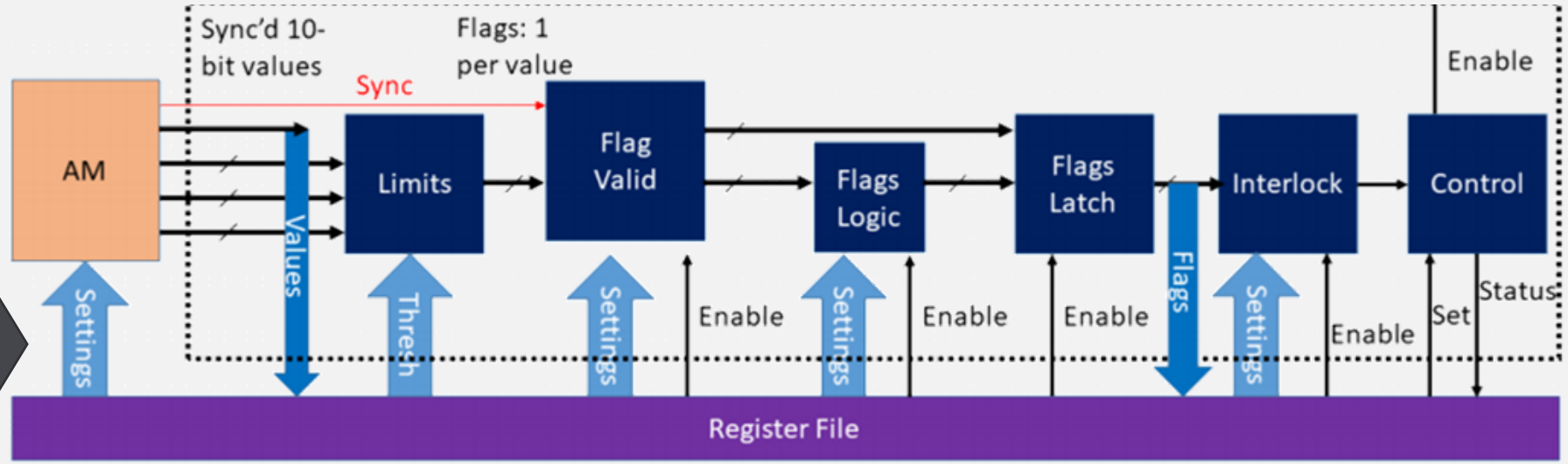


Interlock Switch Output

Example workflow:

Channel:

Hybrid X:

Hybrid Y:

Power-board:

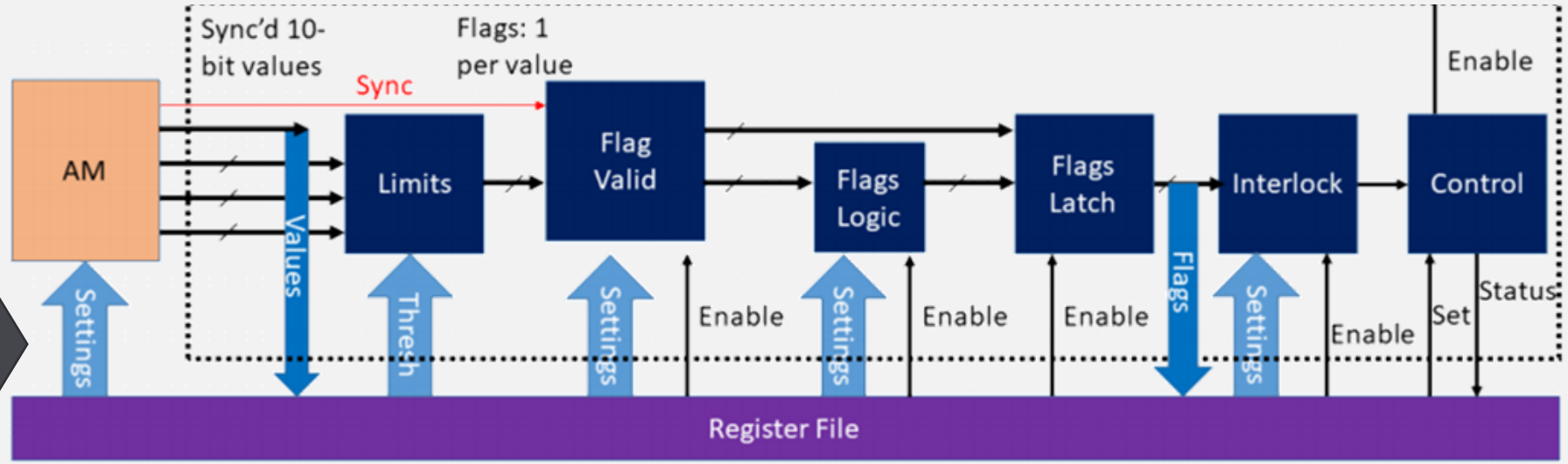
Total Current:

…

Autonomous Monitor And Control (AMAC)

Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Channel



Interlock Switch Output

Example workflow:

Channel:
Hybrid X:
Hybrid Y:
Power-board:
Total Current:
…

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Analog to Digital Converter
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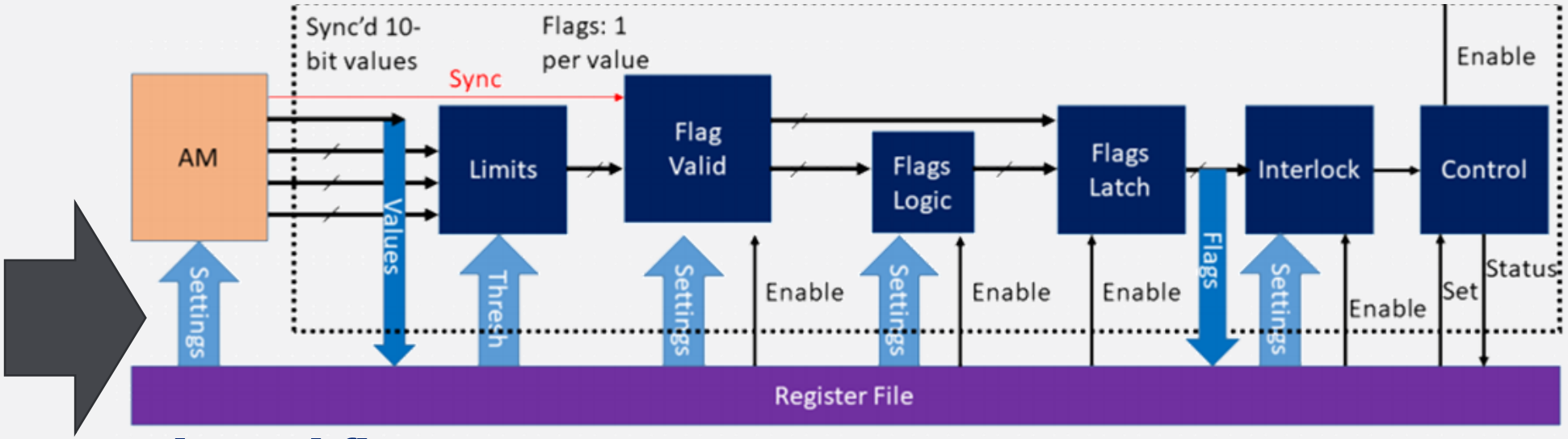
Interlock Channel



Interlock Switch Output

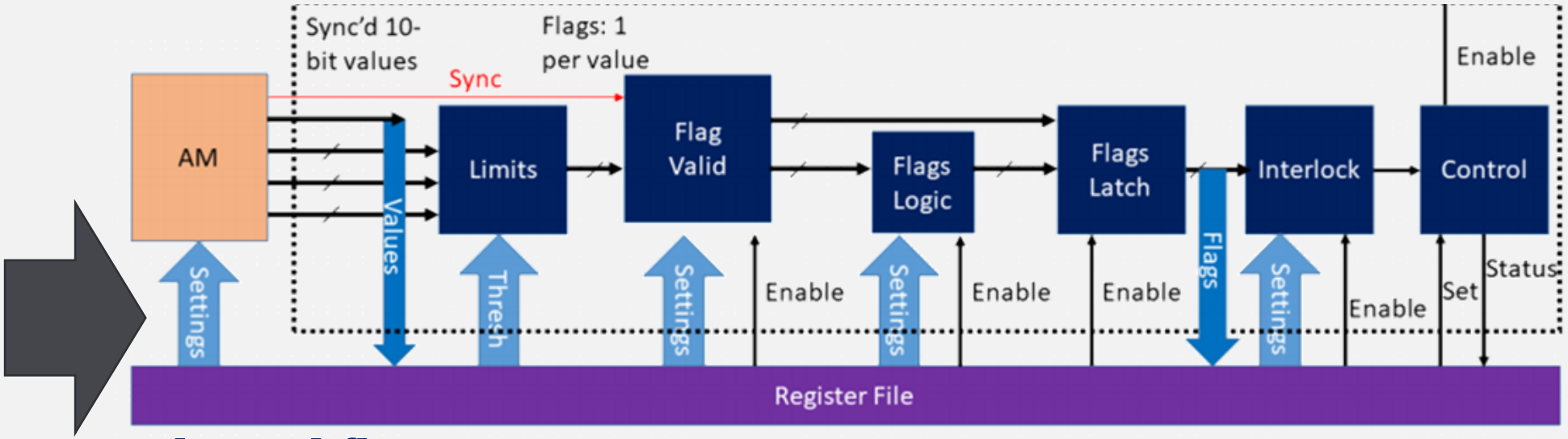
Example workflow:

Channel:	**Value.**
Hybrid X:	10°C
Hybrid Y:	−20°C
Power-board:	−20°C
Total Current:	200mA
…	…

Autonomous Monitor And Control (AMAC)

Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Channel



Interlock Switch Output

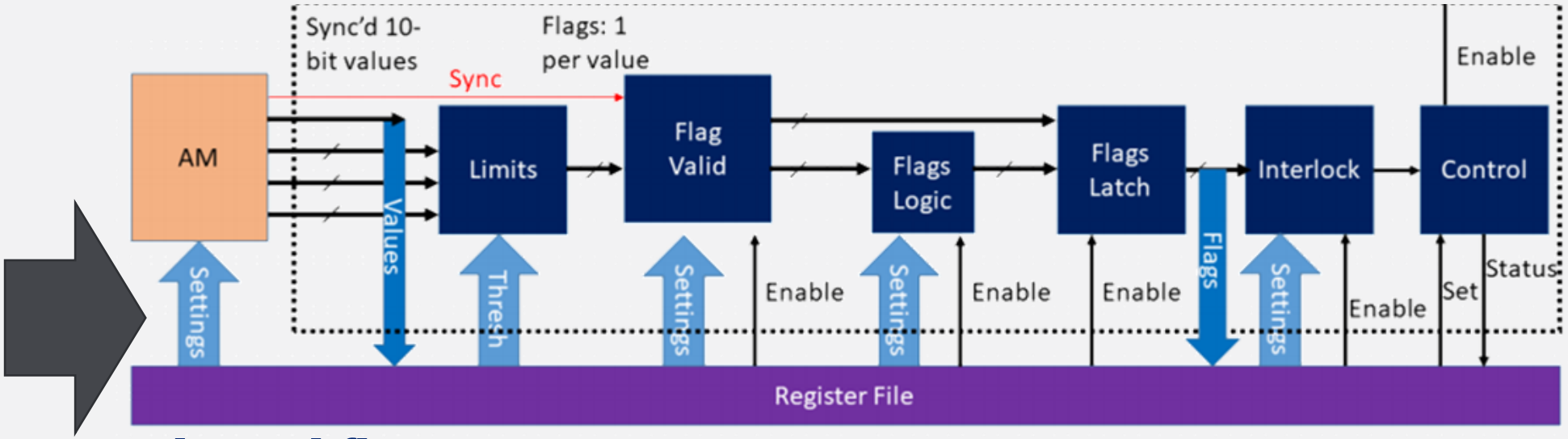
Example workflow:

Channel:	Value.	Check?
Hybrid X:	10°C	≤ -10°C?
Hybrid Y:	−20°C	≤ -10°C?
Power-board:	−20°C	≤ -10°C?
Total Current:	200mA	$\leq$ 150mA?
…	…	…

Autonomous Monitor And Control (AMAC)

Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Channel



Interlock Switch Output

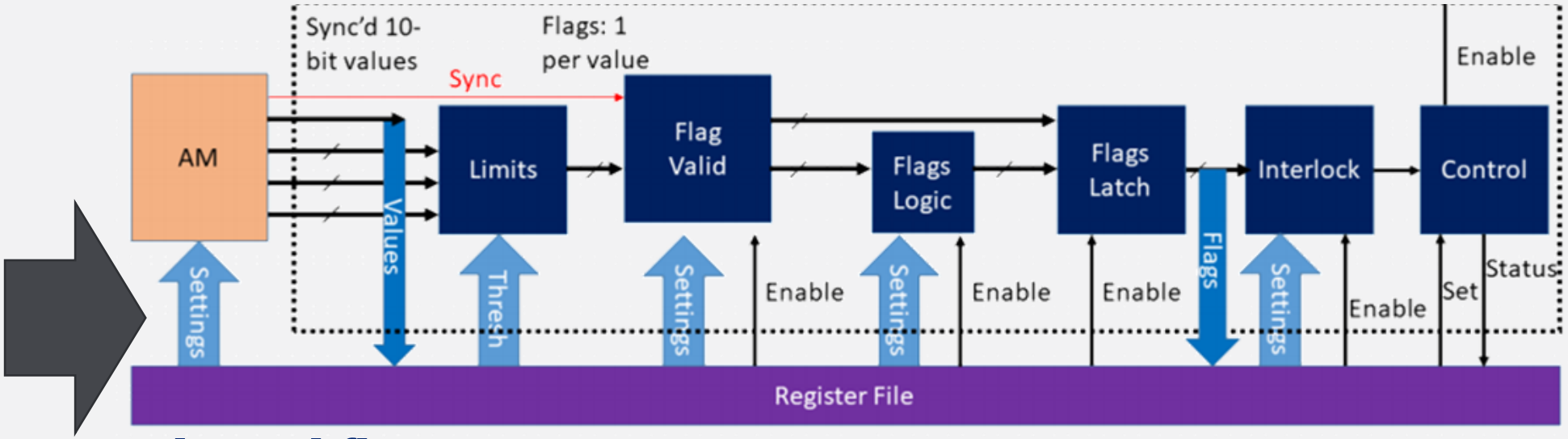
Example workflow:

Channel:	**Value.**	**Check?**
Hybrid X:	10°C	≤ -10°C?
Hybrid Y:	−20°C	≤ -10°C?
Power-board:	−20°C	≤ -10°C?
Total Current:	200mA	$\leq$ 150mA?
…	…	…

Autonomous Monitor And Control (AMAC)

Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Channel



Interlock Switch Output

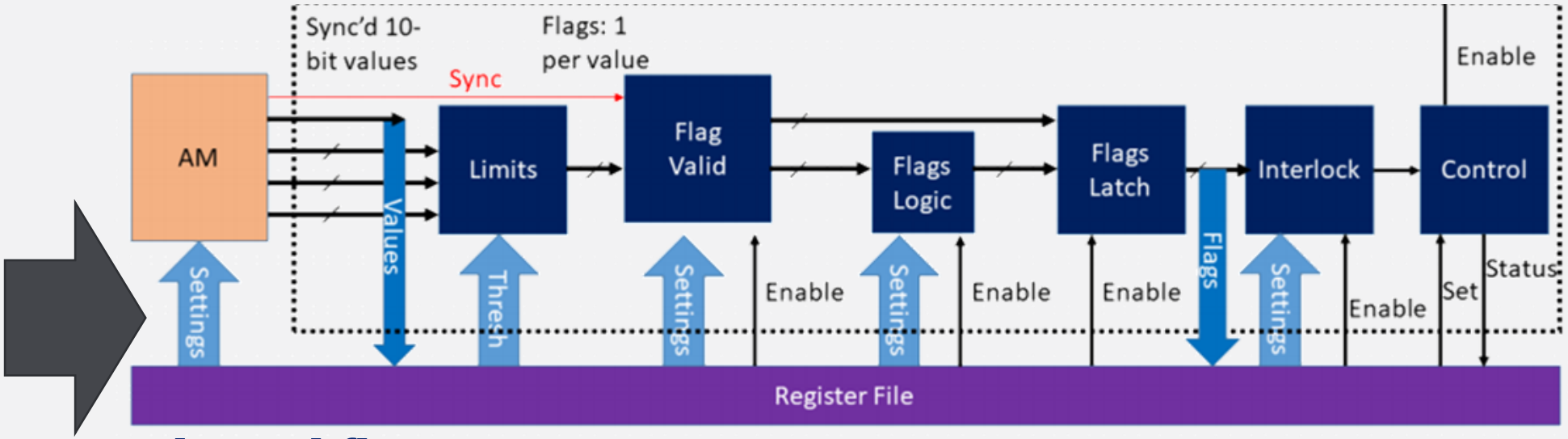
Example workflow:

Channel:	**Value.**	**Check?**	**Flag!**
Hybrid X:	10°C	$\leq -10°C$?	**High** Flag!
Hybrid Y:	−20°C	$\leq -10°C$?	No Flag.
Power-board:	−20°C	$\leq -10°C$?	No Flag.
Total Current:	200mA	$\leq 150mA$?	**High** Flag!
…	…	…	…

Autonomous Monitor And Control (AMAC)

Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Channel



Example workflow:

Channel:	Value.	Check?	Flag!
Hybrid X:	10°C	≤ −10°C?	**High** Flag!
Hybrid Y:	−20°C	≤ −10°C?	No Flag.
Power-board:	−20°C	≤ −10°C?	No Flag.
Total Current:	200mA	≤ 150mA?	**High** Flag!
…	…	…	…

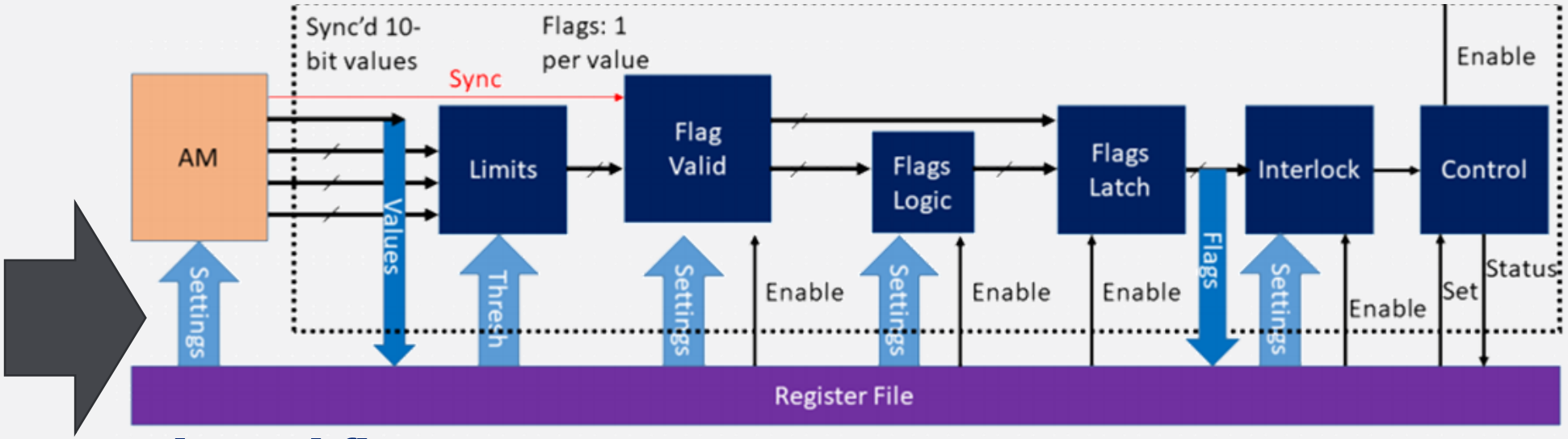
Latch flag to **register** for debugging and analysis…

Interlock Switch Output

Autonomous Monitor And Control (AMAC)

Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Channel



Interlock Switch Output

Example workflow:

Channel:	Value.	Check?	Flag!
Hybrid X:	10°C	≤ −10°C?	**High** Flag!
Hybrid Y:	−20°C	≤ −10°C?	No Flag.
Power-board:	−20°C	≤ −10°C?	No Flag.
Total Current:	200mA	≤ 150mA?	**High** Flag!
…	…	…	…

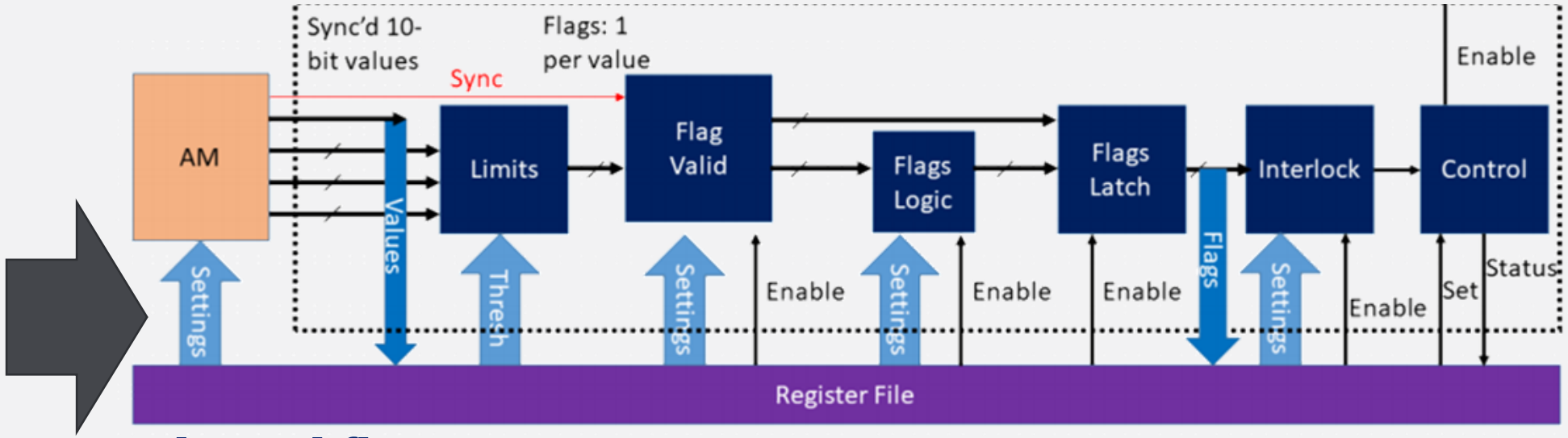
Latch flag to **register** for debugging and analysis…

Move the **interlock state** from **ON** to **LOCK**

Autonomous Monitor And Control (AMAC)

Analog to Digital Converter
(16 Multiplexer Channel)

Interlock Channel



Interlock Switch Output

Example workflow:

Channel:	**Value.**	**Check?**	**Flag!**
Hybrid X:	10°C	$\leq -10°C$?	**High** Flag!
Hybrid Y:	$-20°C$	$\leq -10°C$?	No Flag.
Power-board:	$-20°C$	$\leq -10°C$?	No Flag.
Total Current:	200mA	$\leq$ 150mA?	**High** Flag!
…	…	…	…

Latch flag to **register** for debugging and analysis…

Move the **interlock state** from **ON** to **LOCK**

Turn All **Hybrid X ASICs** to Low-Power Mode!

Radiation Hard Design
Single Event Effects & Triple Module Redundancy

*"A **single event upset** in the flight computers of this Airbus A330 during Qantas Flight 72 on 7 October 2008 is suspected to have resulted in an aircraft upset that nearly ended in a crash after the computers experienced several malfunctions."* ***Rare event in aviation and daily life, but extremely common in particle collider!***

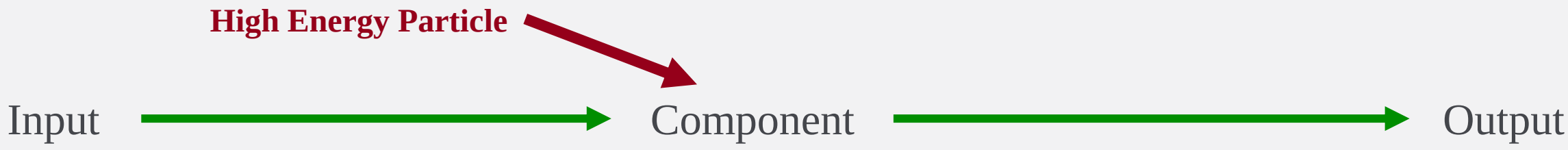
Triple Module Redundancy against SEU & SET

Triple Module Redundancy against SEU & SET

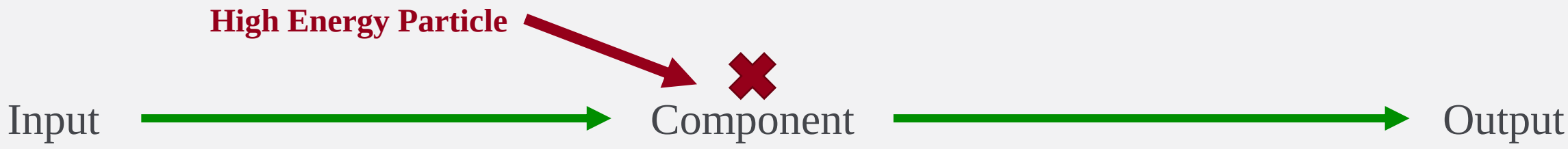
Triple Module Redundancy against SEU & SET

High Energy Particle

Triple Module Redundancy against SEU & SET



Triple Module Redundancy against SEU & SET



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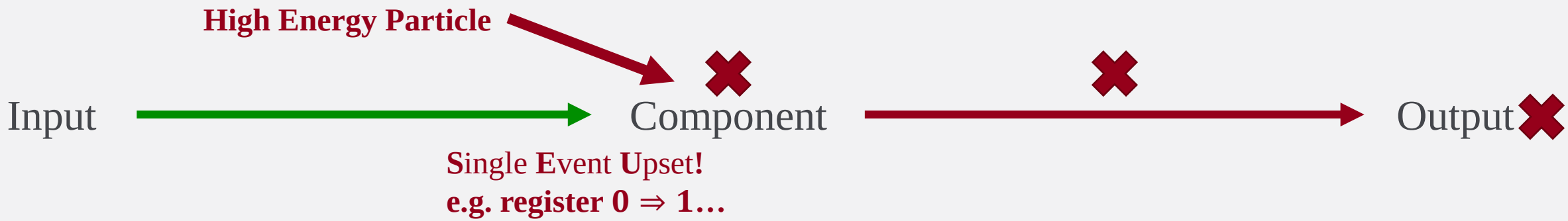
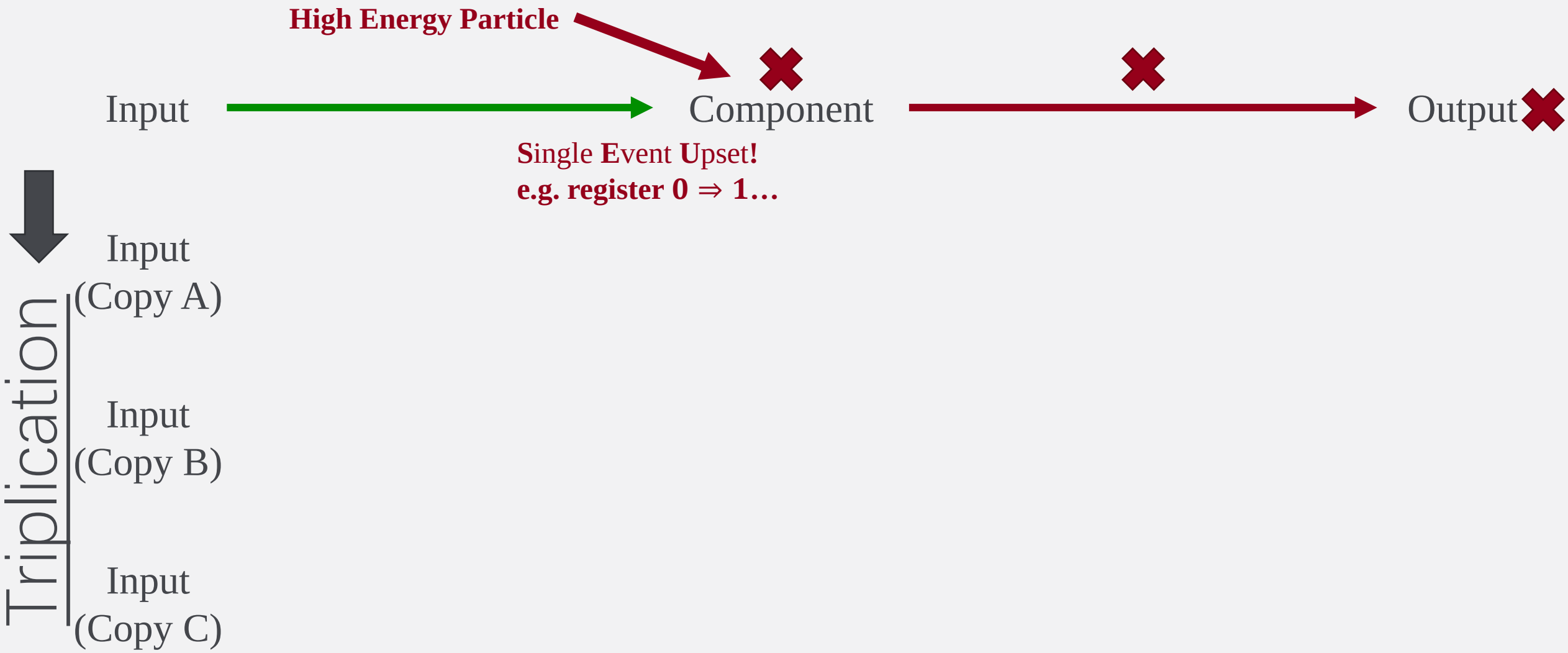


Triplication

Triple Module Redundancy against SEU & SET



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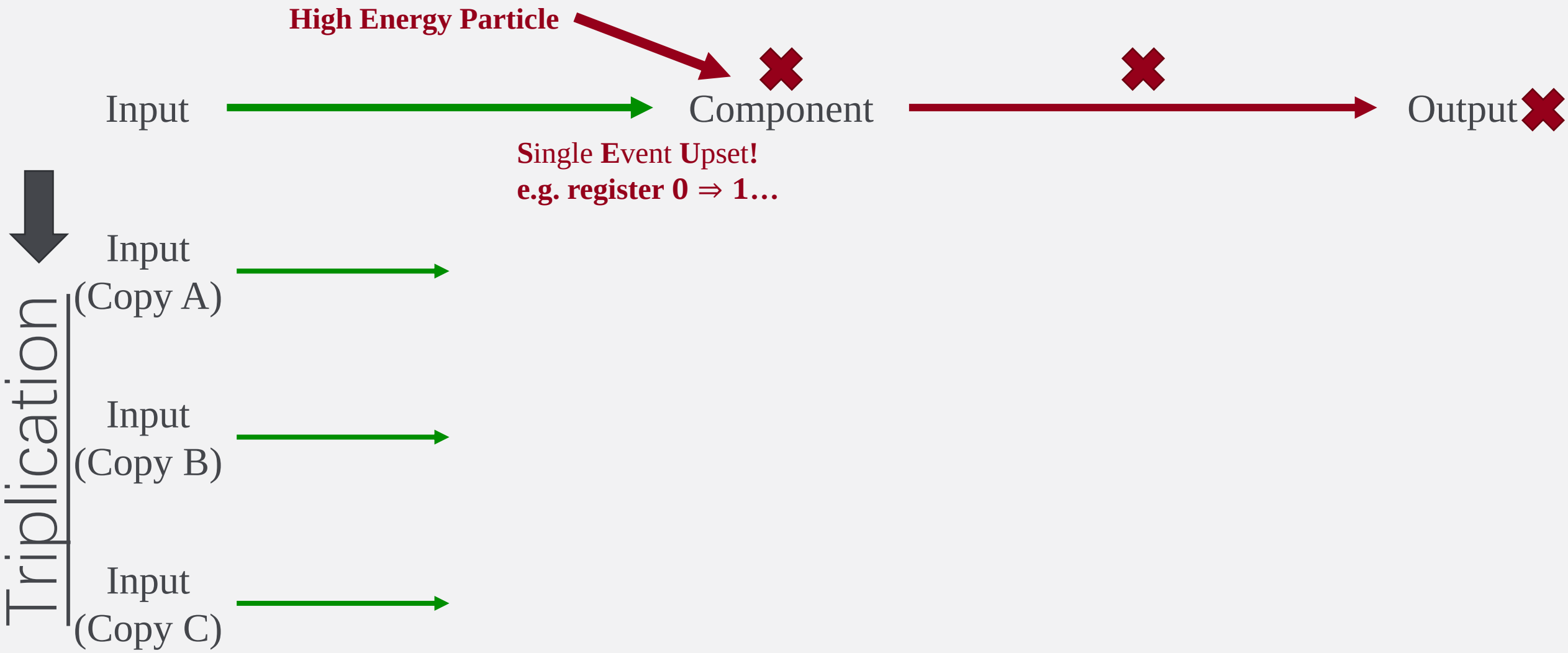

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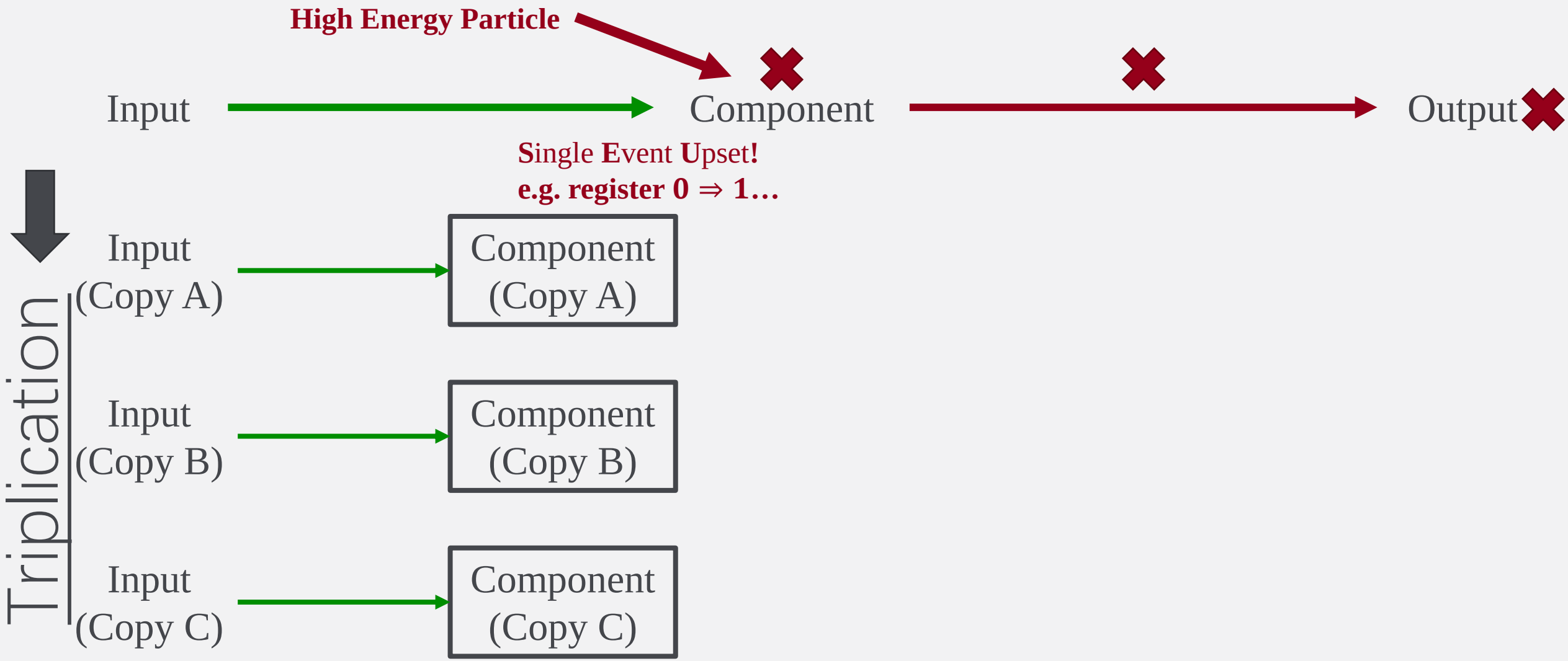

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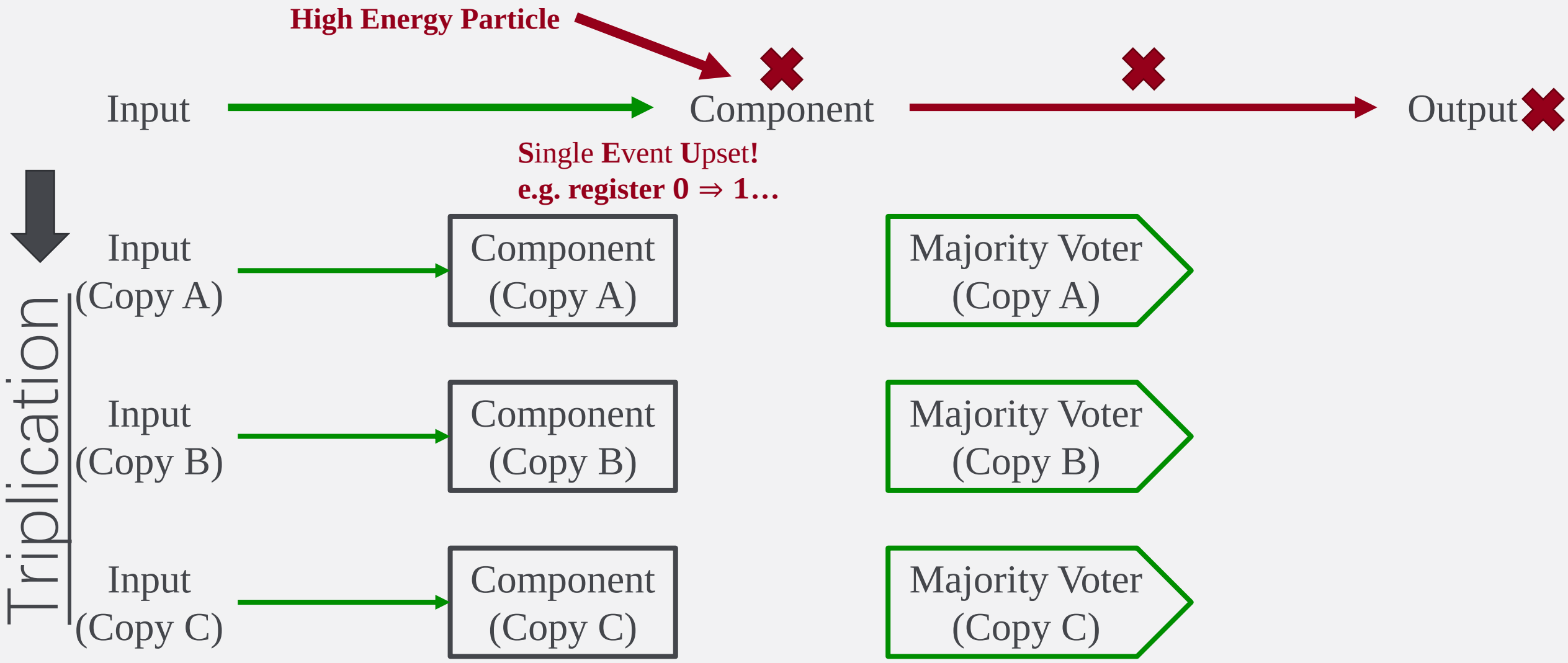

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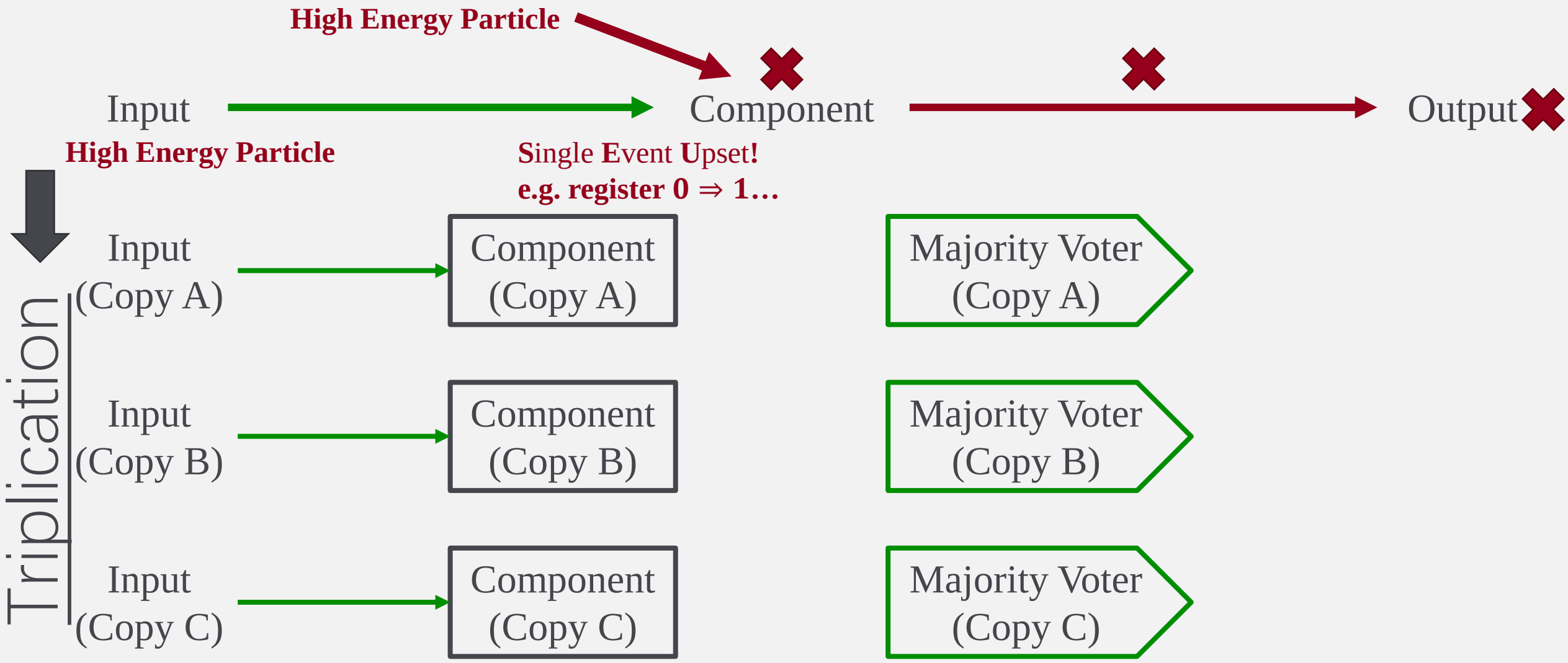

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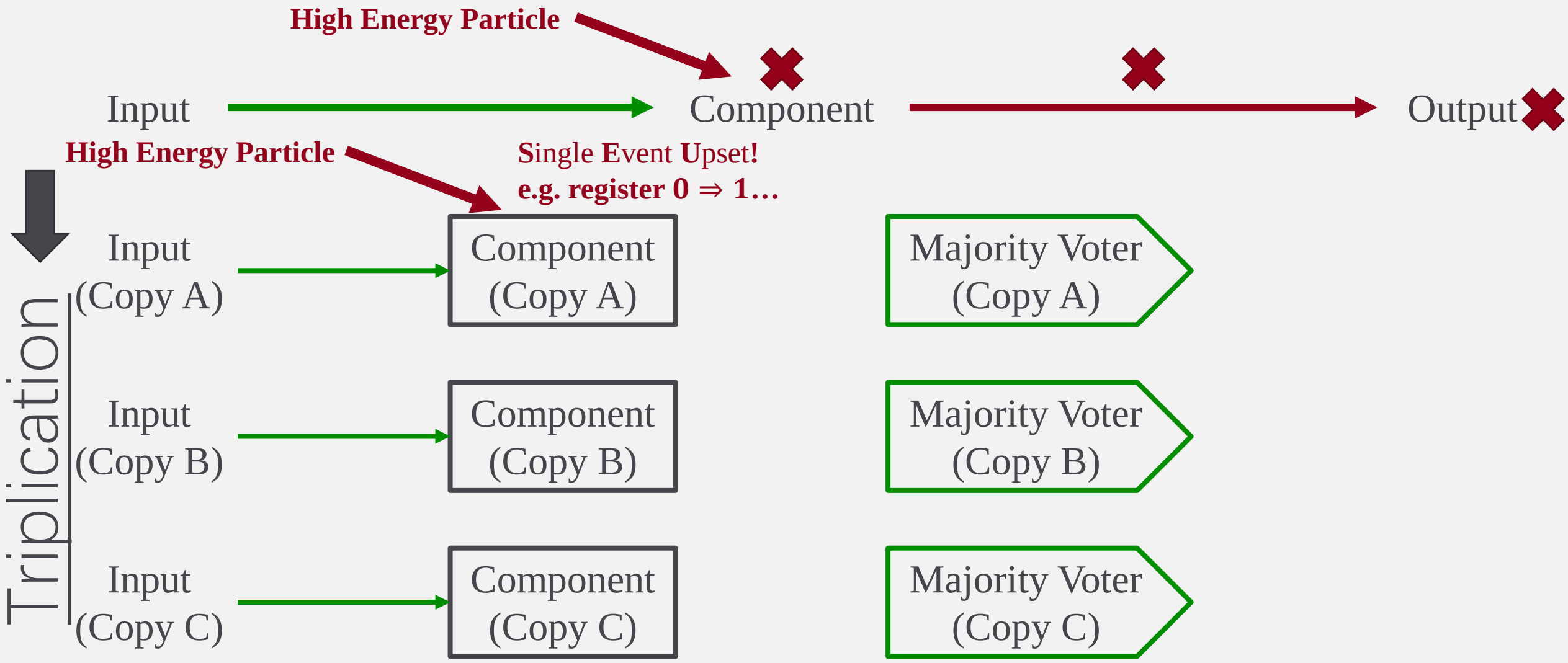

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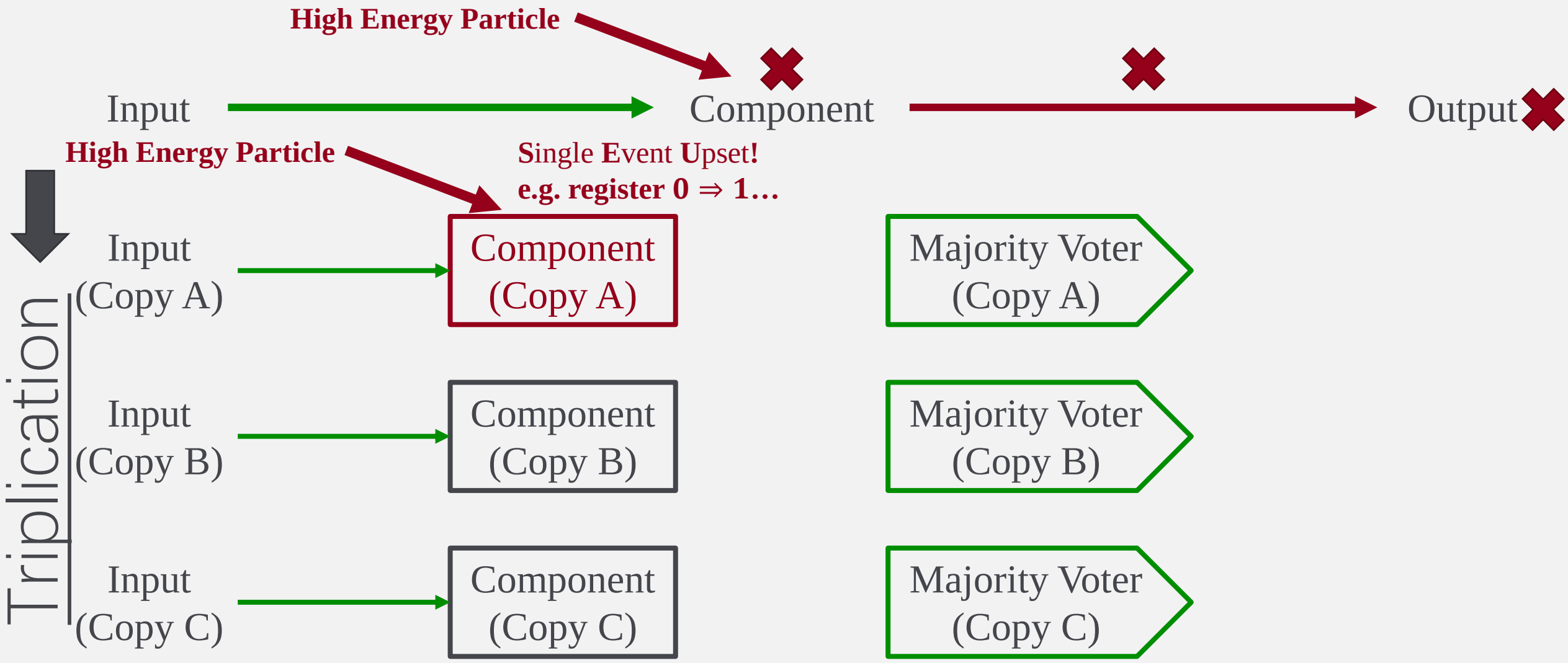

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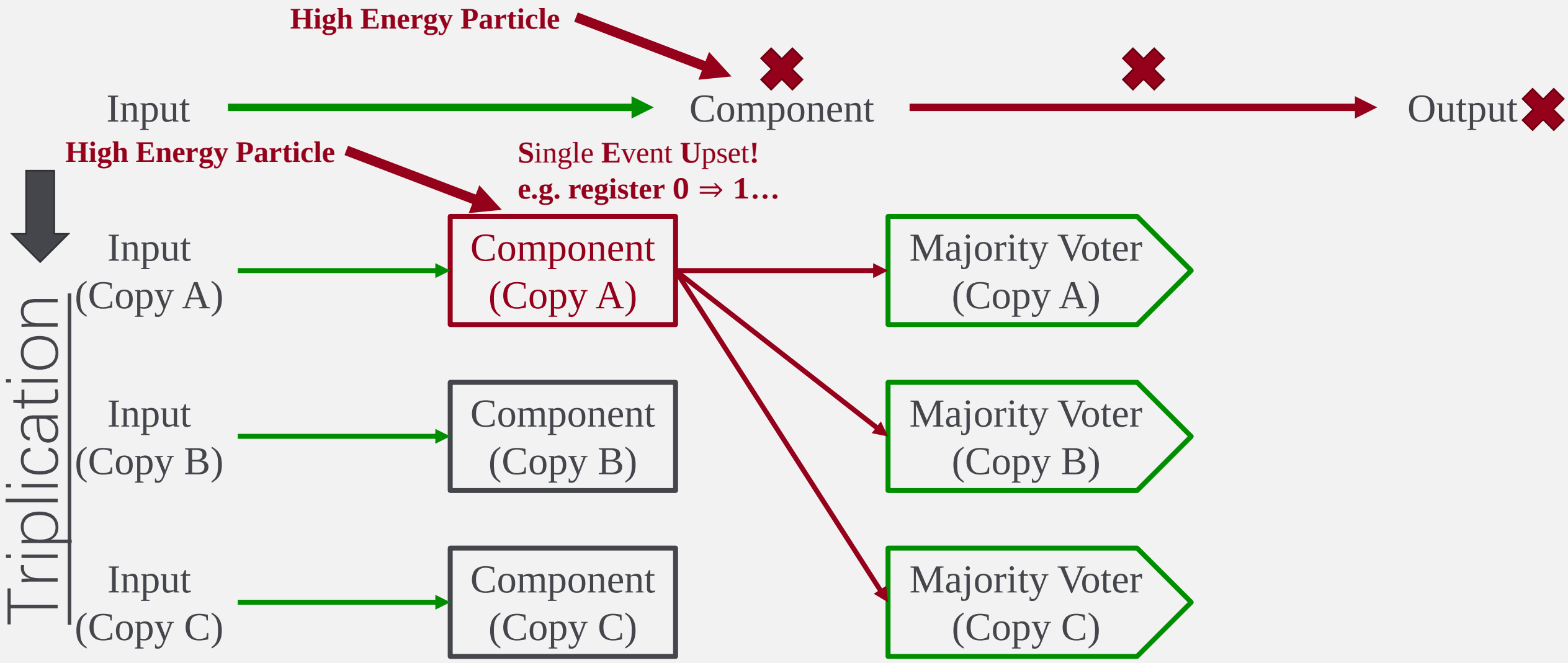

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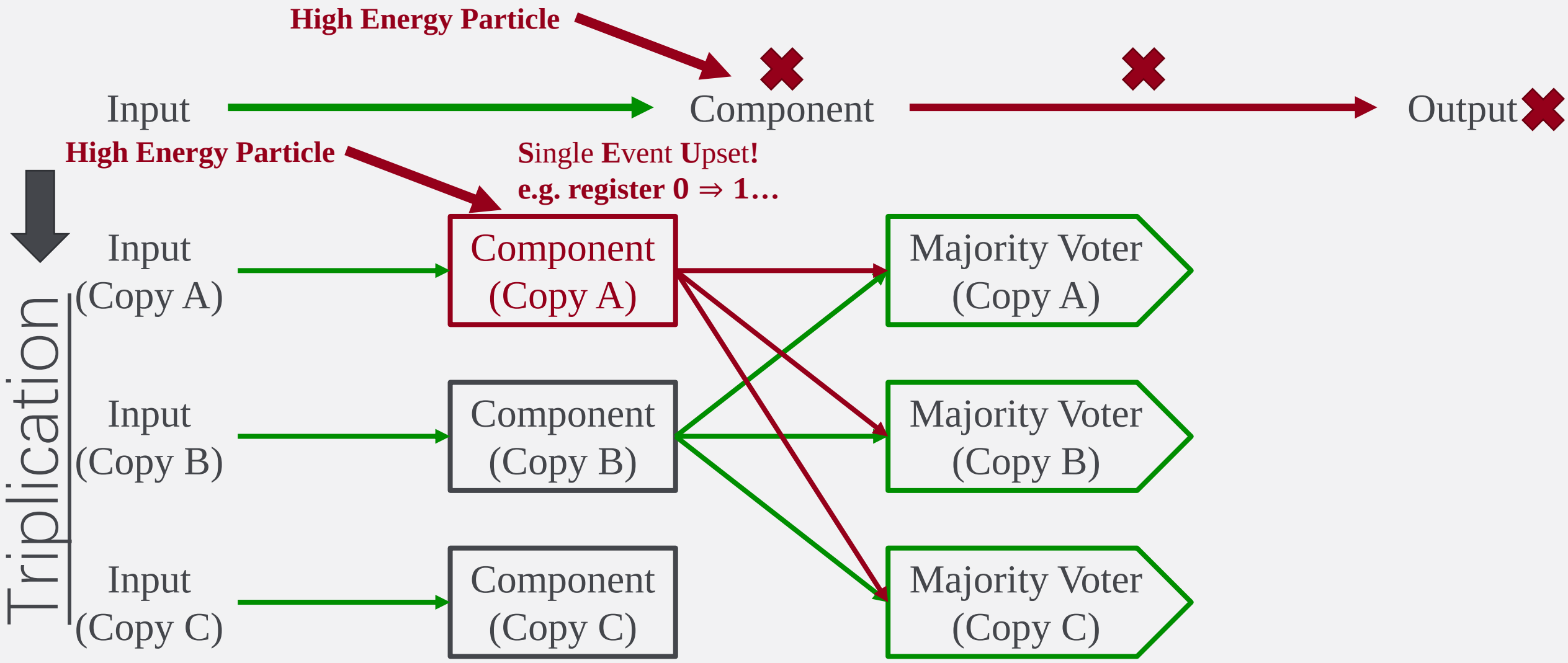

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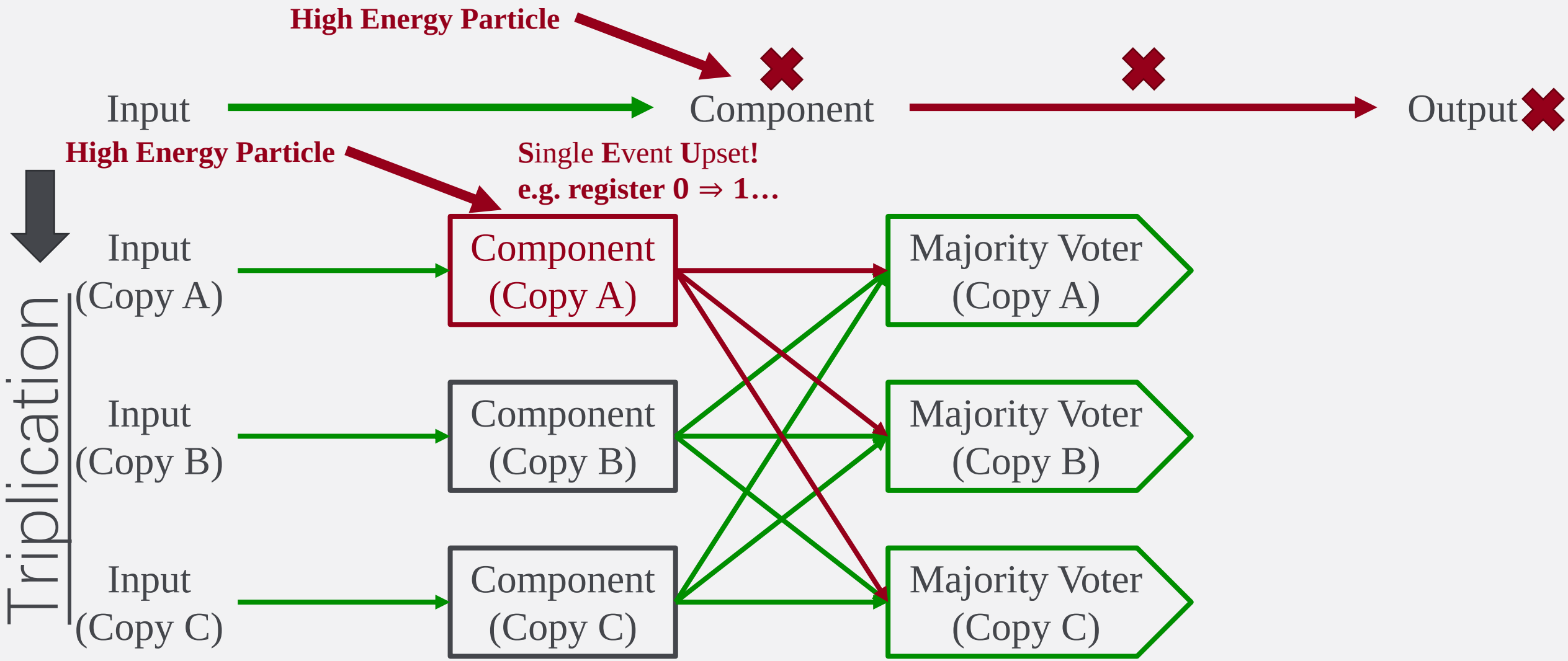

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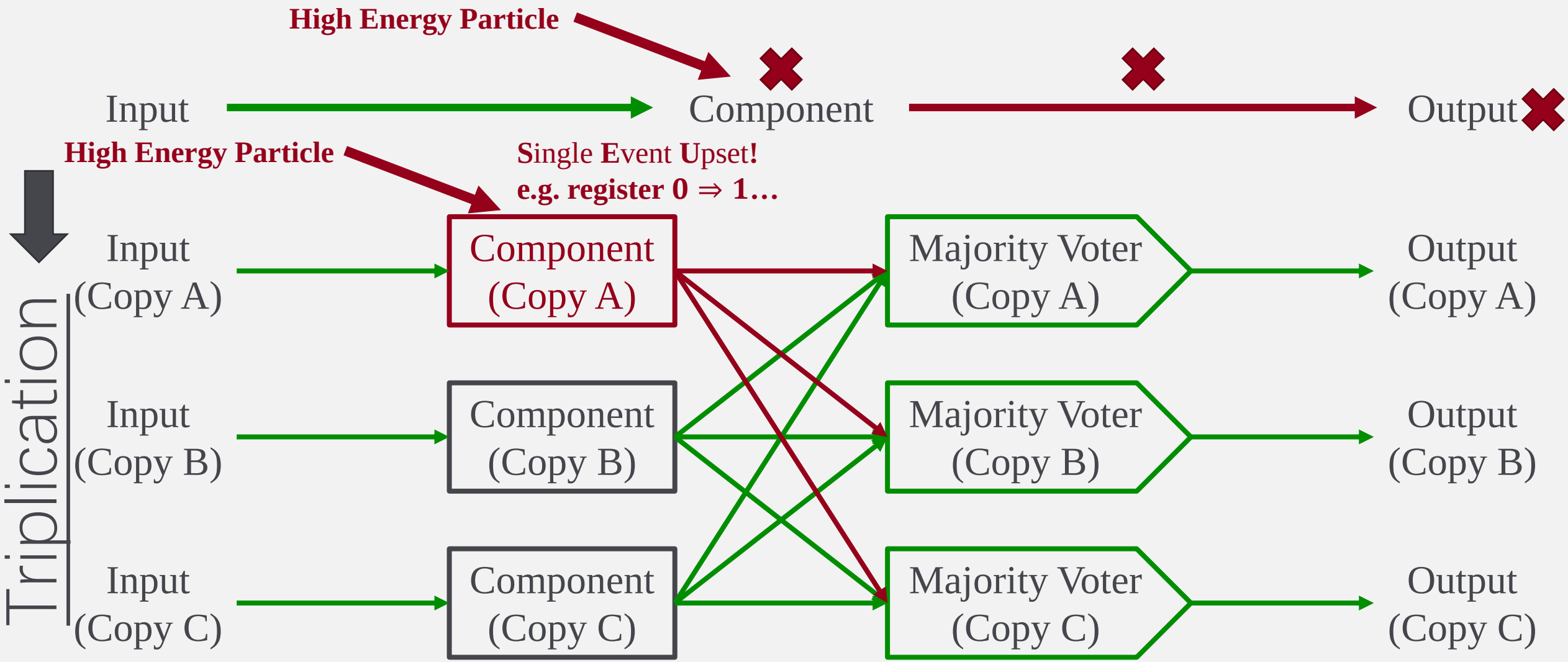


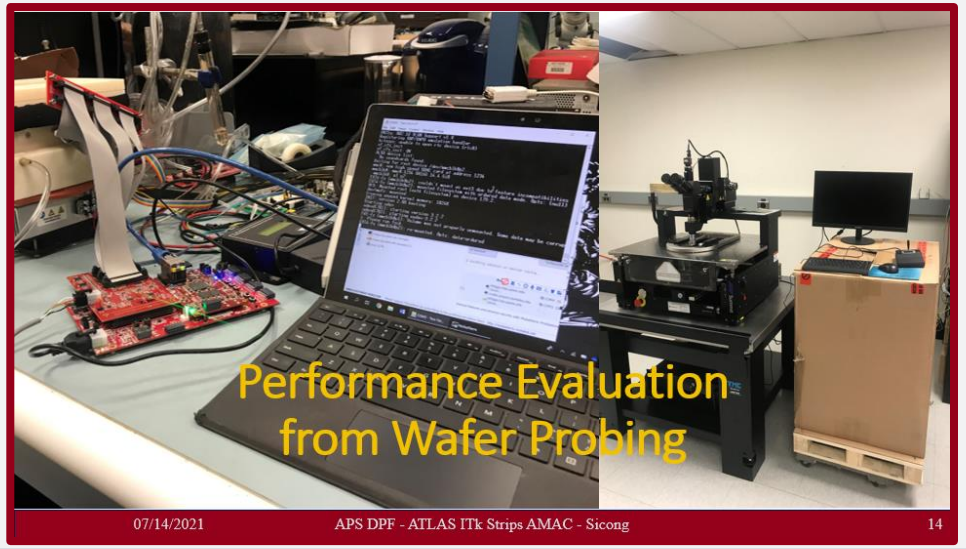
Design Verification: Digital vs Analog

- Digital Logic Block:
  - i) Many revision and updated design version;
  - ii) Relatively independent of the manufacturing;
  - iii) Functions mostly internal;
  - iv) Many scenarios/combinations to be considered!

1010
1010 → **Simulate**

- Analog Block:
  - i) Design relatively fixed;
  - ii) Parameters heavily dependent on manufacturing;
  - iii) Needs a real set-up with external devices;
  - iv) Data needed for each chip!

→ **Probe & Fit**



AMAC Verification based on **cocotb**

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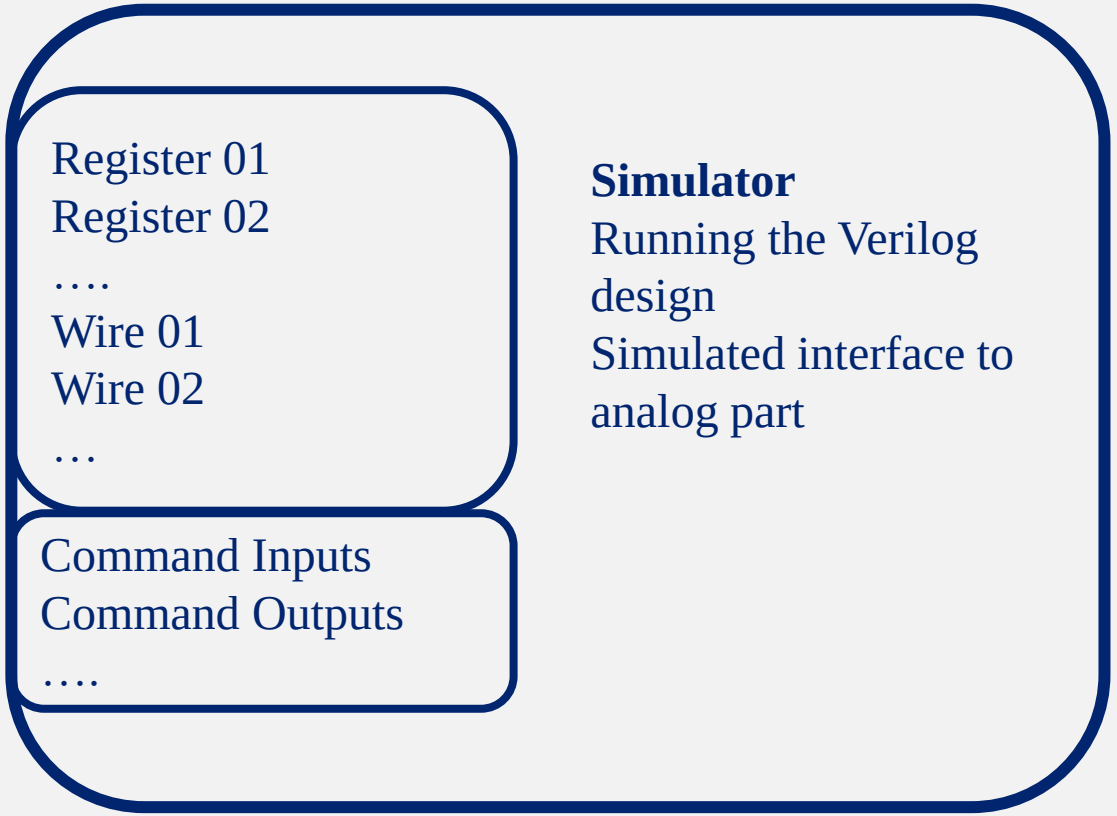

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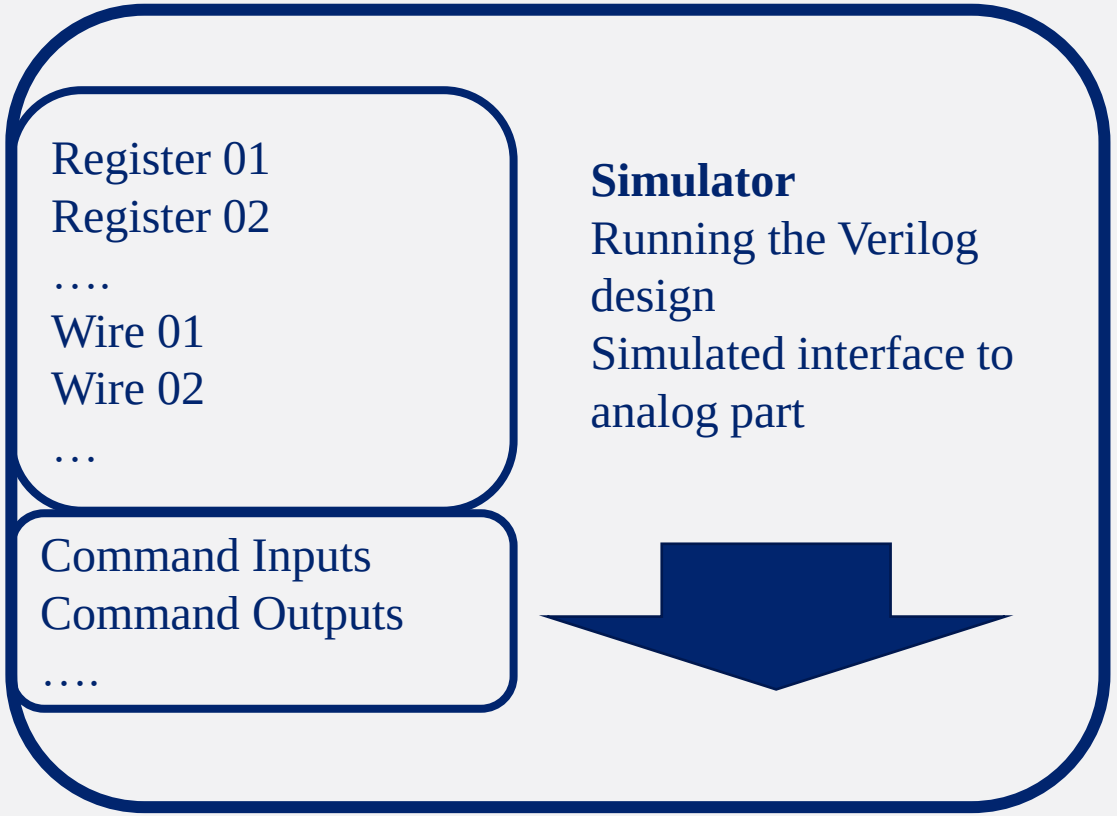

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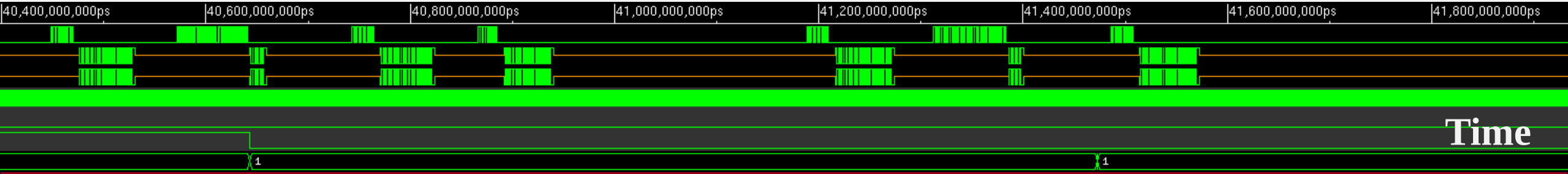
Register 01
Register 02
….
Wire 01
Wire 02
…

Command Inputs
Command Outputs
….

Simulator
Running the Verilog design
Simulated interface to analog part



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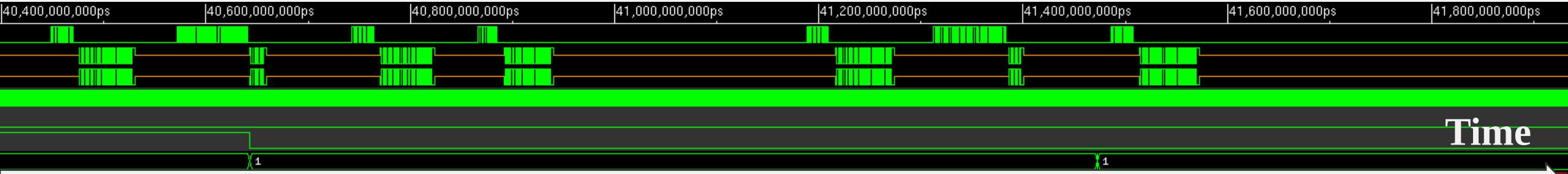

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cocotb.test1

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Wire 01
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Command Inputs
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….

Simulator
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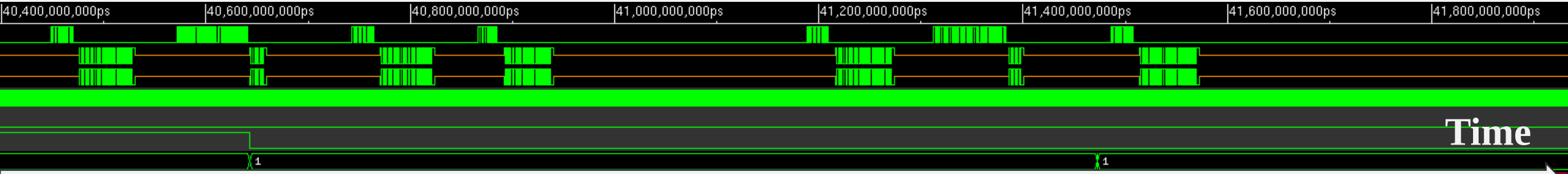

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cocotb.test1

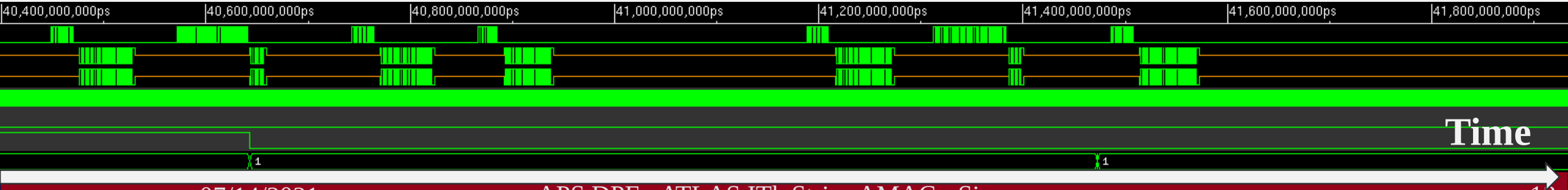
Running Consecutively

cocotb.test2

Register 01
Register 02
….
Wire 01
Wire 02
…

Command Inputs
Command Outputs
….

Simulator
Running the Verilog design
Simulated interface to analog part



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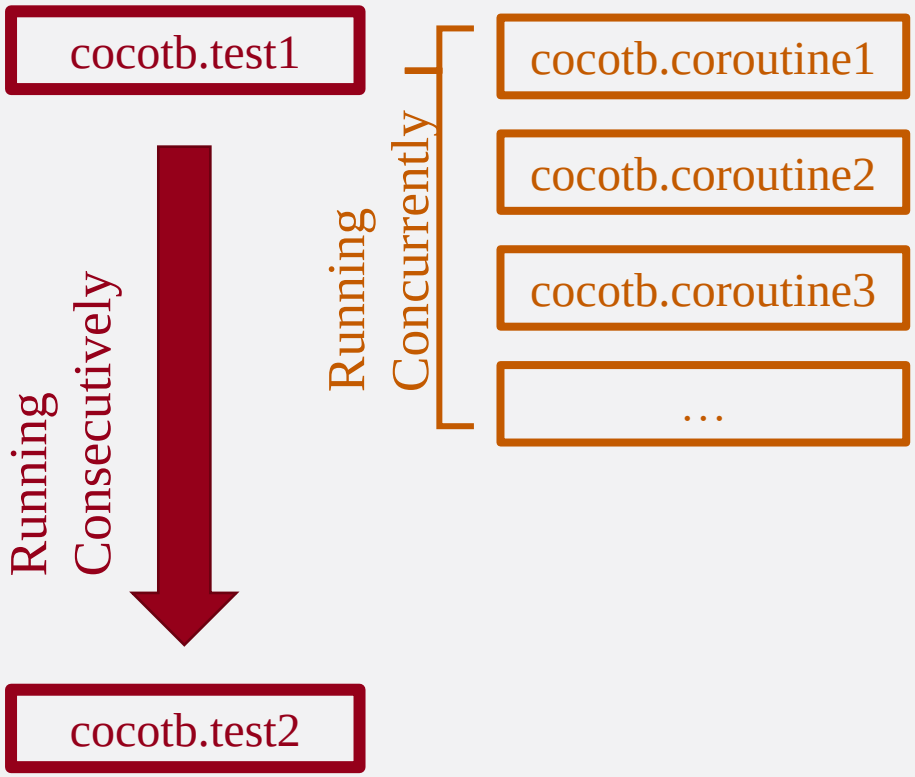

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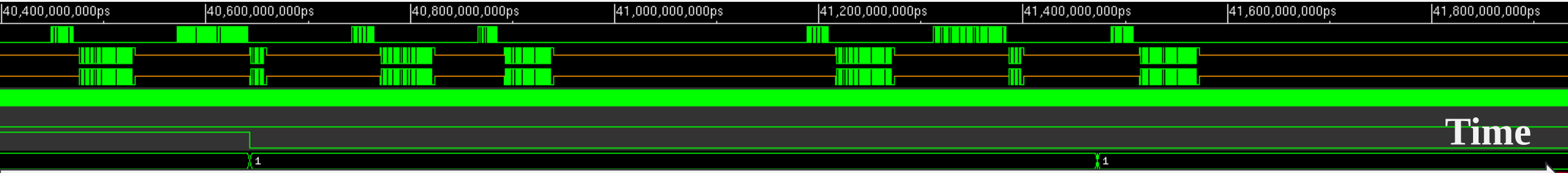

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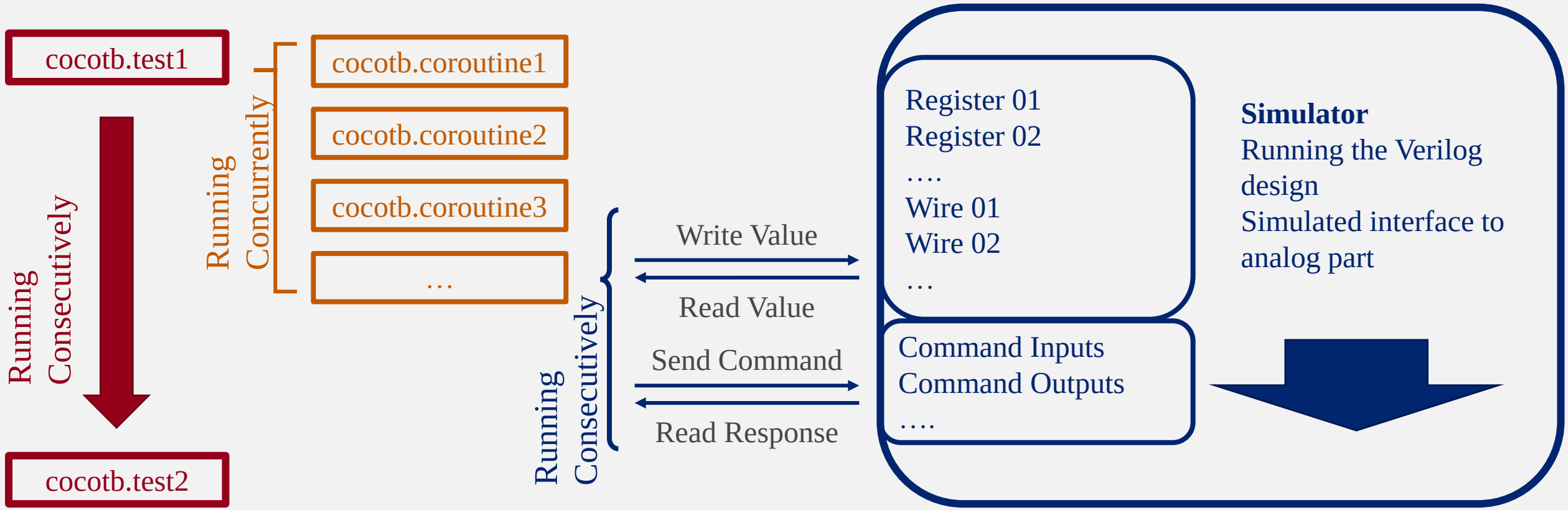

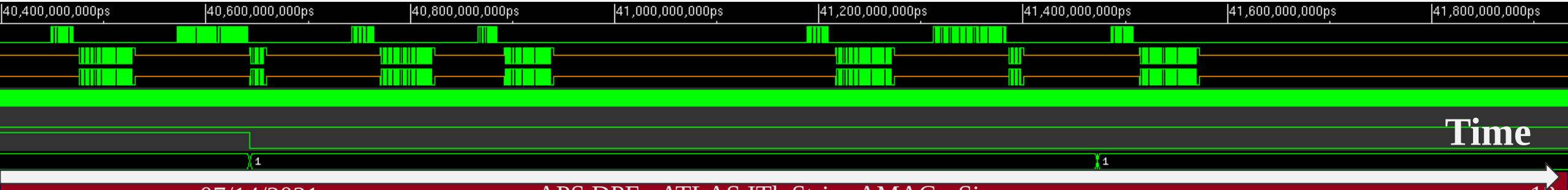

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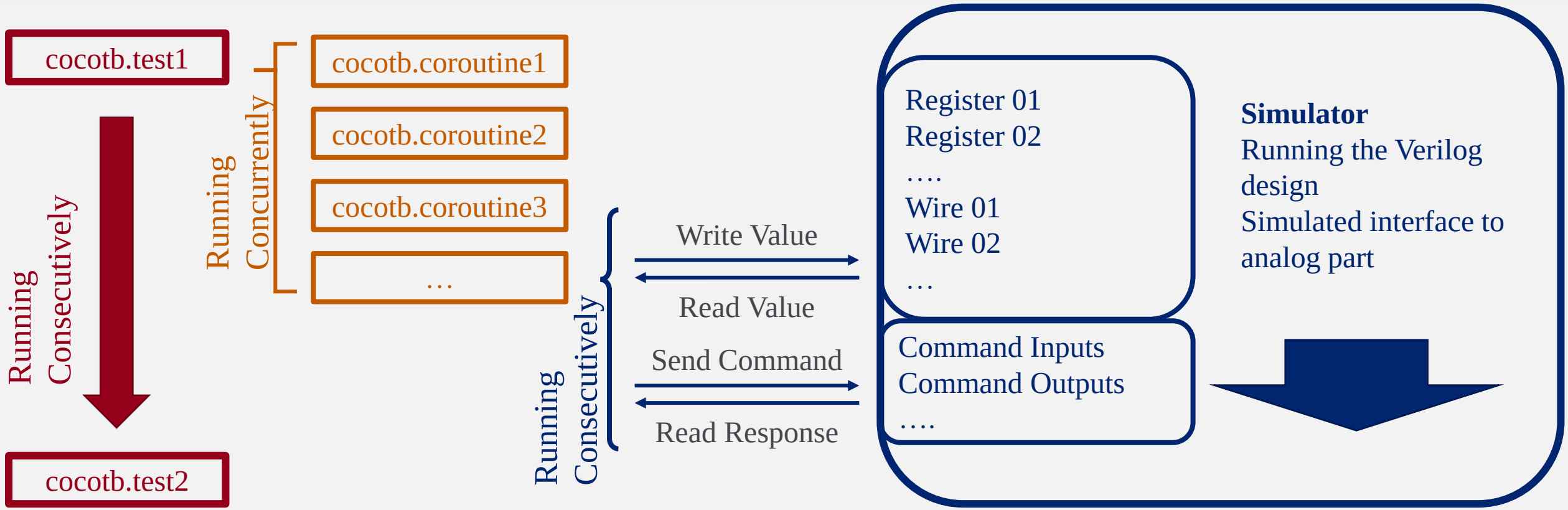

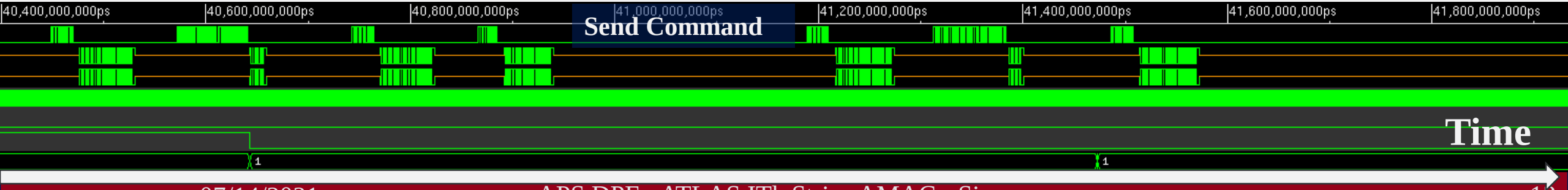

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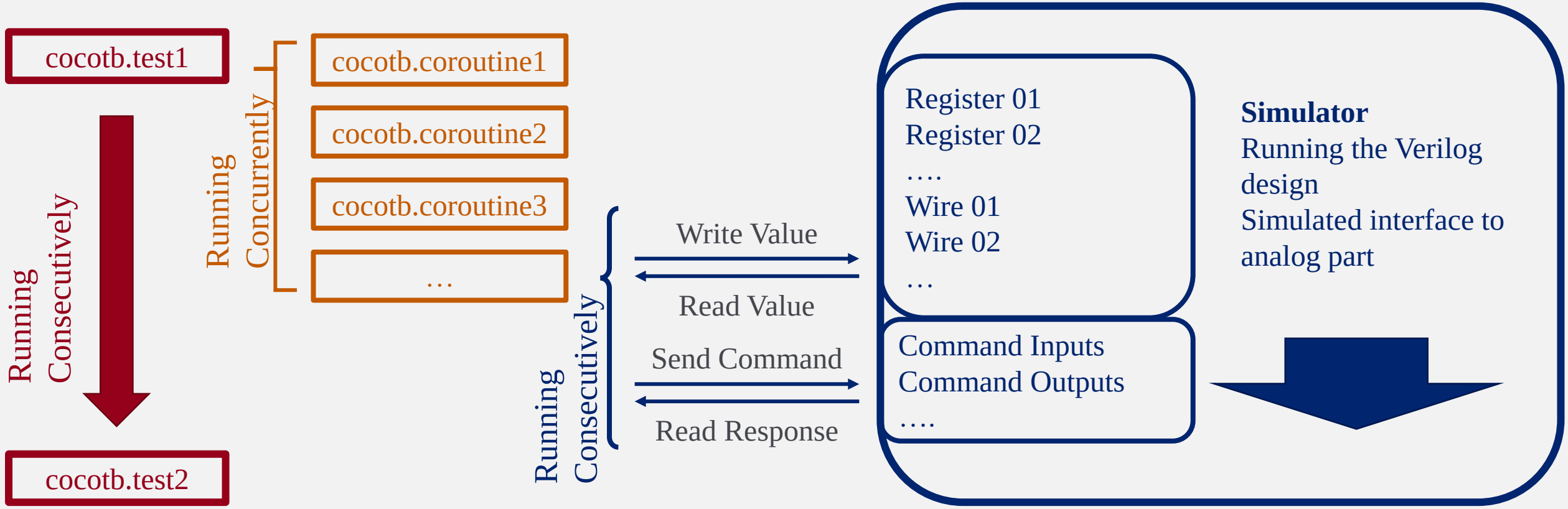

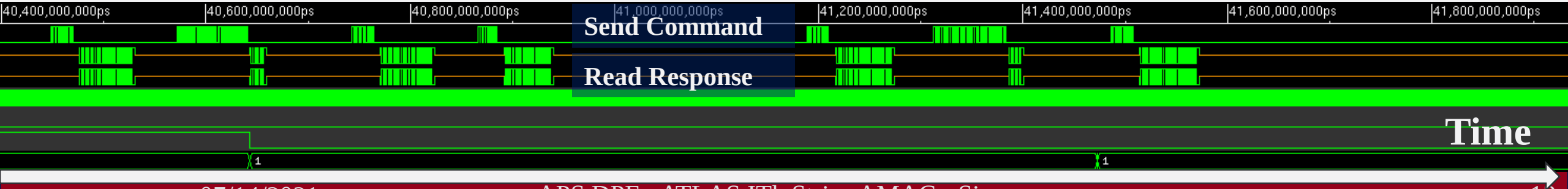

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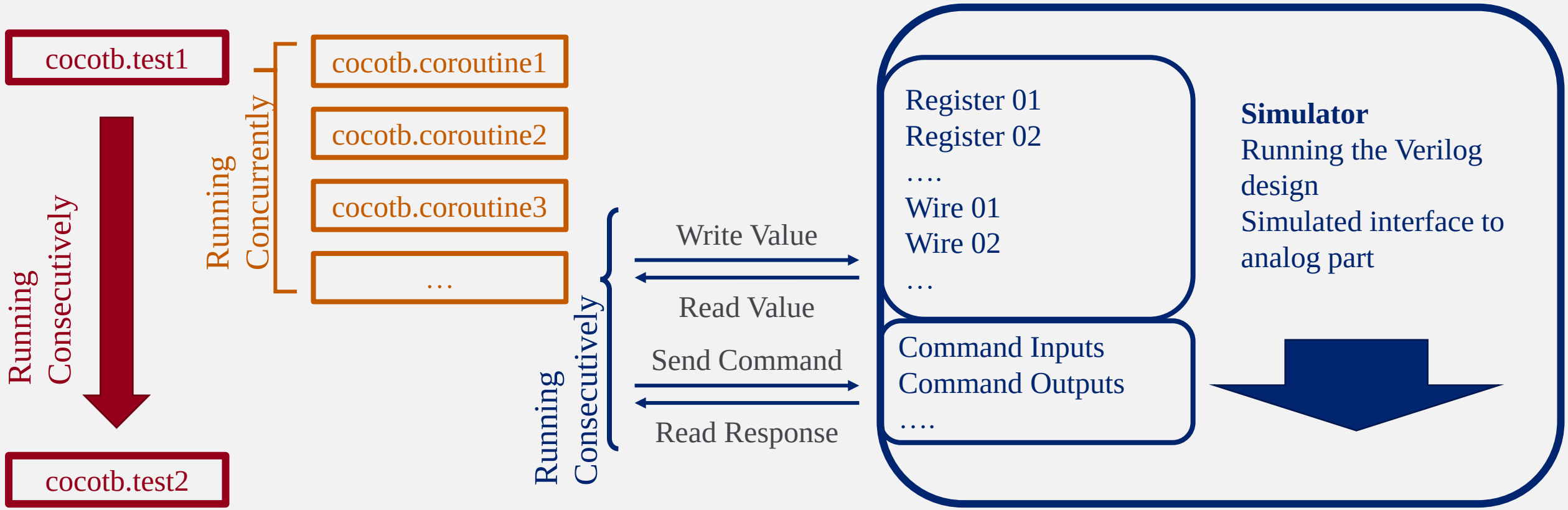

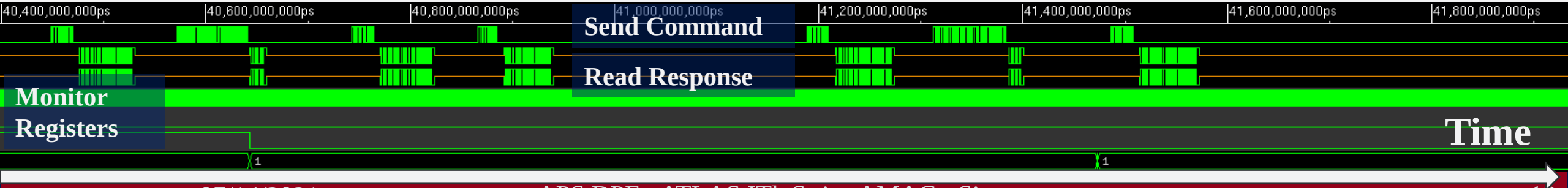

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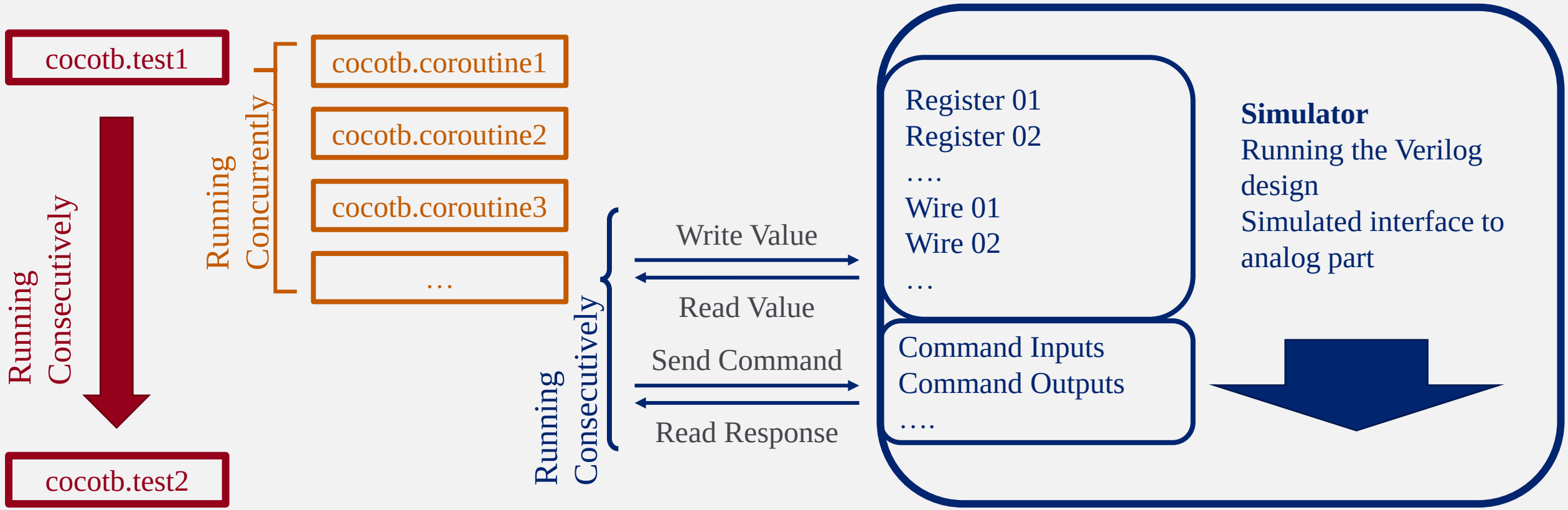
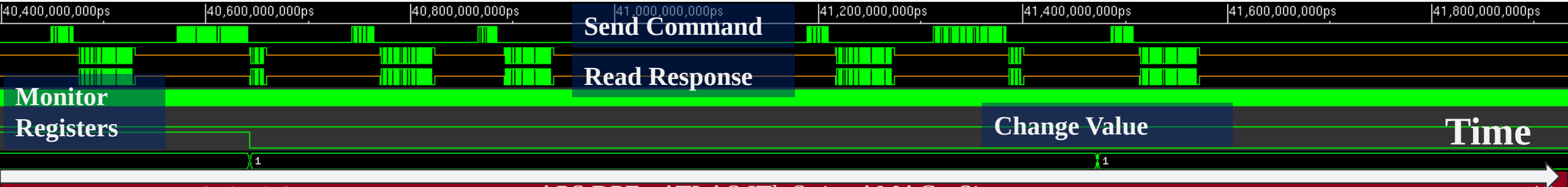
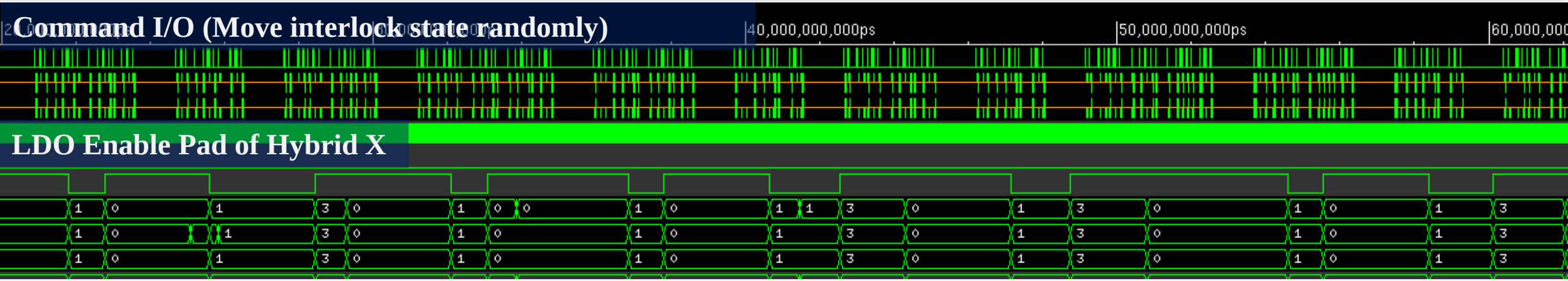




Example Test Routine (Interlock Toggling under single SEU blast)



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  - Simulate the interlock move conditions by commands
  - Verify that the resulting interlock states are correct
- **Coroutine #2:**
  - Continuously inflict random **S**ingle **E**vent **U**pset on any register in related interlock channel
- Note that the **triplicated** register correct themselves!

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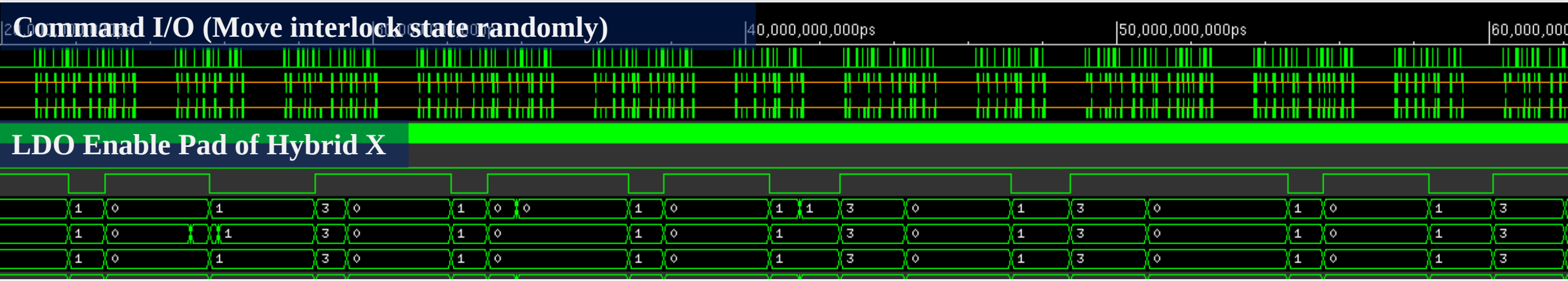

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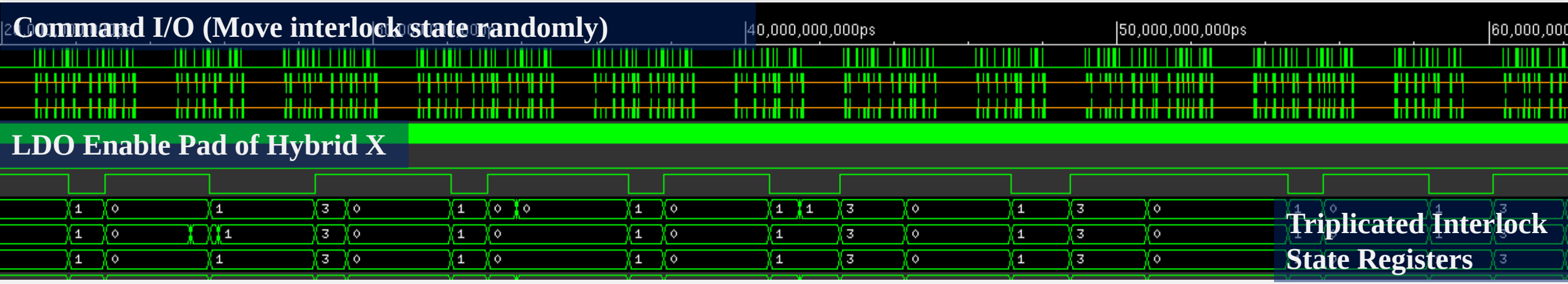

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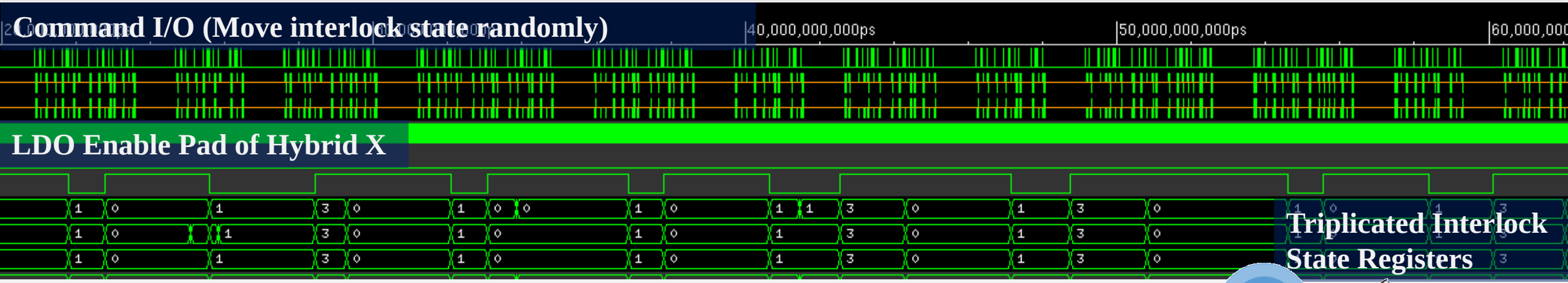

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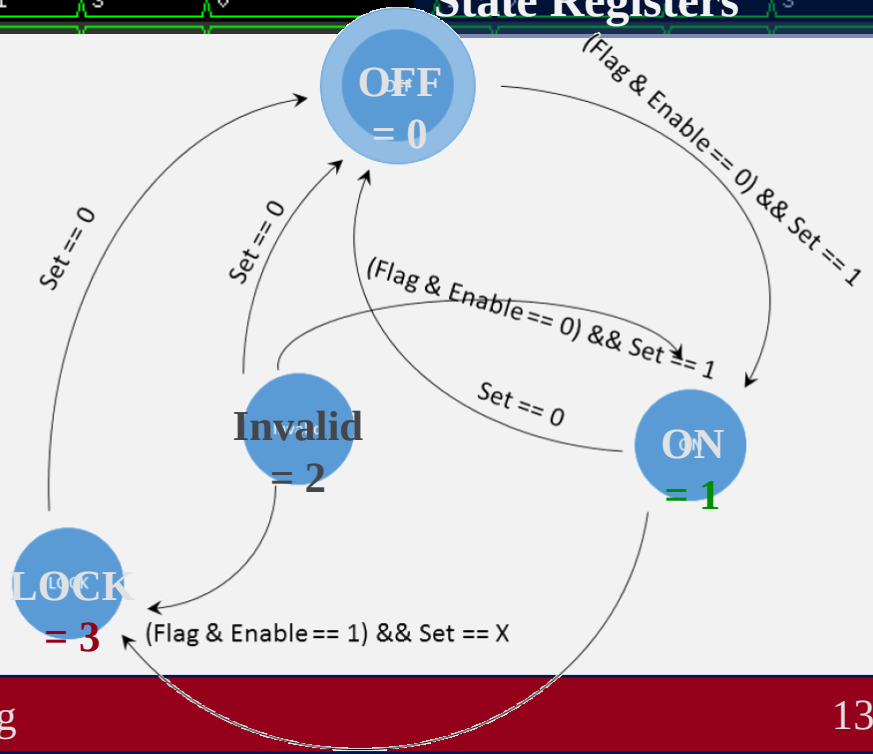

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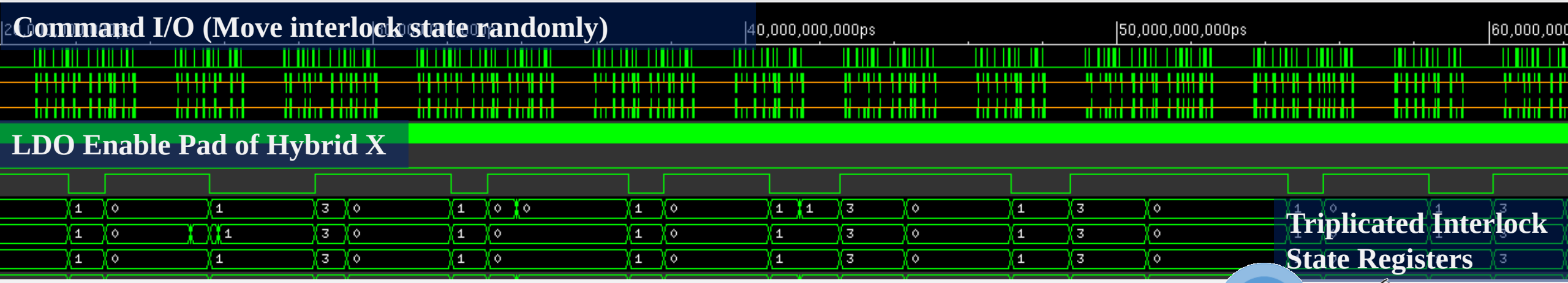

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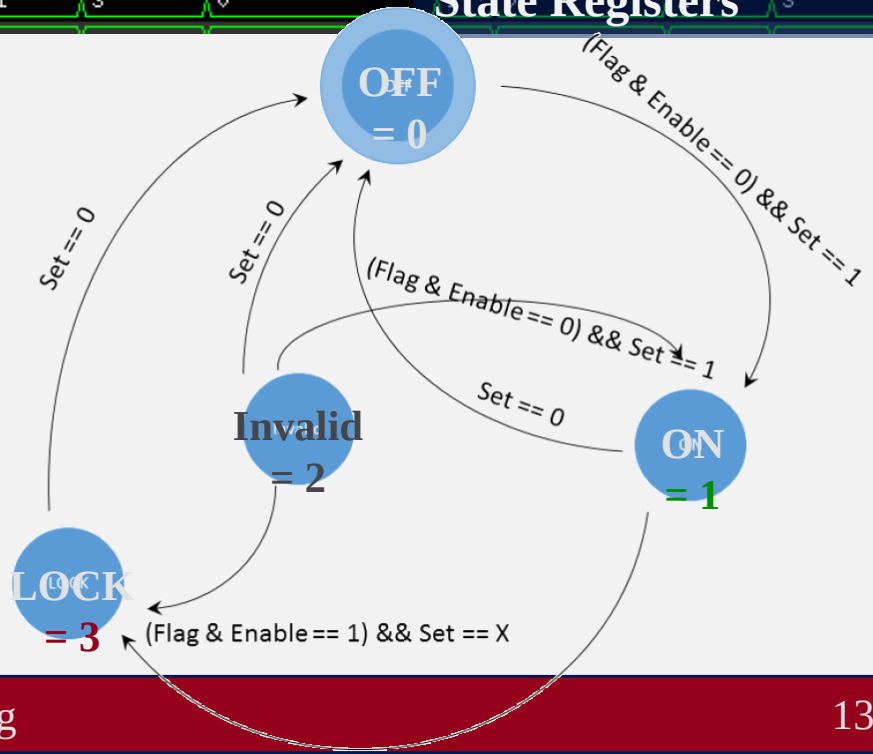

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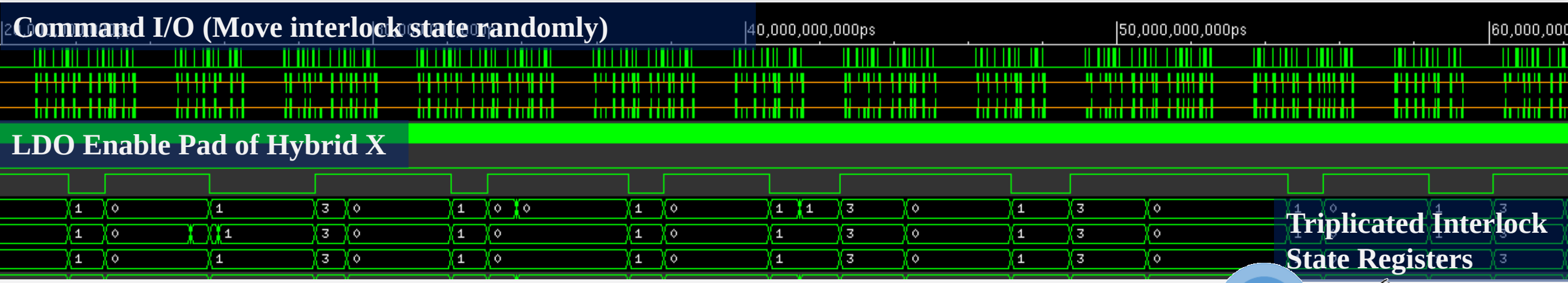

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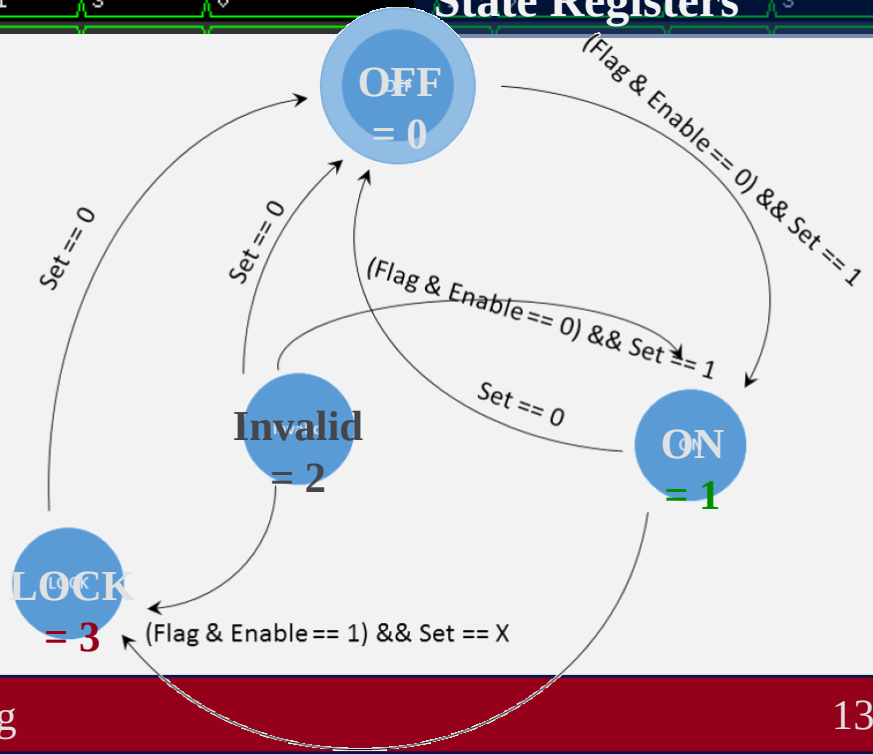

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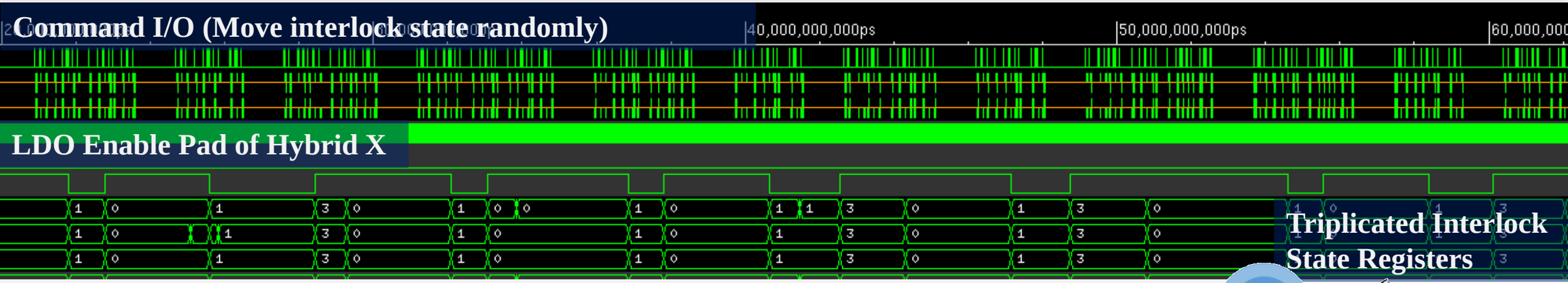

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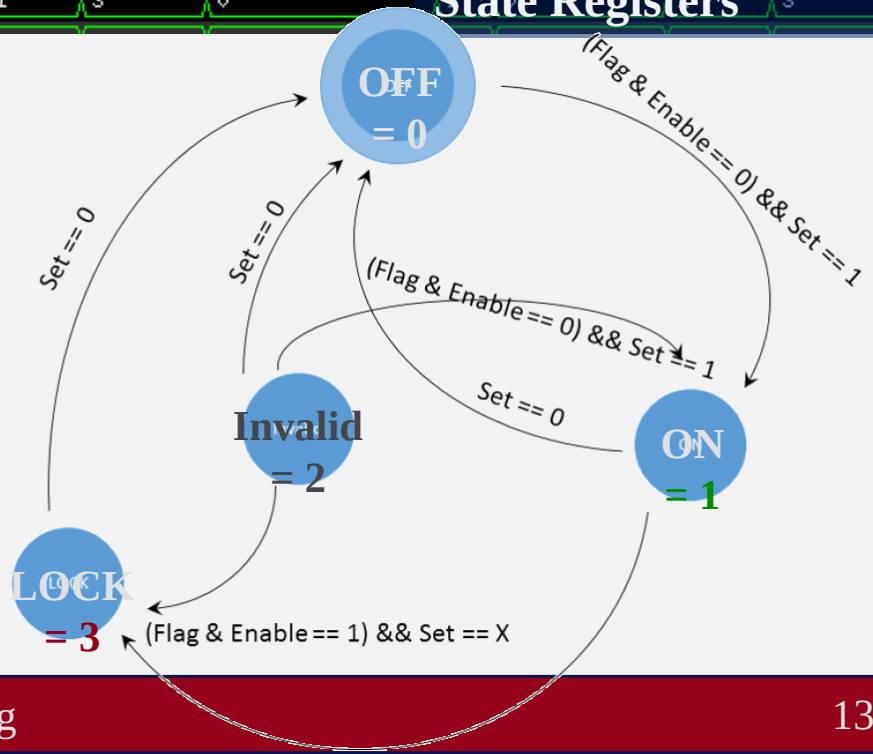

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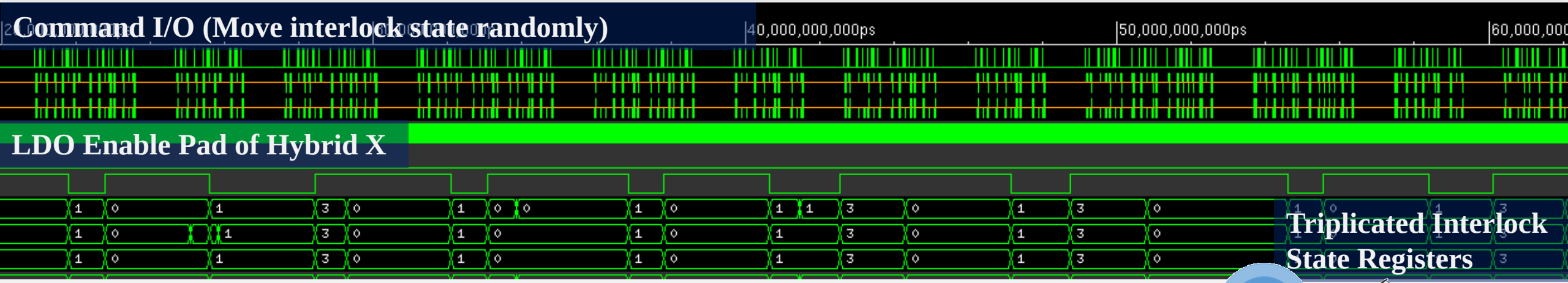

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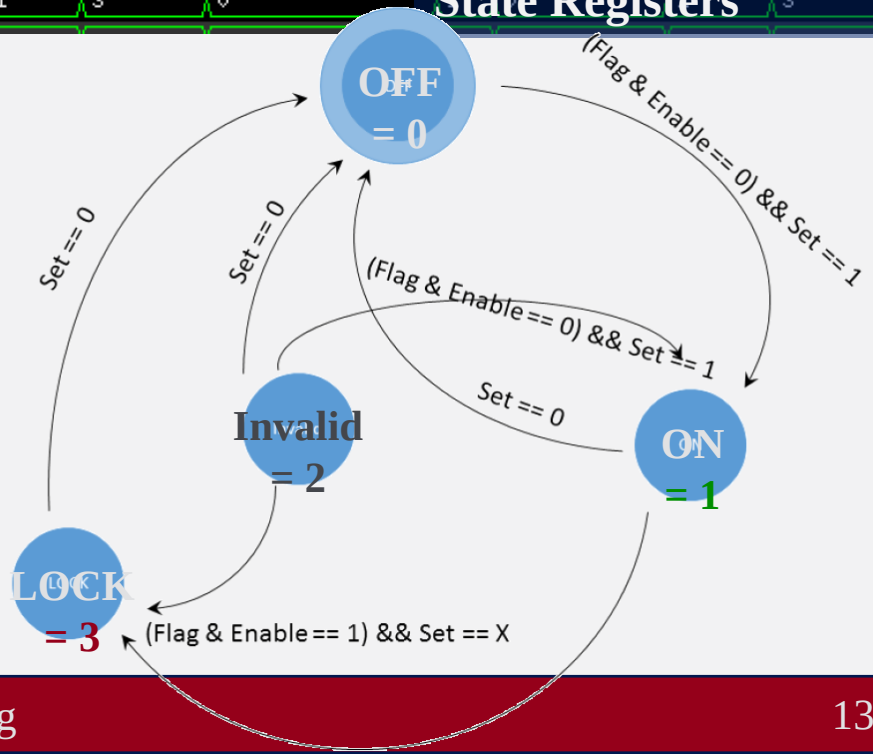

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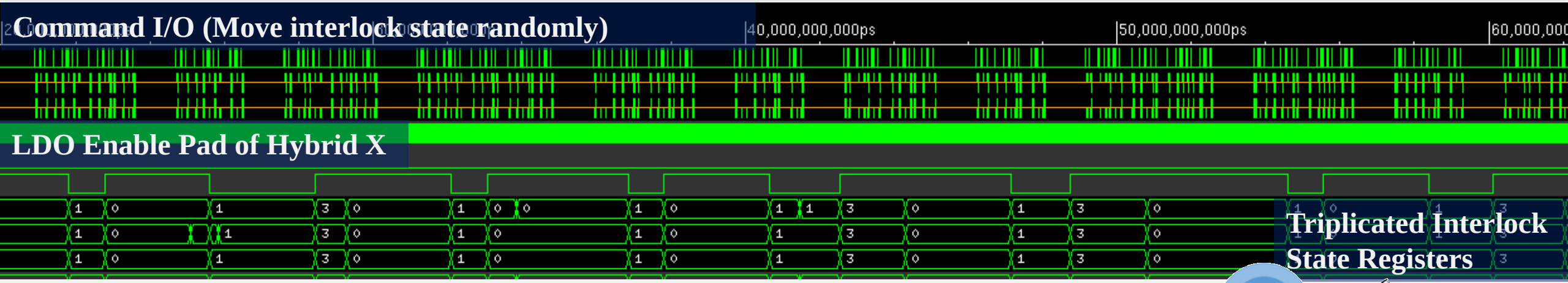

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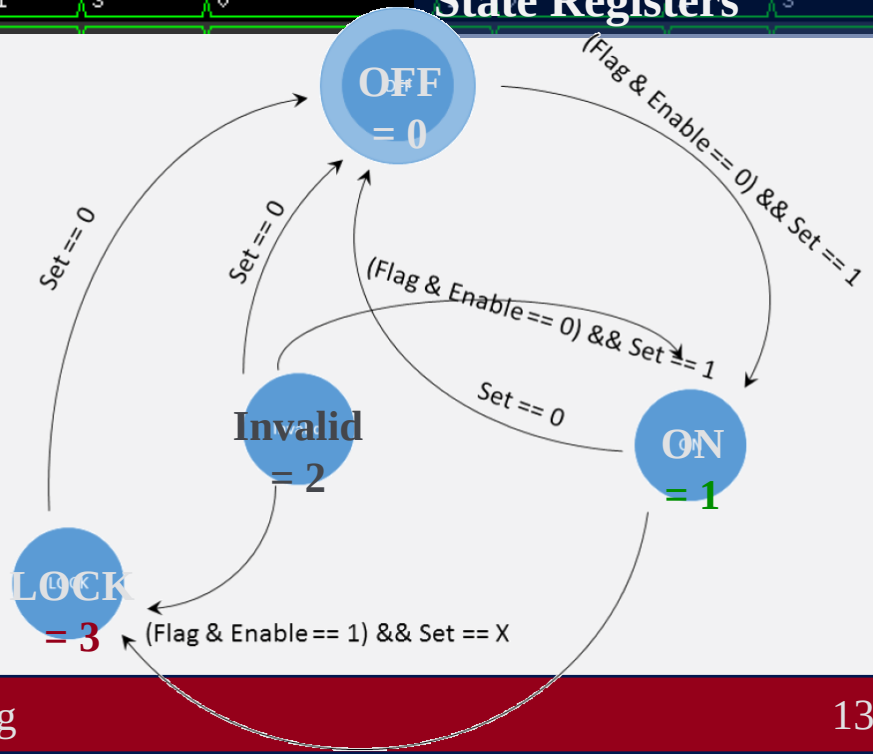

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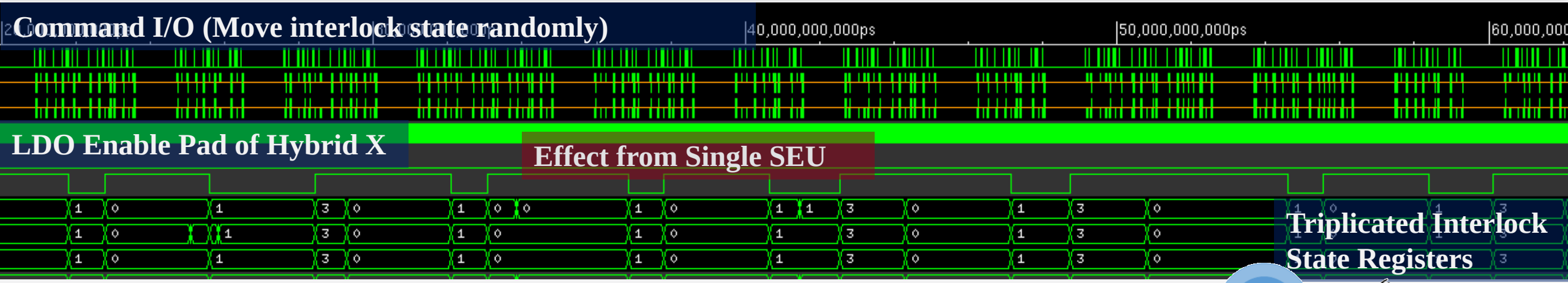

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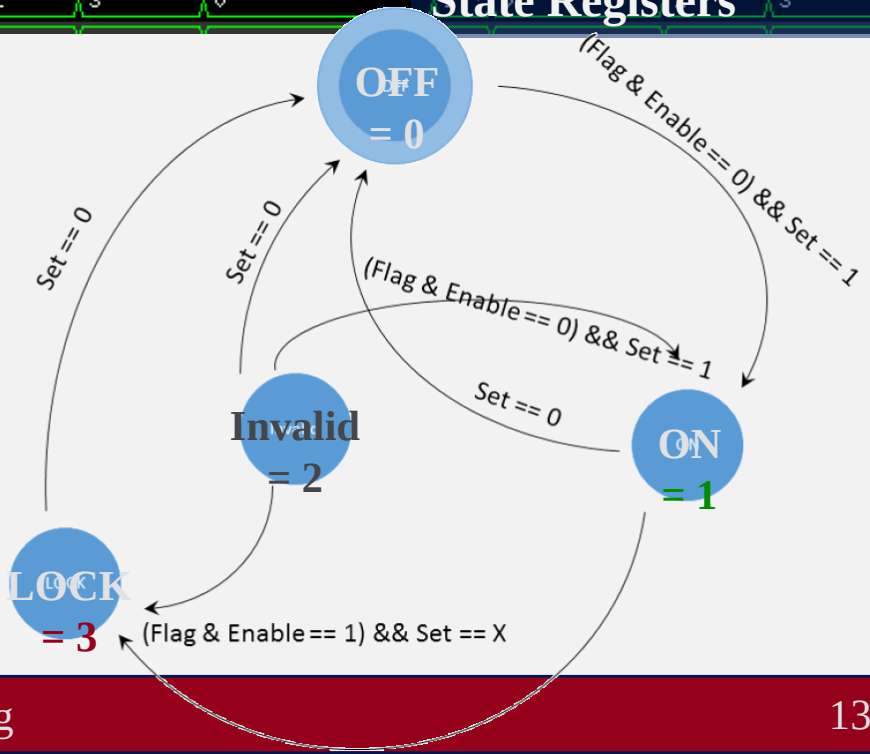

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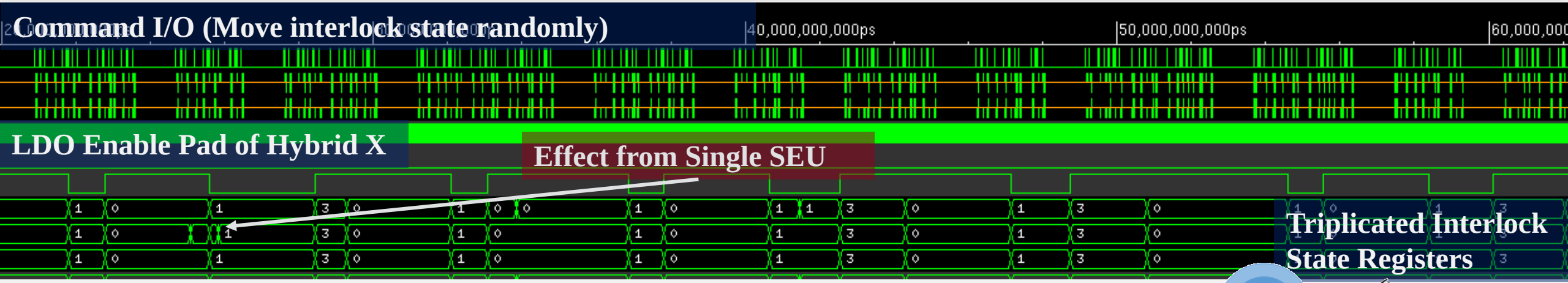

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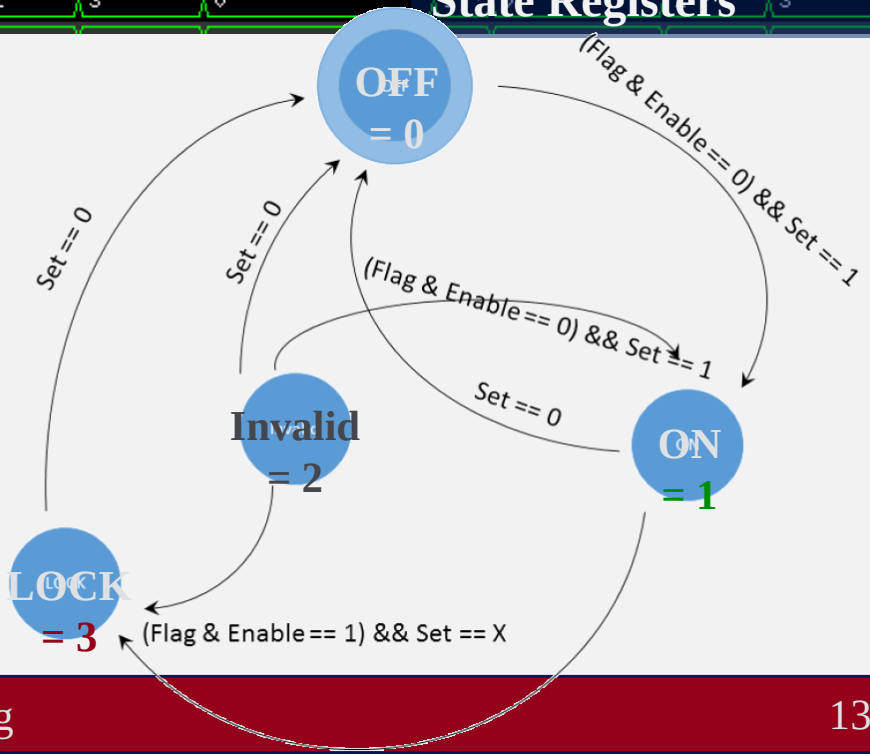

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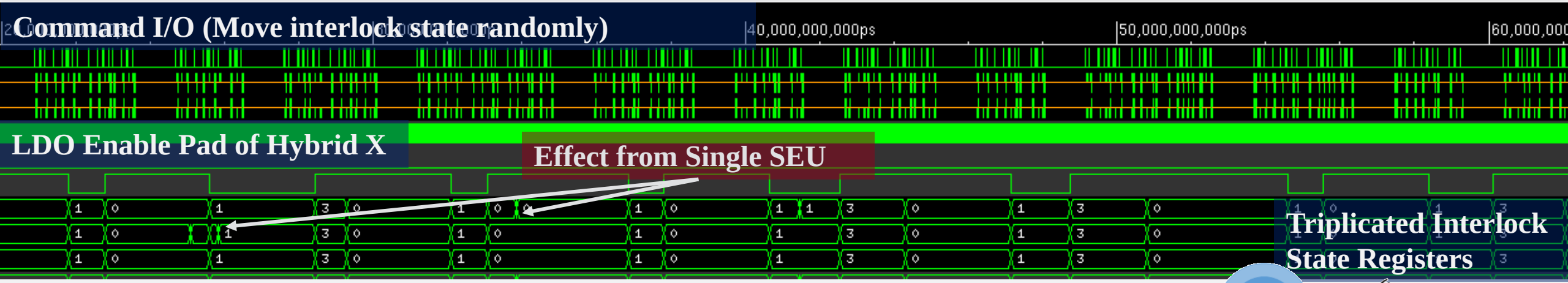

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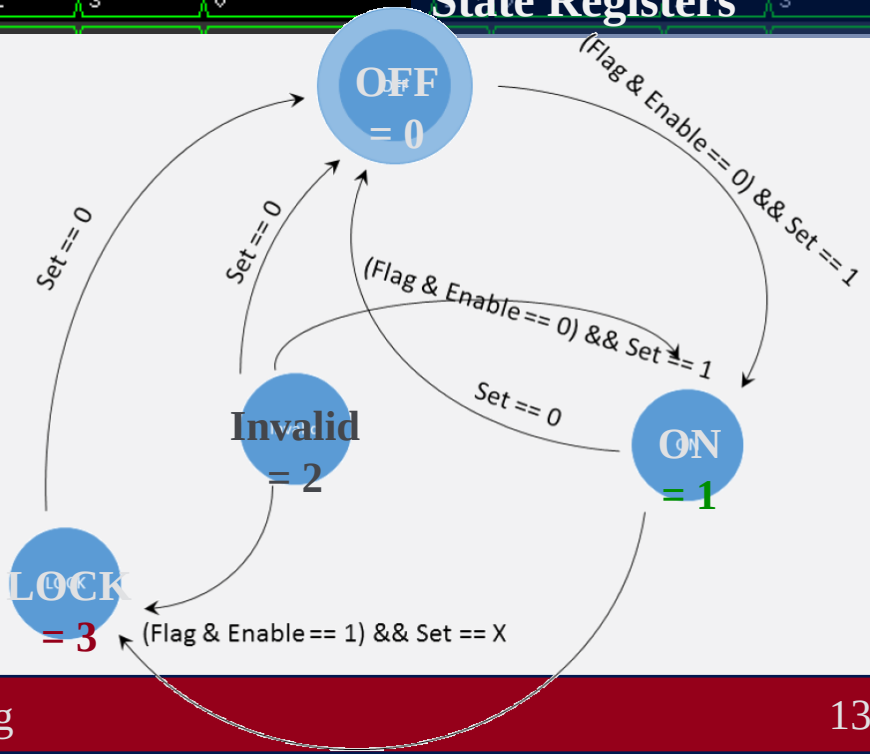

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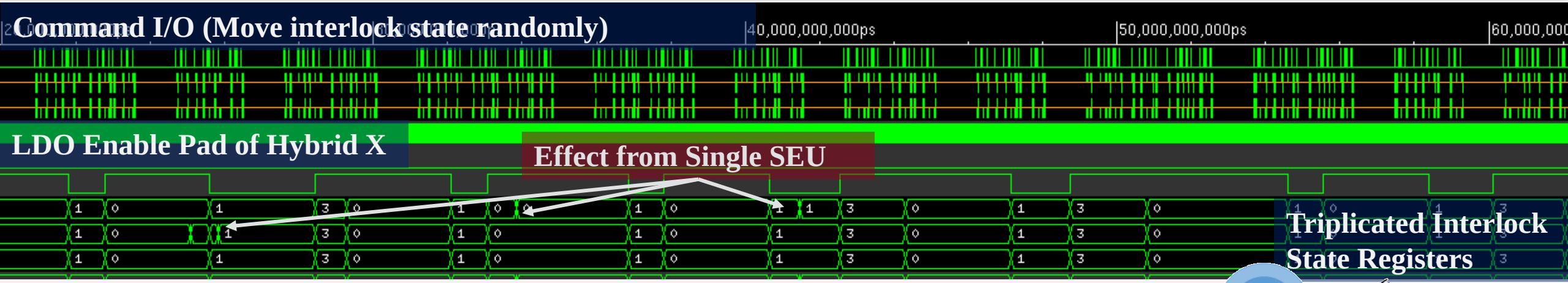

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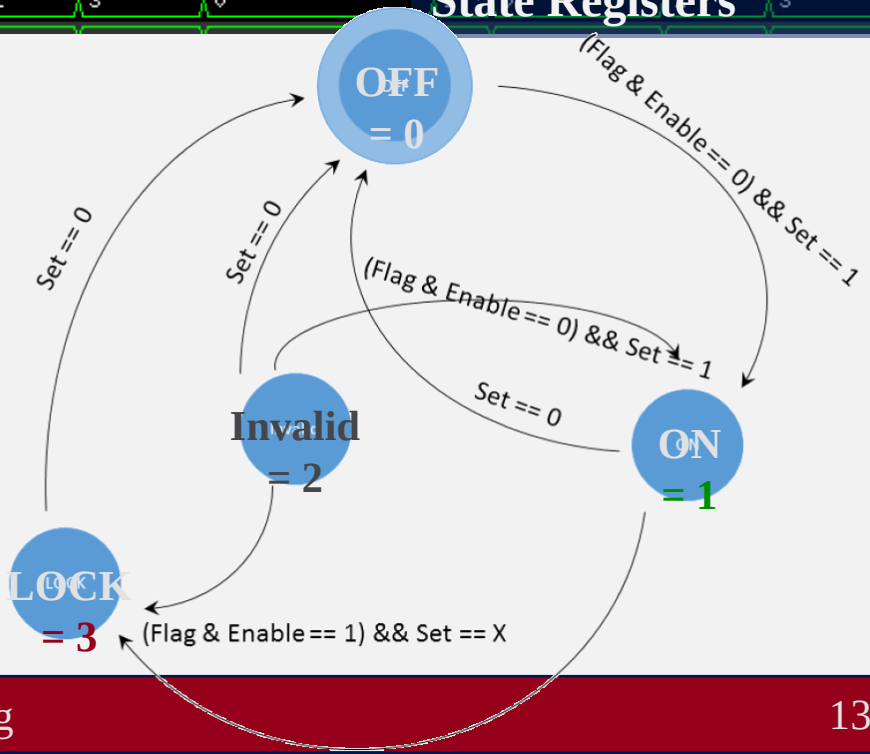

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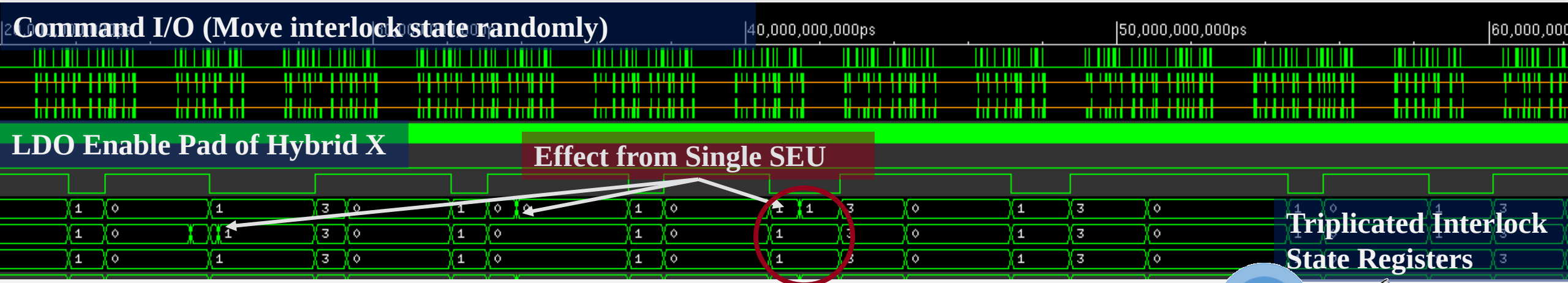

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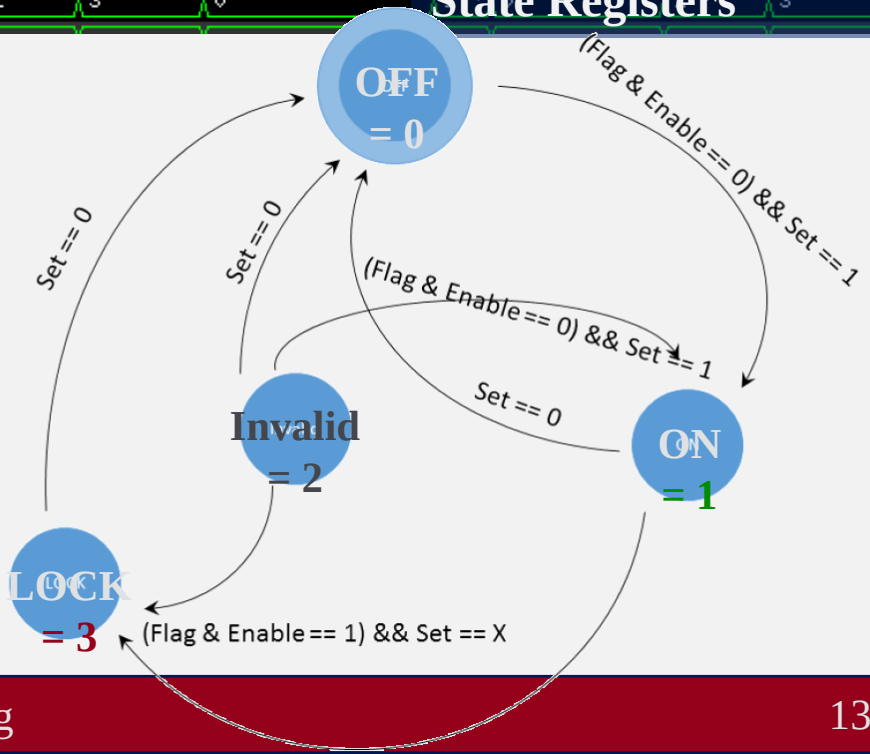

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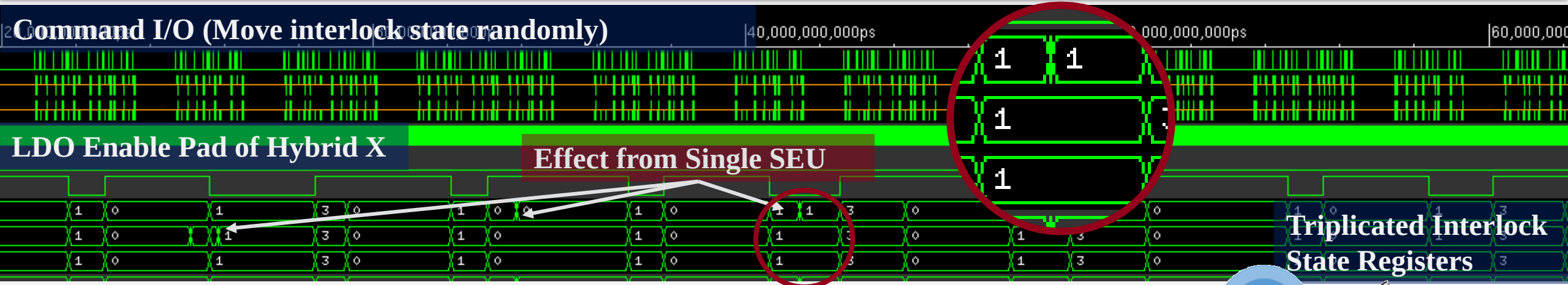

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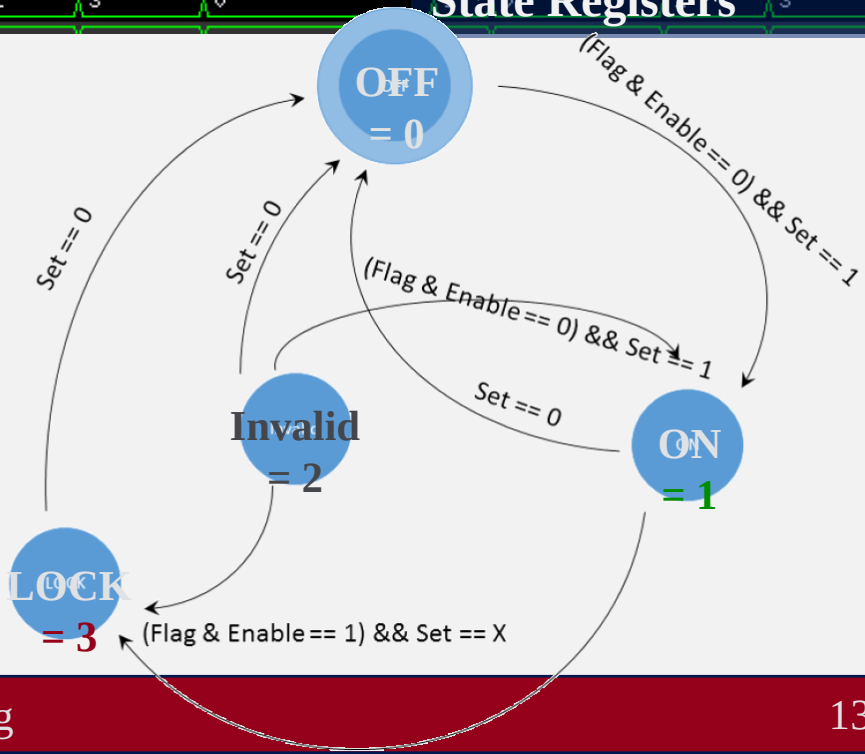

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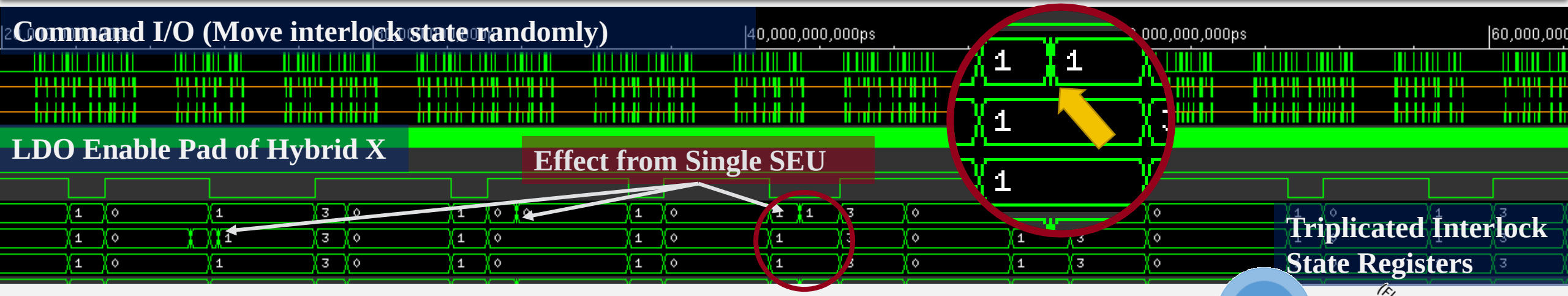

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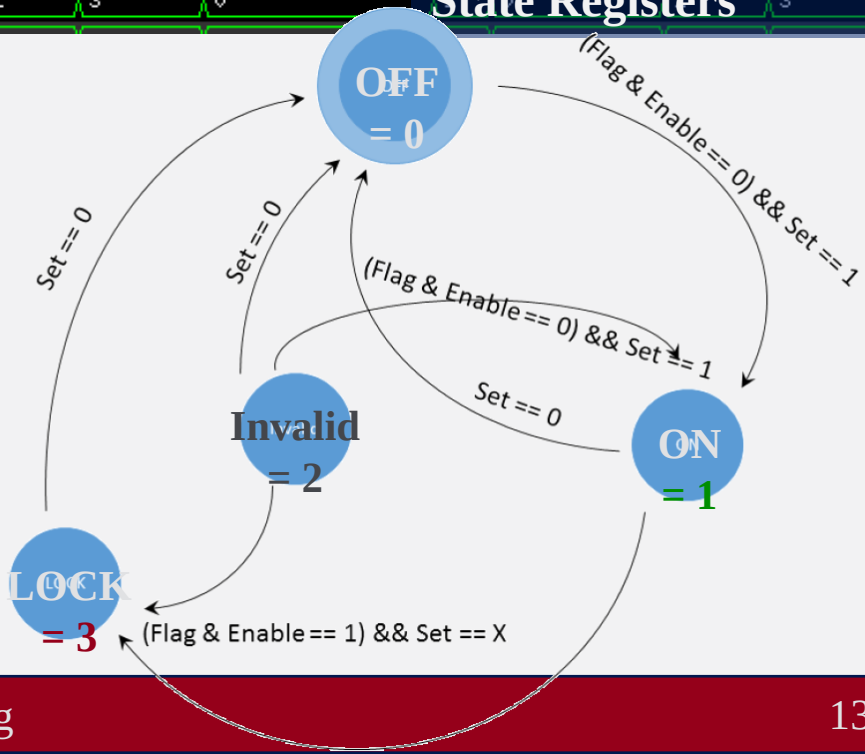

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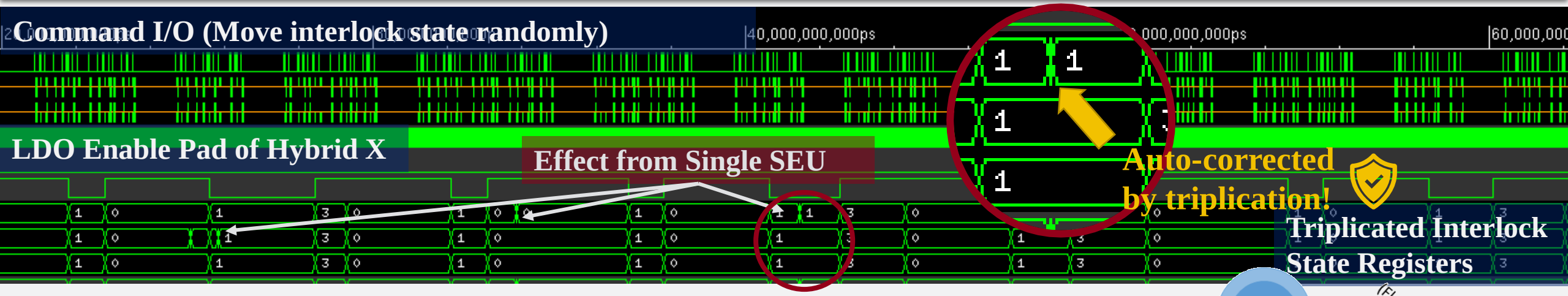

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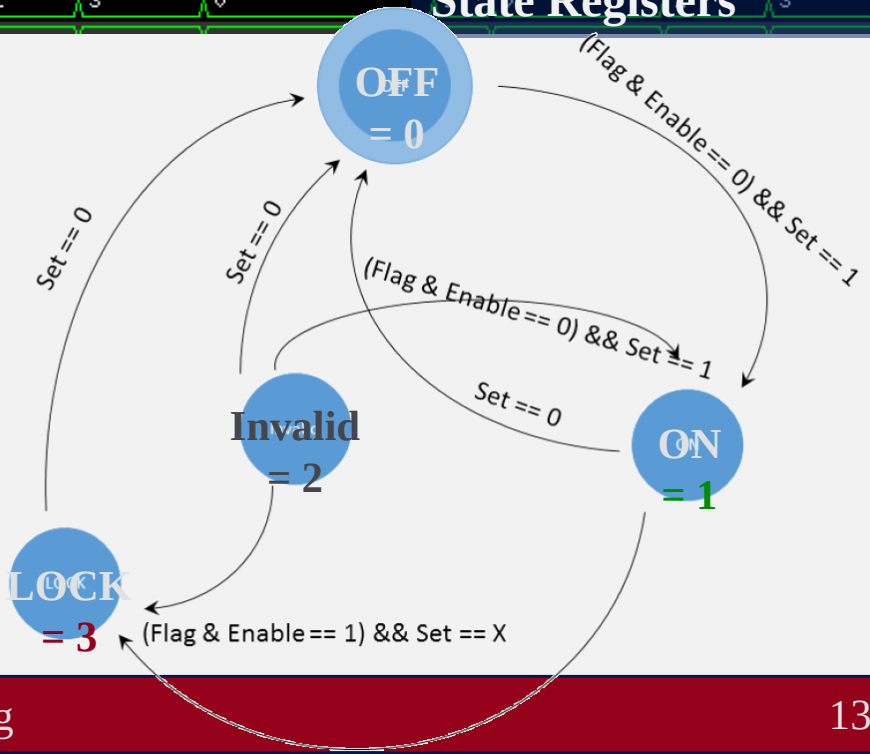
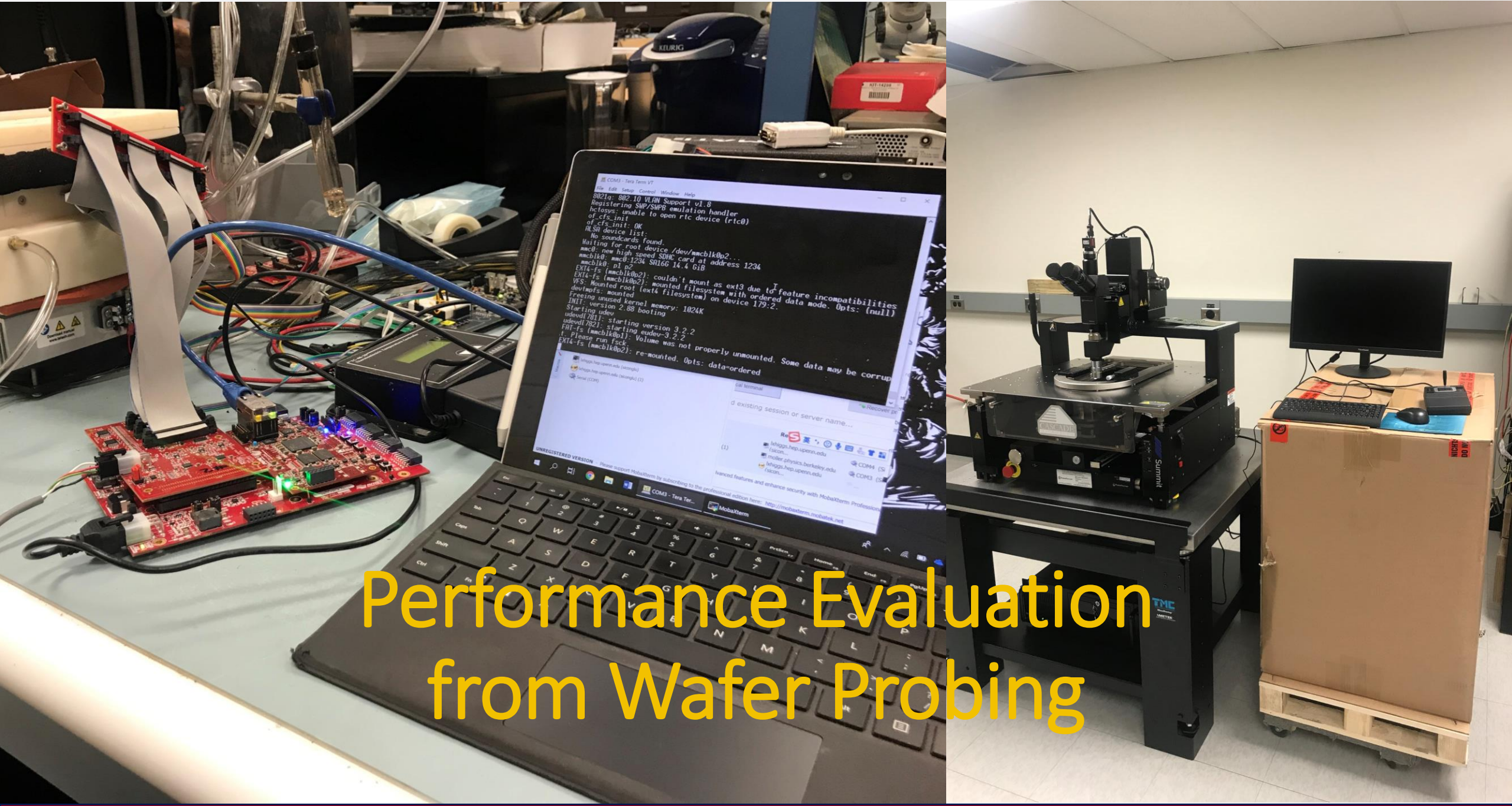



Performance Evaluation
from Wafer Probing

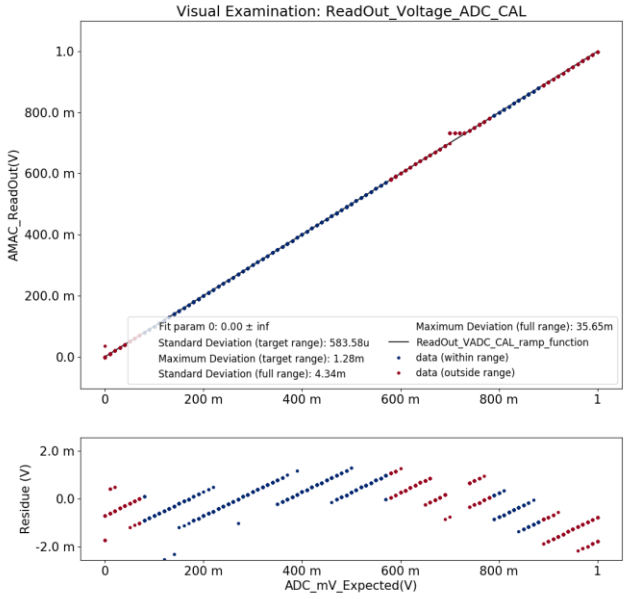
Numerical AMAC Performance Evaluation

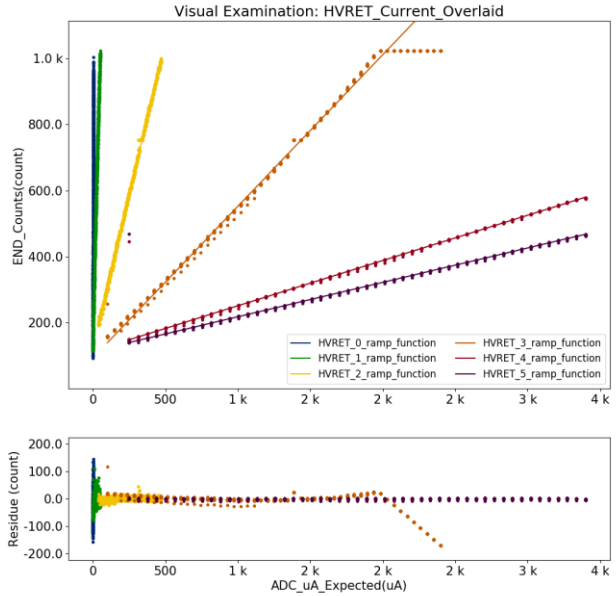
Voltage Measurement

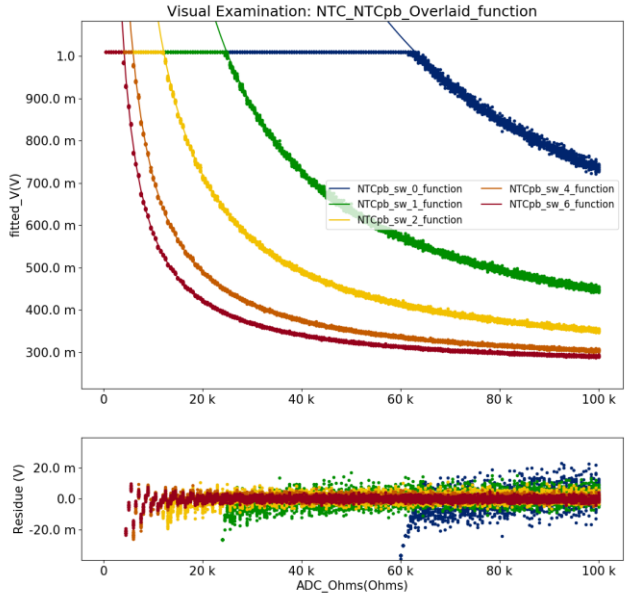
Current Measurement

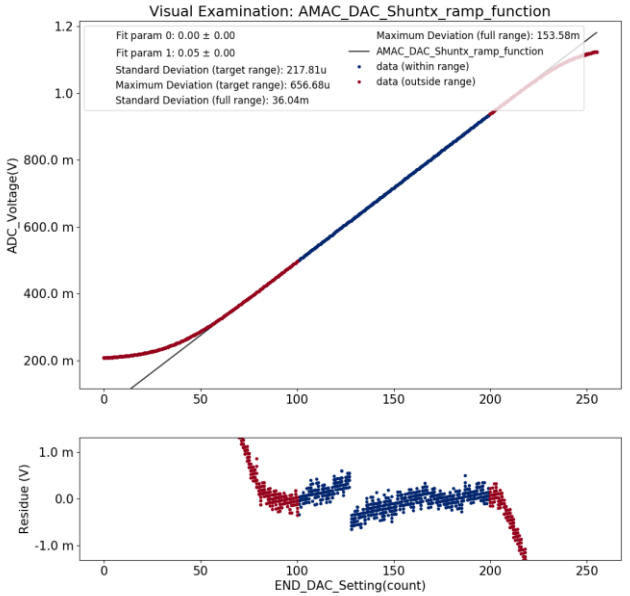
Temperature Measurement

Digital-to-Analog Output









Only NTC measurement will be discussed here as an example of analysis procedure.

Numerical AMAC Performance Evaluation

Voltage Measurement

Current Measurement

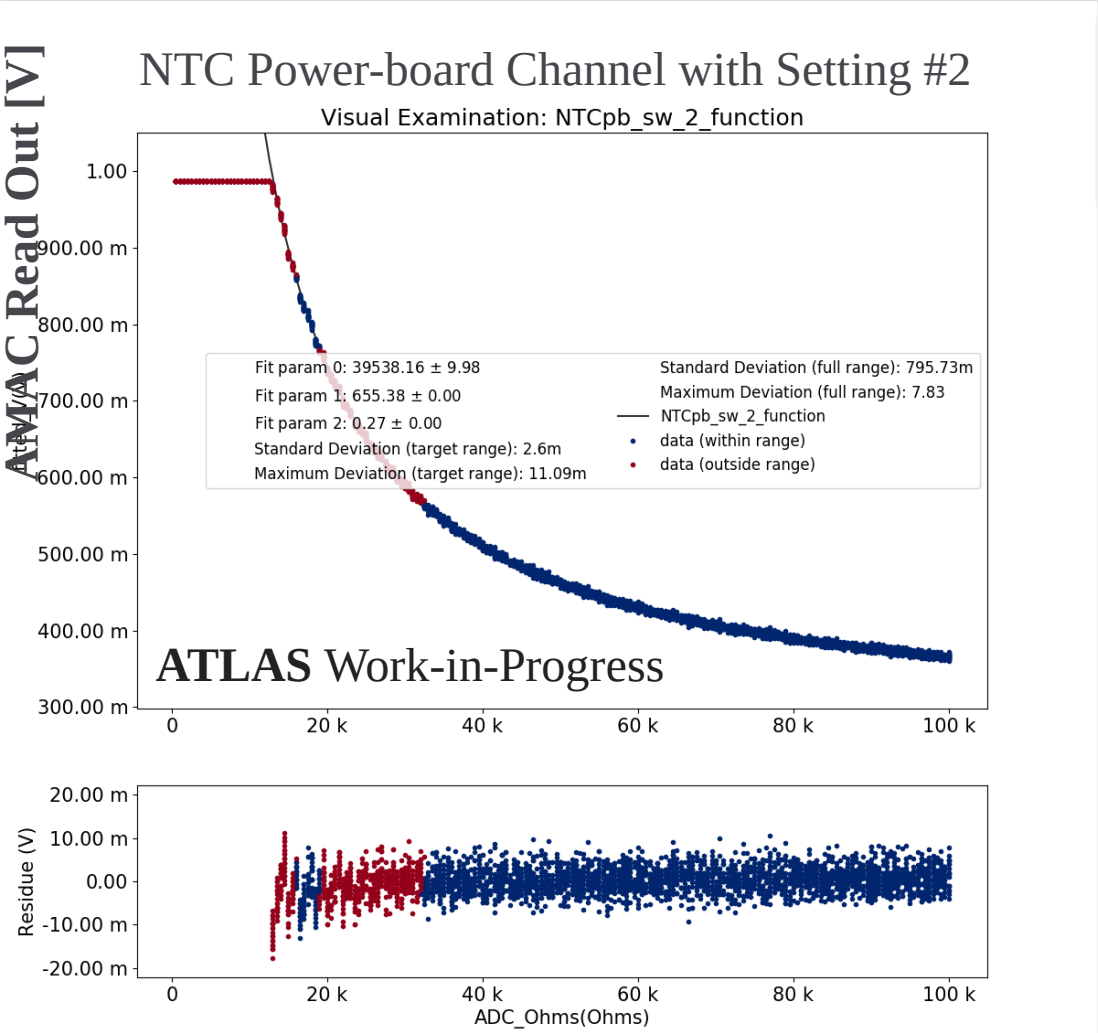
Temperature Measurement

Digital-to-Analog Output

- ✓ Use external digital device to scan the measurement
- ✓ Use AMAC to read the value multiple times
- ✓ Compare input and readout to check that it follows the design
- ✓ Fit to evaluate accuracy & precision

Only NTC measurement will be discussed here as an example of analysis procedure.

Analysis of Individual Tests



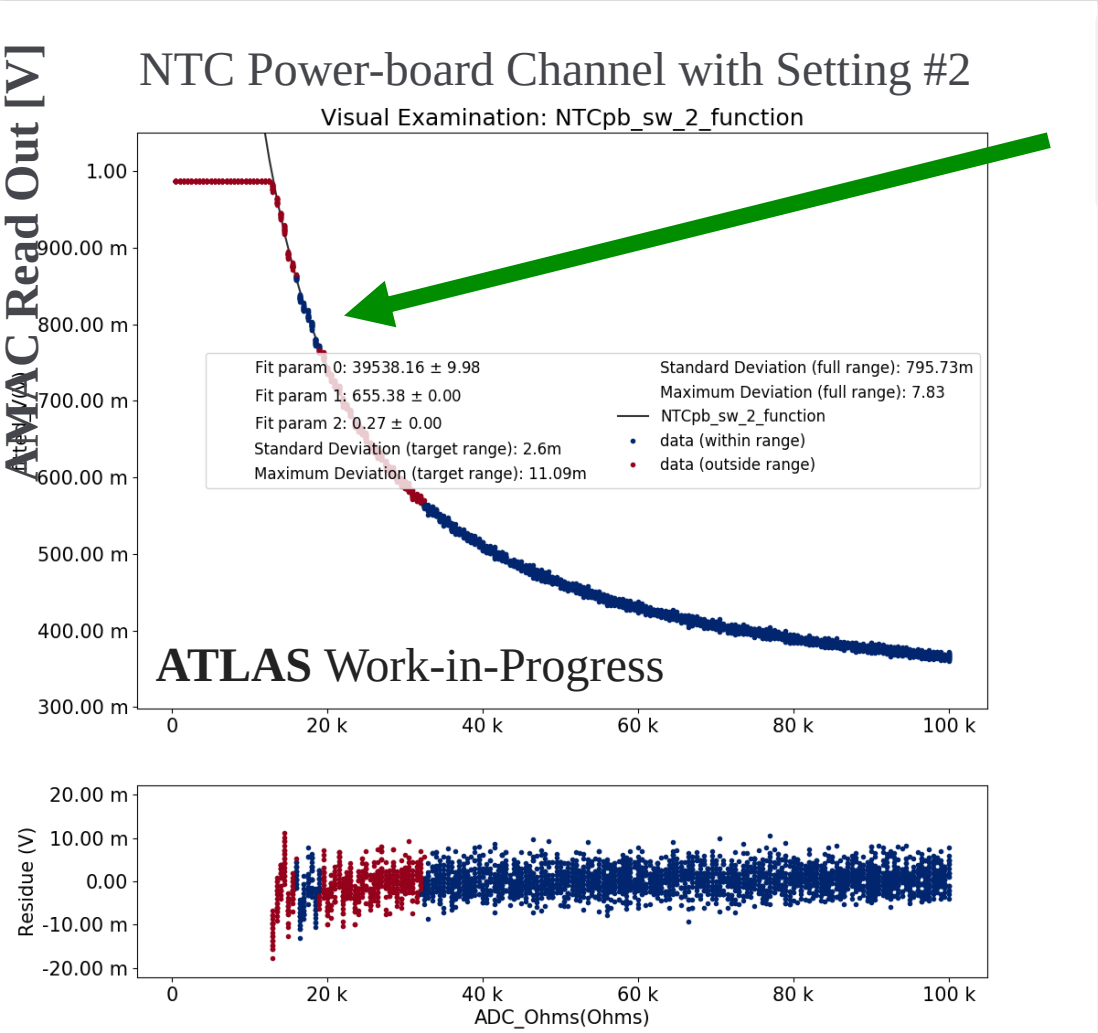
Collect Data Array

Fit to Designed Function

Numerical Fit Parameter & Residual Parameters

Save Result to Local and Online Database ⟹

Analysis of Individual Tests



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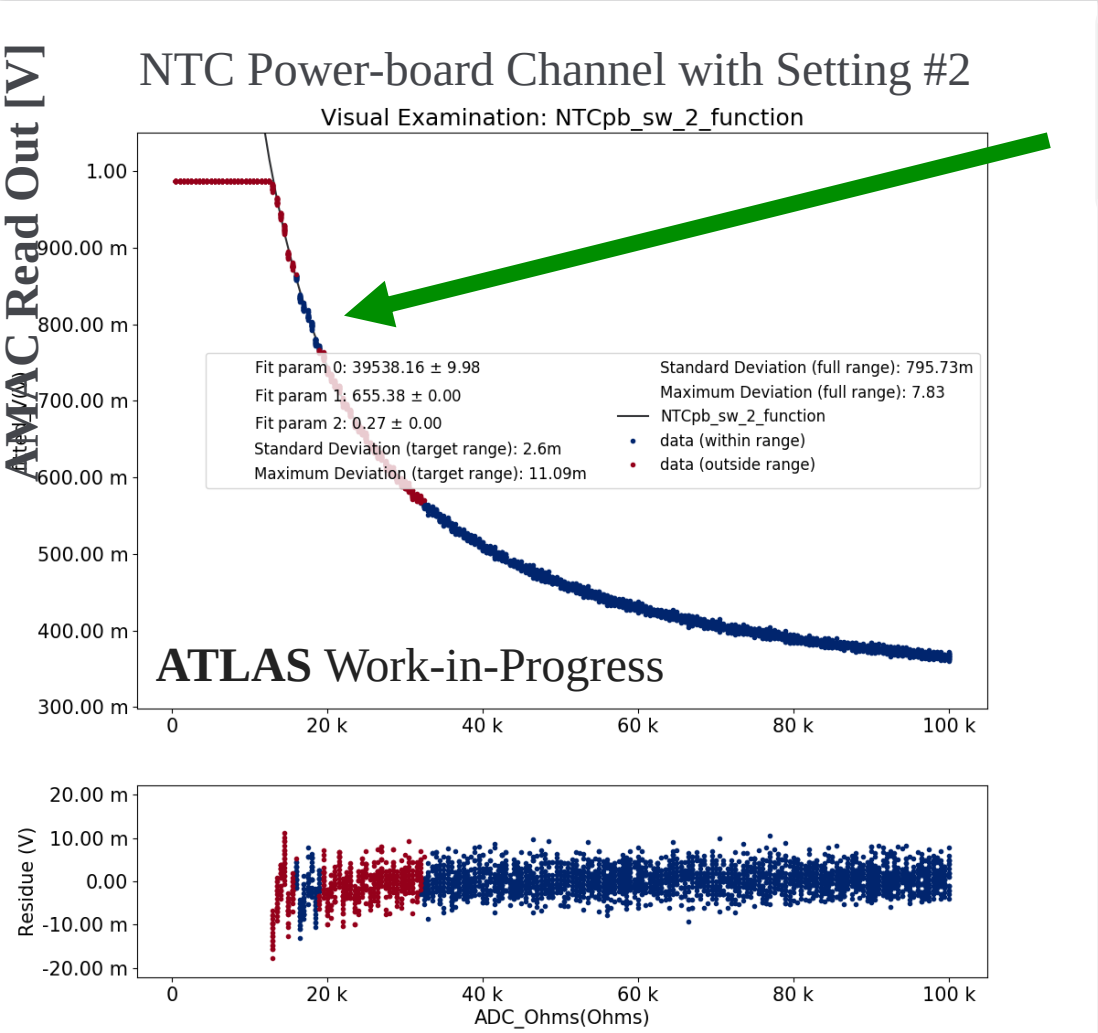
e.g. Fit to a simplified circuit model:

$$V_{\text{measure}} = 250\text{mV}\frac{R_{\text{sw}}}{R_{\text{NTC}} + R_{\text{internal}}} + V_{\text{zero}}$$



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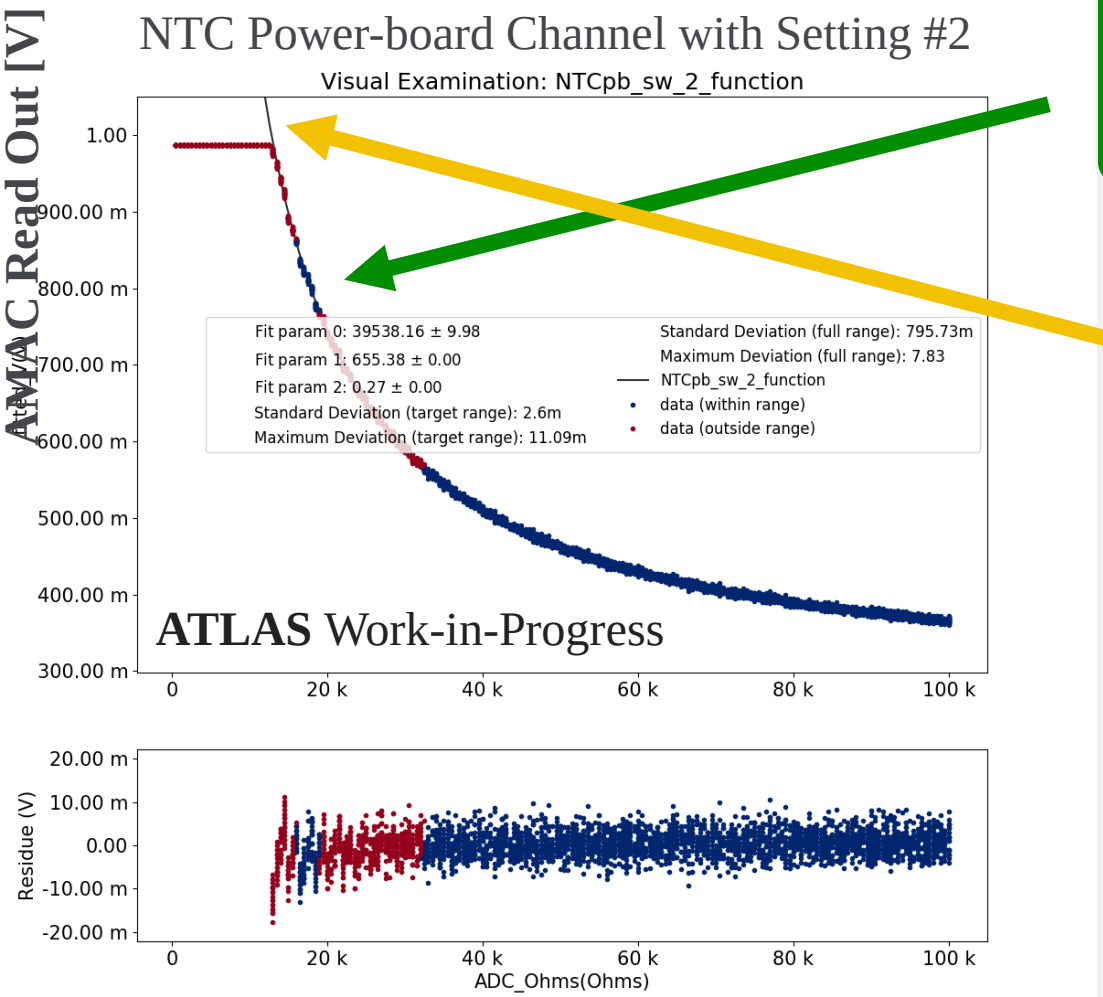

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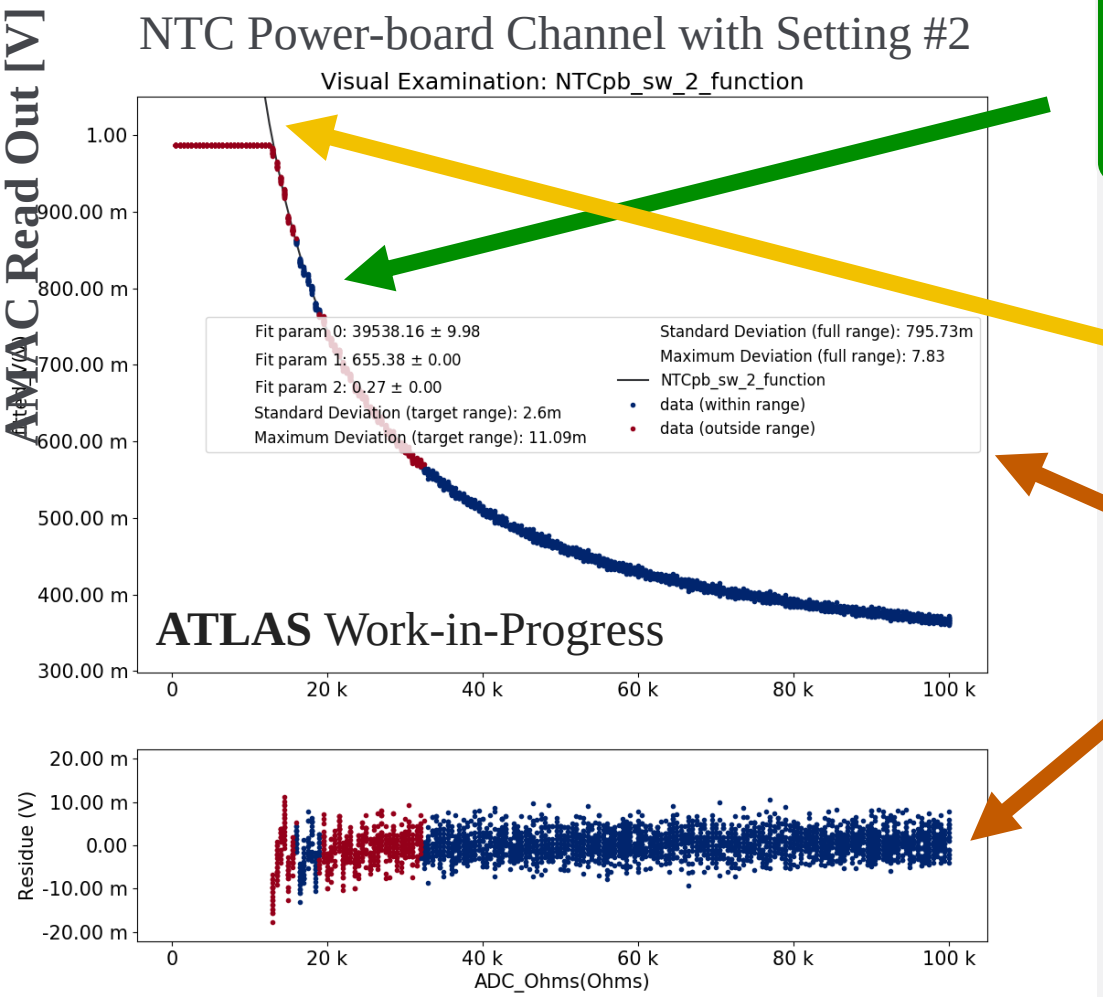

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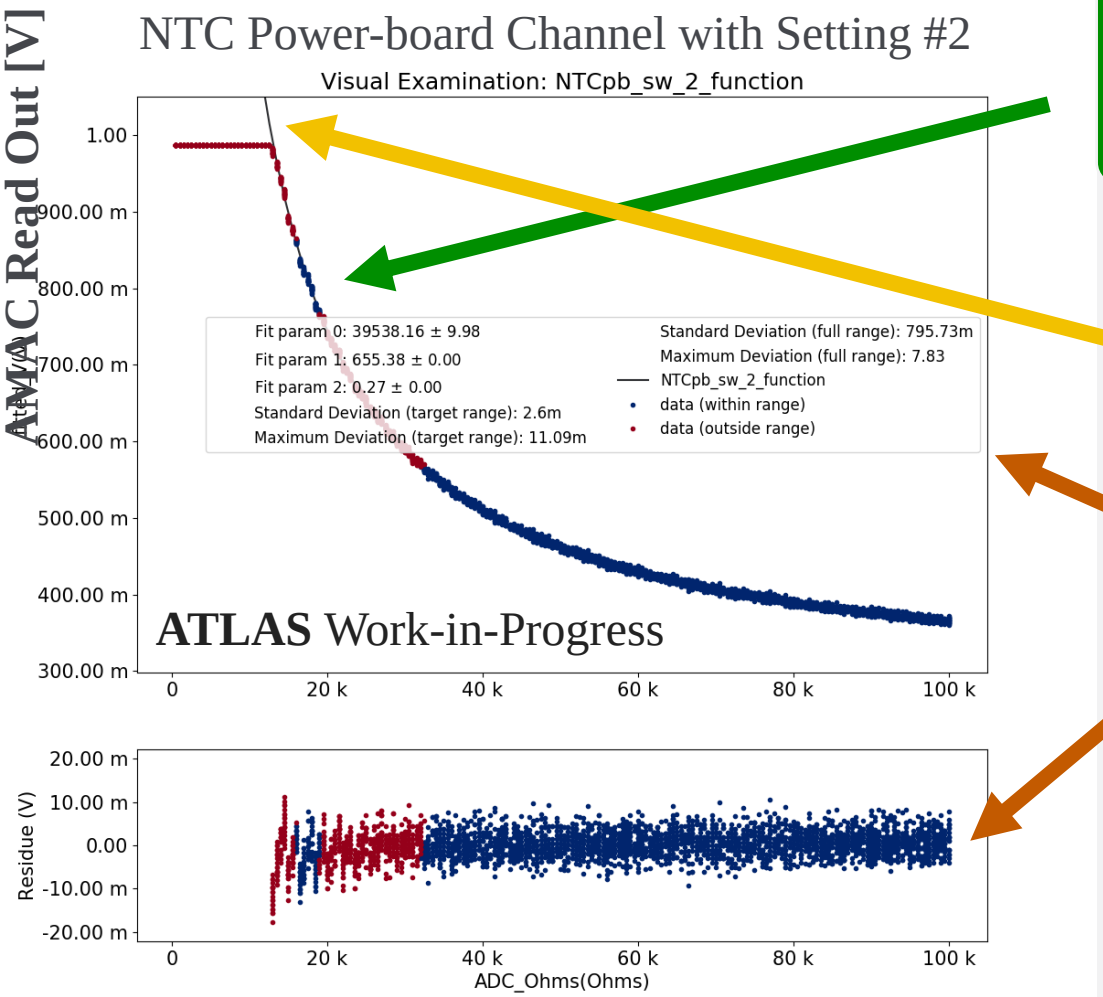

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The prototype has been exceptionally successful!
Luis will tell you more about it in the next presentation!

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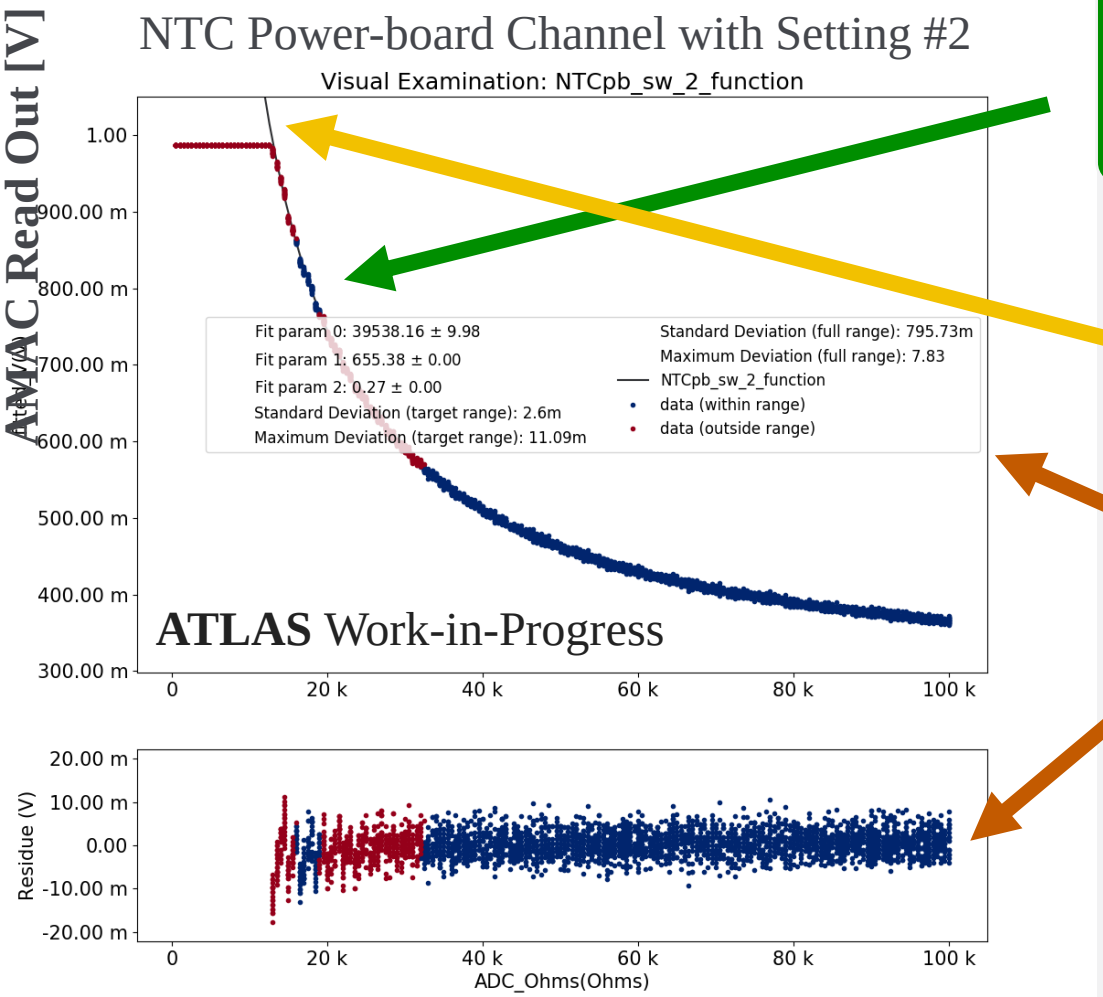

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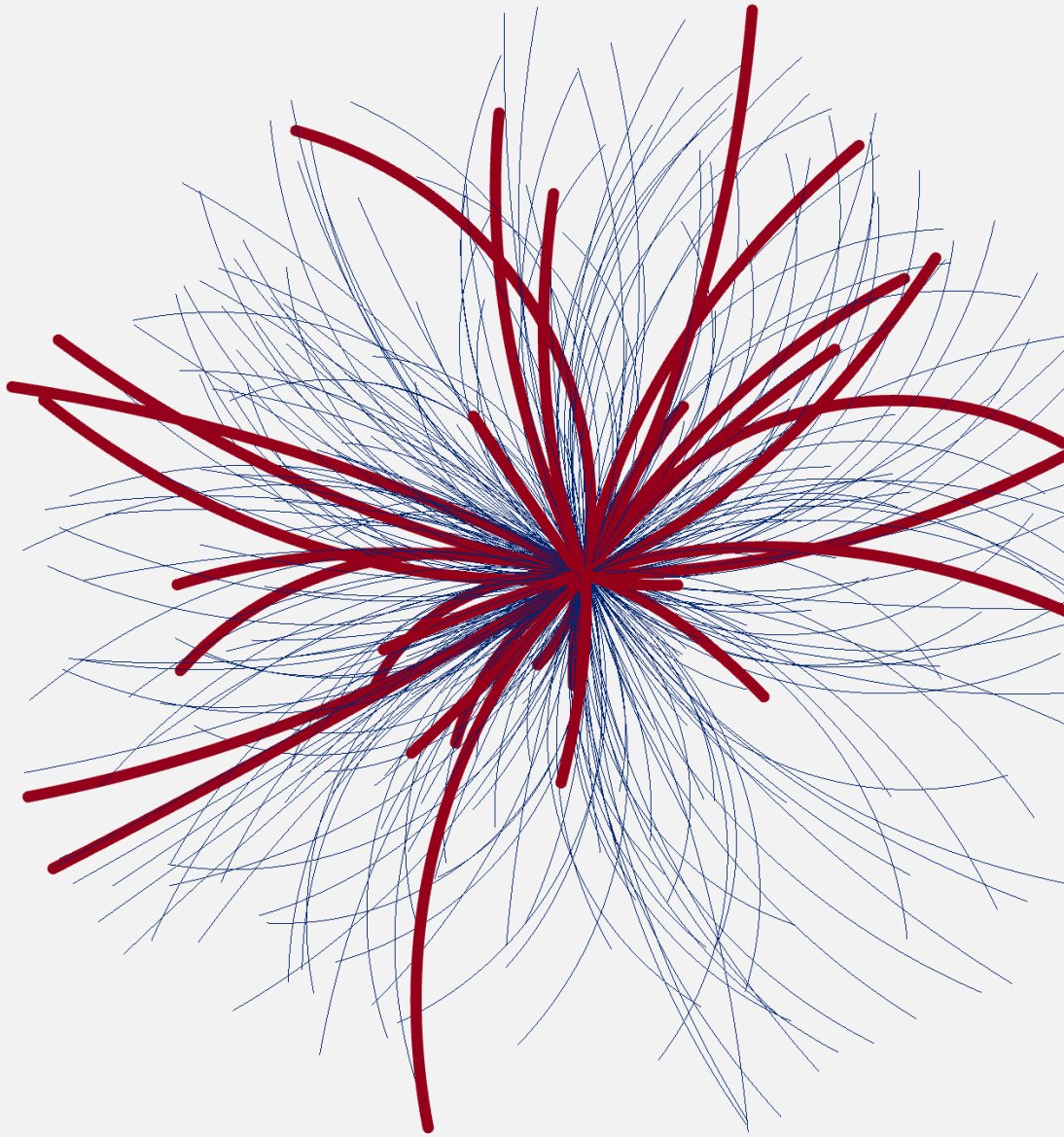
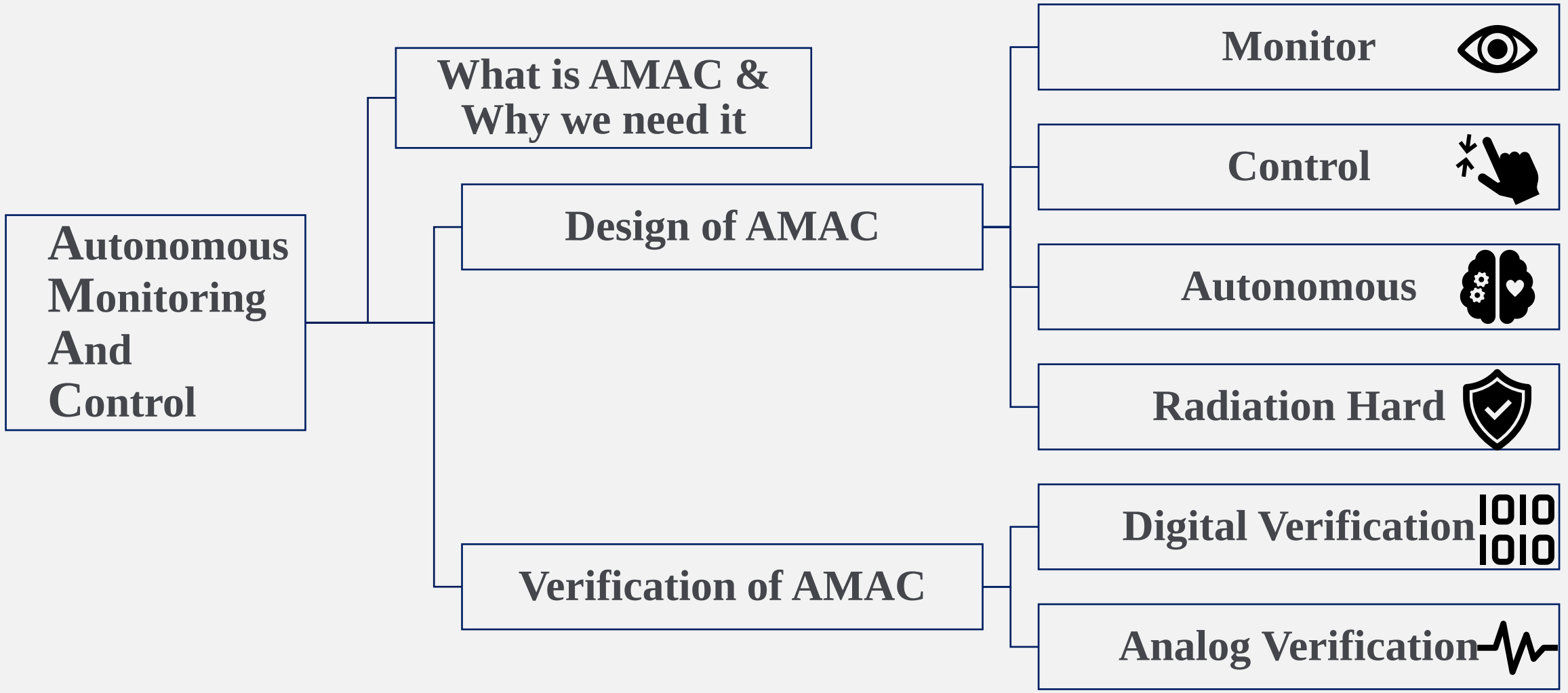
Thank you for your attention!!!



OUTLINE


Autonomous Monitoring And Control
What is AMAC & Why we need it
Design of AMAC
Monitor
Control
Autonomous
Radiation Hard
Verification of AMAC
Digital Verification
Analog Verification

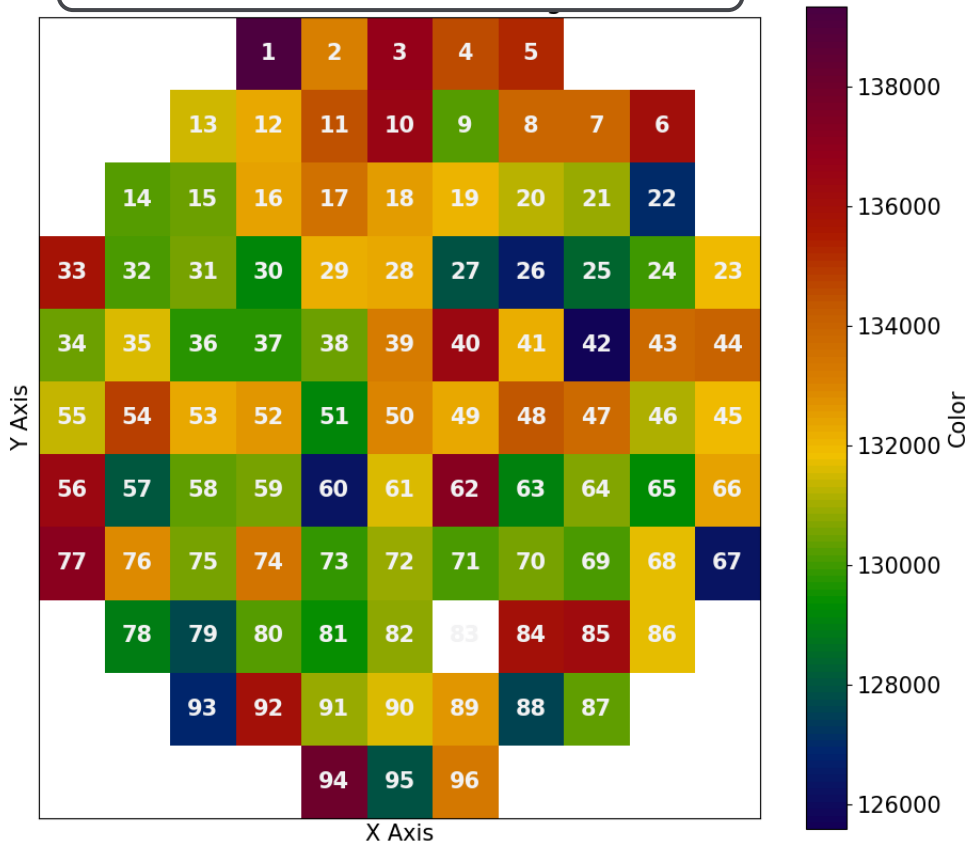
Back-Up

Numerically Fitted Chip Parameter
NTC Power-board Resistance - R_0

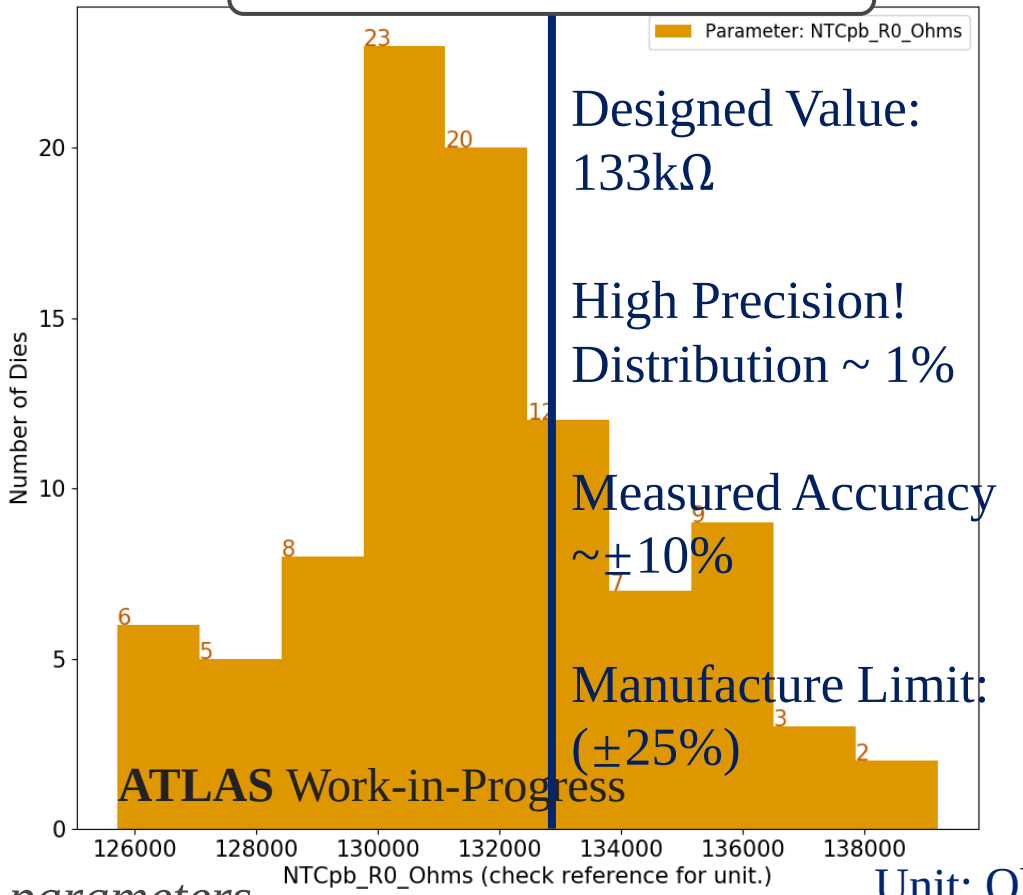
Wafer : **V0CVRFH**
Dice: 95/96 passed

Distribution by Chip on Wafer

Unit: Ohms



Parameter Value Histogram



Like this one above, we have:

>1000 collected parameters

>200 analog diagnostic parameters

>50 analog pass/fail parameters

Data Flow from **Wafer Probing** to **Dicing** & **Database**

*All results except Raw Data are **available online!***

Data Flow from **Wafer Probing** to **Dicing** & **Database**

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Raw Data (.csv)

	ADC_Ohms	END_NTC_SW	END_Count
2	65000	0	935.312 5.90253
3	65500	0	931.5 4.38748
4	66000	0	929.688 3.09675
5	66500	0	922.688 5.13224
6	67000	0	923 4.48609
7	67500	0	915.312 4.1791
8	68000	0	913.125 3.78938
9	68500	0	905 3.96863
10	69000	0	899.188 3.72858
11	69500	0	898.438 5.52233
12	70000	0	891.75 3.78319
13	70500	0	887.125 4.25551
14	71000	0	883.688 4.7791
15	71500	0	880.188 3.20583
16	72000	0	872.125 6.34306
17	72500	0	872.875 4.09077
18	73000	0	869.938 4.87941
19	73500	0	860.688 5.76323
20	74000	0	858.125 4.48435
21	74500	0	854.562 4.21261
22	75000	0	854.375 5.01093
23	75500	0	847.375 4.21122
24	76000	0	846.625 5.23062
25	76500	0	842.625 3.56853

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16	72500	0	872.875 4.09077
17	73000	0	869.938 4.87941
18	73500	0	860.688 5.76323
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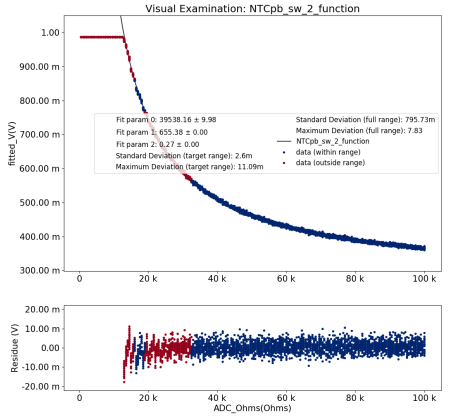
Numerical Fit & Grading (.py)



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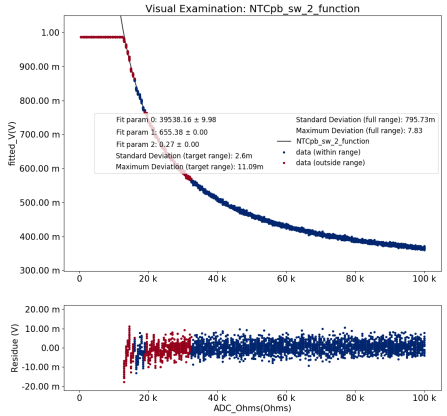
Raw Data (.csv)

	ADC_Ohms	END_NTC_SW	END_Count
1			
2	65000	0	935.312 5.90253
3	65500	0	931.5 4.38748
4	66000	0	929.688 3.09675
5	66500	0	922.688 5.13224
6	67000	0	923 4.48609
7	67500	0	915.312 4.1791
8	68000	0	913.125 3.78938
9	68500	0	905 3.96863
10	69000	0	899.188 3.72858
11	69500	0	898.438 5.52233
12	70000	0	891.75 3.78319
13	70500	0	887.125 4.25551
14	71000	0	883.688 4.7791
15	71500	0	880.188 3.20583
16	72000	0	872.125 6.34306
17	72500	0	872.875 4.09077
18	73000	0	869.938 4.87941
19	73500	0	860.688 5.76323
20	74000	0	858.125 4.48435
21	74500	0	854.562 4.21261
22	75000	0	854.375 5.01093
23	75500	0	847.375 4.21122
24	76000	0	846.625 5.23062
25	76500	0	842.625 3.56853

Numerical Fit & Grading (.py)



Component Property& Test Run (.json)

Parent Directory

AMACv2a_0x0000200a_try2_AMAC_DAC_CALX_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_CALY_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALX_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALY_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_SHUNTX_RAMP_FUNCTION.json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{"component": "20USG000500876", "problems": false, "results": {}, "defects": [], "testTypeState":
"active", "date": "29.05.2020", "testType": "POWER_FUNCTIONS", "institution": "UPENN", "runNumber":
"try2", "comments": [], "properties": {"ADC_VDD_HI_V_OFF": 0.00030518, "BEST_WORKING_VDD": 1.23804,
"ADC_VDDLR": 1.47433, "ADC_AM_VDDLR_V": 1.4831, "ADC_AM_VDDLR_A": 0.0369268, "BEST_AM600BG": 0.620813,
"BEST_AMBG": 13, "ADC_VDD_HI_A_RO7_4HVO0": 0.00421381, "ADC_VDD_HI_A_RO7_4HVO1": 0.00493768,
"ADC_VDD_HI_A_RO7_4HVO2": 0.0048784, "ADC_VDD_HI_A_RO7_4HVO3": 0.0047892, "ADC_AM_VDD_HI_A": 1.49598e-05,
"ADC_VDD_HI_V_RO7_4HVO3": 3.14046, "ADC_VDD_HI_V_RO7_4HVO2": 3.14046, "ADC_VDD_HI_V_RO7_4HVO1": 3.14046,
"ADC_VDD_HI_V_RO7_4HVO0": 3.17639, "BEST_VDD": 1.23804, "ADC_AM_VDD_HI_V": 0.000228885, "BEST_RAMP": 0,
"BEST_SLOPE": 1.00578, "ADC_AM_LVDS_CM1": 0.69482, "ADC_AM_LVDS_CM0": 0.680705, "BEST_WORKING_VDDBG": 11,
"BEST_VDDBG": 11, "ADC_AM_VDCDC_V": 0.00015259, "ADC_VDD_HI_A_STD_RO7_4HVO2": 0.00104764,
"ADC_VDD_HI_A_STD_RO7_4HVO3": 0.00105412, "ADC_VDD_HI_A_STD_RO7_4HVO0": 0.000883412,
"ADC_VDD_HI_A_STD_RO7_4HVO1": 0.00105266, "ADC_VDD_HI_A_OFF": 0, "ADC_AM_VDCDC_A": 0.00015259}, "passed":
true}
```

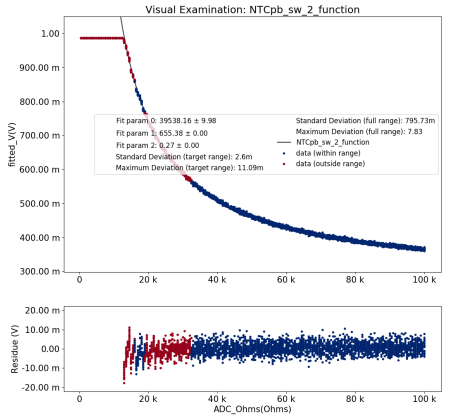
Data Flow from **Wafer Probing** to **Dicing** & **Database**

*All results except Raw Data are **available online!***

Raw Data (.csv)

	ADC_Ohms	END_NTC_SW	END_Count
1			
2	65000	0	935.312 5.90253
3	65500	0	931.5 4.38748
4	66000	0	929.688 3.09675
5	66500	0	922.688 5.13224
6	67000	0	923 4.48609
7	67500	0	915.312 4.1791
8	68000	0	913.125 3.78938
9	68500	0	905 3.96863
10	69000	0	899.188 3.72858
11	69500	0	898.438 5.52233
12	70000	0	891.75 3.78319
13	70500	0	887.125 4.25551
14	71000	0	883.688 4.7791
15	71500	0	880.188 3.20583
16	72000	0	872.125 6.34306
17	72500	0	872.875 4.09077
18	73000	0	869.938 4.87941
19	73500	0	860.688 5.76323
20	74000	0	858.125 4.48435
21	74500	0	854.562 4.21261
22	75000	0	854.375 5.01093
23	75500	0	847.375 4.21122
24	76000	0	846.625 5.23062
25	76500	0	842.625 3.56853

Numerical Fit & Grading (.py)



Component Property& Test Run (.json)

Parent Directory

AMACv2a_0x0000200a_try2_AMAC_DAC_CALX_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_CALY_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALX_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALY_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_SHUNTX_RAMP_FUNCTION.json


```
{"component": "20USG000500876", "problems": false, "results": {}, "defects": [], "testTypeState":
"active", "date": "29.05.2020", "testType": "POWER_FUNCTIONS", "institution": "UPENN", "runNumber":
"try2", "comments": [], "properties": {"ADC_VDD_HI_V_OFF": 0.00030518, "BEST_WORKING_VDD": 1.23804,
"ADC_VDDLR": 1.47433, "ADC_AM_VDDLR_V": 1.4831, "ADC_AM_VDDLR_A": 0.0369268, "BEST_AM600BG": 0.620813,
"BEST_AMBG": 13, "ADC_VDD_HI_A_RO7_4HVO0": 0.00421381, "ADC_VDD_HI_A_RO7_4HVO1": 0.00493768,
"ADC_VDD_HI_A_RO7_4HVO2": 0.0048784, "ADC_VDD_HI_A_RO7_4HVO3": 0.0047892, "ADC_AM_VDD_HI_A": 1.49598e-05,
"ADC_VDD_HI_V_RO7_4HVO3": 3.14046, "ADC_VDD_HI_V_RO7_4HVO2": 3.14046, "ADC_VDD_HI_V_RO7_4HVO1": 3.14046,
"ADC_VDD_HI_V_RO7_4HVO0": 3.17639, "BEST_VDD": 1.23804, "ADC_AM_VDD_HI_V": 0.000228885, "BEST_RAMP": 0,
"BEST_SLOPE": 1.00578, "ADC_AM_LVDS_CM1": 0.69482, "ADC_AM_LVDS_CM0": 0.680705, "BEST_WORKING_VDDBG": 11,
"BEST_VDDBG": 11, "ADC_AM_VDCDC_V": 0.00015259, "ADC_VDD_HI_A_STD_RO7_4HVO2": 0.00104764,
"ADC_VDD_HI_A_STD_RO7_4HVO3": 0.00105412, "ADC_VDD_HI_A_STD_RO7_4HVO0": 0.000883412,
"ADC_VDD_HI_A_STD_RO7_4HVO1": 0.00105266, "ADC_VDD_HI_A_OFF": 0, "ADC_AM_VDCDC_A": 0.00015259}, "passed":
true}
```


ITk Production Database

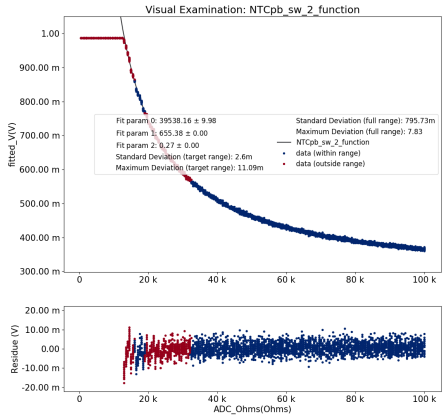
Data Flow from **Wafer Probing** to **Dicing** & **Database**

*All results except Raw Data are **available online!***

Raw Data (.csv)

	ADC_Ohms	END_NTC_SW	END_Count
1	65000	0	935.312 5.90253
2	65500	0	931.5 4.38748
3	66000	0	929.688 3.09675
4	66500	0	922.688 5.13224
5	67000	0	923 4.48609
6	67500	0	915.312 4.1791
7	68000	0	913.125 3.78938
8	68500	0	905 3.96863
9	69000	0	899.188 3.72858
10	69500	0	898.438 5.52233
11	70000	0	891.75 3.78319
12	70500	0	887.125 4.25551
13	71000	0	883.688 4.7791
14	71500	0	880.188 3.20583
15	72000	0	872.125 6.34306
16	72500	0	872.875 4.09077
17	73000	0	869.938 4.87941
18	73500	0	860.688 5.76323
19	74000	0	858.125 4.48435
20	74500	0	854.562 4.21261
21	75000	0	854.375 5.01093
22	75500	0	847.375 4.21122
23	76000	0	846.625 5.23062
24	76500	0	842.625 3.56853

Numerical Fit & Grading (.py)



Parameterized Record (.csv)

NTCx_sw_1_function_fitted_V_residue_std_full_range	2.47422921
NTCx_sw_1_function_xName	ADC_Ohms
NTCx_sw_1_function_ADC_Ohms_range_max	100000
NTCx_sw_1_function_suffix	NTCx_sw_1_function
NTCx_sw_1_function_fitted_V_range_min	0.411553934
NTCx_sw_1_function_mask_str	(END_Counts > 100 & END_
NTCx_sw_1_function_fitted_V_residue_std_target_range	0.007169923
NTCx_sw_1_function_fitted_V_residue_max_dev_target_range	0.043140791
NTCx_sw_1_function_yUnit	V
NTCx_sw_1_function_fitted_V_range_max	0.873929299
NTCx_sw_1_function_fitted_V_residue_max_dev_full_range	27.0844731
NTCx_sw_1_function_xUnit	Ohms
NTCx_sw_1_function_ADC_Ohms_range_min	29000
NTCx_sw_1_function_yName	fitted_V
HVRET_3_ramp_function_slope	0
HVRET_3_ramp_function_xName	ADC_uA_Expected
HVRET_3_ramp_function_END_Counts_residue_std_full_range	0
HVRET_3_ramp_function_END_Counts_range_max	1023
HVRET_3_ramp_function_suffix	HVRET_3_ramp_function
HVRET_3_ramp_function_intercept	0
HVRET_3_ramp_function_END_Counts_residue_std_target_rang	0
HVRET_3_ramp_function_mask_str	(END_Counts > 300 & END_
HVRET_3_ramp_function_yUnit	count
HVRET_3_ramp_function_ADC_uA_Expected_range_min	99.9725

Component Property& Test Run (.json)

ITk Production Database

Parent Directory

AMACv2a_0x0000200a_try2_AMAC_DAC_CALX_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_CALY_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALX_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALY_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_SHUNTX_RAMP_FUNCTION.json


```
{"component": "20USG000500876", "problems": false, "results": {}, "defects": [], "testTypeState":
"active", "date": "29.05.2020", "testType": "POWER_FUNCTIONS", "institution": "UPENN", "runNumber":
"try2", "comments": [], "properties": {"ADC_VDD_HI_V_OFF": 0.00030518, "BEST_WORKING_VDD": 1.23804,
"ADC_VDDLR": 1.47433, "ADC_AM_VDDLR_V": 1.4831, "ADC_AM_VDDLR_A": 0.0369268, "BEST_AM600BG": 0.620813,
"BEST_AMBG": 13, "ADC_VDD_HI_A_RO7_4HVO0": 0.00421381, "ADC_VDD_HI_A_RO7_4HVO1": 0.00493768,
"ADC_VDD_HI_A_RO7_4HVO2": 0.0048784, "ADC_VDD_HI_A_RO7_4HVO3": 0.0047892, "ADC_AM_VDD_HI_A": 1.49598e-05,
"ADC_VDD_HI_V_RO7_4HVO3": 3.14046, "ADC_VDD_HI_V_RO7_4HVO2": 3.14046, "ADC_VDD_HI_V_RO7_4HVO1": 3.14046,
"ADC_VDD_HI_V_RO7_4HVO0": 3.17639, "BEST_VDD": 1.23804, "ADC_AM_VDD_HI_V": 0.000228885, "BEST_RAMP": 0,
"BEST_SLOPE": 1.00578, "ADC_AM_LVDS_CM1": 0.69482, "ADC_AM_LVDS_CM0": 0.680705, "BEST_WORKING_VDDBG": 11,
"BEST_VDDBG": 11, "ADC_AM_VDCDC_V": 0.00015259, "ADC_VDD_HI_A_STD_RO7_4HVO2": 0.00104764,
"ADC_VDD_HI_A_STD_RO7_4HVO3": 0.00105412, "ADC_VDD_HI_A_STD_RO7_4HVO0": 0.000883412,
"ADC_VDD_HI_A_STD_RO7_4HVO1": 0.00105266, "ADC_VDD_HI_A_OFF": 0, "ADC_AM_VDCDC_A": 0.00015259}, "passed":
true}
```

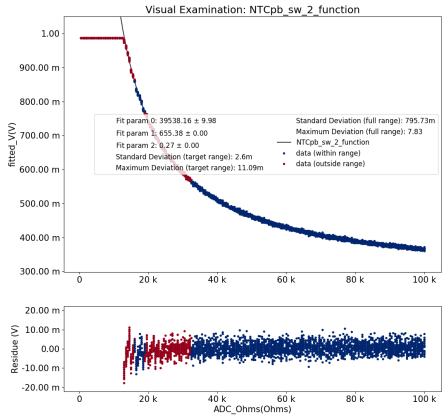
Data Flow from **Wafer Probing** to **Dicing & Database**

*All results except Raw Data are **available online!***

Raw Data (.csv)

	ADC_Ohms	END_NTC_SW	END_Count
1	65000	0	935.312 5.90253
2	65500	0	931.5 4.38748
3	66000	0	929.688 3.09675
4	66500	0	922.688 5.13224
5	67000	0	923 4.48609
6	67500	0	915.312 4.1791
7	68000	0	913.125 3.78938
8	68500	0	905 3.96863
9	69000	0	899.188 3.72858
10	69500	0	898.438 5.52233
11	70000	0	891.75 3.78319
12	70500	0	887.125 4.25551
13	71000	0	883.688 4.7791
14	71500	0	880.188 3.20583
15	72000	0	872.125 6.34306
16	72500	0	872.875 4.09077
17	73000	0	869.938 4.87941
18	73500	0	860.688 5.76323
19	74000	0	858.125 4.48435
20	74500	0	854.562 4.21261
21	75000	0	854.375 5.01093
22	75500	0	847.375 4.21122
23	76000	0	846.625 5.23062
24	76500	0	842.625 3.56853

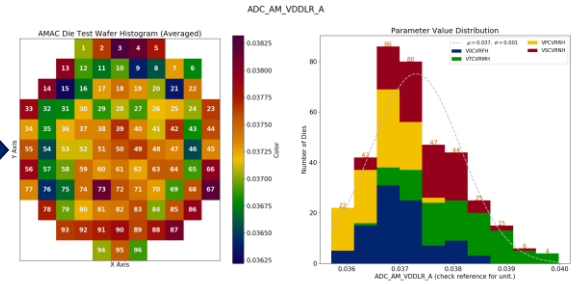
Numerical Fit & Grading (.py)



Parameterized Record (.csv)

NTCx_sw_1_function_fitted_V_residue_std_full_range	2.47422921
NTCx_sw_1_function_xName	ADC_Ohms
NTCx_sw_1_function_ADC_Ohms_range_max	100000
NTCx_sw_1_function_suffix	NTCx_sw_1_function
NTCx_sw_1_function_fitted_V_range_min	0.411553934
NTCx_sw_1_function_mask_str	(END_Counts > 100 & END_
NTCx_sw_1_function_fitted_V_residue_std_target_range	0.007169923
NTCx_sw_1_function_fitted_V_residue_max_dev_target_range	0.043140791
NTCx_sw_1_function_yUnit	V
NTCx_sw_1_function_fitted_V_range_max	0.873929299
NTCx_sw_1_function_fitted_V_residue_max_dev_full_range	27.0844731
NTCx_sw_1_function_xUnit	Ohms
NTCx_sw_1_function_ADC_Ohms_range_min	29000
NTCx_sw_1_function_yName	fitted_V
HVRET_3_ramp_function_slope	0
HVRET_3_ramp_function_xName	ADC_uA_Expected
HVRET_3_ramp_function_END_Counts_residue_std_full_range	0
HVRET_3_ramp_function_END_Counts_range_max	1023
HVRET_3_ramp_function_suffix	HVRET_3_ramp_function
HVRET_3_ramp_function_intercept	0
HVRET_3_ramp_function_END_Counts_residue_std_target_rang	0
HVRET_3_ramp_function_mask_str	(END_Counts > 300 & END_
HVRET_3_ramp_function_yUnit	count
HVRET_3_ramp_function_ADC_uA_Expected_range_min	99.9725

Wafer Statistics Distribution (.csv)



Component Property& Test Run (.json)

Parent Directory

AMACv2a_0x0000200a_try2_AMAC_DAC_CALX_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_CALY_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALX_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALY_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_SHUNTX_RAMP_FUNCTION.json


```
{"component": "20USG000500876", "problems": false, "results": {}, "defects": [], "testTypeState":
"active", "date": "29.05.2020", "testType": "POWER_FUNCTIONS", "institution": "UPENN", "runNumber":
"try2", "comments": [], "properties": {"ADC_VDD_HI_V_OFF": 0.00030518, "BEST_WORKING_VDD": 1.23804,
"ADC_VDDLR": 1.47433, "ADC_AM_VDDLR_V": 1.4831, "ADC_AM_VDDLR_A": 0.0369268, "BEST_AM600BG": 0.620813,
"BEST_AMBG": 13, "ADC_VDD_HI_A_RO7_4HVO0": 0.00421381, "ADC_VDD_HI_A_RO7_4HVO1": 0.00493768,
"ADC_VDD_HI_A_RO7_4HVO2": 0.0048784, "ADC_VDD_HI_A_RO7_4HVO3": 0.0047892, "ADC_AM_VDD_HI_A": 1.49598e-05,
"ADC_VDD_HI_V_RO7_4HVO3": 3.14046, "ADC_VDD_HI_V_RO7_4HVO2": 3.14046, "ADC_VDD_HI_V_RO7_4HVO1": 3.14046,
"ADC_VDD_HI_V_RO7_4HVO0": 3.17639, "BEST_VDD": 1.23804, "ADC_AM_VDD_HI_V": 0.000228885, "BEST_RAMP": 0,
"BEST_SLOPE": 1.00578, "ADC_AM_LVDS_CM1": 0.69482, "ADC_AM_LVDS_CM0": 0.680705, "BEST_WORKING_VDDBG": 11,
"BEST_VDDBG": 11, "ADC_AM_VDCDC_V": 0.00015259, "ADC_VDD_HI_A_STD_RO7_4HVO2": 0.00104764,
"ADC_VDD_HI_A_STD_RO7_4HVO3": 0.00105412, "ADC_VDD_HI_A_STD_RO7_4HVO0": 0.000883412,
"ADC_VDD_HI_A_STD_RO7_4HVO1": 0.00105266, "ADC_VDD_HI_A_OFF": 0, "ADC_AM_VDCDC_A": 0.00015259}, "passed":
true}
```


ITk Production Database

Data Flow from **Wafer Probing** to **Dicing & Database**

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Raw Data (.csv)

	ADC_Ohms	END_NTC_SW	END_Count
1	65000	0	935.312 5.90253
2	65500	0	931.5 4.38748
3	66000	0	929.688 3.09675
4	66500	0	922.688 5.13224
5	67000	0	923 4.48609
6	67500	0	915.312 4.1791
7	68000	0	913.125 3.78938
8	68500	0	905 3.96863
9	69000	0	899.188 3.72858
10	69500	0	898.438 5.52233
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13	71000	0	883.688 4.7791
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17	73000	0	869.938 4.87941
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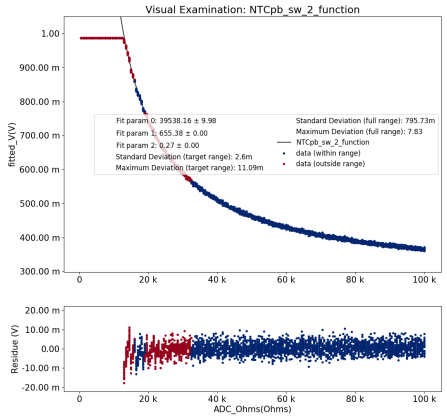
19	74000	0	858.125 4.48435
20	74500	0	854.562 4.21261
21	75000	0	854.375 5.01093
22	75500	0	847.375 4.21122
23	76000	0	846.625 5.23062
24	76500	0	842.625 3.56853

Numerical Fit & Grading (.py)



Parameterized Record (.csv)

NTCx_sw_1_function_fitted_V_residue_std_full_range	2.47422921
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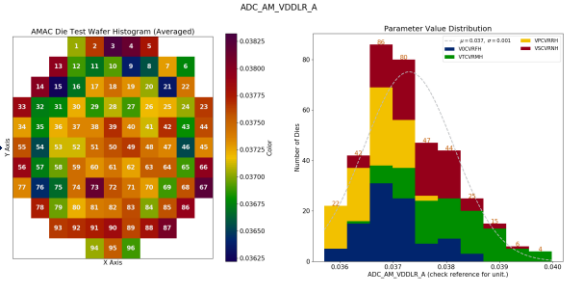
NTCx_sw_1_function_ADC_Ohms_range_max	100000
NTCx_sw_1_function_suffix	NTCx_sw_1_function
NTCx_sw_1_function_fitted_V_range_min	0.411553934
NTCx_sw_1_function_mask_str	(END_Counts > 100 & END_
NTCx_sw_1_function_fitted_V_residue_std_target_range	0.007169923
NTCx_sw_1_function_fitted_V_residue_max_dev_target_range	0.043140791
NTCx_sw_1_function_yUnit	V
NTCx_sw_1_function_fitted_V_range_max	0.873929299
NTCx_sw_1_function_fitted_V_residue_max_dev_full_range	27.0844731
NTCx_sw_1_function_xUnit	Ohms
NTCx_sw_1_function_ADC_Ohms_range_min	29000
NTCx_sw_1_function_yName	fitted_V
HVRET_3_ramp_function_slope	0
HVRET_3_ramp_function_xName	ADC_uA_Expected
HVRET_3_ramp_function_END_Counts_residue_std_full_range	0
HVRET_3_ramp_function_END_Counts_range_max	1023
HVRET_3_ramp_function_suffix	HVRET_3_ramp_function
HVRET_3_ramp_function_intercept	0
HVRET_3_ramp_function_END_Counts_residue_std_target_rang	0
HVRET_3_ramp_function_mask_str	(END_Counts > 300 & END_
HVRET_3_ramp_function_yUnit	count
HVRET_3_ramp_function_ADC_uA_Expected_range_min	99.9725

Wafer Statistics Distribution (.csv)



Component Property& Test Run (.json)

Parent Directory

AMACv2a_0x0000200a_try2_AMAC_DAC_CALX_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_CALY_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALX_RAMP_FUNCTION.json

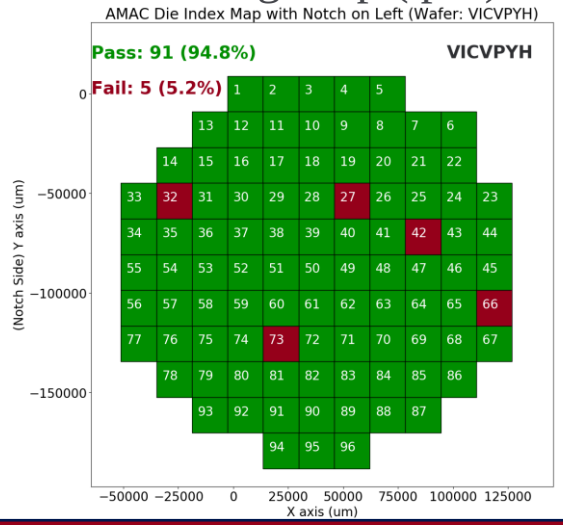
AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALY_RAMP_FUNCTION.json

AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_SHUNTX_RAMP_FUNCTION.json


```
{"component": "20USG000500876", "problems": false, "results": {}, "defects": [], "testTypeState":
"active", "date": "29.05.2020", "testType": "POWER_FUNCTIONS", "institution": "UPENN", "runNumber":
"try2", "comments": [], "properties": {"ADC_VDD_HI_V_OFF": 0.00030518, "BEST_WORKING_VDD": 1.23804,
"ADC_VDDLR": 1.47433, "ADC_AM_VDDLR_V": 1.4831, "ADC_AM_VDDLR_A": 0.0369268, "BEST_AM600BG": 0.620813,
"BEST_AMBG": 13, "ADC_VDD_HI_A_RO7_4HVO0": 0.00421381, "ADC_VDD_HI_A_RO7_4HVO1": 0.00493768,
"ADC_VDD_HI_A_RO7_4HVO2": 0.0048784, "ADC_VDD_HI_A_RO7_4HVO3": 0.0047892, "ADC_AM_VDD_HI_A": 1.49598e-05,
"ADC_VDD_HI_V_RO7_4HVO3": 3.14046, "ADC_VDD_HI_V_RO7_4HVO2": 3.14046, "ADC_VDD_HI_V_RO7_4HVO1": 3.14046,
"ADC_VDD_HI_V_RO7_4HVO0": 3.17639, "BEST_VDD": 1.23804, "ADC_AM_VDD_HI_V": 0.000228885, "BEST_RAMP": 0,
"BEST_SLOPE": 1.00578, "ADC_AM_LVDS_CM1": 0.69482, "ADC_AM_LVDS_CM0": 0.680705, "BEST_WORKING_VDDBG": 11,
"BEST_VDDBG": 11, "ADC_AM_VDCDC_V": 0.00015259, "ADC_VDD_HI_A_STD_RO7_4HVO2": 0.00104764,
"ADC_VDD_HI_A_STD_RO7_4HVO3": 0.00105412, "ADC_VDD_HI_A_STD_RO7_4HVO0": 0.000883412,
"ADC_VDD_HI_A_STD_RO7_4HVO1": 0.00105266, "ADC_VDD_HI_A_OFF": 0, "ADC_AM_VDCDC_A": 0.00015259}, "passed":
true}
```


ITk Production Database

Dicing Map (.pdf)



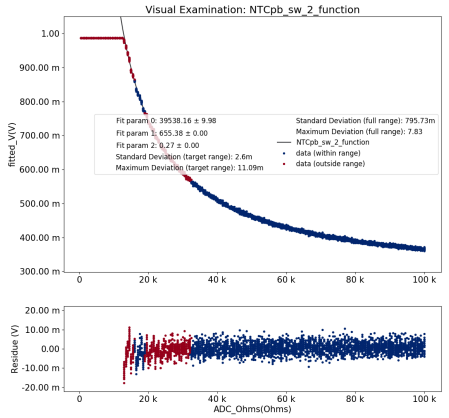
Data Flow from **Wafer Probing** to **Dicing** & **Database**

*All results except Raw Data are **available online!***

Raw Data (.csv)

	ADC_Ohms	END_NTC_SW	END_Count
1	65000	0	935.312 5.90253
2	65500	0	931.5 4.38748
3	66000	0	929.688 3.09675
4	66500	0	922.688 5.13224
5	67000	0	923 4.48609
6	67500	0	915.312 4.1791
7	68000	0	913.125 3.78938
8	68500	0	905 3.96863
9	69000	0	899.188 3.72858
10	69500	0	898.438 5.52233
11	70000	0	891.75 3.78319
12	70500	0	887.125 4.25551
13	71000	0	883.688 4.7791
14	71500	0	880.188 3.20583
15	72000	0	872.125 6.34306
16	72500	0	872.875 4.09077
17	73000	0	869.938 4.87941
18	73500	0	860.688 5.76323
19	74000	0	858.125 4.48435
20	74500	0	854.562 4.21261
21	75000	0	854.375 5.01093
22	75500	0	847.375 4.21122
23	76000	0	846.625 5.23062
24	76500	0	842.625 3.56853

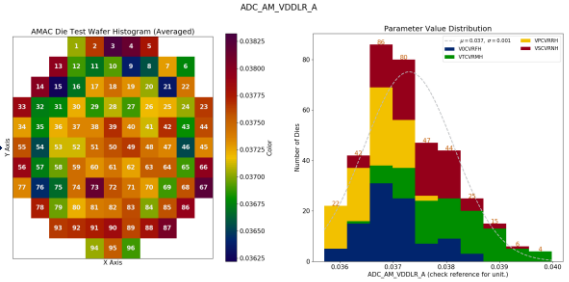
Numerical Fit & Grading (.py)



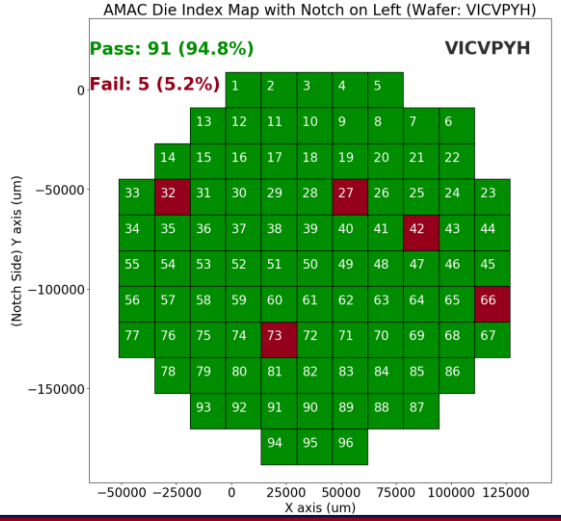
Parameterized Record (.csv)

NTCx_sw_1_function_fitted_V_residue_std_full_range	2.47422921
NTCx_sw_1_function_xName	ADC_Ohms
NTCx_sw_1_function_ADC_Ohms_range_max	100000
NTCx_sw_1_function_suffix	NTCx_sw_1_function
NTCx_sw_1_function_fitted_V_range_min	0.411553934
NTCx_sw_1_function_mask_str	(END_Counts > 100 & END_
NTCx_sw_1_function_fitted_V_residue_std_target_range	0.007169923
NTCx_sw_1_function_fitted_V_residue_max_dev_target_range	0.043140791
NTCx_sw_1_function_yUnit	V
NTCx_sw_1_function_fitted_V_range_max	0.873929299
NTCx_sw_1_function_fitted_V_residue_max_dev_full_range	27.0844731
NTCx_sw_1_function_xUnit	Ohms
NTCx_sw_1_function_ADC_Ohms_range_min	29000
NTCx_sw_1_function_yName	fitted_V
HVRET_3_ramp_function_slope	0
HVRET_3_ramp_function_xName	ADC_uA_Expected
HVRET_3_ramp_function_END_Counts_residue_std_full_range	0
HVRET_3_ramp_function_END_Counts_range_max	1023
HVRET_3_ramp_function_suffix	HVRET_3_ramp_function
HVRET_3_ramp_function_intercept	0
HVRET_3_ramp_function_END_Counts_residue_std_target_rang	0
HVRET_3_ramp_function_mask_str	(END_Counts > 300 & END_
HVRET_3_ramp_function_yUnit	count
HVRET_3_ramp_function_ADC_uA_Expected_range_min	99.9725

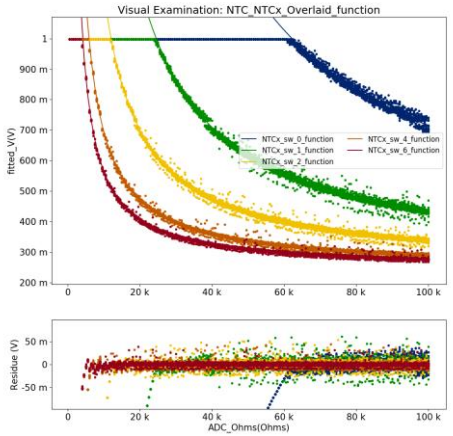
Wafer Statistics Distribution (.csv)



Dicing Map (.pdf)



Visual Examination (.png/.html)



Component Property& Test Run (.json)

Parent Directory

- AMACv2a_0x0000200a_try2_AMAC_DAC_CALX_RAMP_FUNCTION.json
- AMACv2a_0x0000200a_try2_AMAC_DAC_CALY_RAMP_FUNCTION.json
- AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALX_RAMP_FUNCTION.json
- AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_CALY_RAMP_FUNCTION.json
- AMACv2a_0x0000200a_try2_AMAC_DAC_INTERNAL_SHUNTX_RAMP_FUNCTION.json


```
{"component": "20USG000500876", "problems": false, "results": {}, "defects": [], "testTypeState":
"active", "date": "29.05.2020", "testType": "POWER_FUNCTIONS", "institution": "UPENN", "runNumber":
"try2", "comments": [], "properties": {"ADC_VDD_HI_V_OFF": 0.00030518, "BEST_WORKING_VDD": 1.23804,
"ADC_VDDLR": 1.47433, "ADC_AM_VDDLR_V": 1.4831, "ADC_AM_VDDLR_A": 0.0369268, "BEST_AM600BG": 0.620813,
"BEST_AMBG": 13, "ADC_VDD_HI_A_RO7_4HVO0": 0.00421381, "ADC_VDD_HI_A_RO7_4HVO1": 0.00493768,
"ADC_VDD_HI_A_RO7_4HVO2": 0.0048784, "ADC_VDD_HI_A_RO7_4HVO3": 0.0047892, "ADC_AM_VDD_HI_A": 1.49598e-05,
"ADC_VDD_HI_V_RO7_4HVO3": 3.14046, "ADC_VDD_HI_V_RO7_4HVO2": 3.14046, "ADC_VDD_HI_V_RO7_4HVO1": 3.14046,
"ADC_VDD_HI_V_RO7_4HVO0": 3.17639, "BEST_VDD": 1.23804, "ADC_AM_VDD_HI_V": 0.000228885, "BEST_RAMP": 0,
"BEST_SLOPE": 1.00578, "ADC_AM_LVDS_CM1": 0.69482, "ADC_AM_LVDS_CM0": 0.680705, "BEST_WORKING_VDDBG": 11,
"BEST_VDDBG": 11, "ADC_AM_VDCDC_V": 0.00015259, "ADC_VDD_HI_A_STD_RO7_4HVO2": 0.00104764,
"ADC_VDD_HI_A_STD_RO7_4HVO3": 0.00105412, "ADC_VDD_HI_A_STD_RO7_4HVO0": 0.000883412,
"ADC_VDD_HI_A_STD_RO7_4HVO1": 0.00105266, "ADC_VDD_HI_A_OFF": 0, "ADC_AM_VDCDC_A": 0.00015259}, "passed":
true}
```


ITk Production Database

ITk Production Database

https://itkpd-test.unicorncollege.cz/

Component Details

Show details of selected Component of the Inner Tracker.

20USG000501034

AMAC Chip - AMACv2a

Basic Properties

ATLAS SERIAL NUMBER
20USG000501034

COMPONENT TYPE
AMAC Chip AMAC

TYPE
AMACv2a

CURRENT STAGE
Probed at University of Pennsylvania

CURRENT LOCATION
University of Pennsylvania UPENN

PROJECT
Strips

SUBPROJECT
Strip general

REGISTRATION
03.06.2020 11:44
Sicong Lu

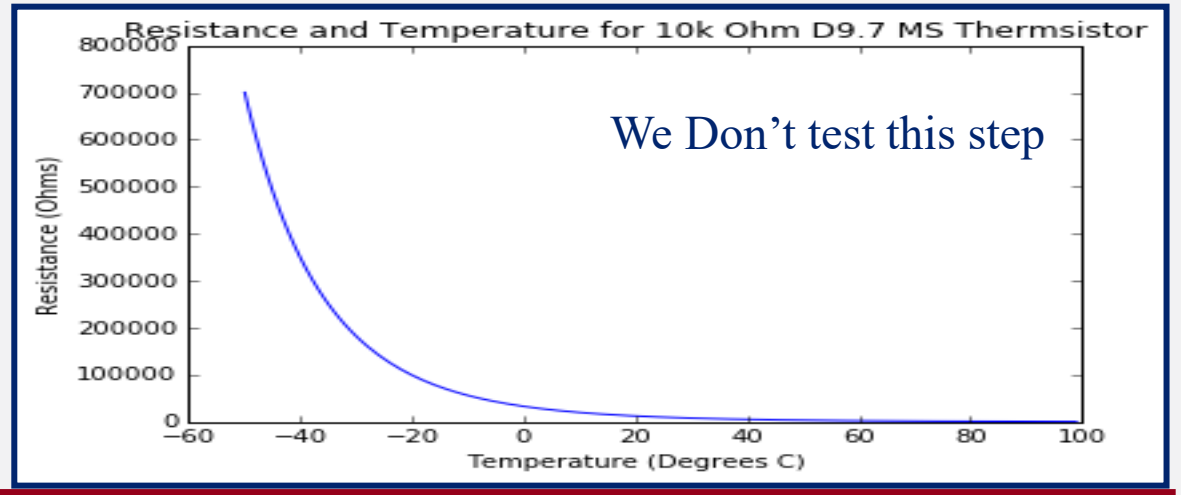
OWNER INSTITUTE
University of Pennsylvania UPENN

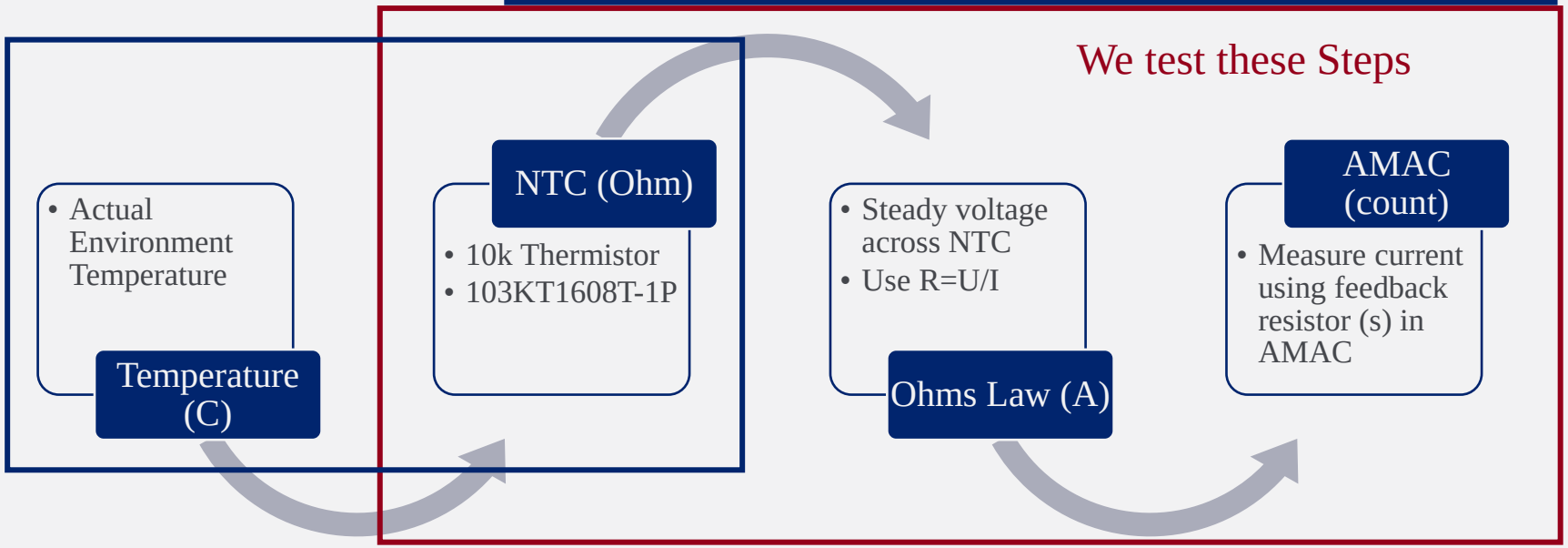
SHIPMENT DESTINATION
No current shipment destination

a73982646f2503de102f1bbe27254ca9

Example Temperature Measurement

- The way we measure the temperature:
  - Use industrial NTC
  - Measure Resistance through current
  - Measure Current (through resistor to voltage) by AMAC
- Simple Circuit:
  - Simple amplifier
  - Can measure resistance



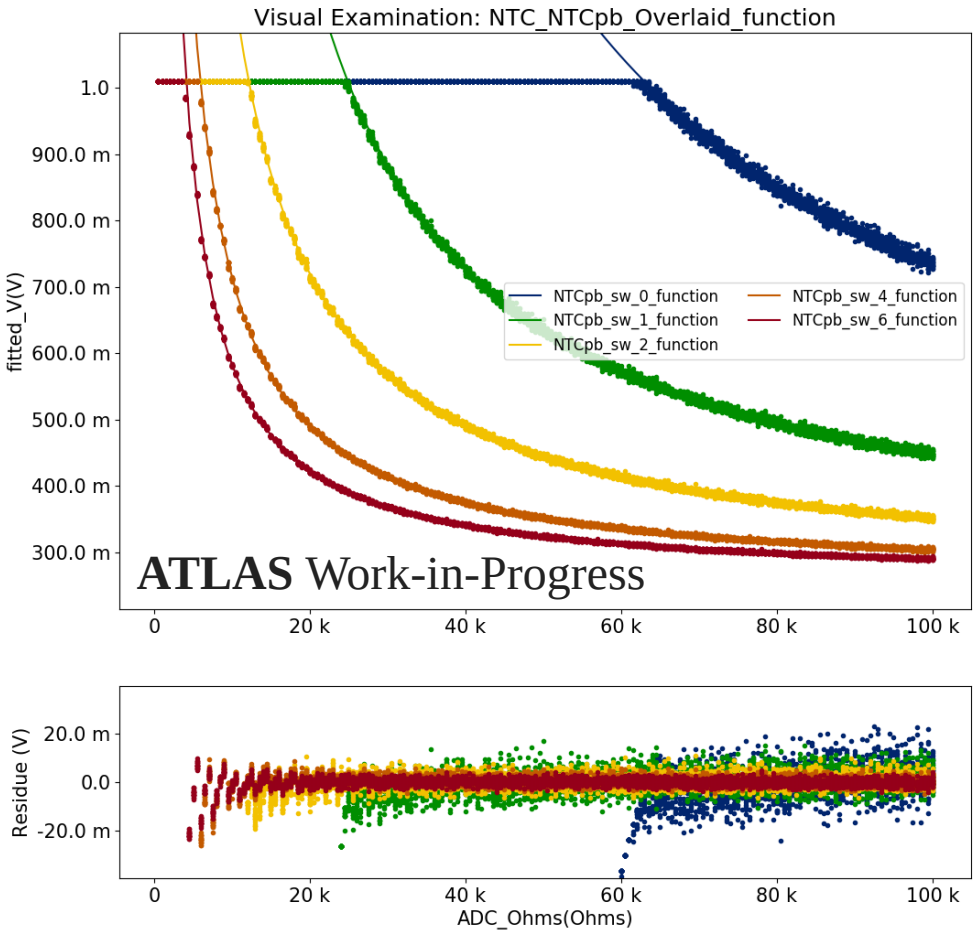


We also measure:
BPol12V by PTAT
(proportional to absolute temperature)
AMAC by CTAT
(complementary to absolute temperature)

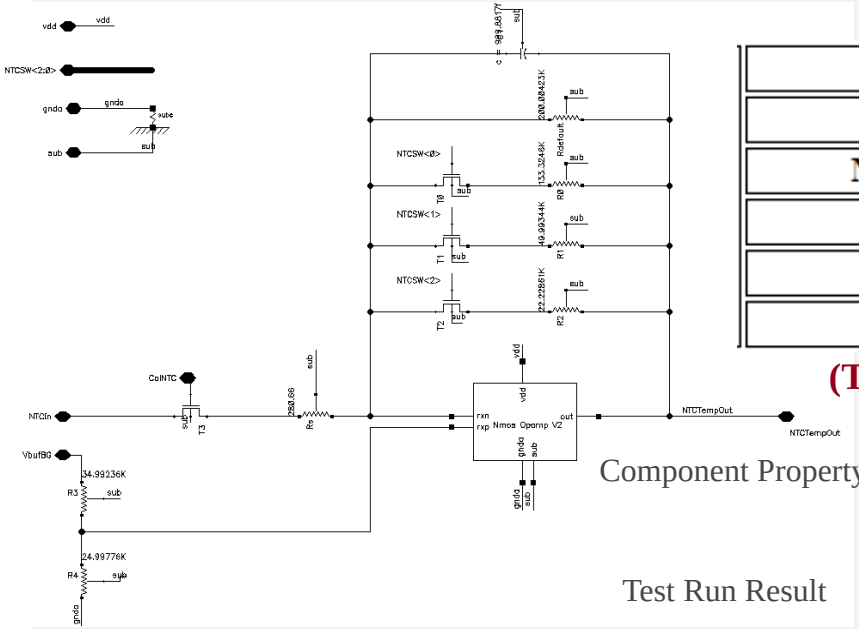
Example: Validation & Fit

Plot Fit by Simplified Circiuit Model:

$$V_{\text{measure}} = 250\text{mV}\frac{R_{\text{sw}}}{\boldsymbol{R_{\text{NTC}}} + R_{\text{internal}}} + V_{\text{zero}}$$

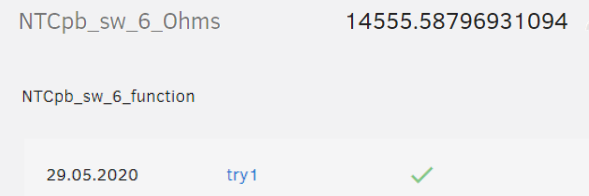


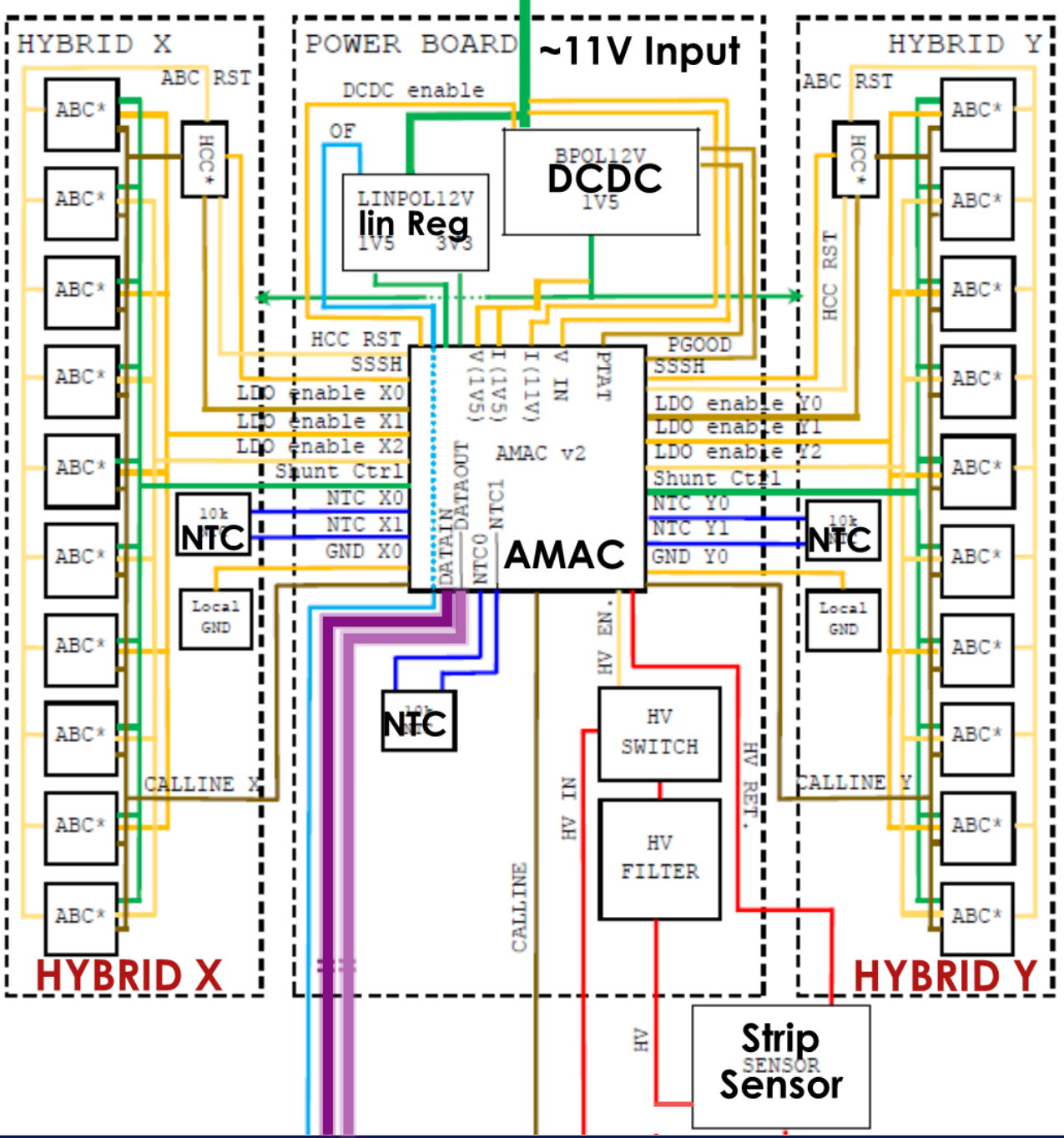
- Given the simple design, we can perform numerical fit for the individual resistance
- We could also use this to verify the how well is the manufacturer on producing resistors



NTCx_R_internal	171.65
NTCx_V_zero	243.85m
NTCx_Rdefault_Ohms	188.77k
NTCx_R0_Ohms	123.86k
NTCx_R1_Ohms	45.87k
NTCx_R2_Ohms	20.31k

(They agree with the designed value!)





Reset in:
→SSSHx
→SSSHy
→ OFIn;
Resets Out
2 HCC Reset→
OFOut→
Voltage DAC:
Calx/y →;
Shuntx/y →;
Communications lines:
→ **Command Data In**;
Command Data Response →

- For each successful **AMAC - Test Run**:
  - 60 characterization **properties**
  - 72 **test** with fits and analysis (most of them has)
    - 8 **test parameters** per **test**
      - Each is an array of some type
    - 18 **test properties** per **test**
    - See next slides for example
- Database Structure Visualization ⇒
  - The center represent AMAC **Component**
  - Each arrow represent an object in database
    - Parameters, properties, tests, etc
  - Each cluster is a **TestType**