Readout Tests of the ATLAS ITk Pixel System Toward the HL-LHC Upgrade

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ATLAS Detector: ITk Upgrade

- The entire tracking system of the ATLAS detector will be replaced during the LHC Phase II shutdown (~2025y) by an all-silicon detector called the Inner Tracker (ITk).
- The new Inner Tracker will consist of 5 innermost barrel / many rings pixel layers and 4 barrel / 6 end-caps strip layers.
- A readout speed of up to 5 $Gbit/s$ per data link will be needed in the innermost layer.
- Various readout systems are under development and must be tested.
- Test stands for each readout system must be assembled, and results of tests must be compared.
- SLAC is building prototypes of the upgraded ITk for integration and readout tests.

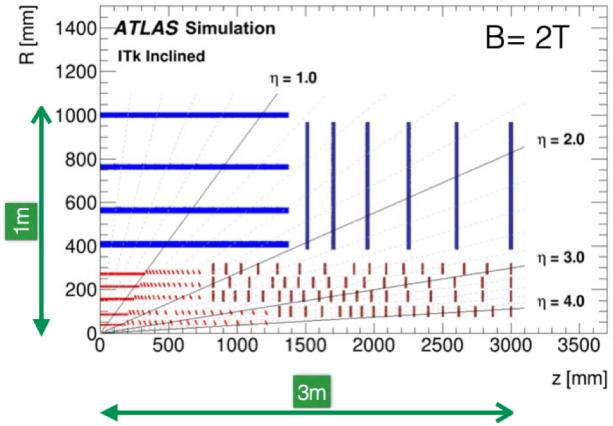


Figure: ITk structure

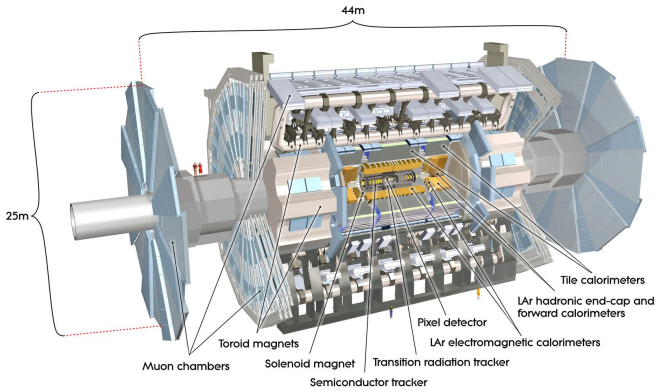


Figure: The ATLAS detector

RD53a Readout Chip

- A new pixel readout chip is being developed by the RD53 community.

- Pixel readout chip serves as an analog to digital converter:
  - Receives trigger and command.
  - Collects charge deposited in each pixel of a sensor and transforms it to digital signal.
  - Send the digital signal to the computer/server.

- Front-end (FE) matrix of RD53a has dimensions of 400 columns by 192 rows. Its analog matrix has three regions with different front-end designs.

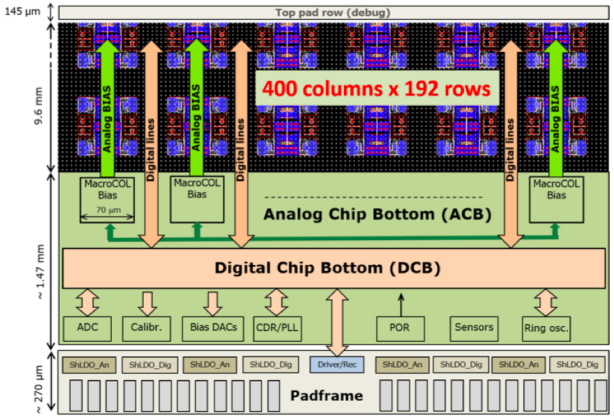


Figure: RD53a functional view

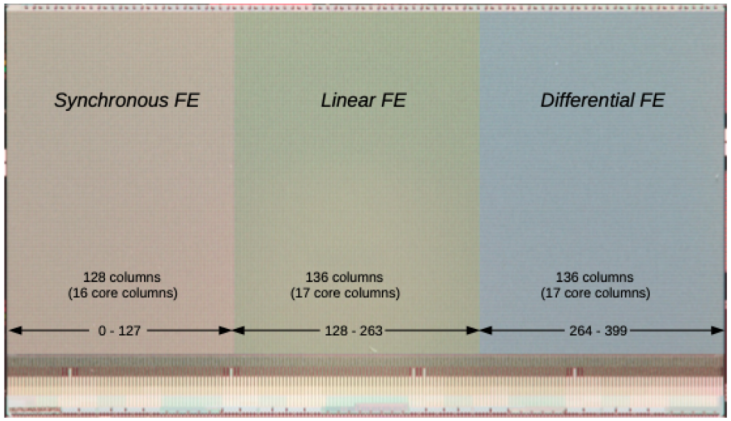
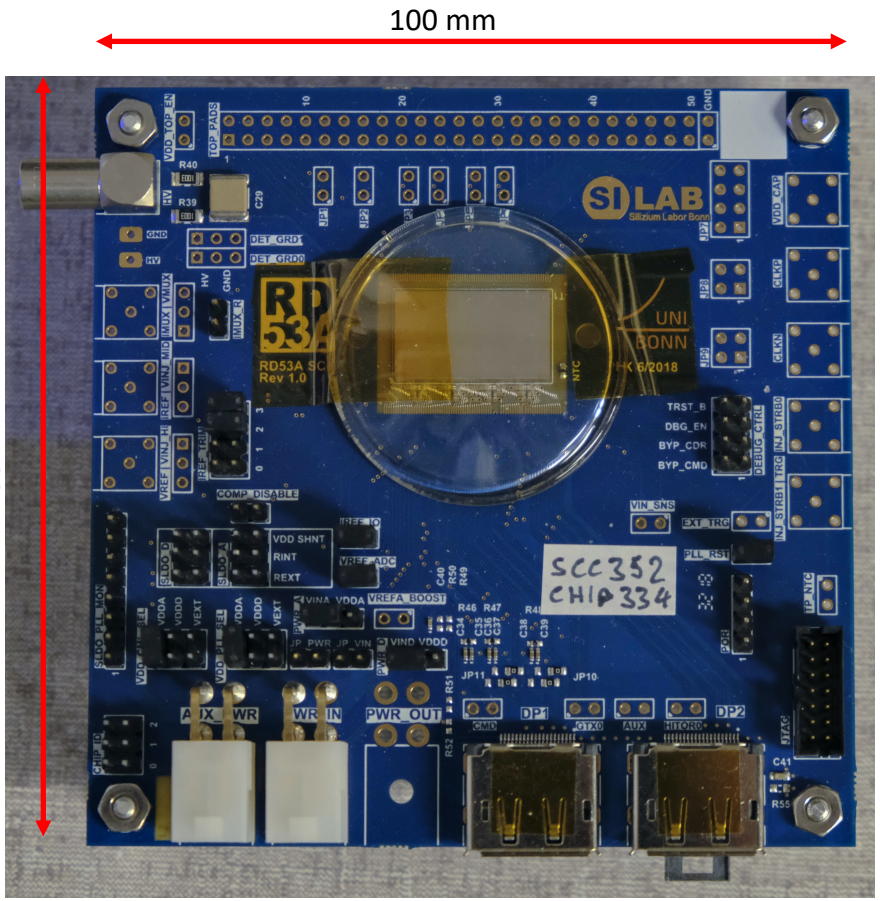
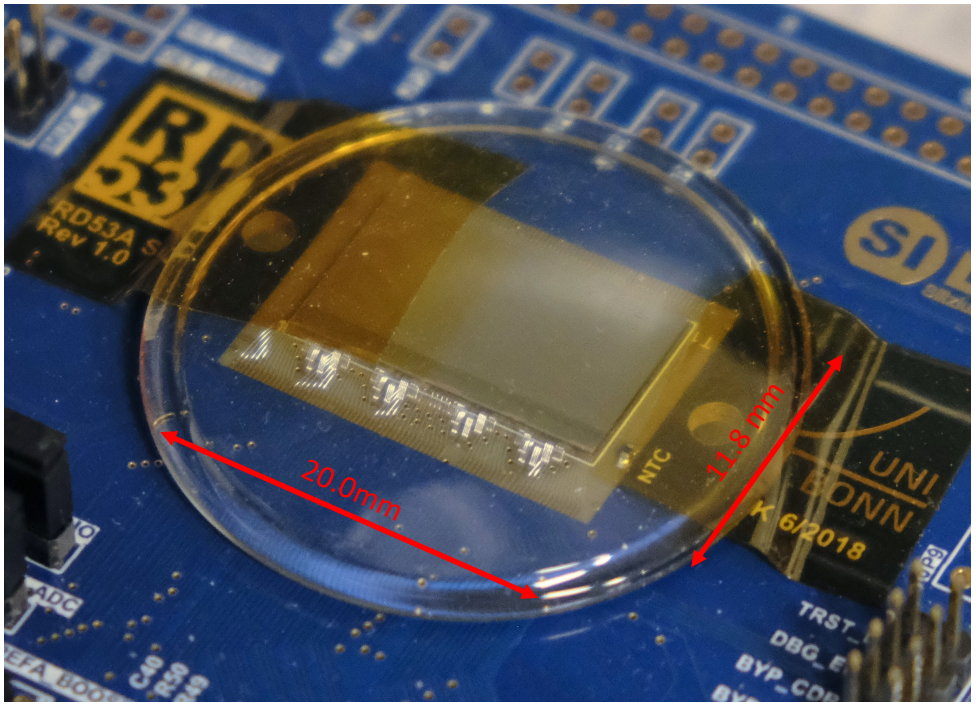


Figure: Arrangement of FE flavors in RD53a

RD53a Single Chip Card

- Left: RD53a Single Chip Card (testing board).
- Right: RD53a chip.





YARR Software

- **YARR** – Yet Another Rapid Readout.
  - Originally designed for FE-I4 readout chips and works with RD53a and ITkPix.v1 too.

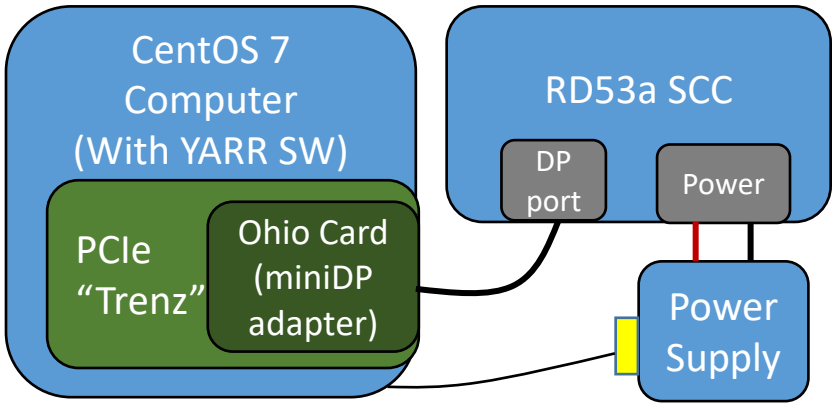
- **Current readout scheme:**
  - Most of the functionality is contained inside the firmware running on FPGA.
  - The computer controlling the cards is performing tasks which mainly consist of managing configurations and downloading scan loops to the scan engine.

- **YARR** decouples firmware and software, and moves more intelligence to the latter:
  - It is easer to work with software than firmware for developers and testers.
  - Flexibility of the software results into support of wide range of FPGA platforms.

- **Actions/Scans:**
  - FE tuning.
  - Digital scan.
  - Analog scan (threshold scan, cross-talk scan)

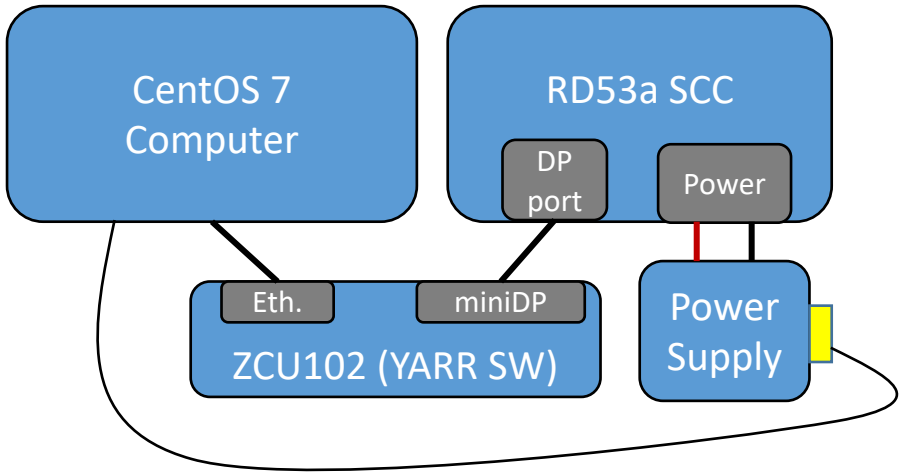
YARR (HW) Test Stand at SLAC

- **Purpose:** quality control of RD53a modules before loading the on a mechanical support.
- **Hardware:** CentOS 7 machine equipped with up to 4 PCIe cards.
  - PCIe: Trenz TEF-1001 with Ohio cards.
  - One Ohio card hosts 4 miniDP ports, thus up to 16 connections in total.
  - However chips connected to different Trenz cards cannot be scanned simultaneously.
- **Software:** YARR.
- **Status:**
  - Works at 640 Mbps.



RCE Test Stand

- **RCE** stands for Reconfigurable Cluster Element.
- **Purpose:** cross-check info between different readout systems; use as a backup option.
- **Hardware:** ZCU102.
  - ZCU102 is an evaluation board with different interfaces, ports and transceivers.
  - FPGA logic provides a flexible prototyping platform.
- **Software:** YARR.
  - Optimized for RCE.



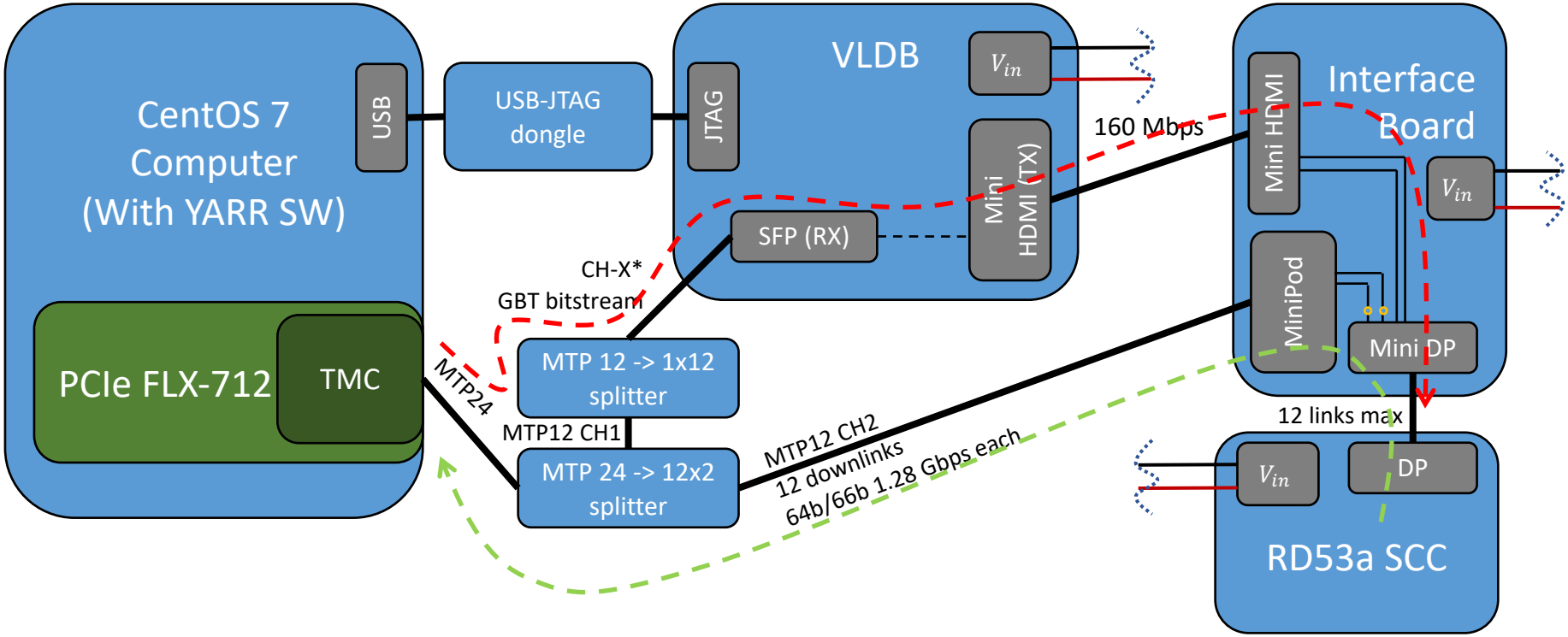
Direct FELIX Readout System

- **FELIX** – Front-End Link eXchange.

- **Definition:**
  - FELIX is a new detector readout component being developed as part of the ATLAS upgrade effort.
  - FELIX is designed to act as a data router, receiving packets from detector front-end electronics and send it to programmable peers on a commodity high bandwidth network.

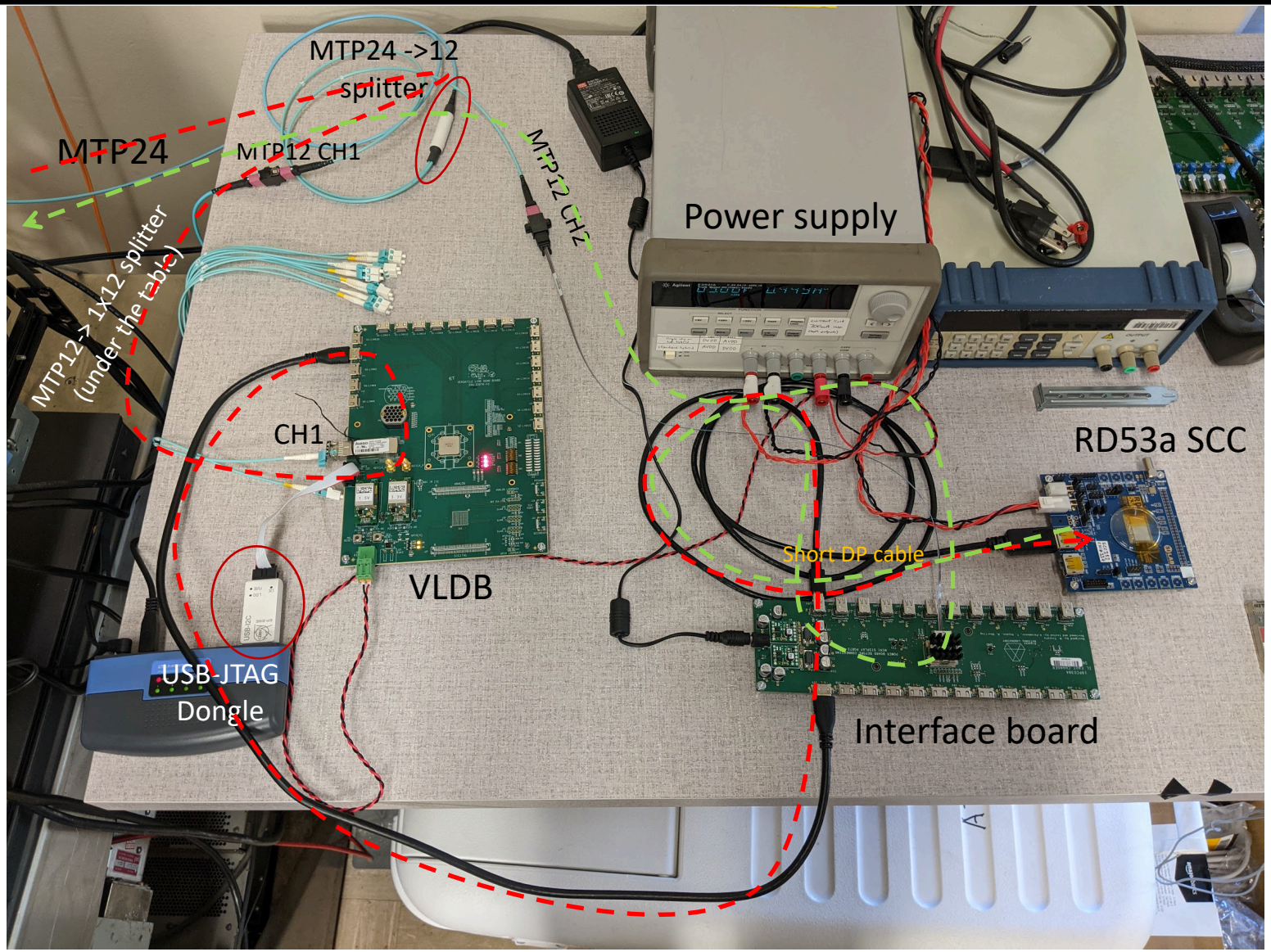
- **Motivation:**
  - The idea behind FELIX is to unify all readout across one well supported and flexible platform, compared to previous detector readout implementations relied on diverse custom hardware platforms.
  - Detector data processing will be implemented in software hosted by commodity server systems subscribed to FELIX data, compared to previous detector FPGA-based data processing.

Direct FELIX Test Stand for 24 Links

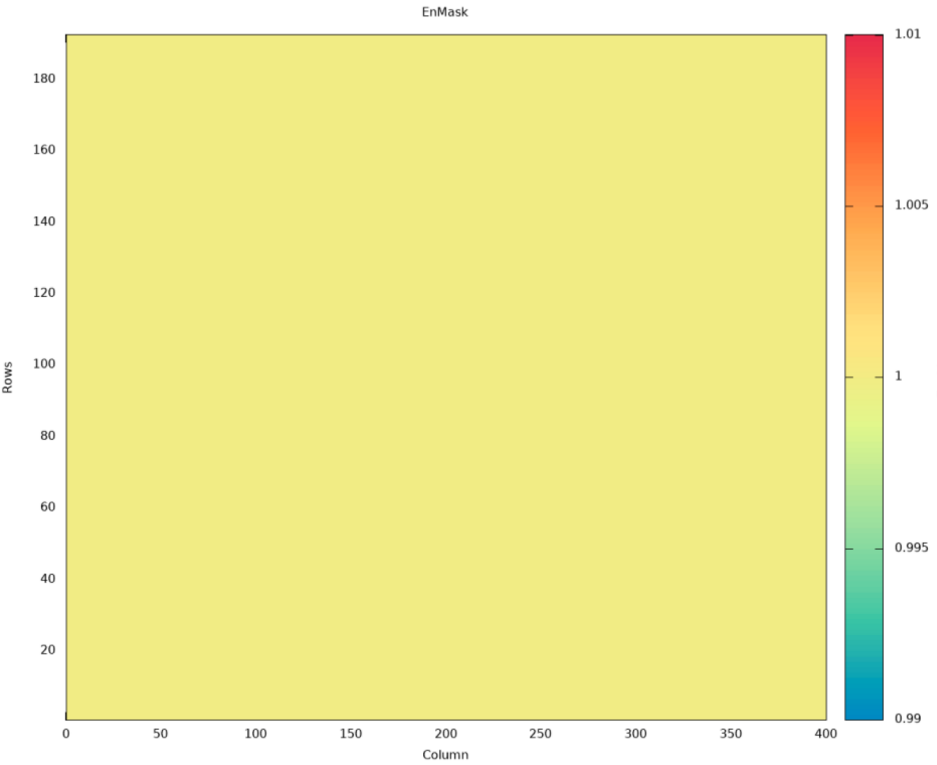


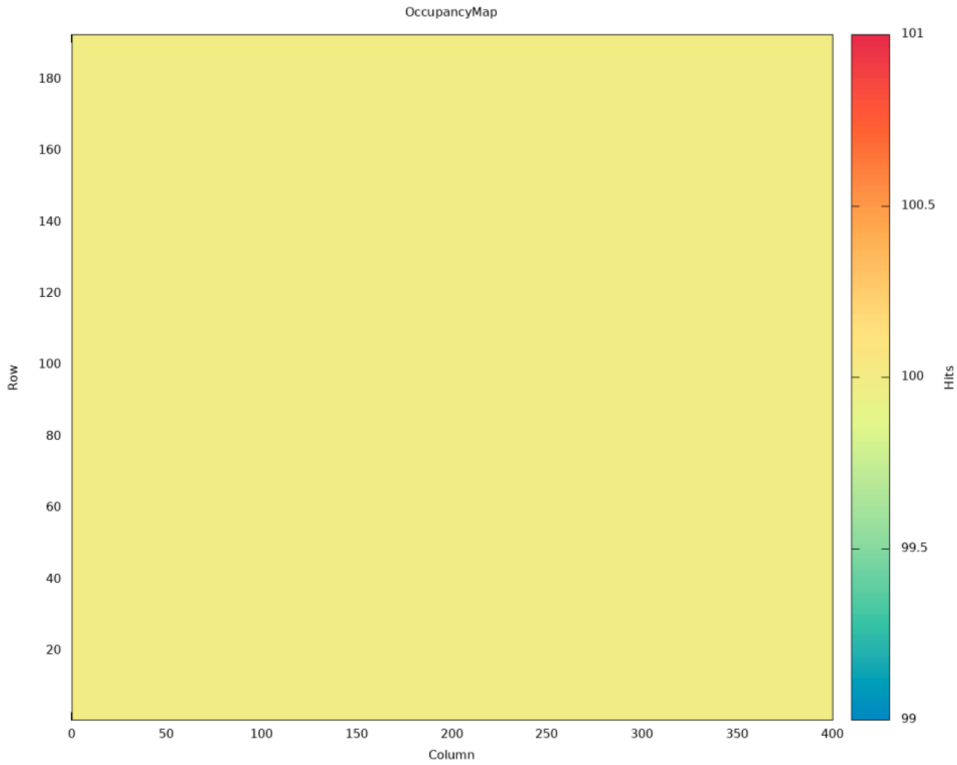
- FELIX test stand components:
  - A computer with CentOS7.
  - PCIe FLX-712 (aka BNL-712) with Timing Mezzanine Card (TMC) that has two MTP with 48 or 24 channels: 8 or 4 miniPODs installed on FLX card.
  - Versatile Link Demonstrator Board –VLDB.
  - Interface board.

Direct FELIX Test Stand at SLAC



Digital Scan: Updated YARR SW





- YARR SW has been optimized for FELIX direct readout system: git.
- Left: Enable mask.
- Right: Occupancy map.
- FELIX + short cable, frequency 30kHz.

Readout Tests with Long Cables

Direct FELIX Signal Quality Measurements

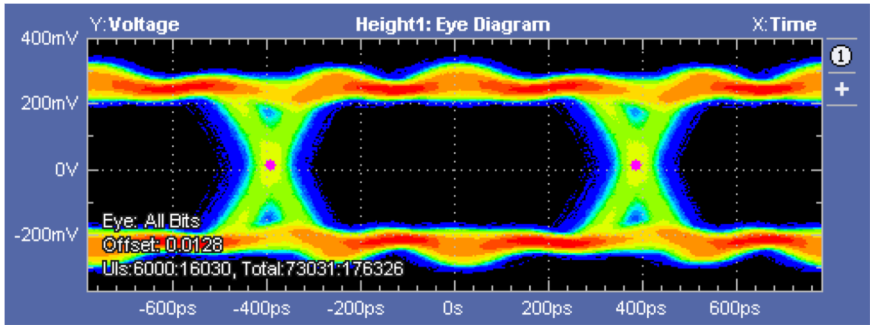
- Preliminary specs: the expected maximal loss of the whole final readout chain (from the pixel module to a digital-optical converter) is $18\ dB$ before irradiation.

- Use different cables to test the readout system with different losses in Data channel: ≤3dB, 6dB, 12dB, 18dB.

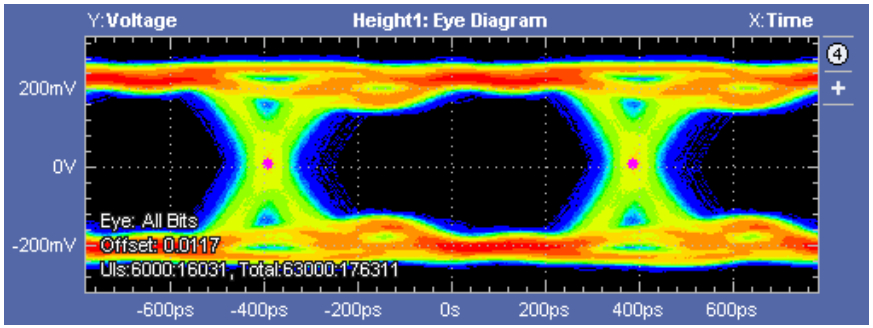
- Parameters of evaluation of the readout system:
  - Measure eye diagram on RD53a SCC and on the interface board.
  - Monitor FELIX's registers (clock and 64b/66b decoding).
  - Run the digital scan.

Data Eye Diagrams with Different Loss Cables: FELIX

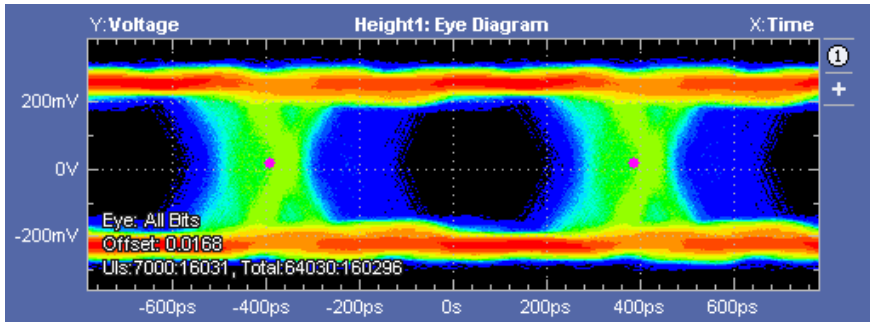
- Top row diagrams: short cable with loss<3dB, reference measurement
- Bottom row diagrams: 12dB loss cables.
- The digital scan was successful only with loss in cables ≤6dB.



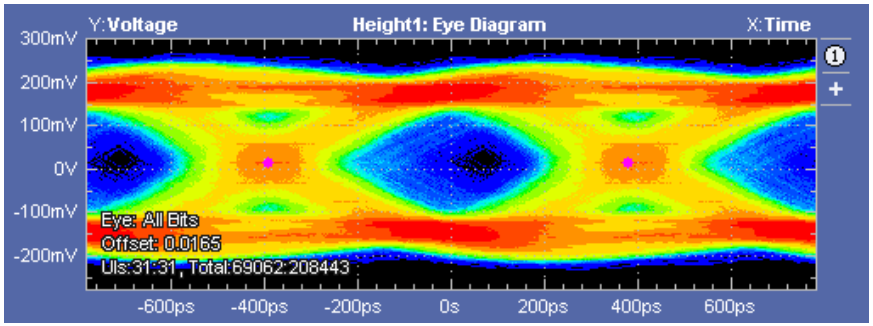
RD53a SCC, reference signal measurement



Interface, reference signal measurement



RD53a SCC, 12dB cables signal measurement

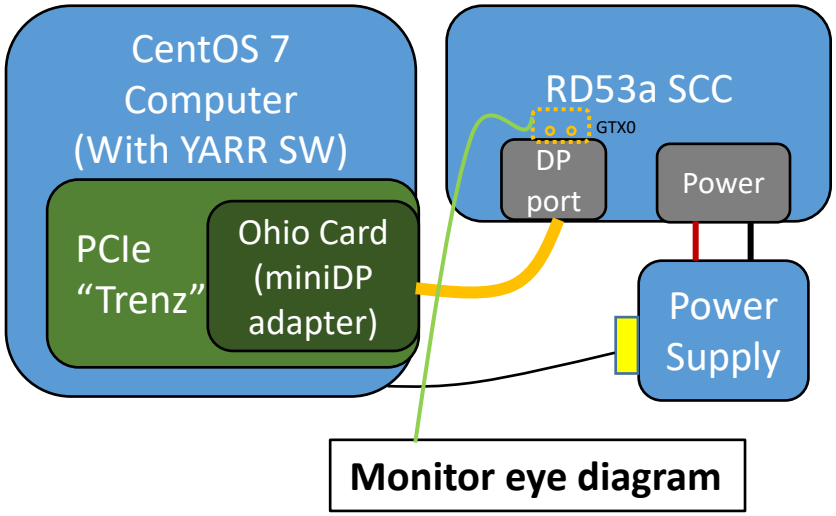


Interface, 12dB cables signal measurement

YARR Test Stand Signal Quality Measurements

- Use different cables (orange): ≤3dB, 6db, 12dB, 18dB.

- Parameters of evaluation of the readout system:
  - Measure eye diagram on RD53a SCC.
  - Run the digital scan.



- <u>The digital scan ran successfully for measurements with ≤6dB loss cables only.</u>

Summary and Conclusions

- YARR, direct FELIX and RCE readout test stands were assembled, configured and are operating at SLAC for pixel readout tests for the ATLAS ITk upgrade.
- Readout performance of the readout systems with different signal loss in cables was tested.

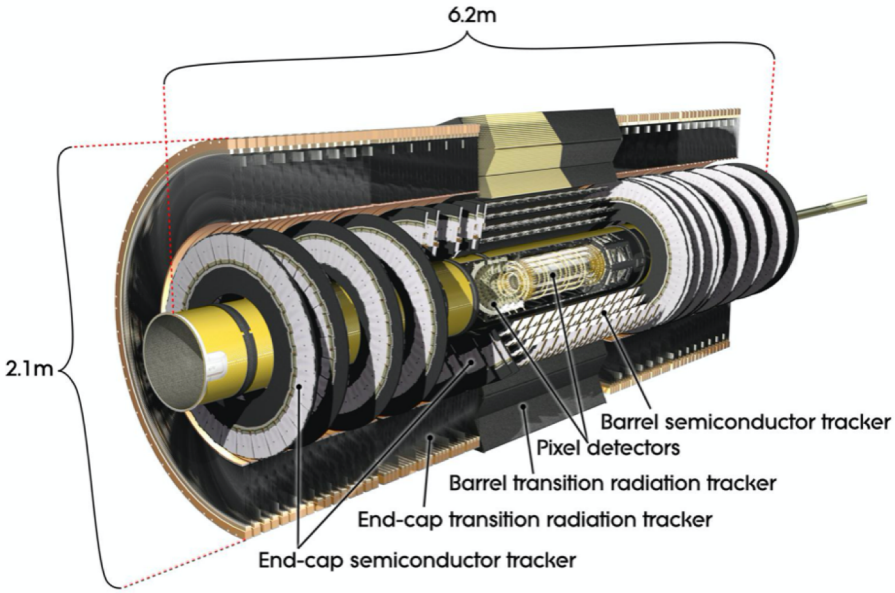
- Summary of the readout performance is given in the chart below:
  - * RCE performance was studied by SLAC group.

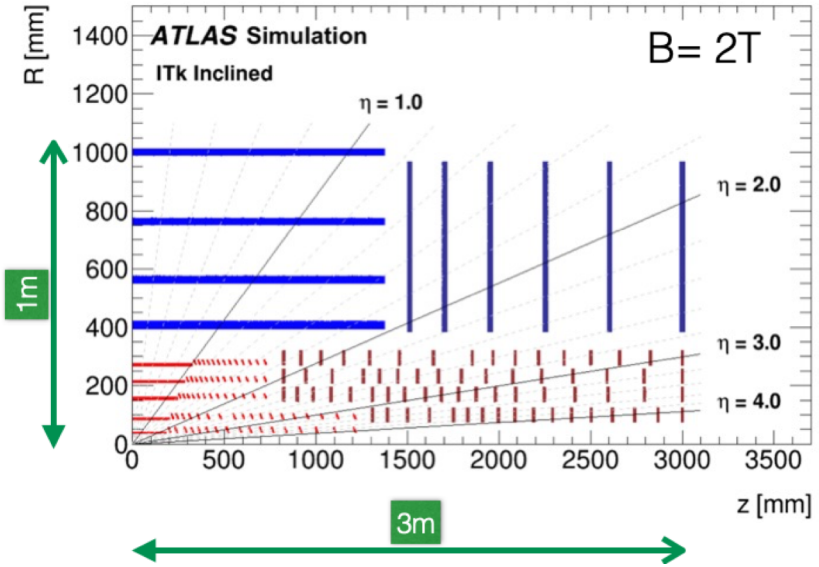
	<3dB	6dB	12dB	18dB
FELIX	works	works	fails	**fails**
YARR	works	works	fails	**fails**
RCE*	works	works	works	**works**

- **RCE readout system can be used as the baseline readout system for ITk prototypes at SLAC.**
- **FELIX readout system will be upgraded and studied further.**

Backup Slides

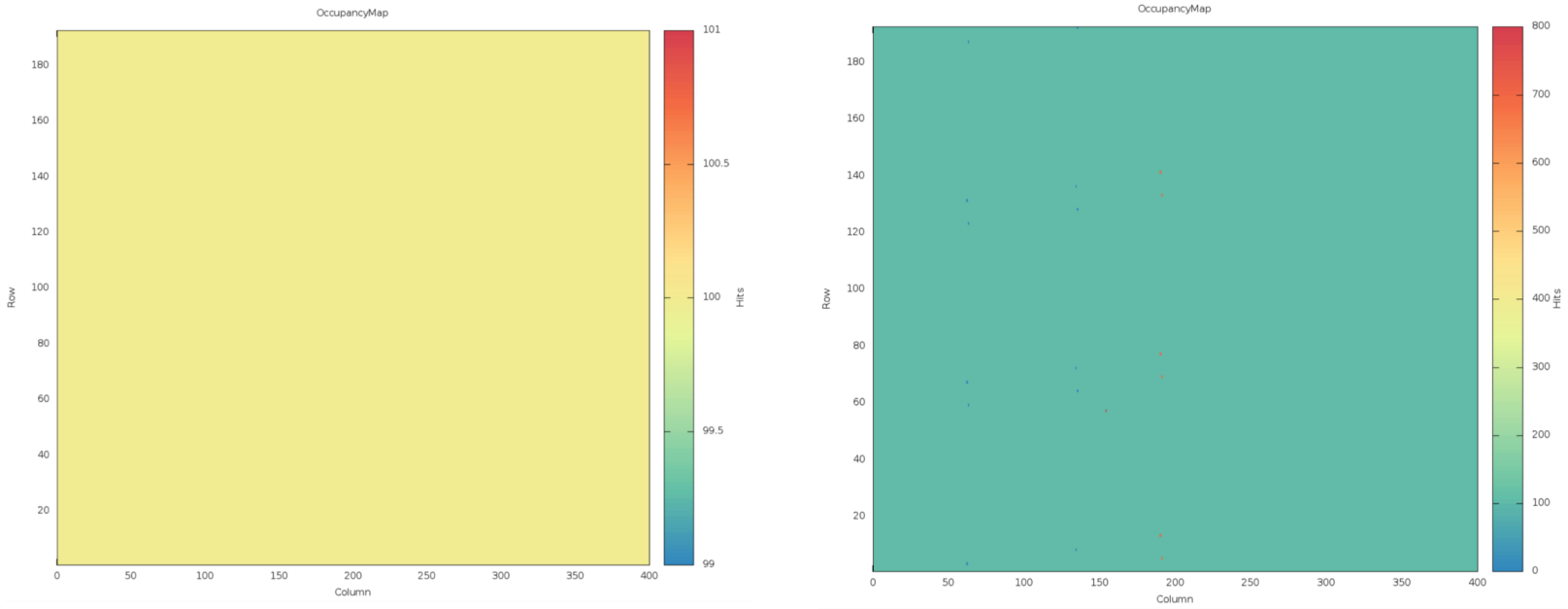
Current Inner Tracker vs. ITk





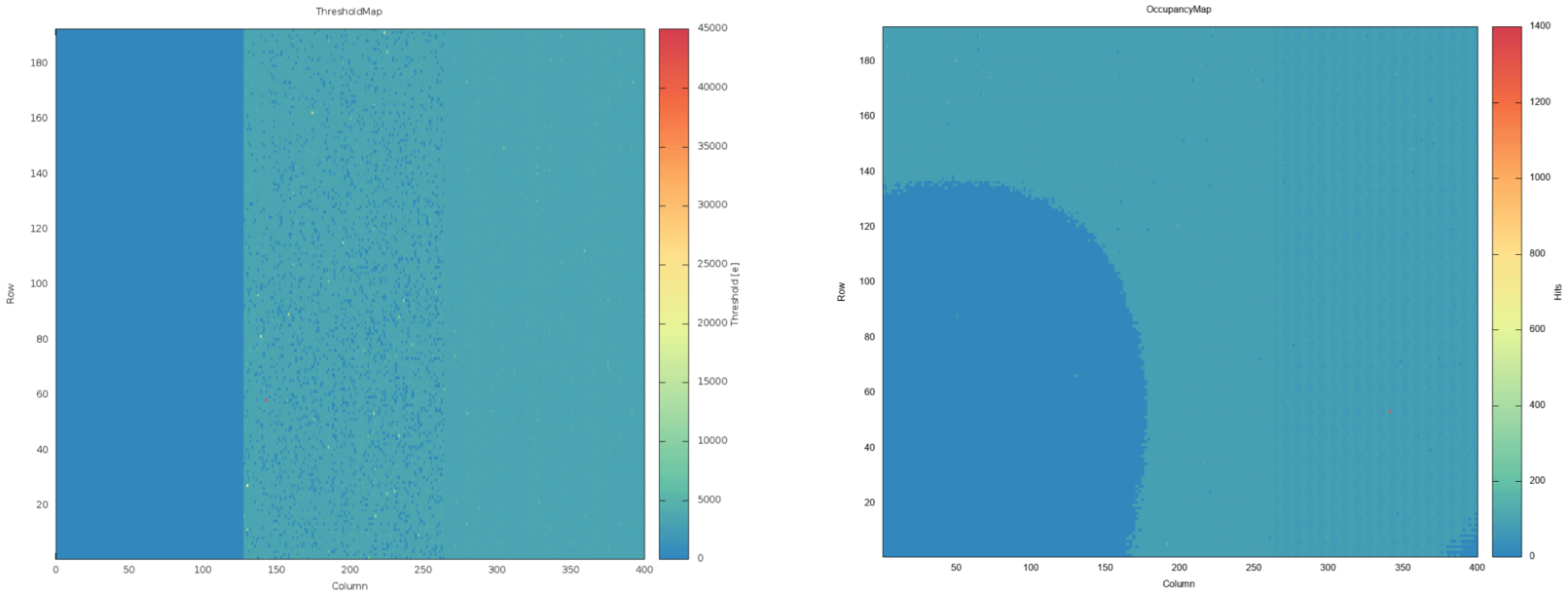
- Left: current inner tracker.
- Right: new all-silicon inner tracker.
- The outermost layer named Transition Radiation Tracker will be completely removed.
- More pixel and strips layer will be added.

YARR (SW) Digital and Analog Scans Results (RD53a)



- YARR documentation histograms: Trenz PCIe card, RD53a SCC.
- Left: occupancy map of a digital scan.
  - No “hot” pixels are expected.
- Right: occupancy map of an analog scan.
  - A few randomly distributed “hot” pixels might be present.

YARR (SW) Threshold and DBB Scans Results (RD53a)



- YARR documentation histograms: Trenz PCIe card, RD53a SCC.
- Left: Threshold Scan.
  - Synchronous FE is disabled.
  - Some variation in pixels' threshold is expected.
- Right: Disconnected bump bounds scan.
  - Uses crosstalk scan to identify pixels without any crosstalk - which are likely be due to disconnected bumps.

Signal Loss in Cables

- Signal losses in cables will affect the readout; the goal of this study is to find out the maximal loss of a signal in cables, which still allows to read out the module.

- RD53 is connected to the readout system with a DP-miniDP cable.
  - Both Data (from RD53a) and CMD (to RD53a) are differential signals.

- Signal quality deteriorates in cables:
  - Jitter increases.
  - Depends on the cable quality and length.
  - Depends on signal frequency.

- Loss in cables is calculated in dB:

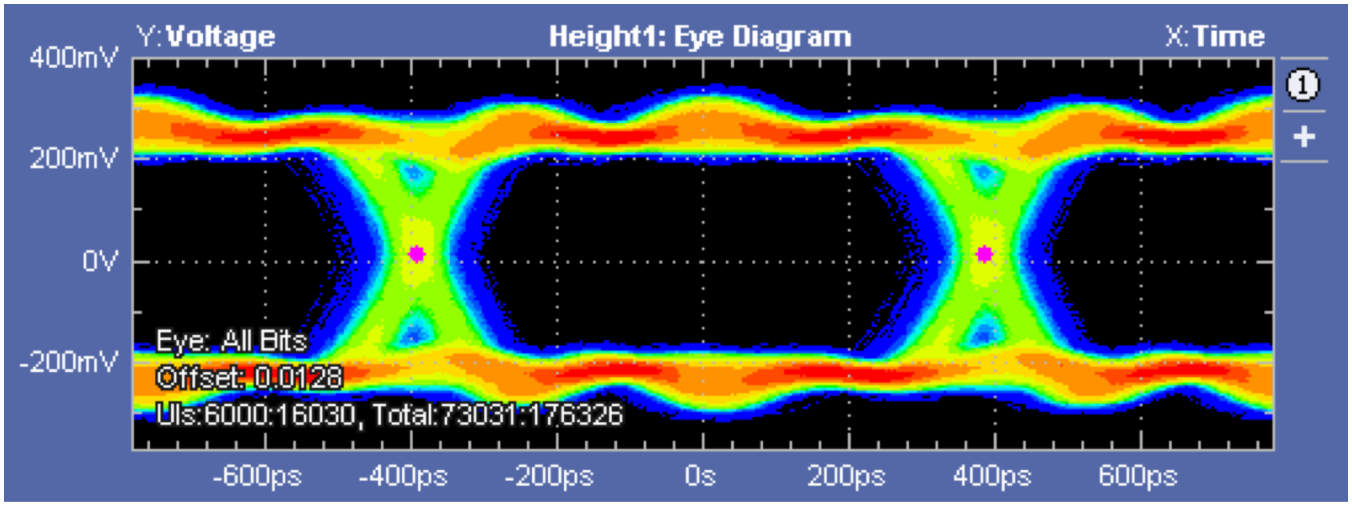
$$dB = 10 * \log_{10}\left(\frac{P_{out}}{P_{in}}\right) = 20 * \log_{10}\left(\frac{V_{out}}{V_{in}}\right);$$

$$\frac{V_{out}}{V_{in}} = 10^{dB/20};$$

RD53a: Reference Measurement

- Measurement: at RD53a SCC.
- Cable: loss<3dB in Data channel – the smallest loss cable that we have.

- Plot: eye diagram:
  - Jitter is due to RD53a itself (RD53b has smaller intrinsic jitter).
  - Eye is open.

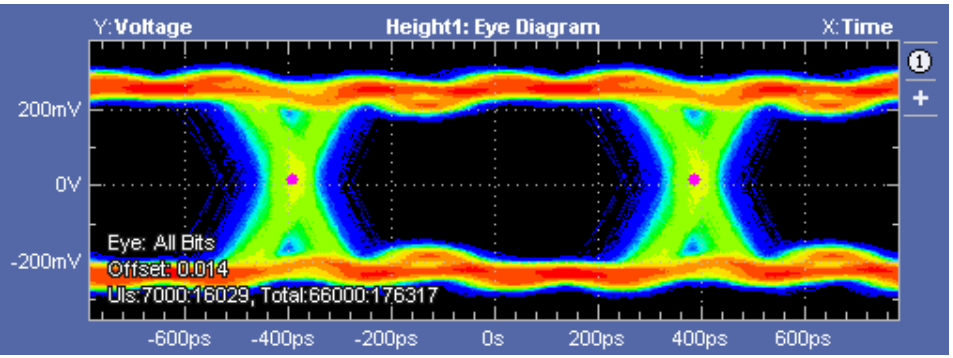


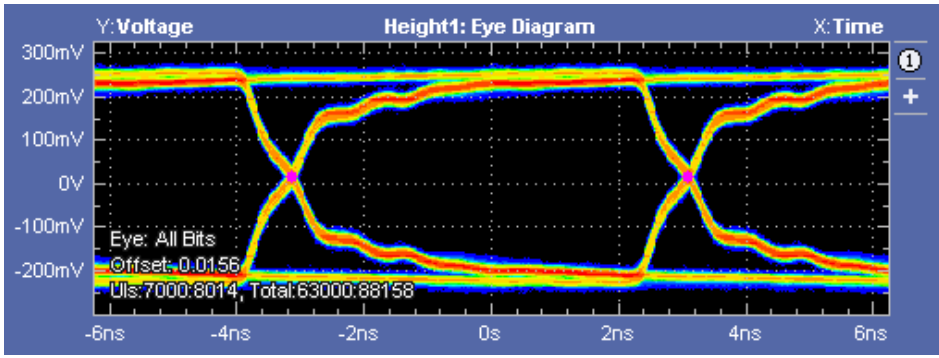
RD53a: 6.14dB Loss Cable

- Measurement: at RD53a SCC.
- Cable: 6.14dB loss in Data channel.

- Left: Data eye diagram:
  - Jitter is almost same as with <3dB loss cable.
  - Eye is open.

- Right: CMD eye diagram.



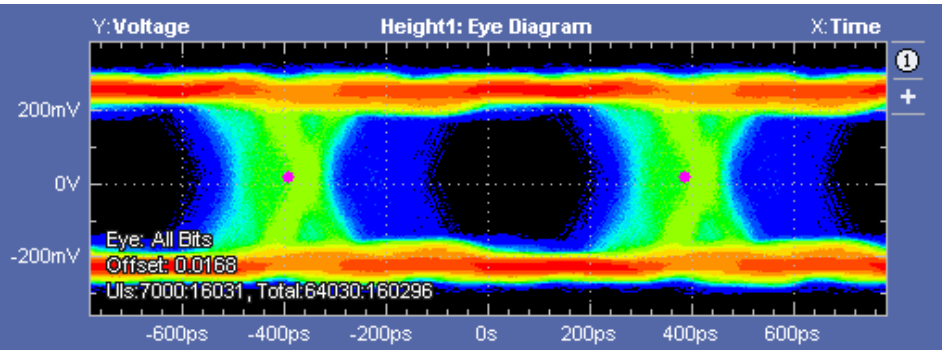


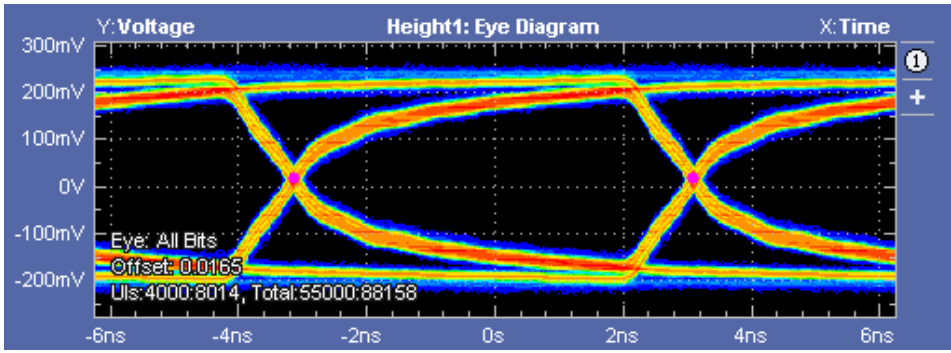
RD53a: 12.17dB Loss Cables

- Measurement: at RD53a SCC.
- Cable: 12.17dB loss in Data channel.

- Left: Data eye diagram:
  - Jitter is larger. Loss in cables come into play.
  - Eye opening is bad.

- Right: CMD eye diagram.
  - “Slower” rising edge leads to worse clock recovery thus larger jitter in Data.



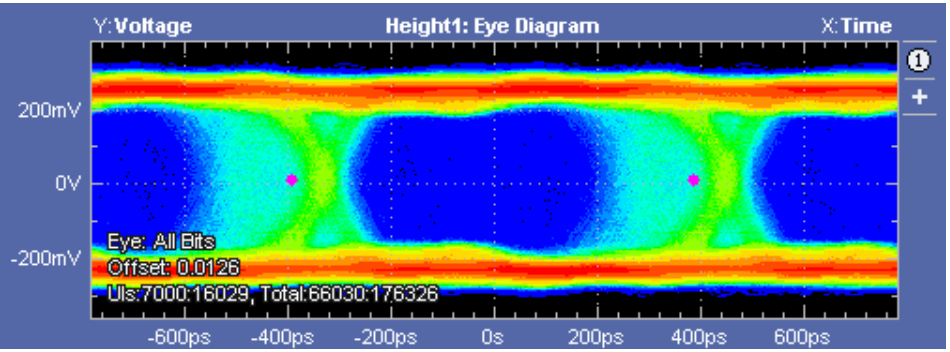


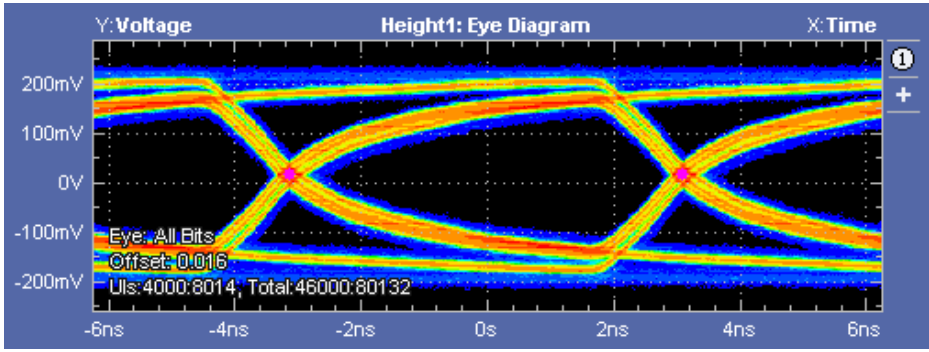
RD53a: 18.26dB Loss Cables

- Measurement: at RD53a SCC.
- Cable: 18.26 dB loss in Data channel.

- Left: Data eye diagram:
  - Jitter is larger. Loss in cables come into play.
  - Eye is closed.

- Right: CDM eye diagram.
  - “Slower” rising edge leads to worse clock recovery thus larger jitter in Data

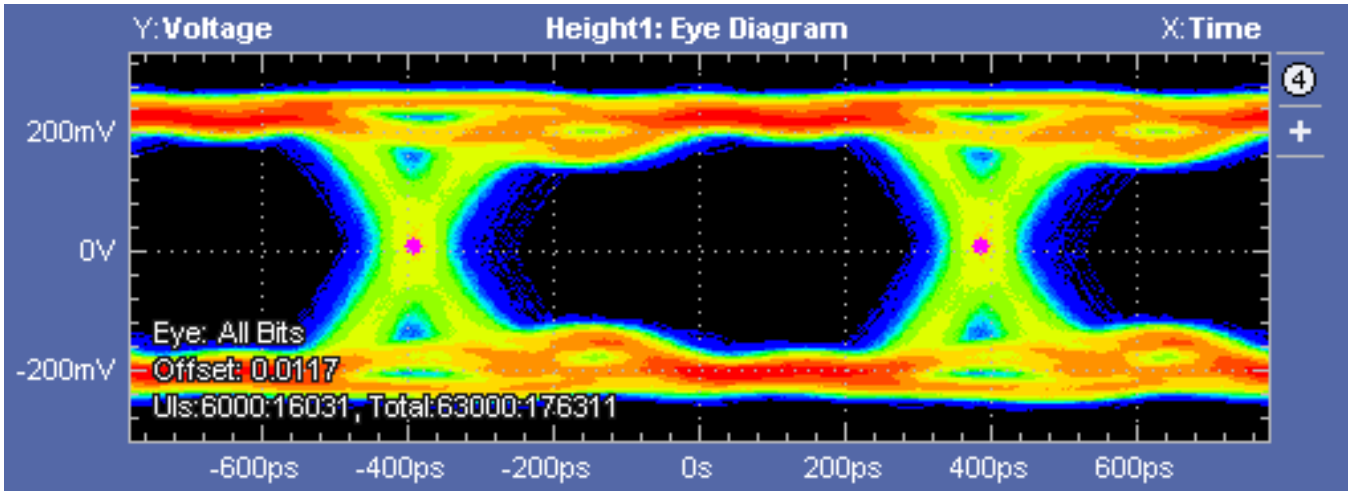




Interface Board: “Short” Cable

- Measurement: at Interface Board.
- Cable: loss<3dB in Data channel.

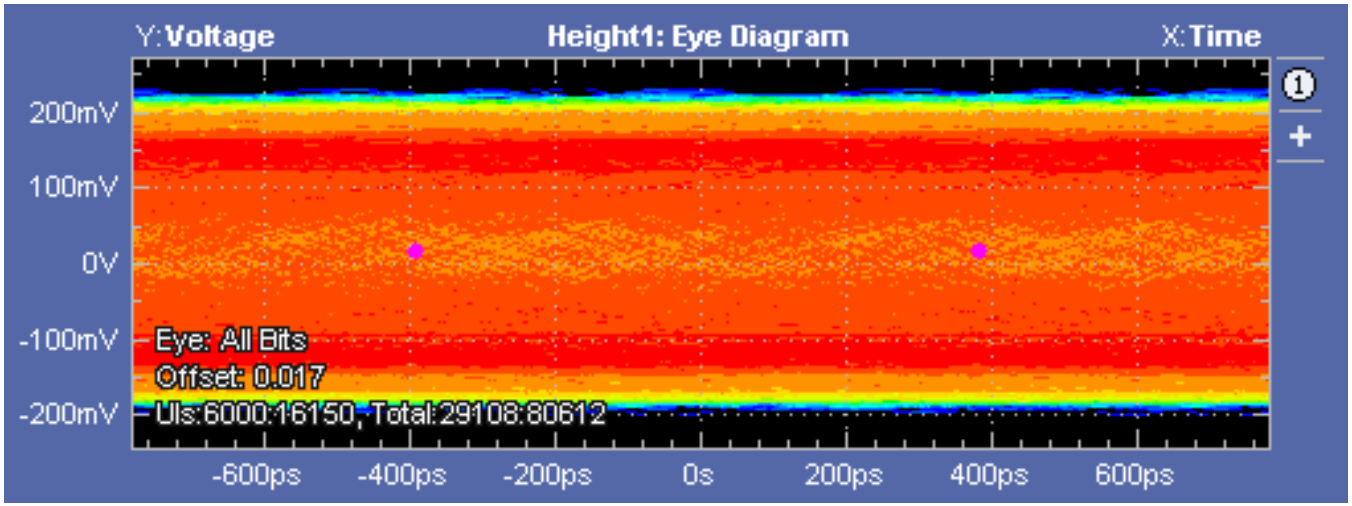
- Plot: Data eye diagram:
  - Jitter is larger than what is measured on the SCC.
  - Eye is open.



Interface Board: J0+J1 Cables

- Measurement: at Interface Board.
- Cable: 12.1dB loss in Data channel.

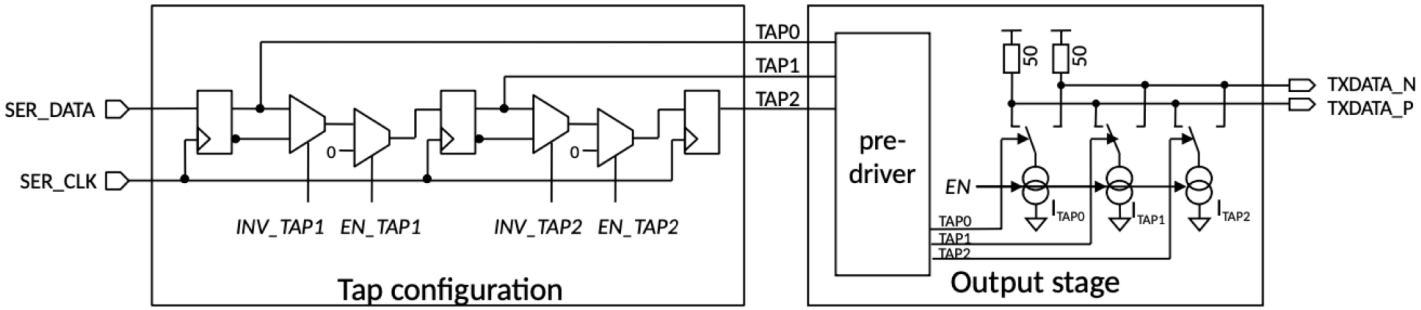
- Plot: Data “eye diagram”.



Study of the Effect of Chip Settings on the Readout Quality

- Improvement is possible! Make the rising and falling edge of the step function of differential signal sharper.

- RD53a SCC has an option to control V_{high} (step-function) shape within one bit.
- Registers 70, 71 and 72 correspond to tap0, tap1 and tap2.
- Values in each register are $0 \div 1023$ with $(500, 0, 0)$ as the default state (also we can invert each).



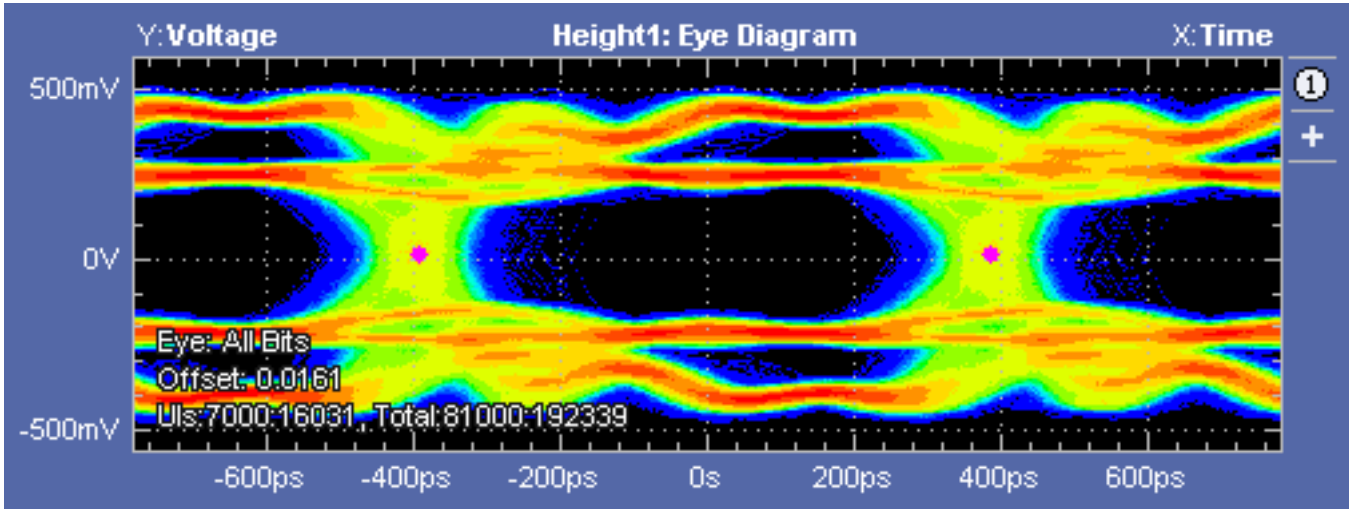
TAP configuration
- *INV_TAP[2:1]*
- *EN_TAP[2:1]*

CML output configuration
- *EN*
- *TAP0_BIAS[9:0]*
- *TAP1_BIAS[9:0]*
- *TAP2_BIAS[9:0]*

RD53a: “Short” Cable with RD53a Pre-Emph.

- Measurement: at RD53a SCC.
- Cable: loss<3dB in Data channel.
- Pre-emphasis registers: (1023, -200, 0).

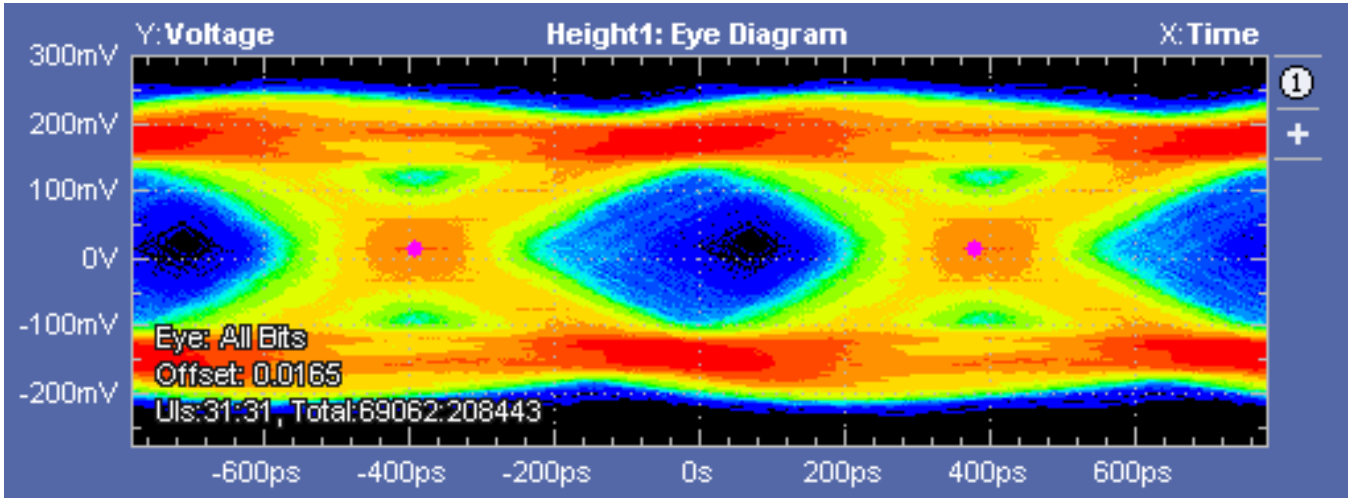
- Plot: Data eye diagram:
  - Significant jitter presents.
  - Eye is weird, but open.



Interface Board: 12.1dB Loss Cable with RD53a Pre-Emph.

- Measurement: at Interface Board.
- Cable: 12.1dB loss in Data channel.
- Pre-emphasis registers: (1023, -200, 0).

- Plot: Data eye diagram:
  - The best eye opening. Large jitter, small eye opening.
  - **Digital scan fails:** significant number of raw bit error lead to unreliable digital scan results.



Data Eye Diagrams with 12dB Loss Cables: YARR