Development of a High-Speed Hit Decoder for the RD53B Chip

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ATLAS

- Major experiment site in Large Hadron Collider (LHC)
- High Luminosity LHC upgrade
  - Roughly factor of 4x [2]
- New ITk Pixel detector
  - Read out chip upgrade
- RD53 collaboration started to create new read out chips

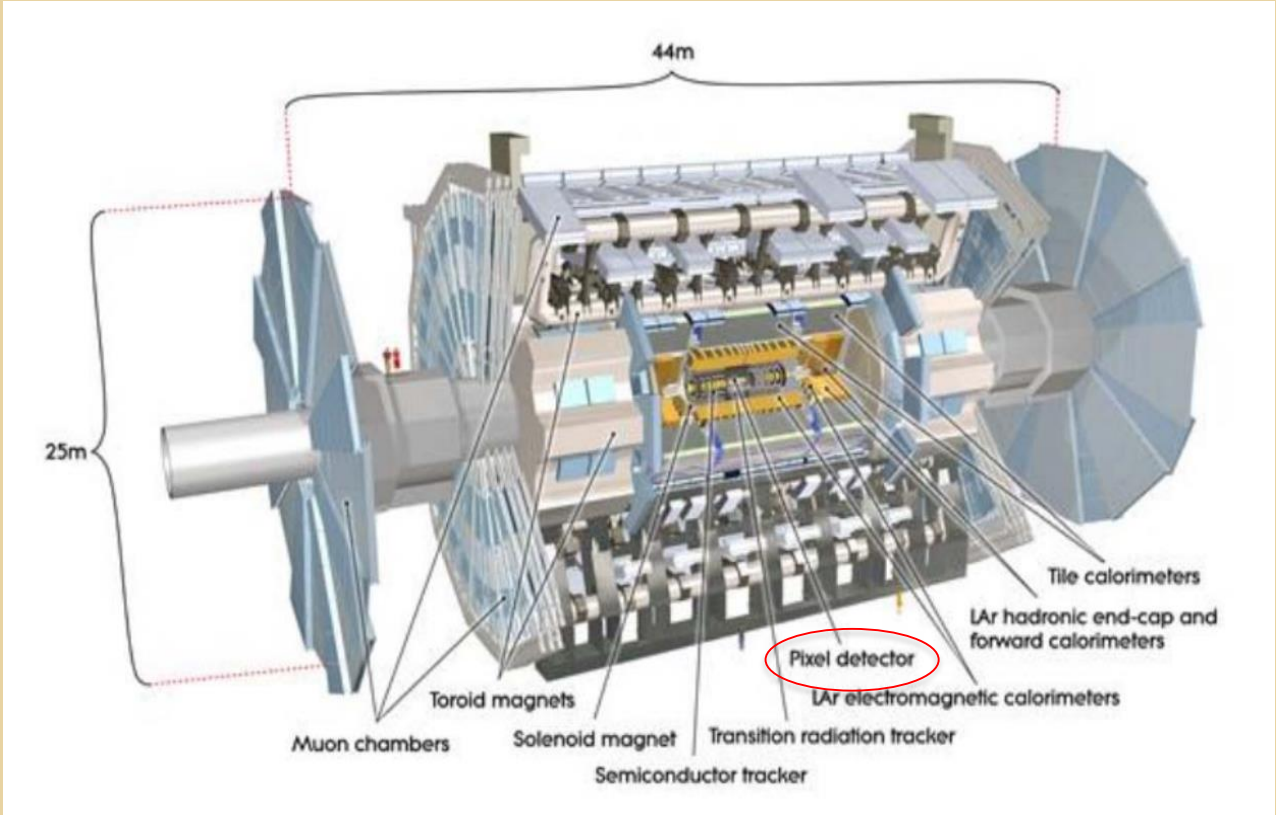

Figure 2: Computer rendering of the ATLAS detector system. [1]

RD53B

- Analog islands in digital sea [4]
- 4-pixel analog front ends per island
- Pixel front end detects when passing charge reaches threshold value (“Hit”)
- Digital logic for read out and Time over Threshold (ToT)

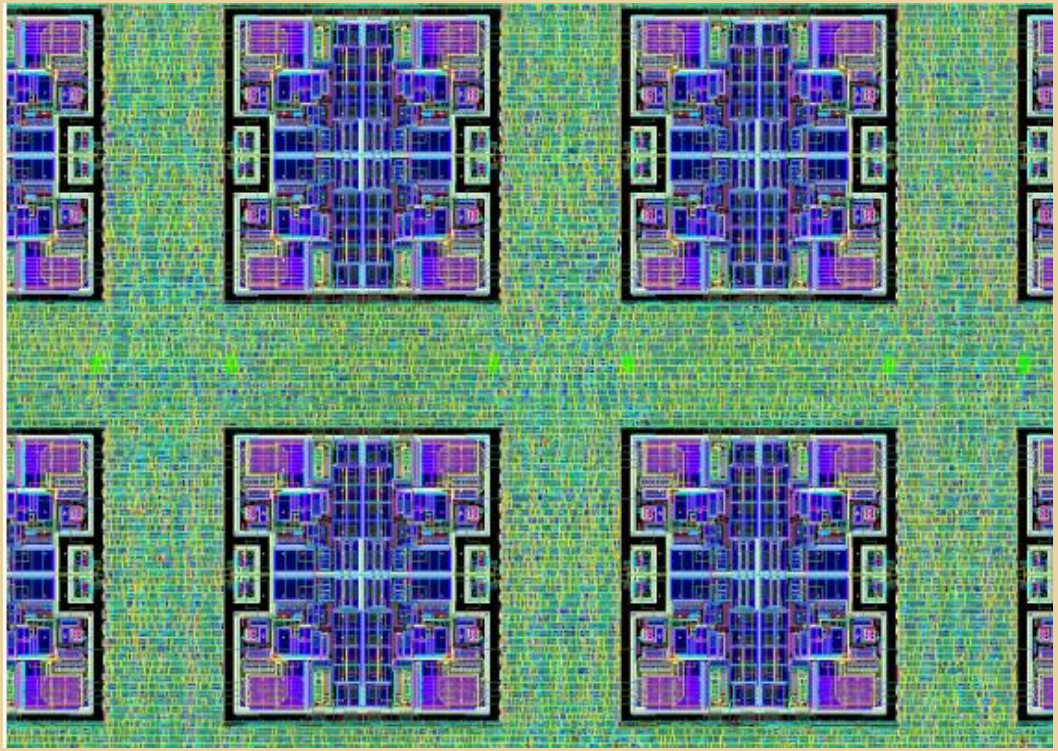

Figure 3: Layout of analog islands with surrounding digital logic. Four complete islands are seen in the middle of the image. [4]

RD53B

- Arranged into cores (8x8 pixels or 16 analog islands) [4]
- ATLAS configuration
  - 48 core rows
  - 50 core columns
- Hits separated into quarter rows (16 pixels total in 2X8 format)

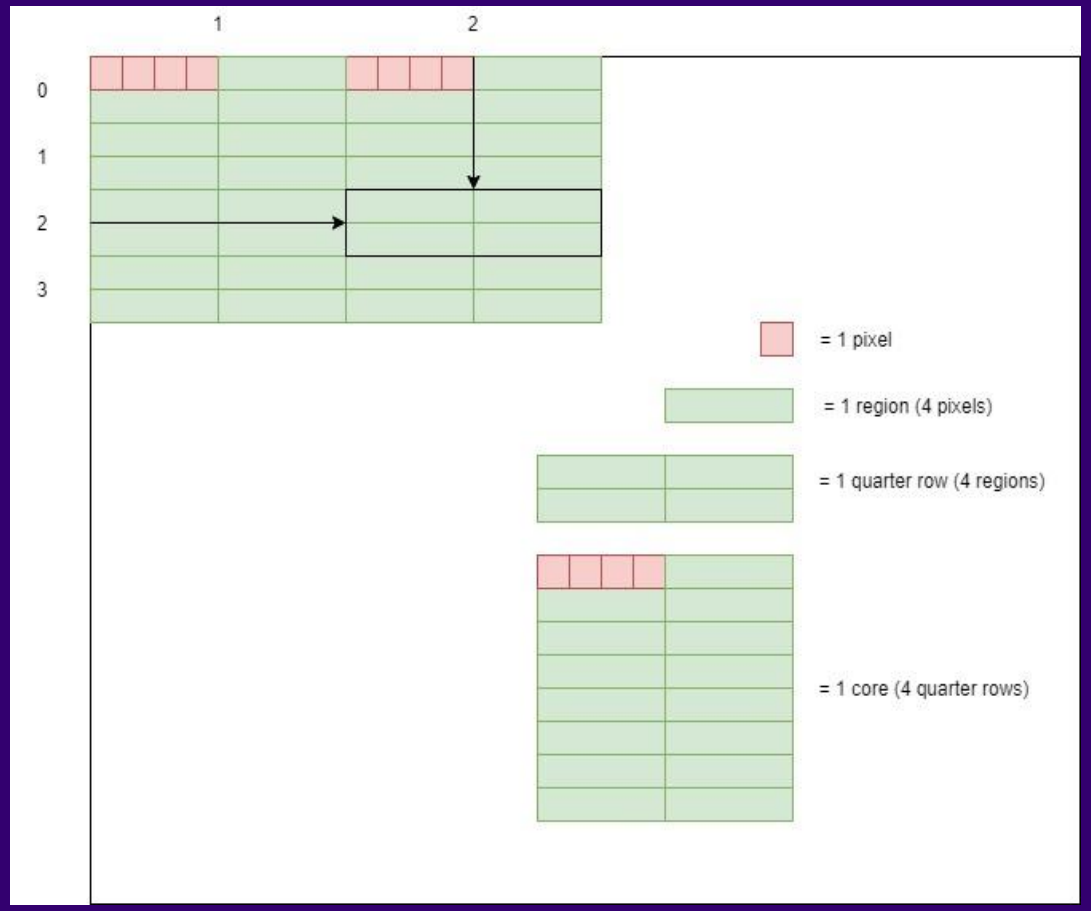

Figure 4: Visualization of RD53B quarter row selection process.

Data Streams

- Captures all quarter rows with active hits [4]
- Sent in 64 bit packets
- Meta data for stream packing
- Quarter rows packed back to back

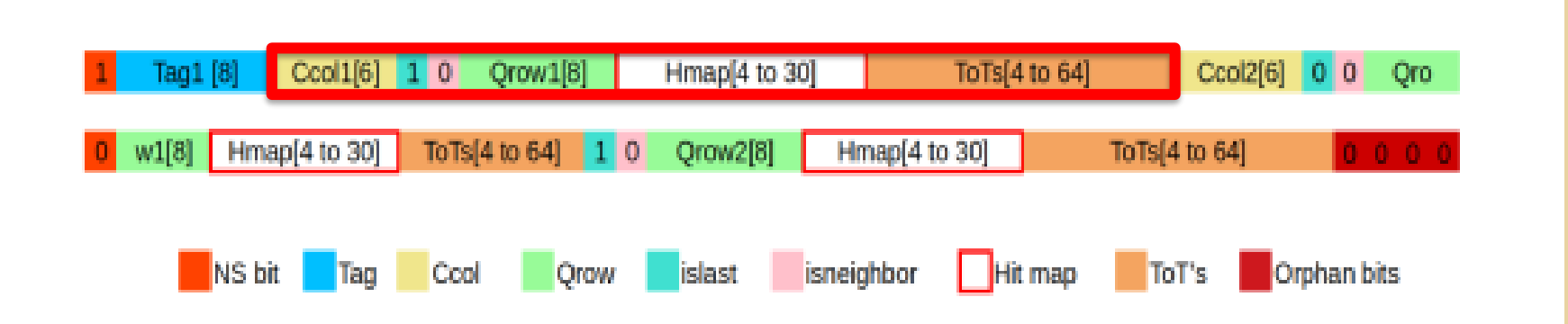

Figure 5: Example RD53B stream data. [4]

Encoding Method

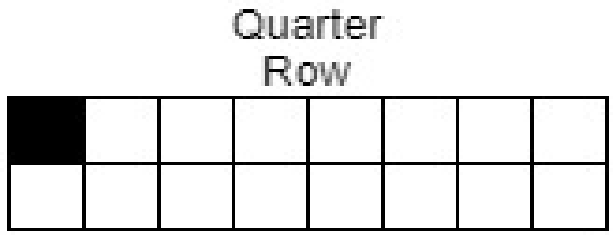

Figure 6: RD53B encoding cut pattern.

Hitmap Encoding

- Encode using bit pairs (11, 10, 01) [4]
- Final encoding {first two bits, first row, second row}
- No 00 pairs allows for Huffman encoding
- Swap all 01 bits with 0

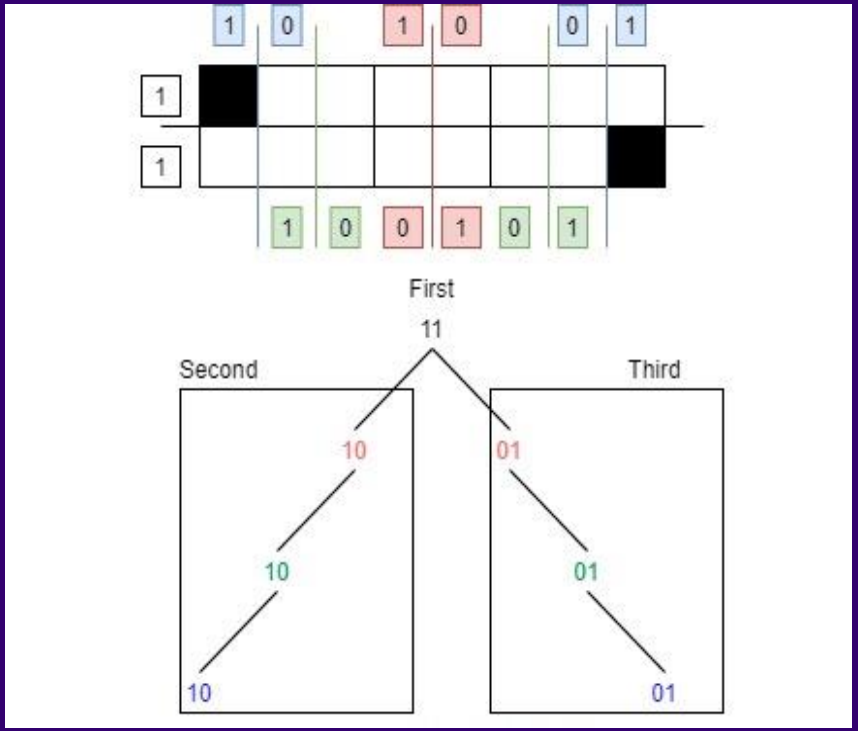

Figure 7: Hitmap encoding breakdown using two hits

Result: 11.101010.010101

Swap 01 with 0

Compressed Result: 11.101010.000

ROM Split

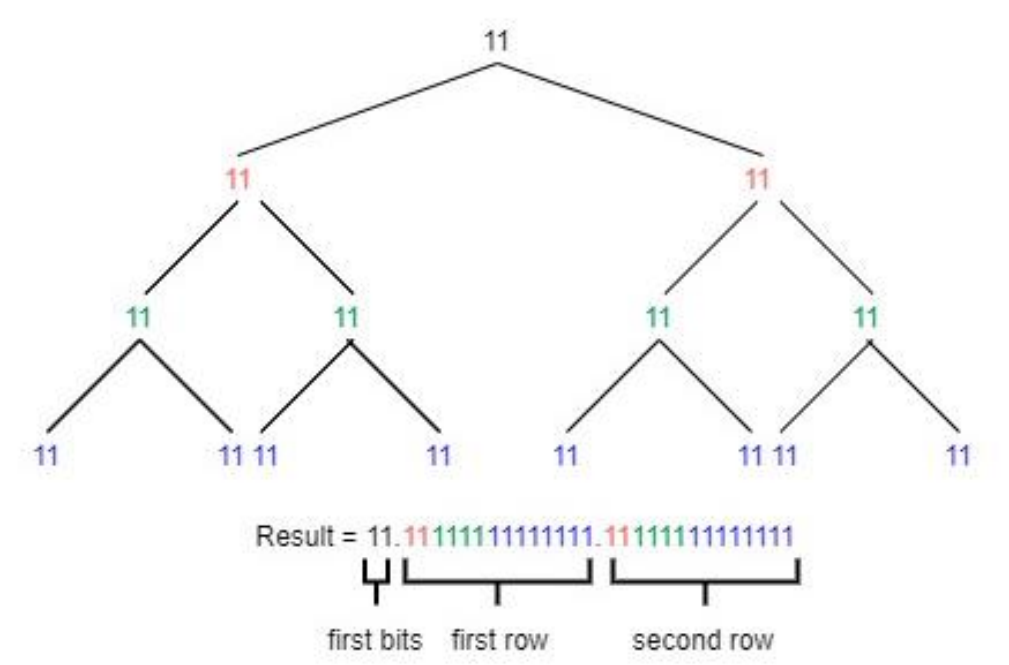

Figure 8: Encoded hitmap with maximum number of values.

- Row data no longer than 14 bits
- First 2 bits show which rows have hits
- One 14-bit ROM per row

ROM Split

- Software to hardware conversion
- Creates two 14x16 ROMs
- Large outputs for meta data and decoded hitmap

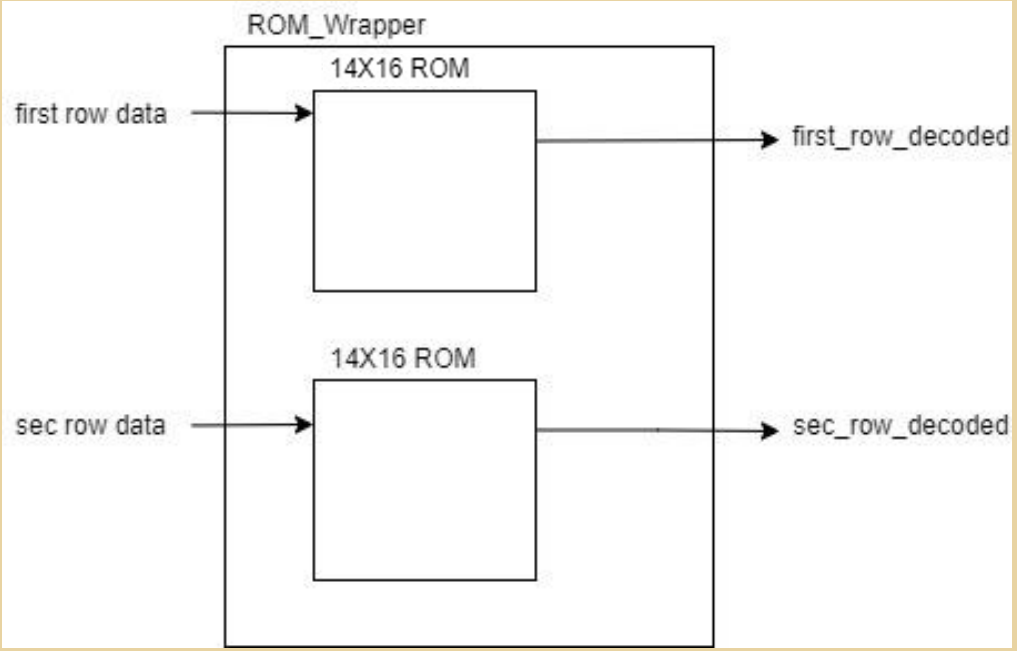

Figure 9: High level block diagram of split ROM system.

Decode Engine: ROM & data storage

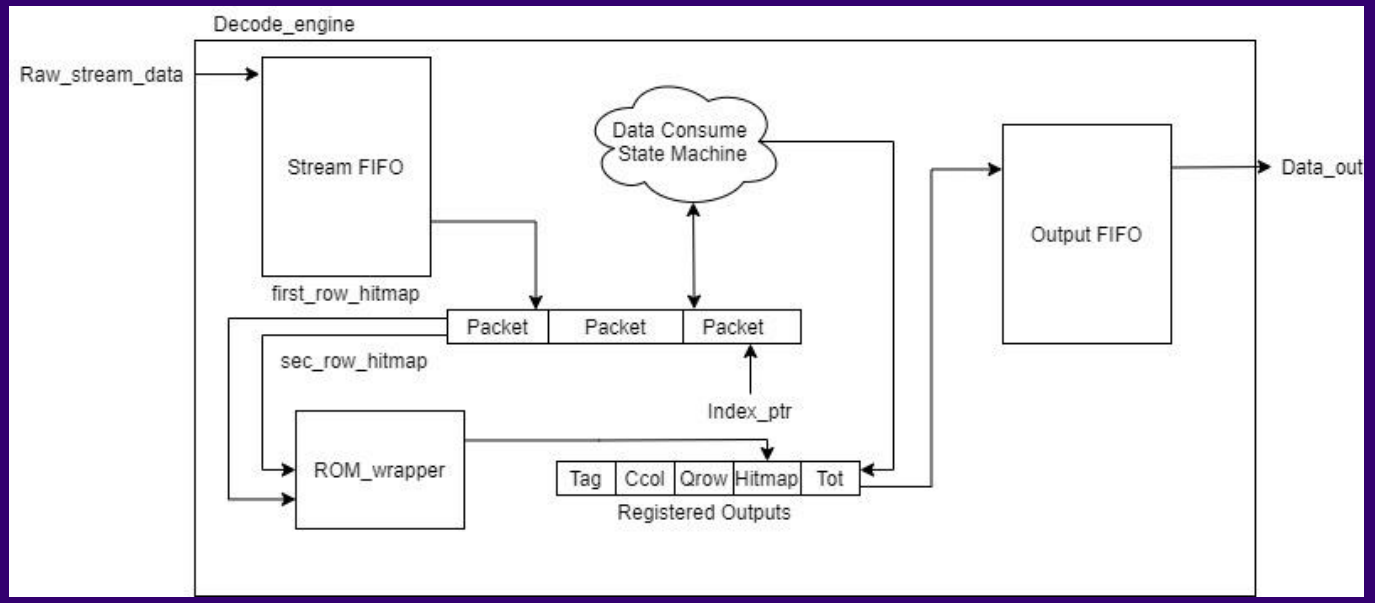

Figure 10: Decode engine high level full diagram.

- Buffer to store stream data
- Data consume state machine to process data
- Creates registered output

Base Design

- Stream distribute to pass data to engines
- Variable amount of decode engines
- Shared ROM distribute system

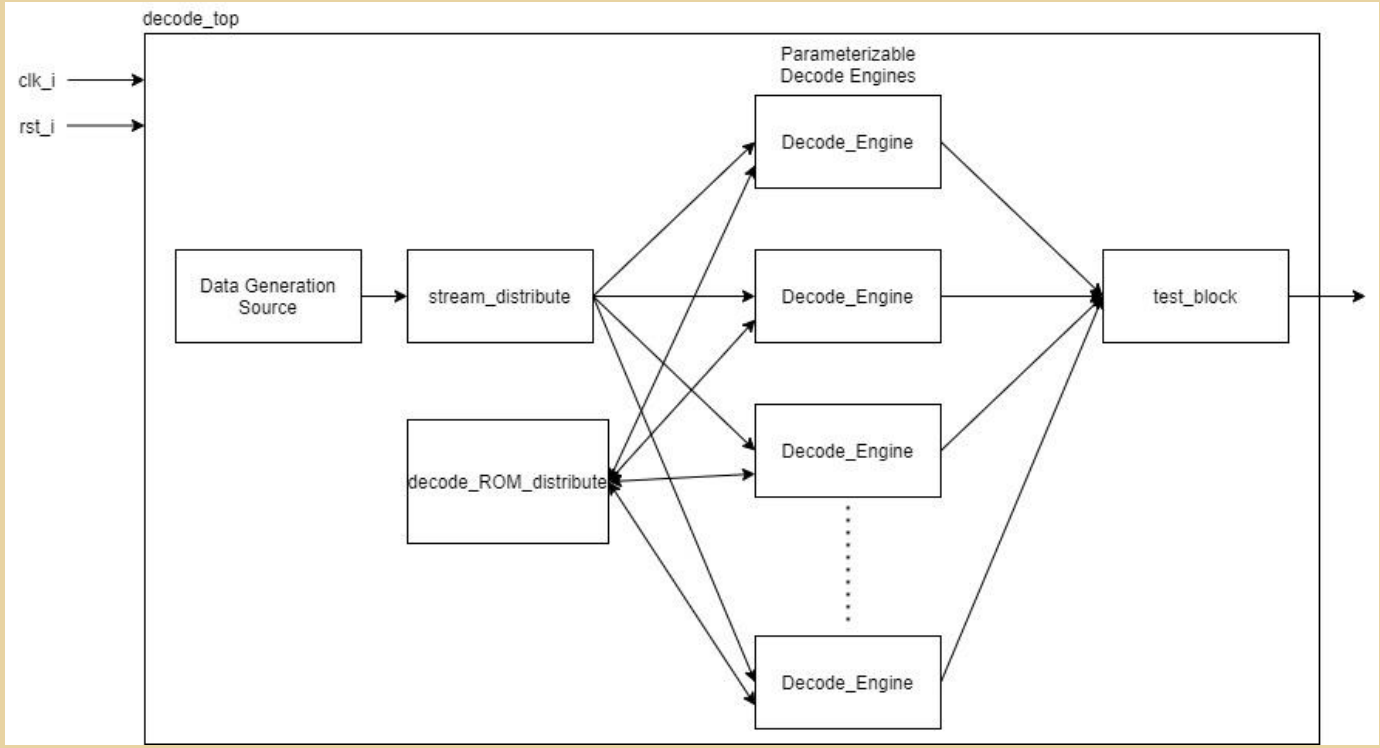

Figure 11: Top level diagram of initial full design for hardware decoder.

ROM Timing

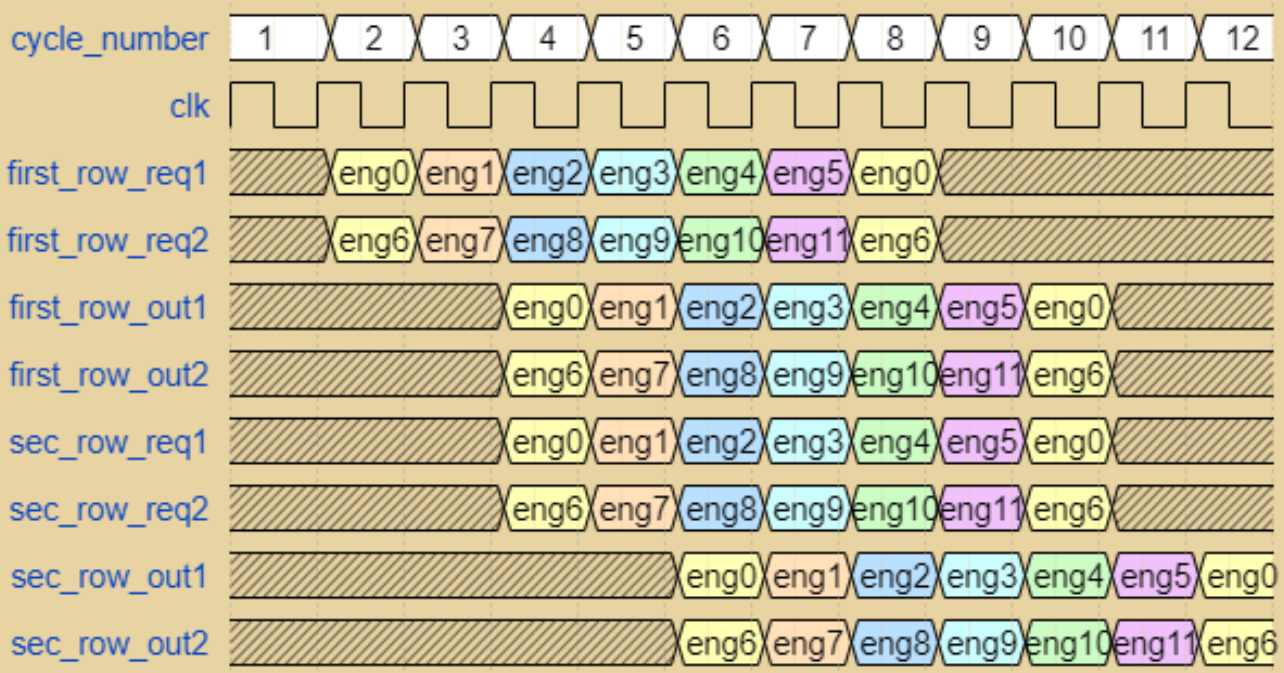

Figure 12: Timing diagram for the engine offsets for accessing centralized ROM system.

- 6 cycles to process hitmap
- Offset engines
- 12 engines with dual port ROMs

Interpretation of Results

Table 1: Number of engines need based on hits per quarter row and compression.

Max/Min compression	Ccol + Qrow size	Hitmap	TOT	Total	Speed Per Engine (Gb/s)	# Engine Needed
1 hit max	2 bits	4 bits	4 bits	10 bits	10/37.5ns = 0.267	5.12/0.267 = 19.23 (20)
1 hit min	16 bits	8 bits	4 bits	28 bits	28/37.5ns = 0.747	5.12/0.747 = 6.86 (7)
2 hit max	2 bits	5 bits	8 bits	15 bits	15/37.5ns = 0.4	5.12/0.4 = 12.8 (13)
2 hit min	16 bits	14 bits	8 bits	38 bits	38/37.5ns = 1.01	5.12/1.01 = 5.069 (6)

- Analyzed ATLAS simulation data
  - Average of 1-2 hits per quarter row
- 37.5ns per quarter row of data
- Target of 5.12 Gb/s
  - Max output of RD53B chip

Resources for Each Configuration

Table 2: The summary of resource usage cases for different hardware decoder configurations based on hits per quarter row.

Hits per quarter row w/ compression	Bits per quarter row	Single engine (Gb/s)	12 engine (Gb/s)	Engines needed	Estimated BRAM usage	Estimated LUT usage
1 max	10 bits	0.267	3.2	20	94	42,000
2 max	15 bits	0.4	4.8	13	73	27,300
1 min	28 bits	0.747	8.96	7	38	14,700
2 min	38 bits	1.01	12.16	6	35	12,600

- Each hardware decoder instantiation
  - 15 BRAM for ROM split
  - 2 BRAM for stream distributer
  - Max 12 engines per instantiation
- Each decode engine 3 BRAM, 2100 LUTs

Conclusion

- LHC upgrade to High Luminosity LHC
- RD53B specific encoding
- Create base design hardware based decoding
- Estimate use case resource numbers

References

> [1]. “CERN website”, CERN, [Online], Available: https://home.cern/

> [2]. “High Luminosity LHC Project”, CERN, [Online], Available: https://hilumilhc.web.cern.ch/

> [3]. Chistiansen, Jorgen, Loddo, Flavio, “RD53 Collaboration Proposal: Extension of RD53”, RD53, September 6, 2018

> [4]. “The RD53B Pixel Readout Chip Manual v1.31”, RD53, September, 2020

> [5]. “The RD53B Pixel Readout Chip Manual v0.38”, RD53, April 14, 2020

> [6]. “7 Series FPGAs Memory Resources v1.14”, Xilinx, July 3, 2019

> [7]. Timon Heim, private communication, 2021

> [8]. McMahon, Stephen; Pontecorvo, Ludovico, “Technical Design Report for the ATLAS Inner Tracker Strip Detector”, CERN, April 1, 2017

> [9]. “CERN atlas website”, CERN, [Online], https://atlas.cern/discover/detector