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Development of a High-Speed Hit Decoder for the RD53B Chip

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The Large Hadron Collider (LHC) will soon undergo an upgrade, referred to as the High-Luminosity LHC (HL-LHC), which will increase the instantaneous luminosity beyond the LHC's design value. The ATLAS experiment is upgrading the innermost portion of the detector to the ITk pixel detector to accommodate the increase in luminosity. The RD53 collaboration was formed to develop the ASIC read out chips that are used inside the ITk pixel detector. In the preproduction RD53B chip, an encoding system was implemented to help shrink data streams and reduce the overall bandwidth of the system. An exploratory effort was undertaken to create a hardware decoder for Field Programmable Gate Arrays (FPGA) to cut down on CPU usage from software decoders later in the system. A parallelized hardware decoder was designed to meet the data rates produced by an RD53B chip. Overall, the final product is a base hardware decoder design that can handle the throughput constraints of a single RD53B and is resource efficient. In this talk I will report necessary background, hardware decoder design, and conclusions based on this design.

Are you are a member of the APS Division of Particles and Fields?

No

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