Contribution ID: **227** Type: **talk**

FPGA filter for fast tracking in the ATLAS HL-LHC trigger

Tuesday, July 13, 2021 3:15 PM (15 minutes)

This talk introduces and shows the simulated performance of an FPGA-based technique to improve fast track finding in the ATLAS trigger. A fast track trigger is being developed in ATLAS for the High Luminosity upgrade of the Large Hadron Collider (HL-LHC), the goal of which is to provide the high-level trigger with full-scan tracking at 100 kHz in the high pile-up conditions of the HL-LHC. Options under development for achieving this include a method based on matching detector hits to pattern banks of simulated tracks stored in a custom made Associative Memory ASIC (Hardware Track Trigger, "HTT") and one using the Hough transform (whereby detector hits are mapped onto a 2D parameter space with one parameter related to the transverse momentum and one to the initial track direction) on FPGAs ("Hough").

Both of these methods can benefit from a pre-filtering step, to reduce the number of hit clusters that need to be considered and hence reduce the overall system size and/or power consumption, by examining pairs of clusters in adjacent strip detector layers (or lack thereof). This stub-filtering was first investigated by CMS but has been unexplored in ATLAS until now, and we will show the reduction in throughput enabled along with the performance impact on both HTT and Hough systems of track finding, as well as estimates of resource usage.

Are you are a member of the APS Division of Particles and Fields?

Yes

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Session Classification: Computation, Machine Learning, and AI

Track Classification: Computation, Machine Learning, and AI