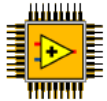# LabVIEW FPGA hands-on part 2

Adriaan Rijllart

Odd Øyvind Andreassen

CERN

Content of LabVIEW FPGA hands-on 2
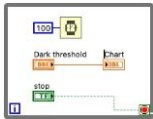
- A few more LabVIEW basics

- Introduction to LabVIEW FPGA

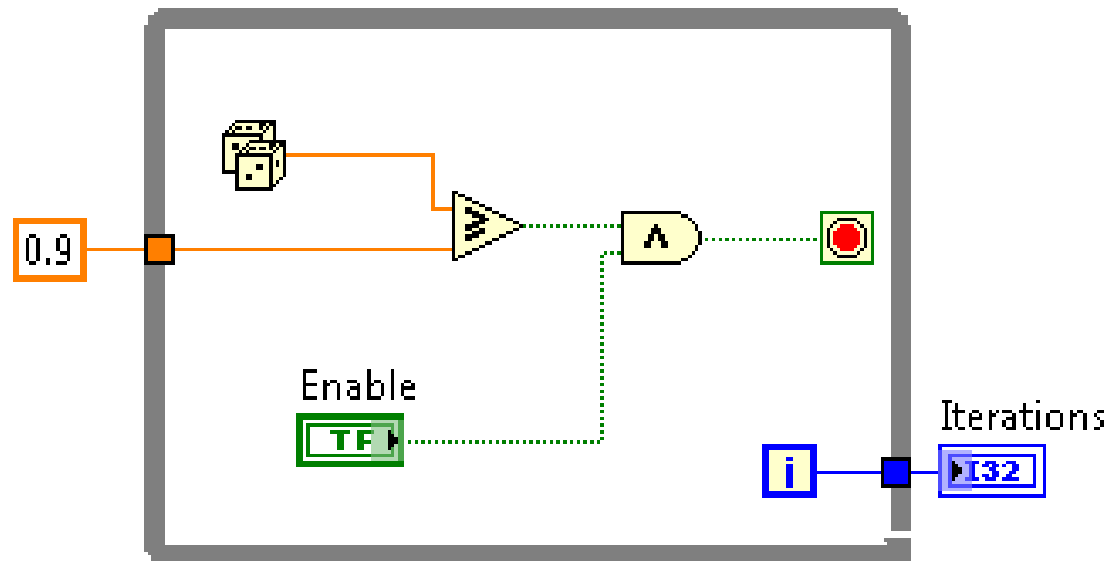- Overview of NI myRIO

- Exercises

- Resources and Next Steps

A few more LabVIEW basics

While loop tunnel

- Tunnels transfer data into and out of structures.
- When a tunnel passes data into a loop, the loop executes only after data arrive at the tunnel (at all tunnels, if there is more than one).
- Data pass out of a loop after the loop terminates.

For loop

- The value in the count terminal (an input terminal) indicates how many times to repeat the subdiagram


Last value

Indexed
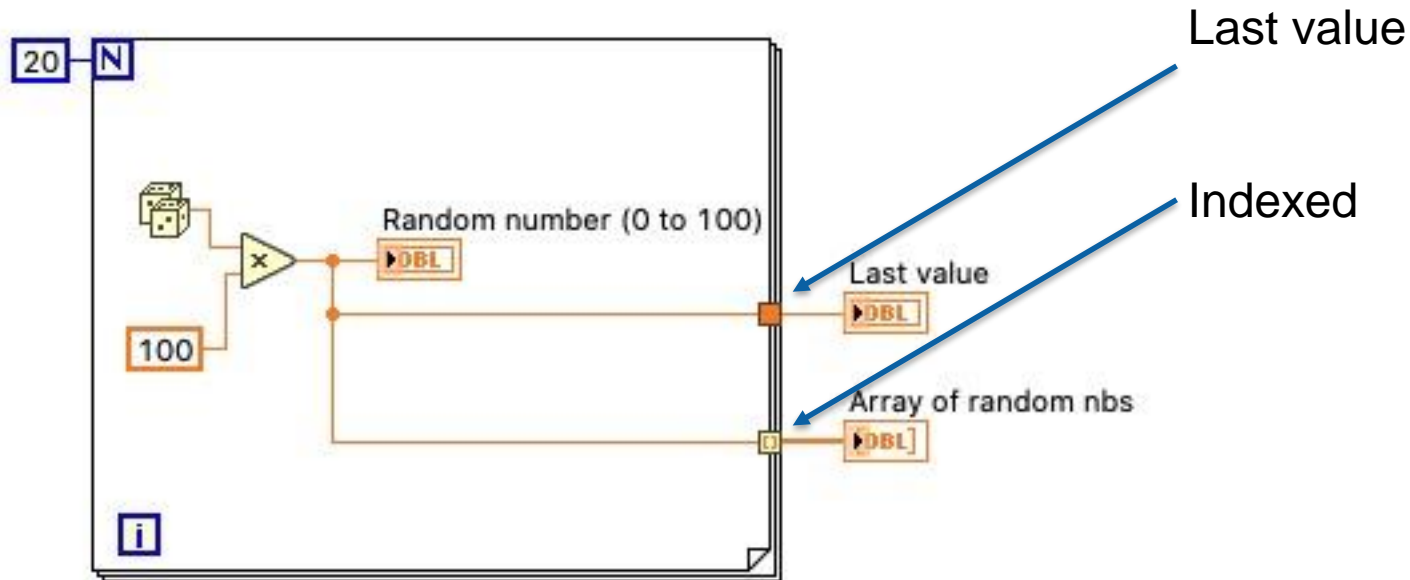
Shift register

- When programming with loops, you often need to know the values of data from previous iterations of the loop.

- Shift registers transfer values from one loop iteration to the next.
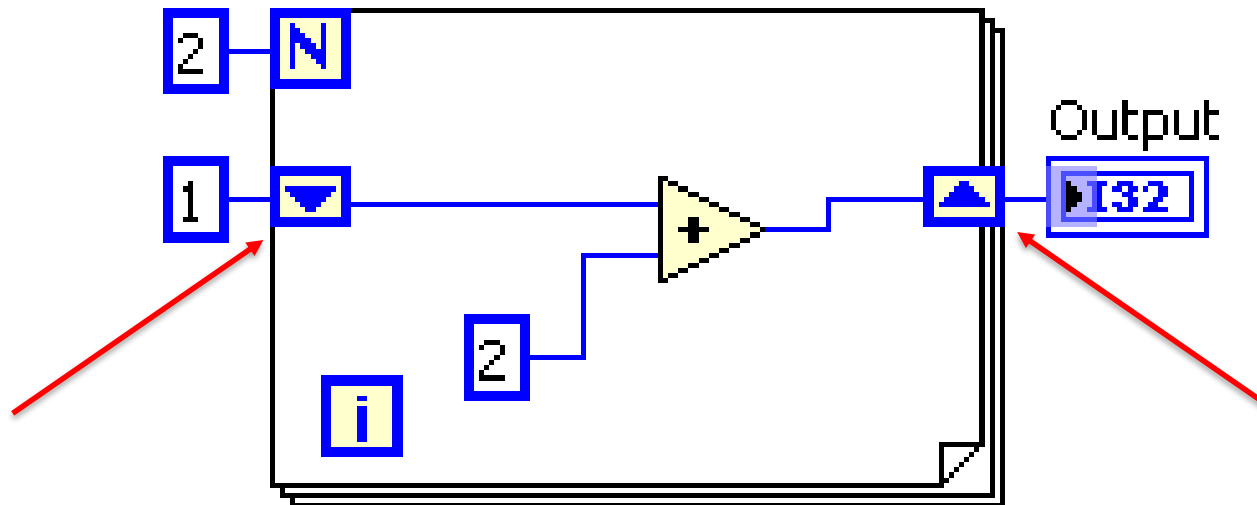
Shift register, multiple values

- Stacked shift registers remember values from multiple previous iterations and carry those values to the next iterations.

- Right-click the left shift register and select **Add Element** from the shortcut menu to stack a shift register.
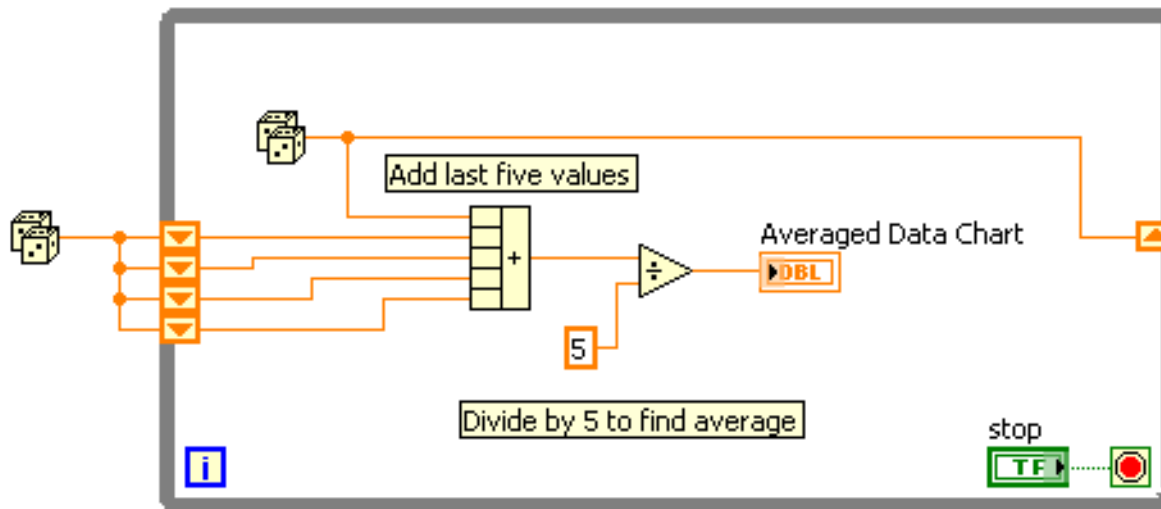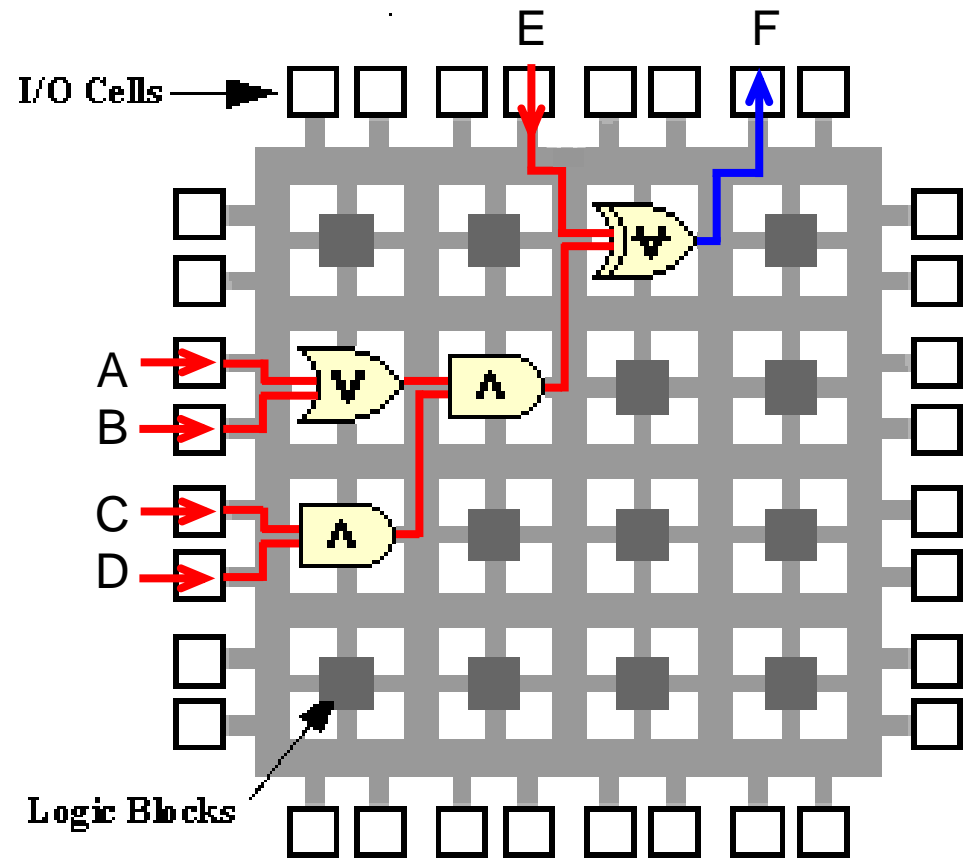
Introduction to LabVIEW FPGA

FPGA Technology

Programmable
Interconnects

Logic
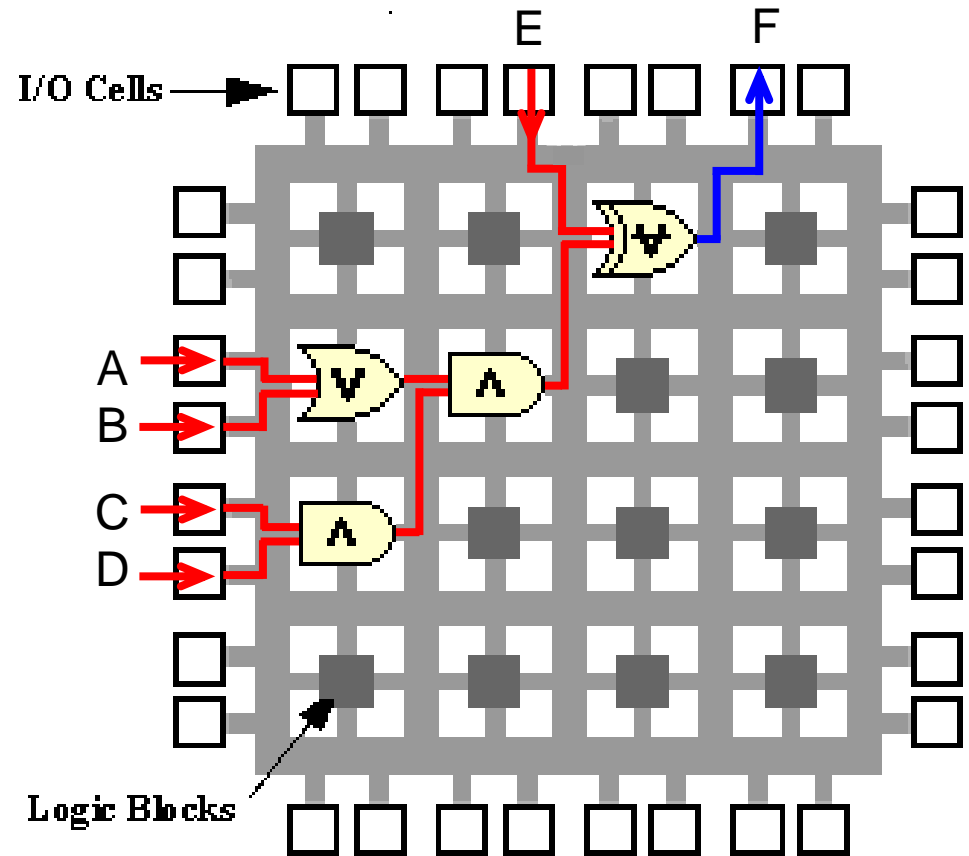Blocks

I/O Blocks
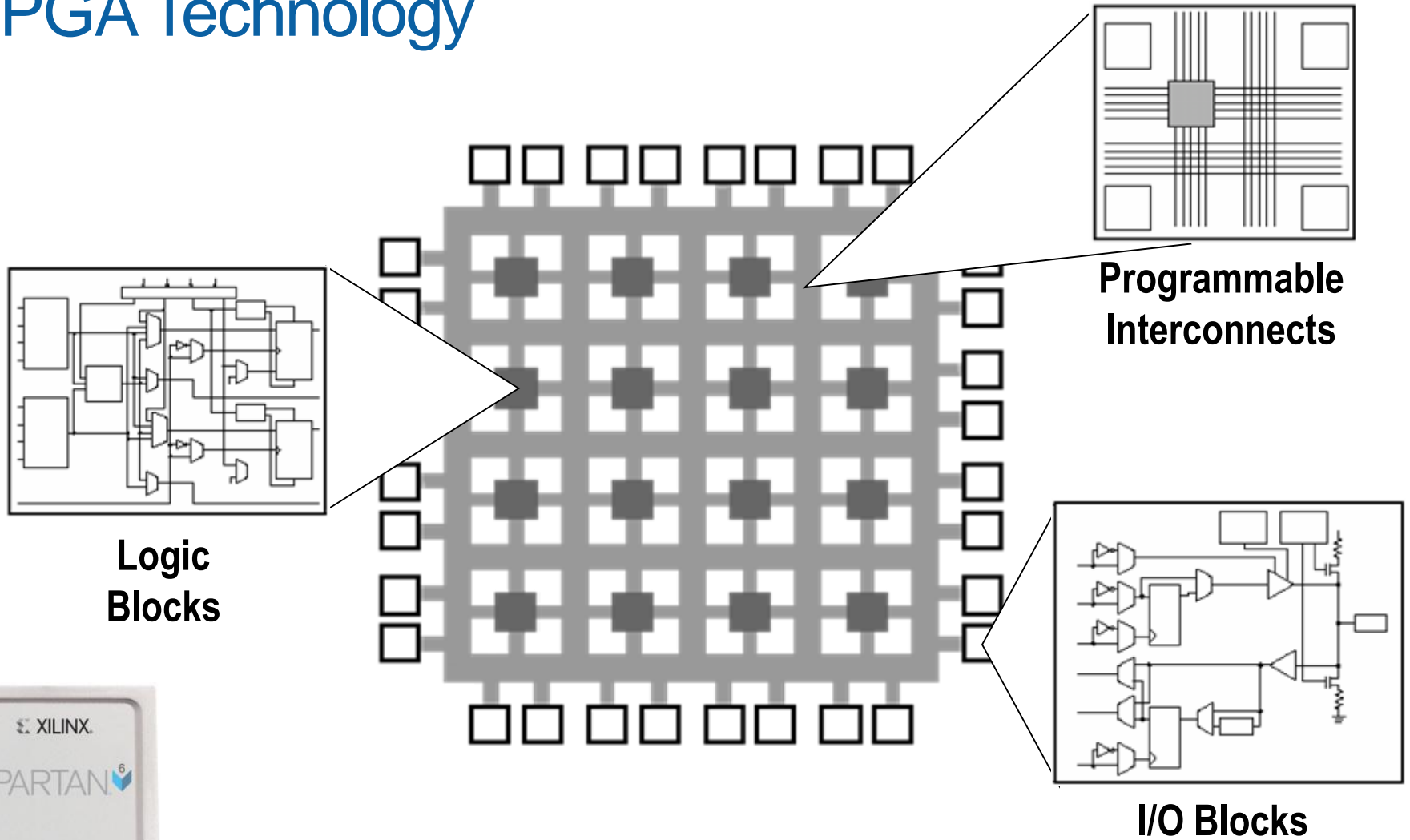
FPGAs are Dataflow Systems

Implementing
Logic on FPGA:
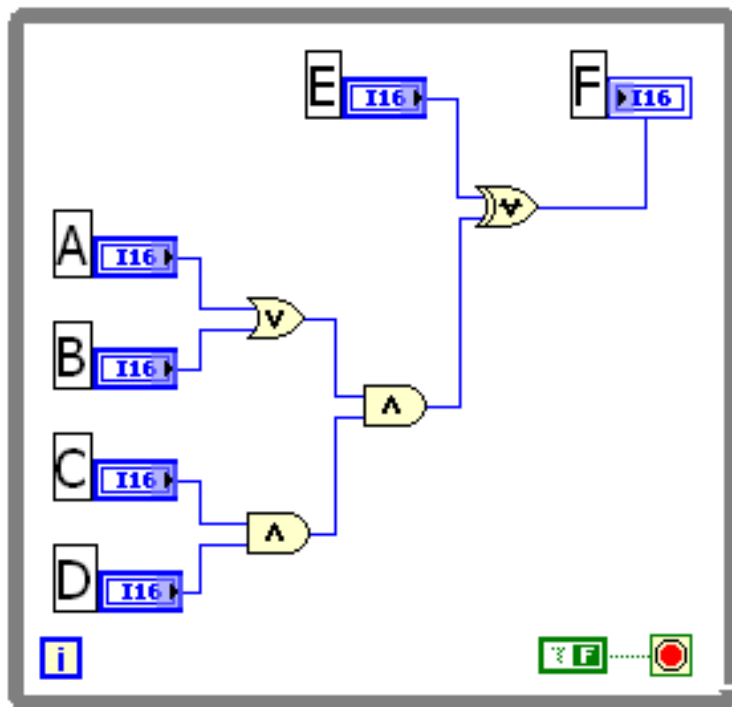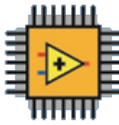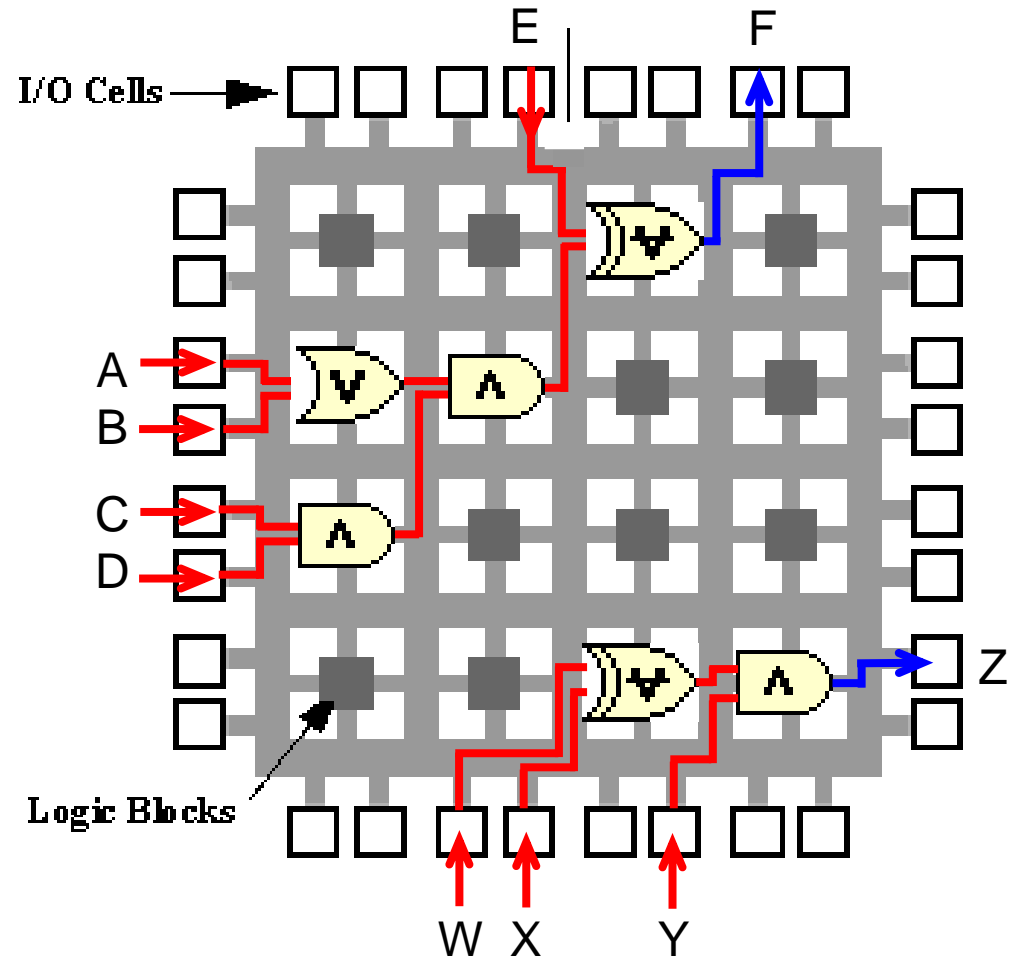
$F = \{(A+B)CD\} \oplus E$

FPGAs are Dataflow Systems

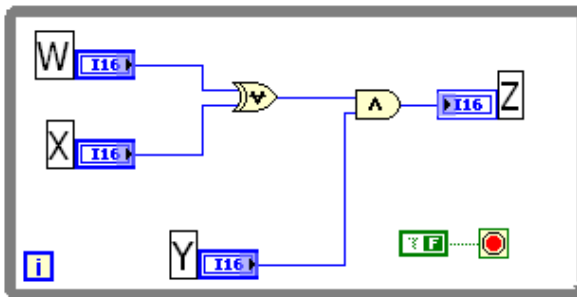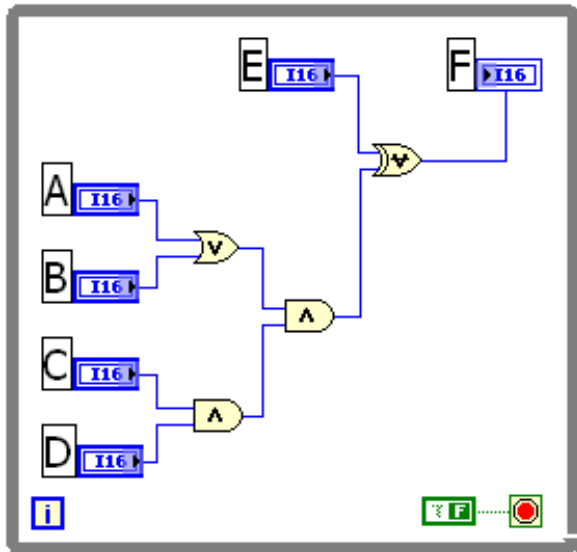Implementing Logic on FPGA: F = {(A+B)CD} $\oplus$ E

LabVIEW FPGA Code

FPGAs are Parallel Dataflow Systems

I/O Cells

Logic Blocks

LabVIEW FPGA   vs.   VHDL
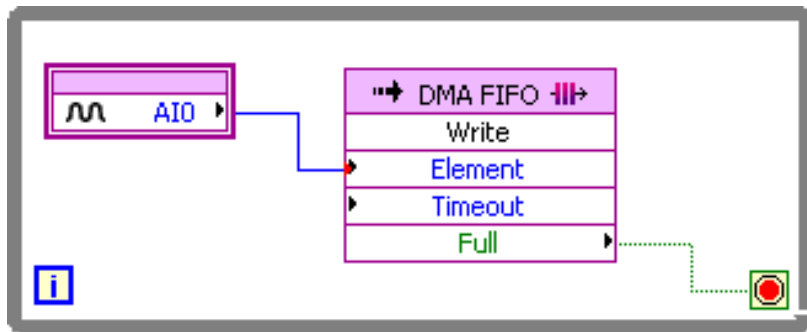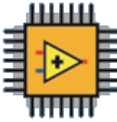
I/O with DMA

66 Pages ~4000 lines
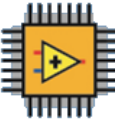
Why Are FPGAs Useful?

- **True Parallelism**
  Provides parallel tasks and pipelining

- **High Reliability**
  Designs become a custom circuit

- **High Determinism**
  Runs algorithms at deterministic rates down to 25 ns (faster in many cases)

- **Reconfigurable**
  Create new and alter existing tasks easily

LabVIEW FPGA: How does it work?

LabVIEW VI → VHDL → Bitfile → Xilinx FPGA Chip

LabVIEW FPGA

Xilinx ISE Compiler

LabVIEW FPGA
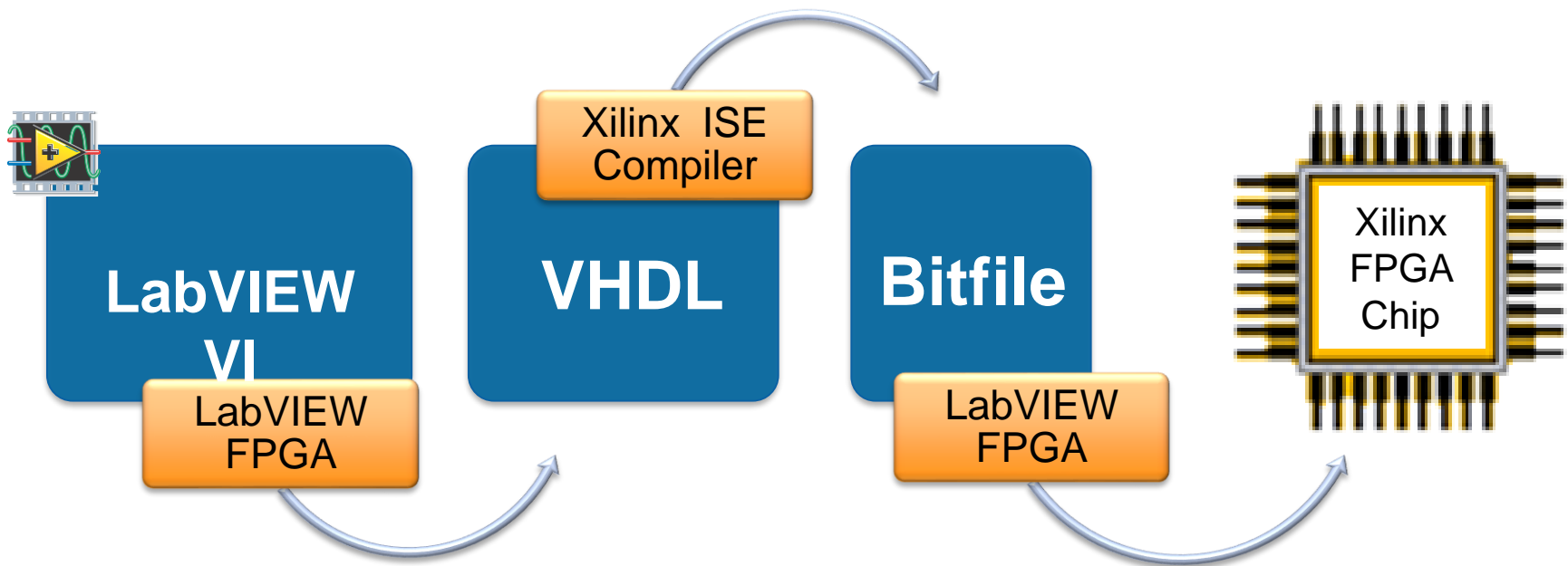
NI myRIO Product Overview: Front View
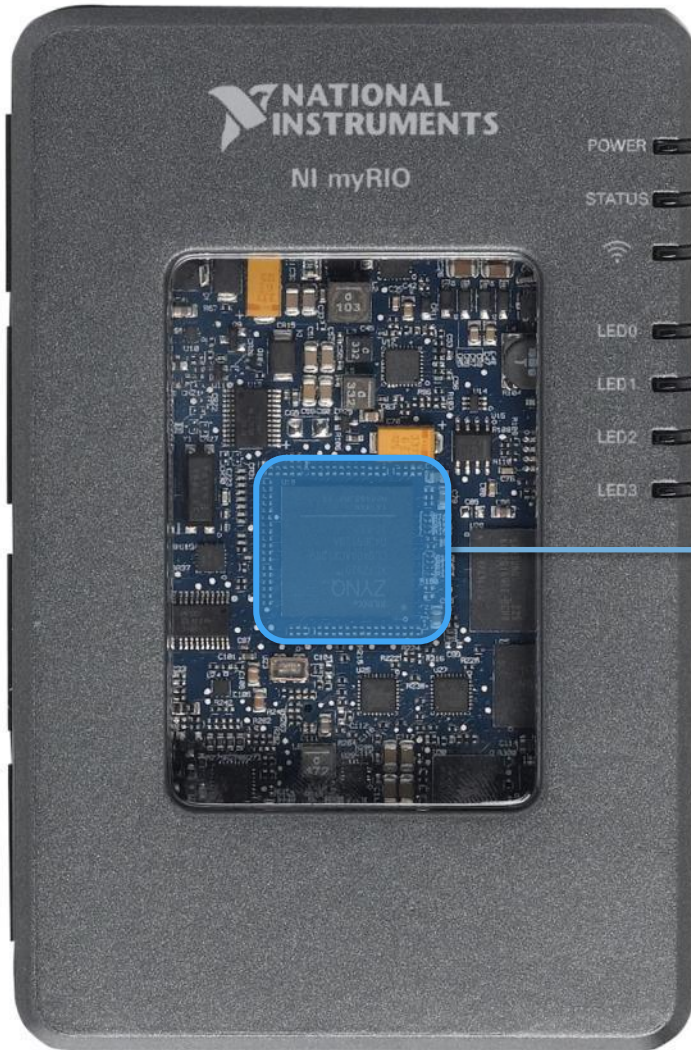
XILINX Zynq SoC

What is Zynq?

Traditional Implementation

Processor — **AXI Bus** — FPGA

Analogue Input

Analogue Output

Digital I/O

Custom I/O

Single System on Chip
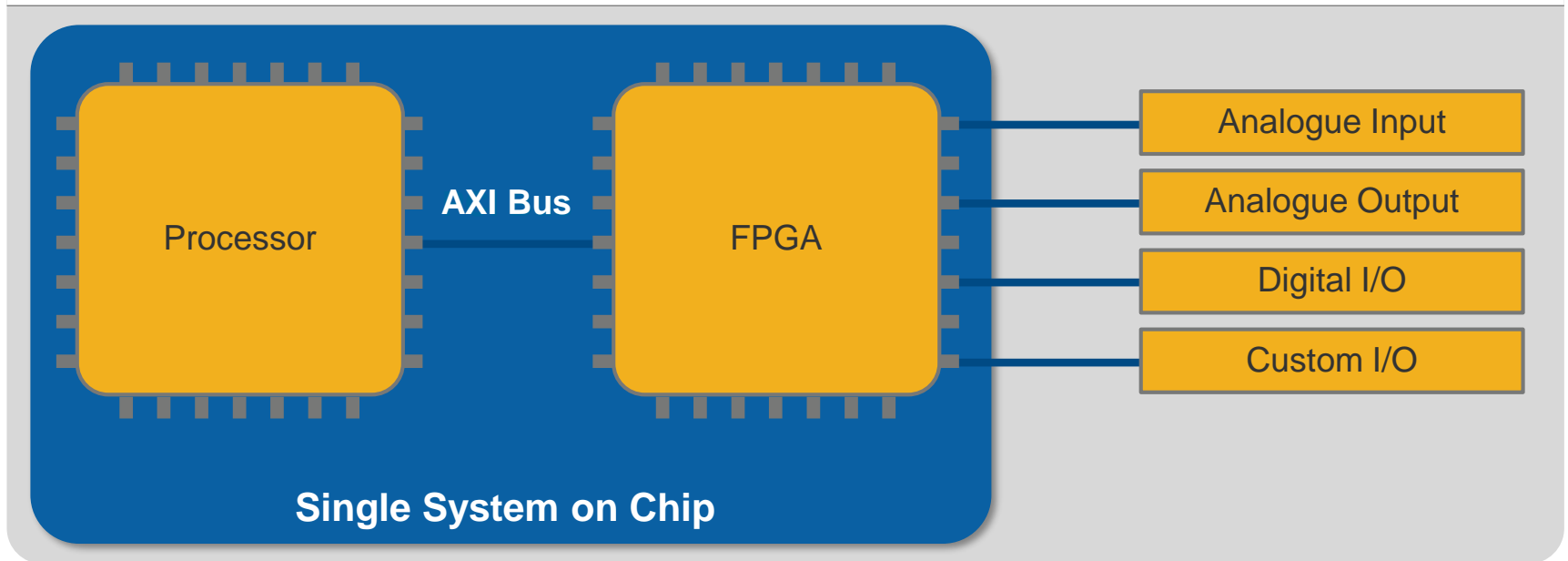
Why Zynq Matters in Education

- Smaller Size, Lower Power

- 667 MHz Dual-Core ARM Cortex-A9 Processor

- Artix-7 FPGA, 28k logic cells

- 16 DMA Channels

- 92 Billion calculations per second

Why Zynq **Really** Matters in Education

Leading Industry Grade Technology

The same technology is used in our latest industry and research ready Compact RIO systems

Robotic Table Football
Revolutionising Mechatronics Education

The Challenge

Students struggled to realise their innovations using textual programming, due to unintuitive syntax and complex hardware integration. Following many research successes, Loughborough wanted to incorporate LabVIEW into their refined Mechatronic module
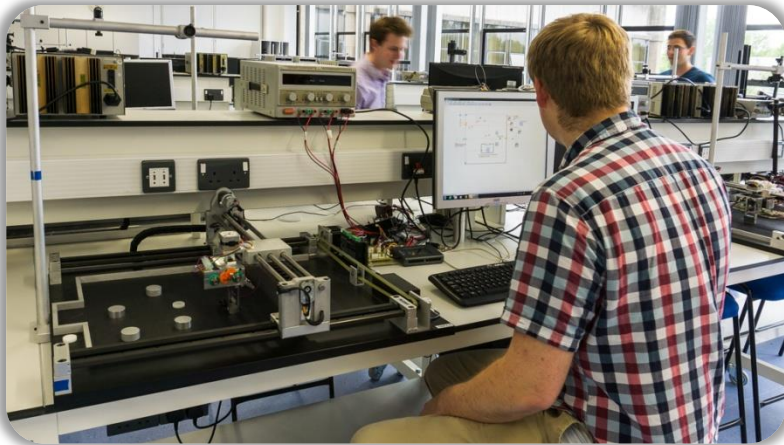
The Solution
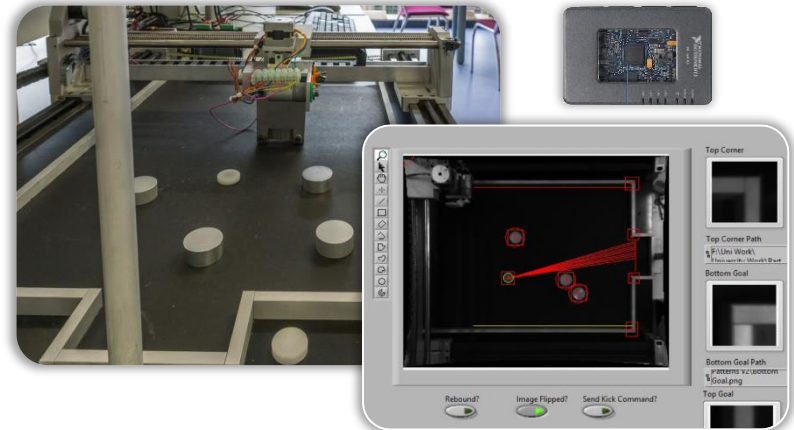
Using **LabVIEW** and **myRIO** to develop the Robotic Table Football challenge. This practical approach to teaching *mechatronic systems integration* resulted in a marked increase in student engagement, improved grades and the best system implementations to date.

Orseus
myRIO in Space

UNIVERSITÉ PARIS SUD

IUT D'ORSAY

The Challenge
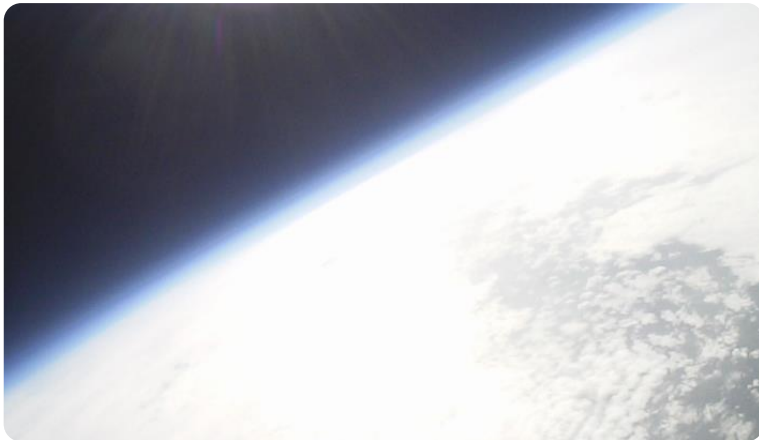
Developing an embedded system which operates under low pressure and temperature conditions - **space**. The system must carry out various experiments, including the study of solar radiation and atmospheric pollution

The Solution

Final Payload

Onboard Camera

Radio Communication

Using **myRIO** to control all on-board sensors and experimental equipment in a high altitude balloon, from the launch to the landing with real time monitoring and post processing.

Student Design Contest Winner 2014

Sepios, the Omnidirectional Cuttlefish Robot

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

The Challenge

Creating a nautical robot driven by cuttlefish inspired fins to study this unique propulsion mechanism and its advantages

The Solution

A four-finned robot, each fin equipped with nine servo motors to generate waves of various shapes and perform any conceivable manoeuver. All this is coordinated by a single NI myRIO at the heart of the drone.
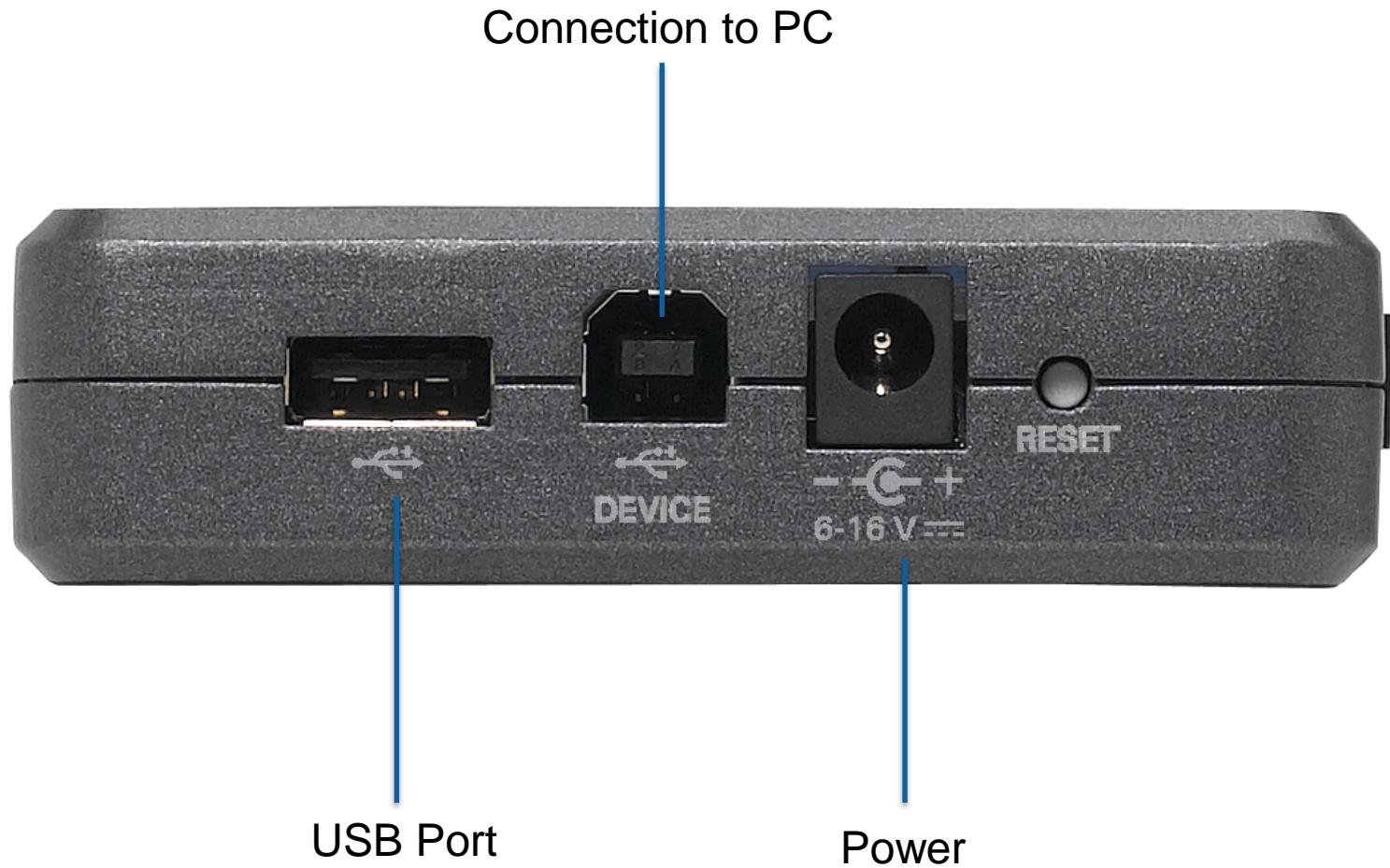
NI myRIO Product Overview: Front View
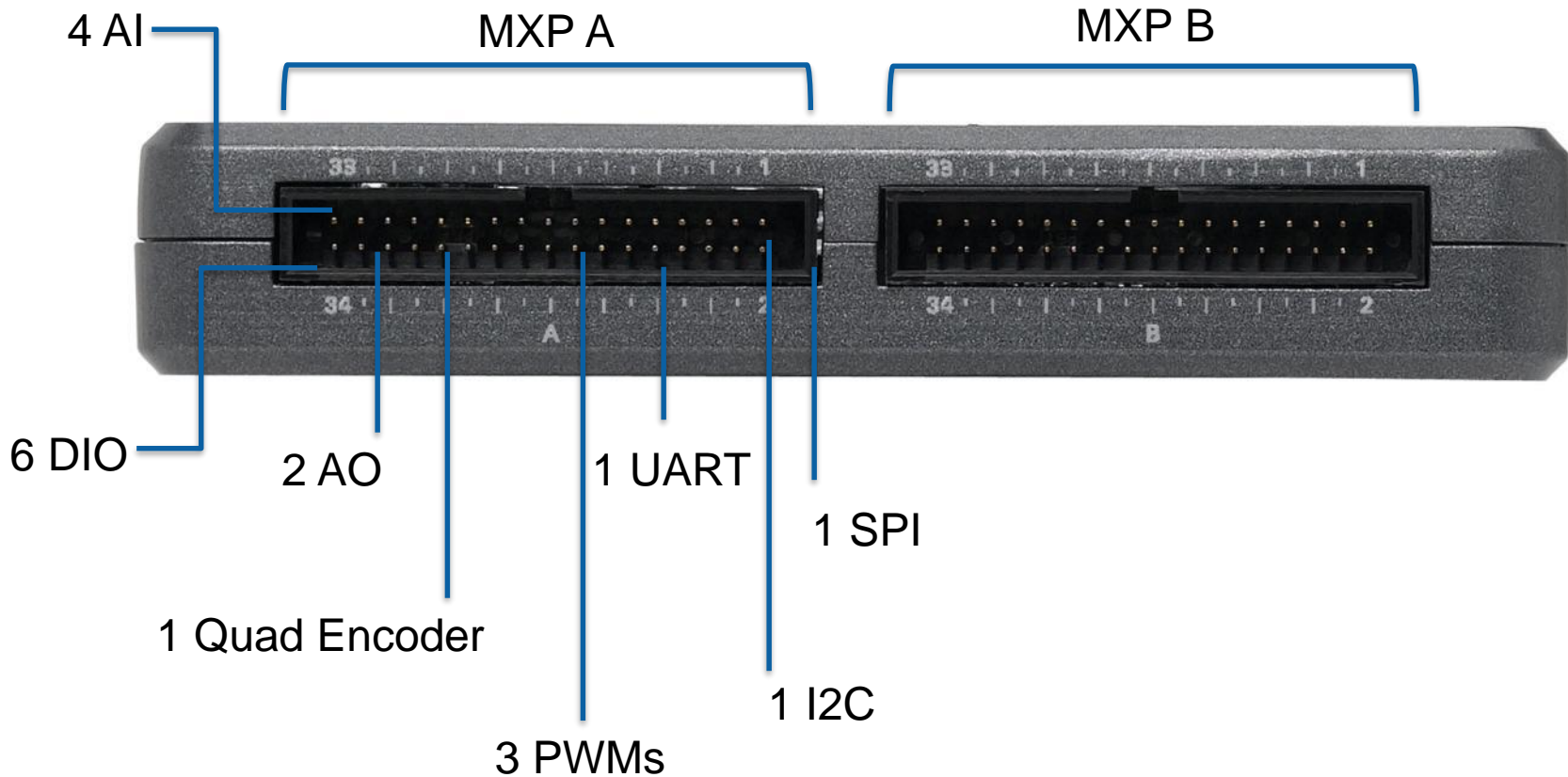
User Defined LEDs

Built-in Accelerometer

Top View

Connection to PC

USB Port   Power

NI myRIO Expansion Port (MXP)

Identical Connectors

4 AI

MXP A

MXP B

6 DIO

2 AO

1 Quad Encoder

3 PWMs

1 UART

1 I2C

1 SPI

NI miniSystems Port (MSP)

Audio in/out   more analog and digital I/O

myRIO exercise board

Exercise board

3.3 V

2.2 kΩ

DIO4

DIO0 —— DIO1

DIO2 —— DIO3

5 V

AI0

1 MΩ

AO0 —— AI1

47 kΩ

AI2

10 nF
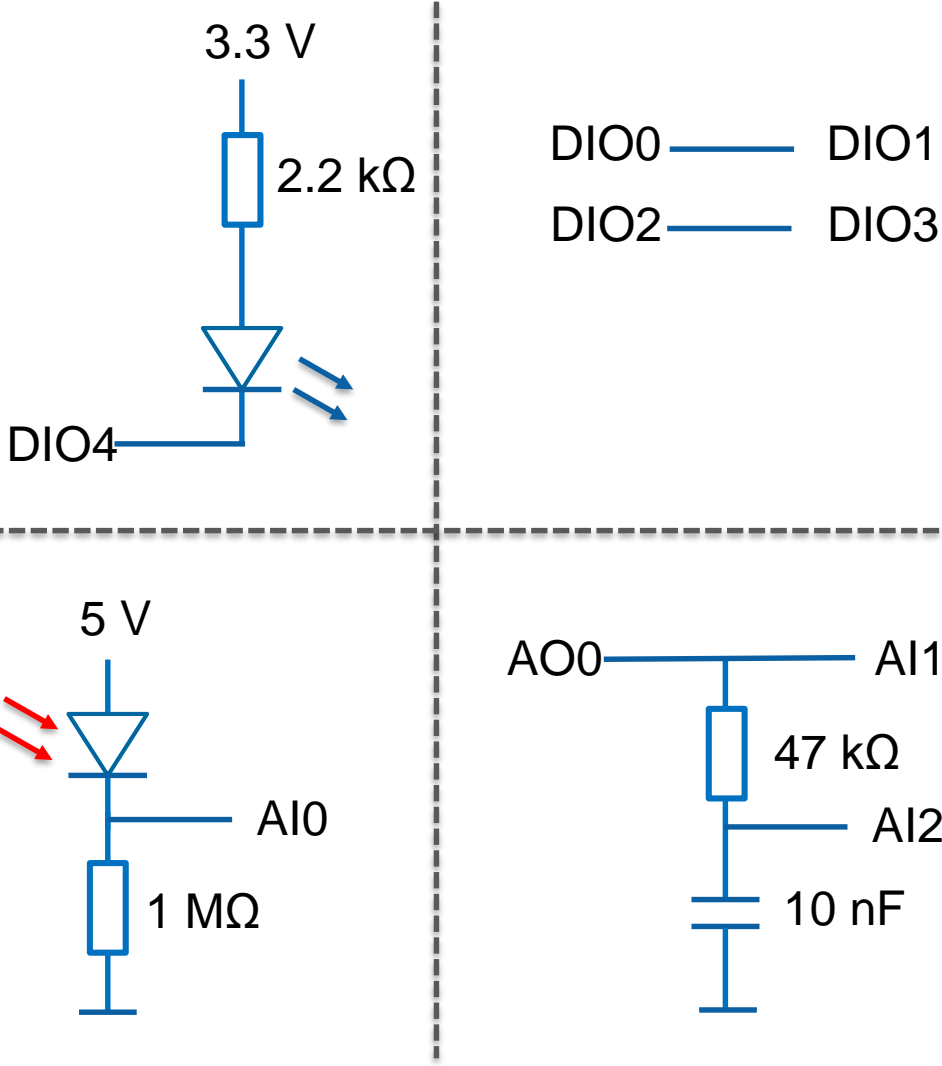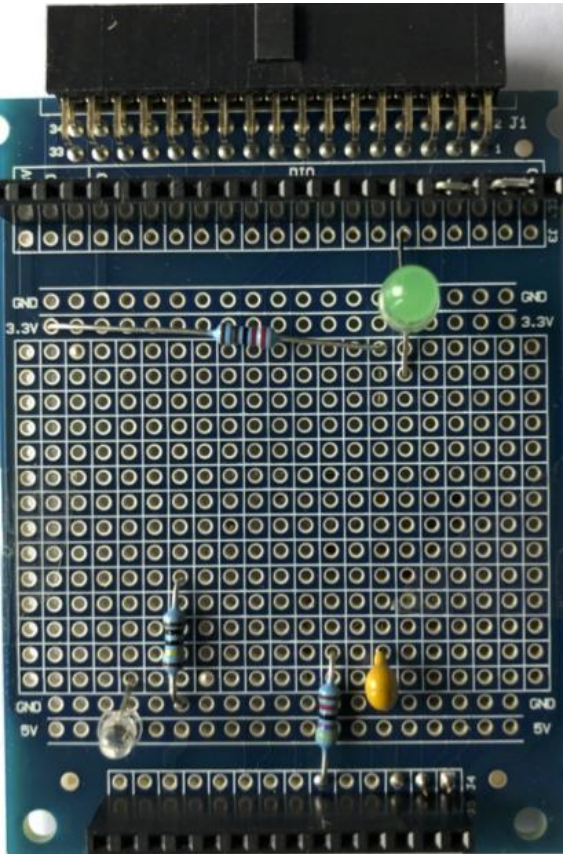
Exercise 1 Blinking LED

3.3 V

47 kΩ

DIO4
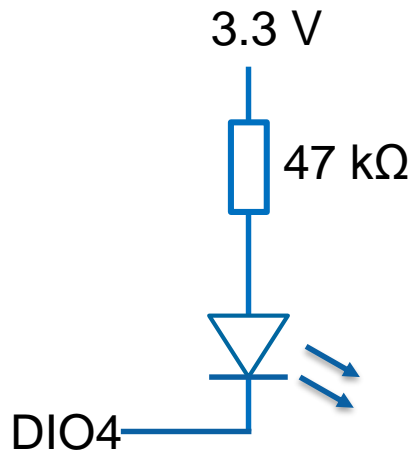
Make the LED blink with a controllable speed from 1 to 40 Hz

Blinking speed [Hz]

20
15   25
10   30
5   35
0   40

10

STOP

Question:
At what frequency you don't see the blinking anymore?

Exercise 2 Switch on when it's dark

5 V   3.3 V

photodiode

2.2 kΩ

AI0

LED

1 MΩ

D4
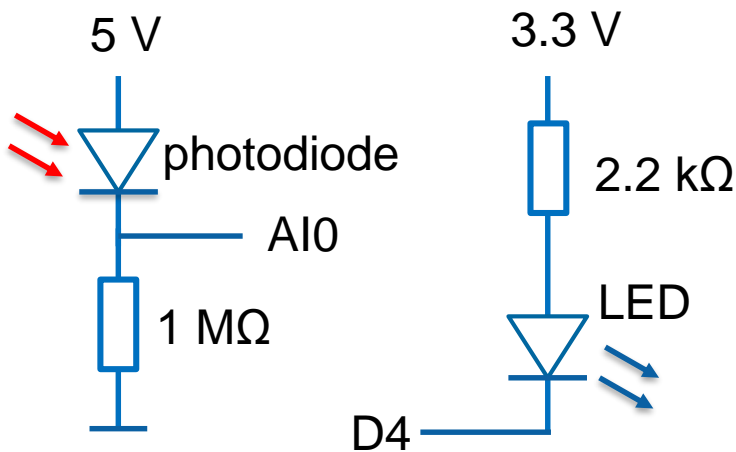
Switch on the LED when the photodiode signal is below the threshold 100 (arbritrary units)

- Plot the photodiode signal in a chart
- The threshold value should be set using a control
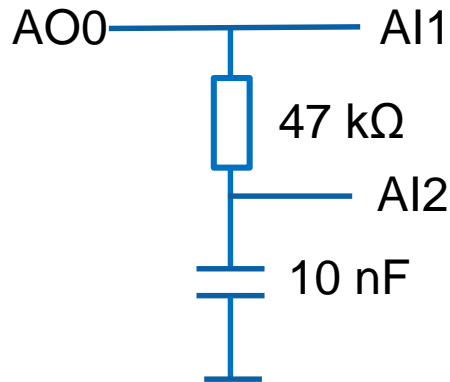- Remember the LED is on when D4 is False

To test, block the light to the photodiode or increase light using your mobile phone
Question:
- What would happen when the photodiode would pick up the LED light?
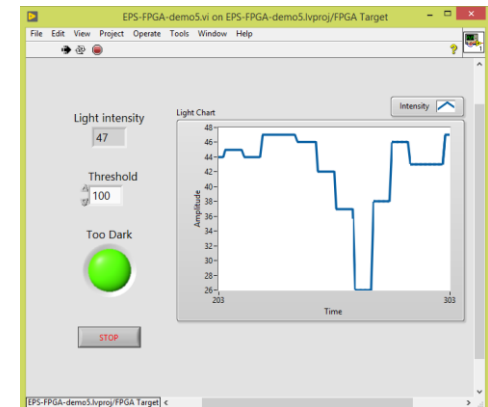
Exercise 3 Acquire transient

AO0 ———————— AI1

47 kΩ

AI2

10 nF

Generate a step function from 0 – 5 V (int. value 4095)

Acquire step function signal and response of RC circuit

- Once per second
- Generate output voltage from 0 to 5 V (and reverse)
- Acquire both AI1 and AI2 signals using 20 points
- Show both in a graph
- RC value is 470 µs
- Set DAQ loop time (with   )s

Questions:
- Is the step function (AI1) really a step?
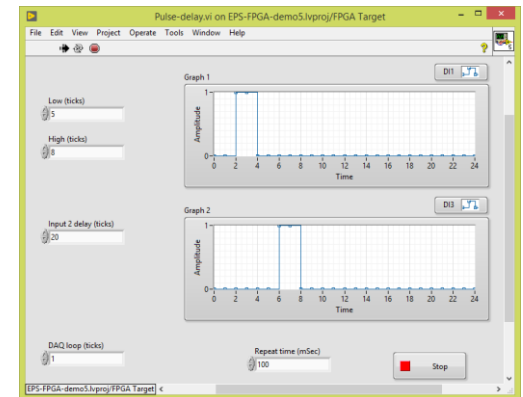- What do you see when changing the DAQ loop time (both AI1 and 2)?
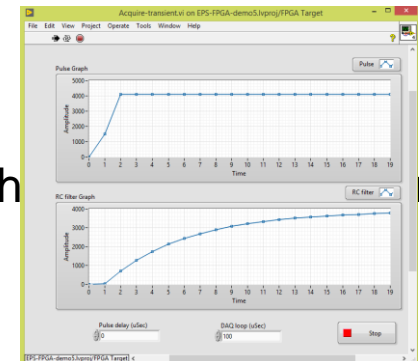
Exercise 4 Pulse delay

DIO0 ⟶ DIO1

DIO2 ⟶ DIO3

Generate short pulse on D0 and D2 (low – high – low)
Make a separate control for low D0 and D2 (using ticks)
Acquire 20 points on D1 and D3 with 1 tick loop delay
Repeat at 100 ms (10 Hz)

- Control for low time of pulse (4 ticks)
- Control for high time of pulse (8 ticks)
- Control for DAQ loop (1 tick)
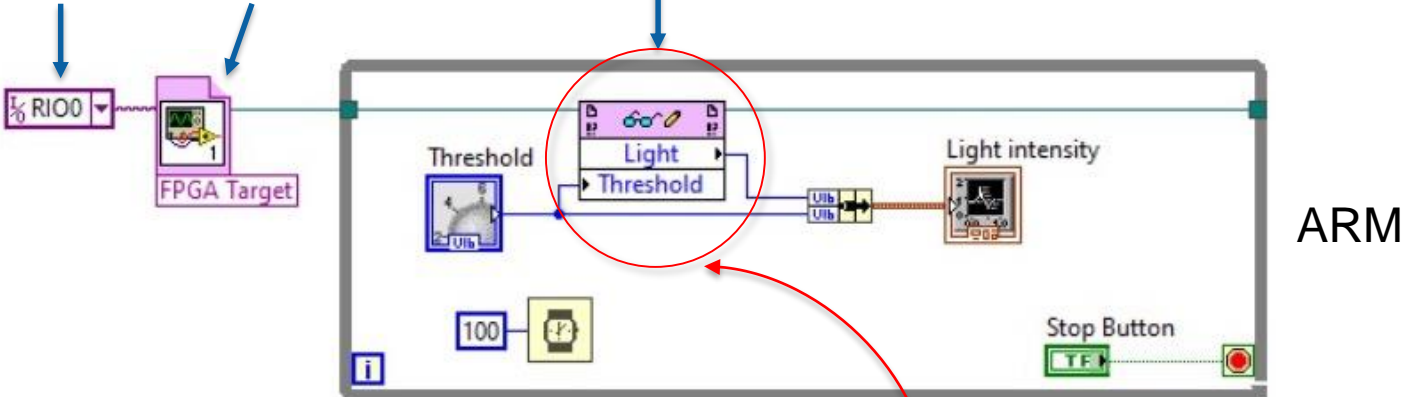- Graph D1
- Graph D3

Questions:
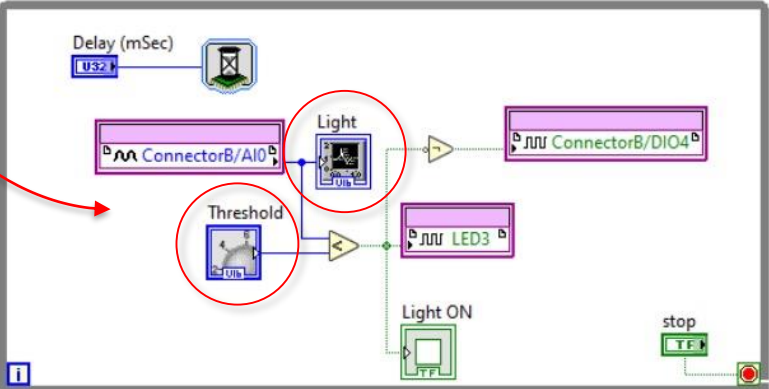- What do you see when changing the high and low values?
- Can you explain?

FPGA to ARM communication

Which myRIO?

Which VI?

Which data?

ARM

FPGA

Resources and Next Steps

NI myRIO Kits | ni.com/myrio

Starter

LEDs & switches
7-segment display
Potentiometer
Thermistor
Photo resistor
Hall effect
Microphone/Speaker
Battery holder
DC motor

Mechatronics

DC gear motors/encoders
H-bridge driver
Accelerometer
Triple-axis gyro
Infrared proximity sensor
Ambient light sensor
Ultrasonic range finder
Compass
Hobby servo motors

Embedded

RFID reader kit
Numeric keypad
LED matrix
Digital potentiometer
Character LCD
Digital temp sensor
EEPROM

From small to big

1. myRIO

2. sbRIO

3. cRIO

4. PXIe R-series boards

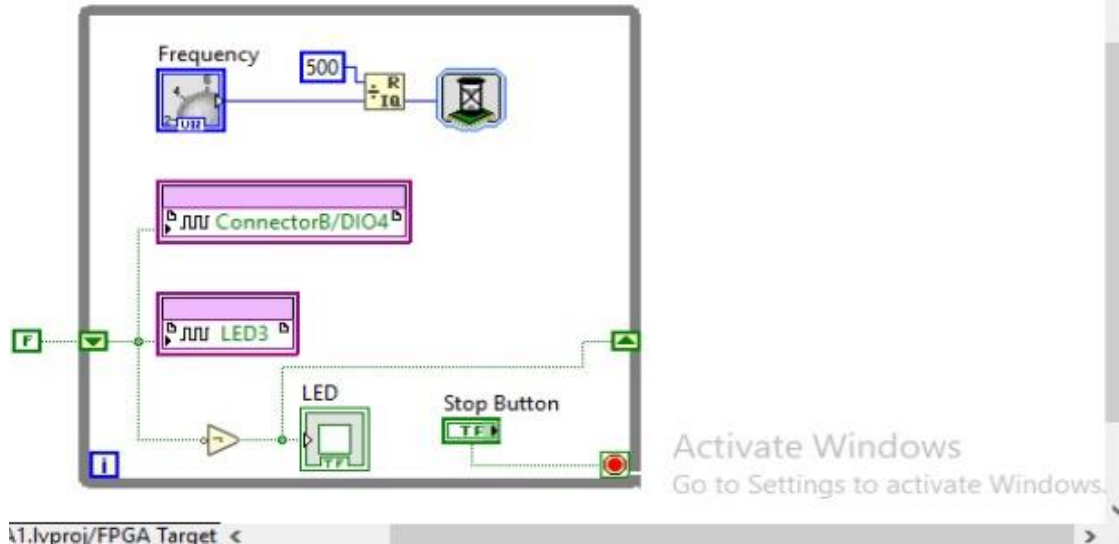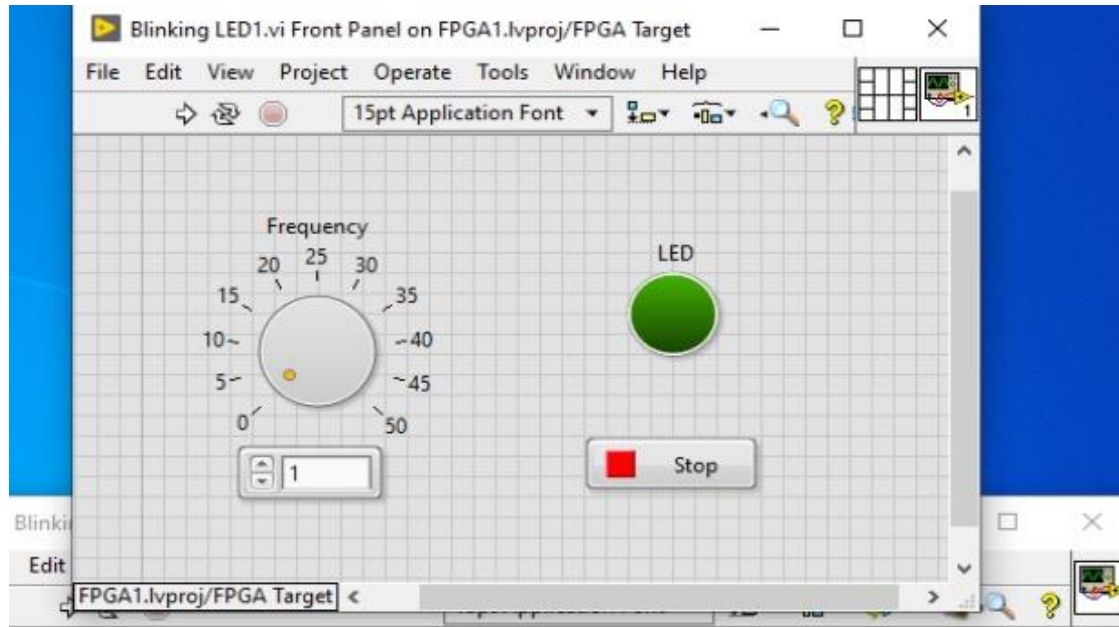5. PXIe FlexRIO boards

Learn More About Programming NI myRIO

ni.com/learn-myRIO
ni.com/community/myrio

Thank you !!!
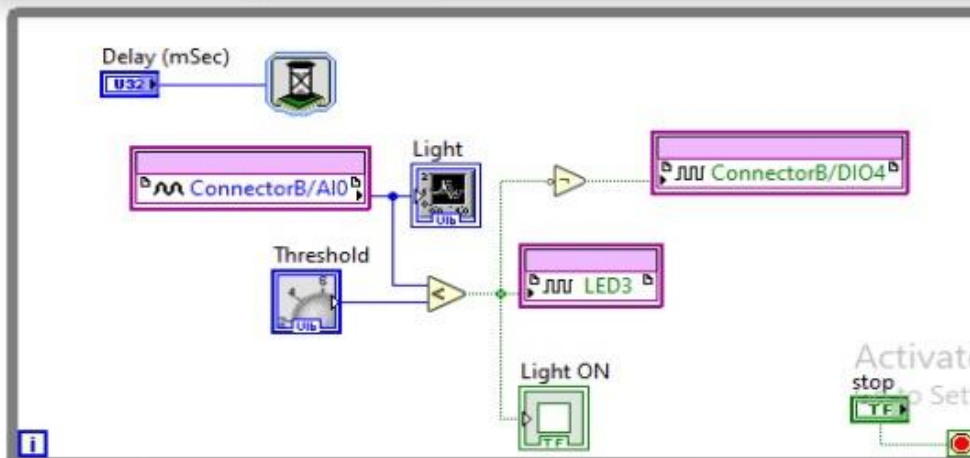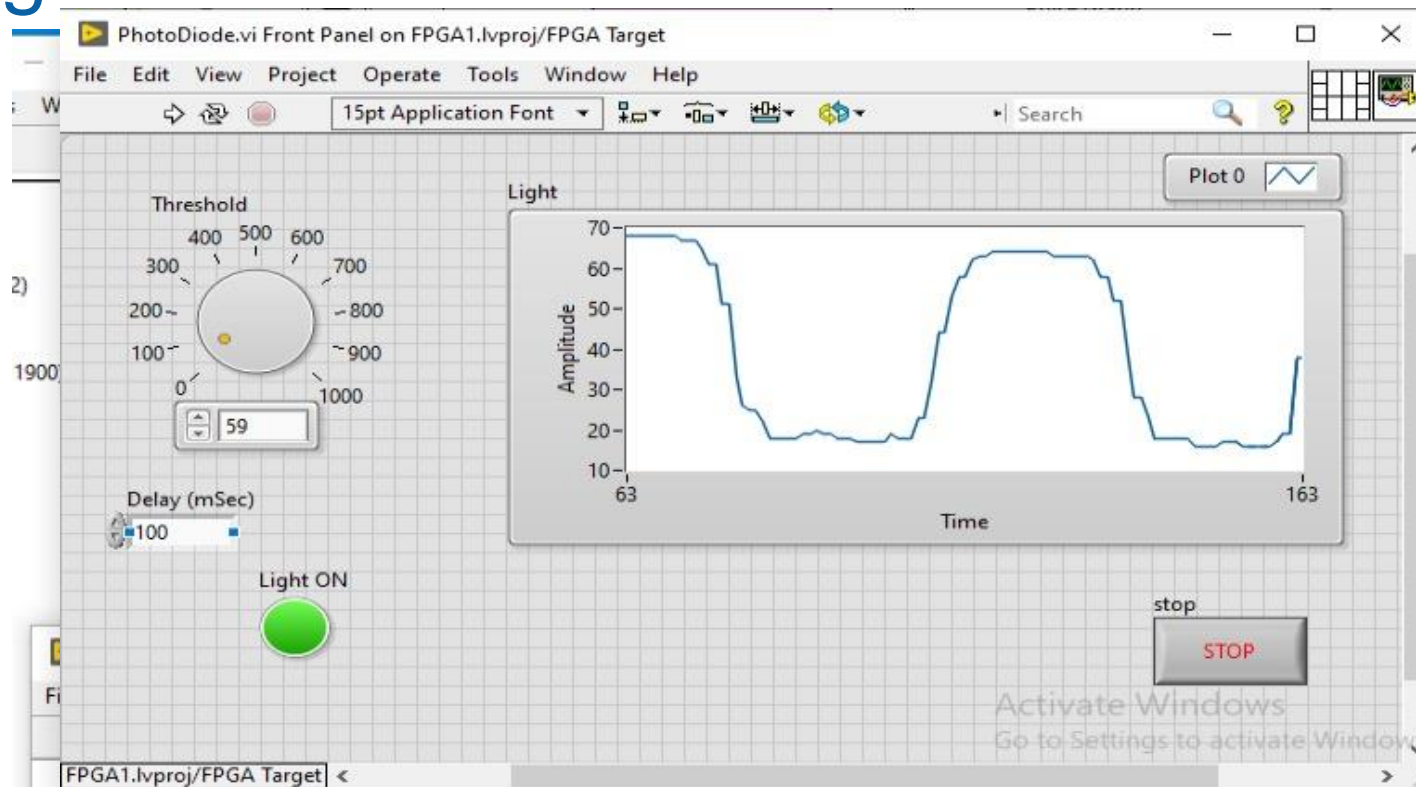
Solutions

Diagram: Blinking LED
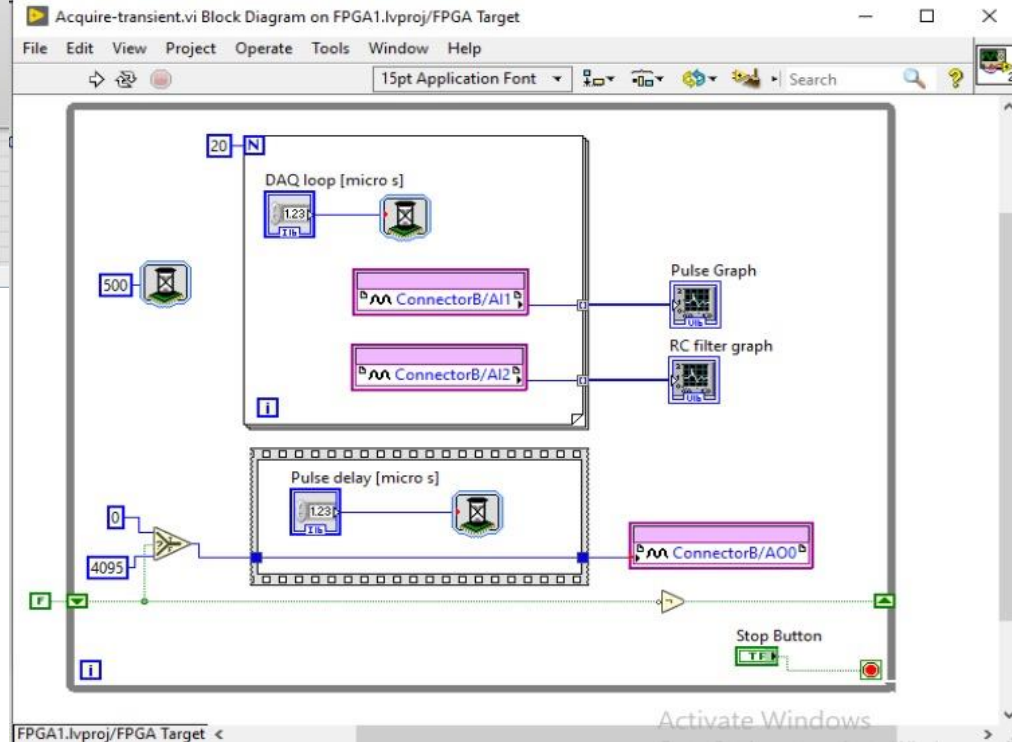
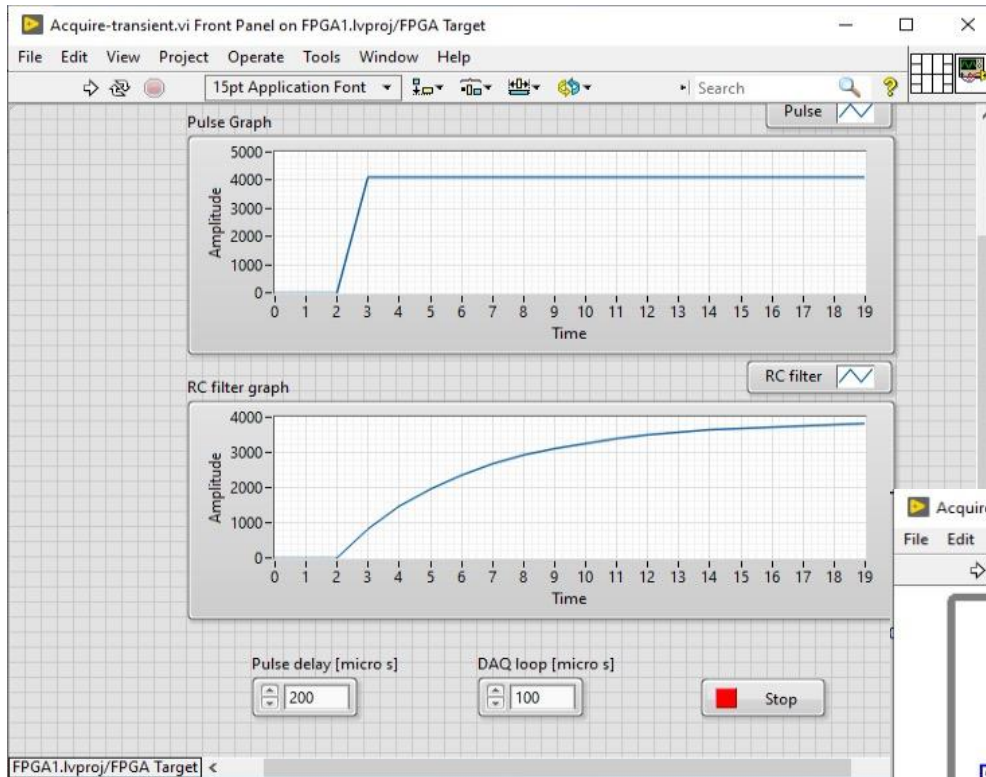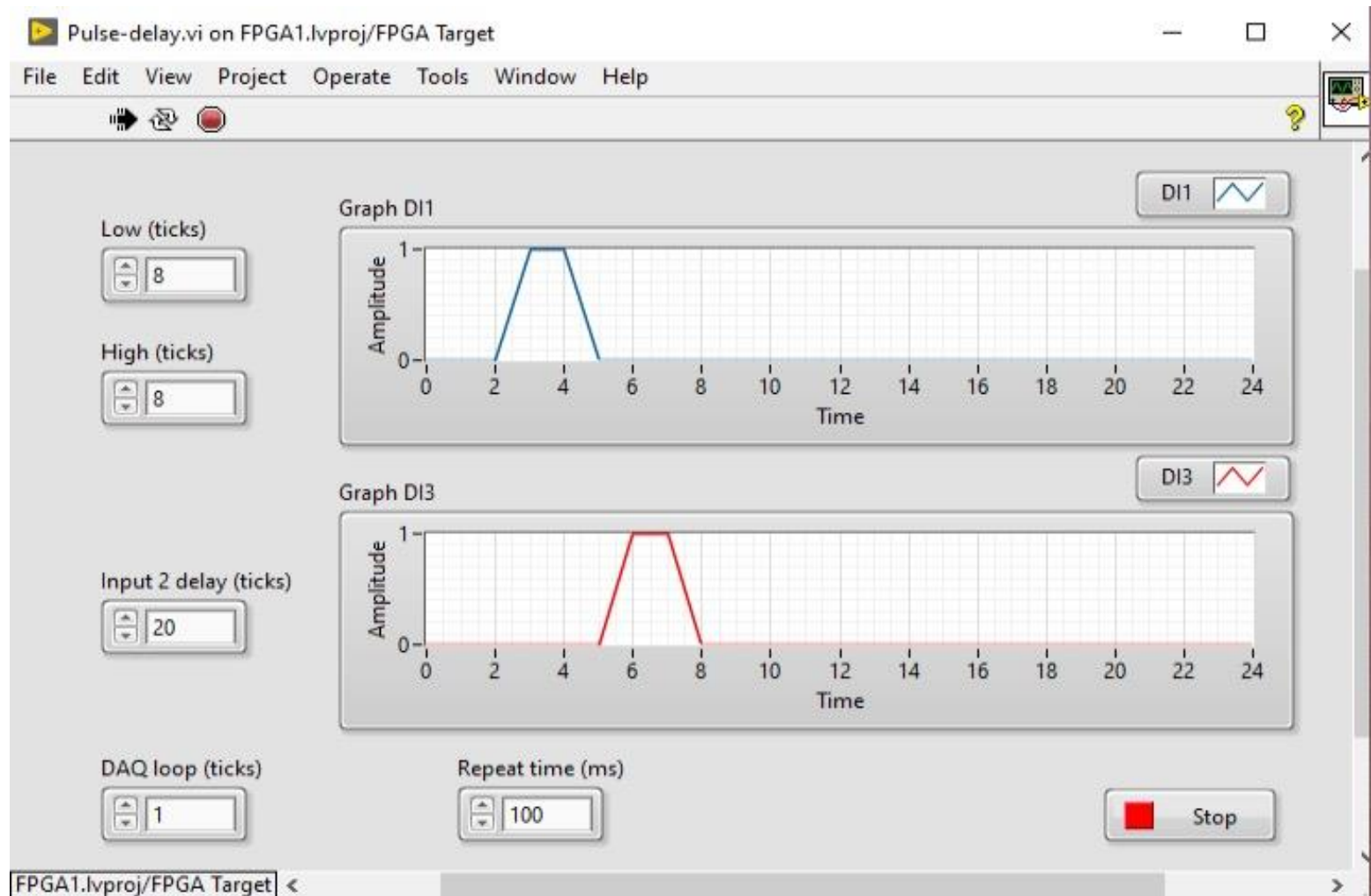# Diagram: Photodiode

Diagram: Acquire transient

Diagram: Pulse delay (front panel)

Diagram: Pulse delay (diagram)