Electronic Systems For Experiments

ESE meets BI

June 14 2021

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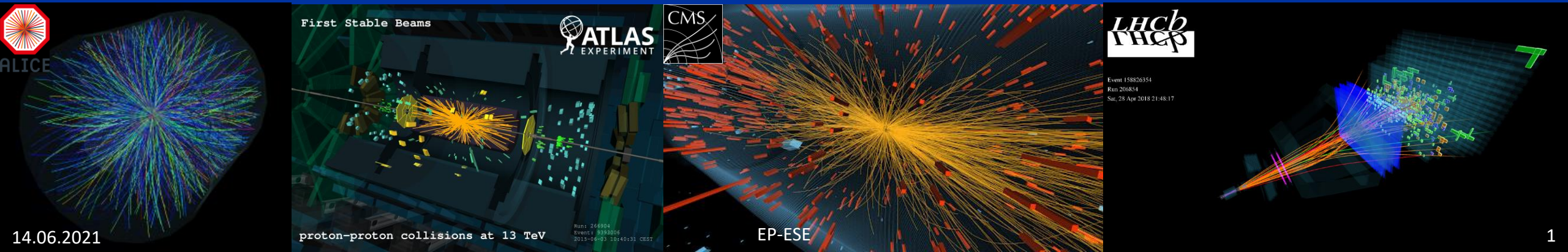
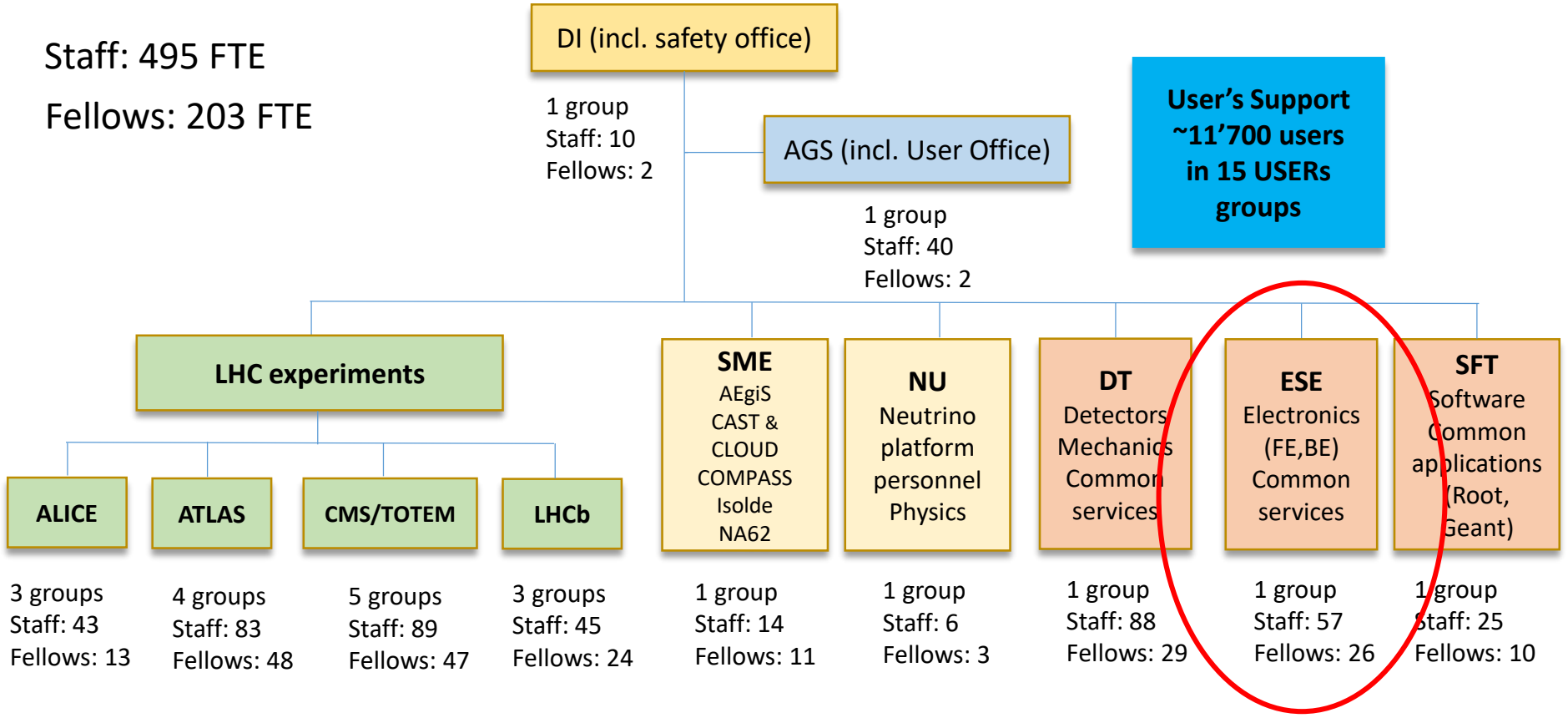


EP Department Structure

Staff: 495 FTE

Fellows: 203 FTE

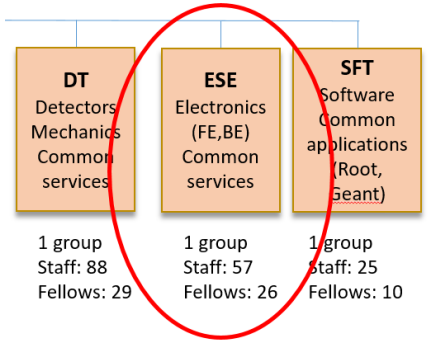


~90% of resources are focused on LHC experiments and their upgrades

The EP-ESE Group

designs and maintains Electronic Systems for the Experiments *at CERN* and supplies a series of **electronics related services**.

- Development/qualification/production/maintenance of specific technologies and products required for experiments
  - Radiation-hard ASICs, electronics, systems
  - Common building blocks: Optical links, Power conversion, Control/monitoring
  - Readout electronics of detectors: from sensors to processor farms
  - Infrastructure: Crates, Racks, Power supplies
- Services
  - Microelectronic design, electronics pool, crates and power supplies procurement
- Electronics coordination
  - "Electronic Project Management" for experiments
  - CERN ESE is at the center of wide collaborations from all over the world for design, prototyping, testing, production…



We estimate that CERN contributes ~20% to the electronics of the experiments.

Electronics for Experiments

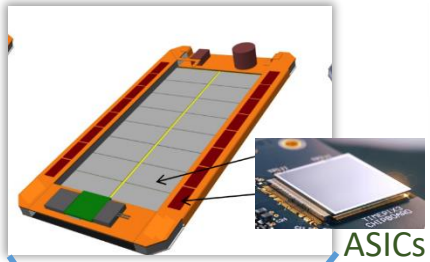
ON DETECTOR ELECTRONICS (FRONT-END)

OFF DETECTOR ELECTRONICS (BACK-END)

OPTICAL DATA LINKS
(100-300m)

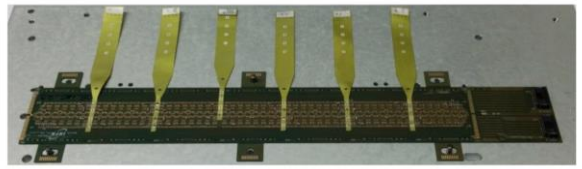
Electronics for Experiments

ON DETECTOR ELECTRONICS (FRONT-END)

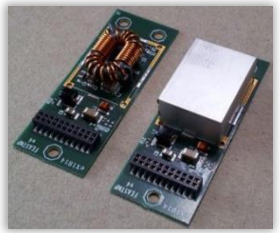


ASICs

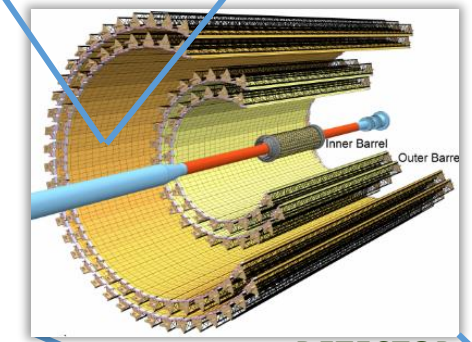
SENSOR MODULE



Interconnects



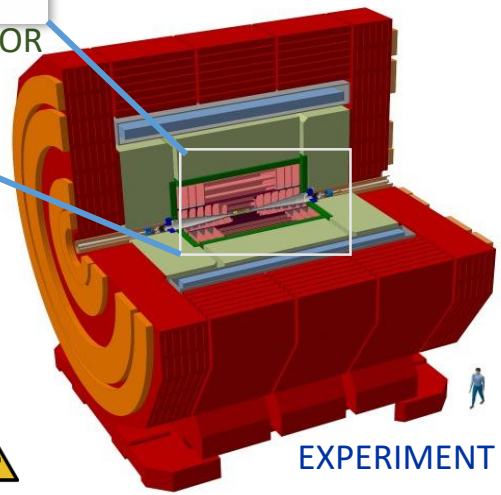
Power



DETECTOR

Optics

OPTICAL DATA LINKS
(100-300m)



EXPERIMENT

OFF DETECTOR ELECTRONICS (BACK-END)

CONTROL - READOUT

RACKS & SHELVES

BOARDS

POWER SUPPLIES

Electronics for Experiments: Common Projects

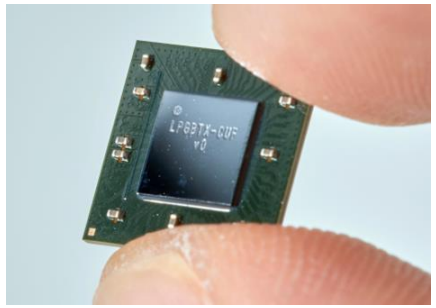
ON DETECTOR ELECTRONICS (FRONT-END)

OFF DETECTOR ELECTRONICS (BACK-END)

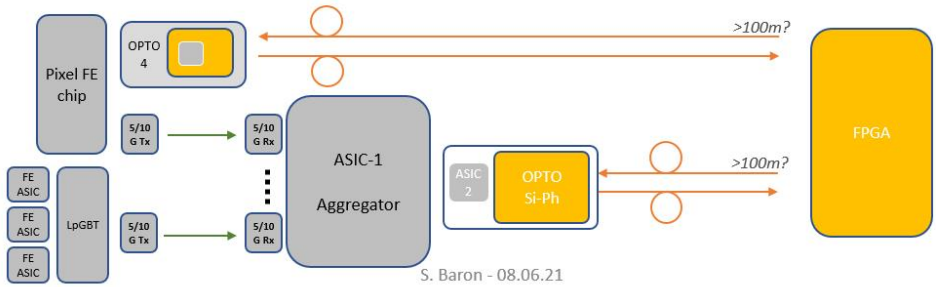
OPTICAL DATA LINKS
(100-300m)

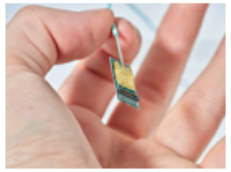
Common Projects: 1. Links, timing, infrastucture

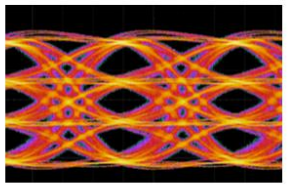
ON DETECTOR ELECTRONICS (FRONT-END)



- EP RnD WP6 *Links*
  - Future Rad Hard high speed links
    - Upstream (from Front-End to Back-End)
    - NRZ-28 (28 Gbps) or PAM-4 (56 Gbps)
  - ESE-BE
    - Back-End: COTS Studies
      - PAM-4 and NRZ-28 COTS characterization (O/E transceivers and FPGAs)
      - FEC studies and design for future upstream links
    - Front End: Silicon Photonics
      - Photonics chip including
        - Ge Photodiodes, Modulators and polarization structures
        - Structures for both O-band optics and C-band WDM
        - PAM-4 and NRZ-28
      - Studies on simulation, characterization, radiation hardness
      - Packaging
    - Asics are handled by ME section in the same Work Package

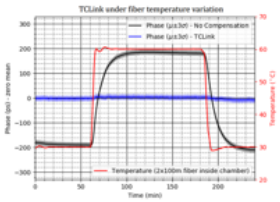




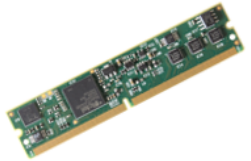


- Links
  - Versatile Link
    - VTRx design, production and support
    - GBTx support
  - Versatile Link +
    - VTRx+ design, production and support
    - lpGBT support
  - CWDM Optical Links
    - Design, qualification, production

OPTICAL DATA LINKS
(100-300m)



- TTC
  - Legacy system Support
  - RF to TTC backbone
  - TTC-PON design and support (LHCb & ALICE)
- HPTD (High Precision Timing Distribution)
  - Interest Group
  - Guidance to users
  - Timing lab
  - Hardware & Firmware studies, design and support
    - HPT Clock Generator
    - Tx Phase Aligner, TCLink



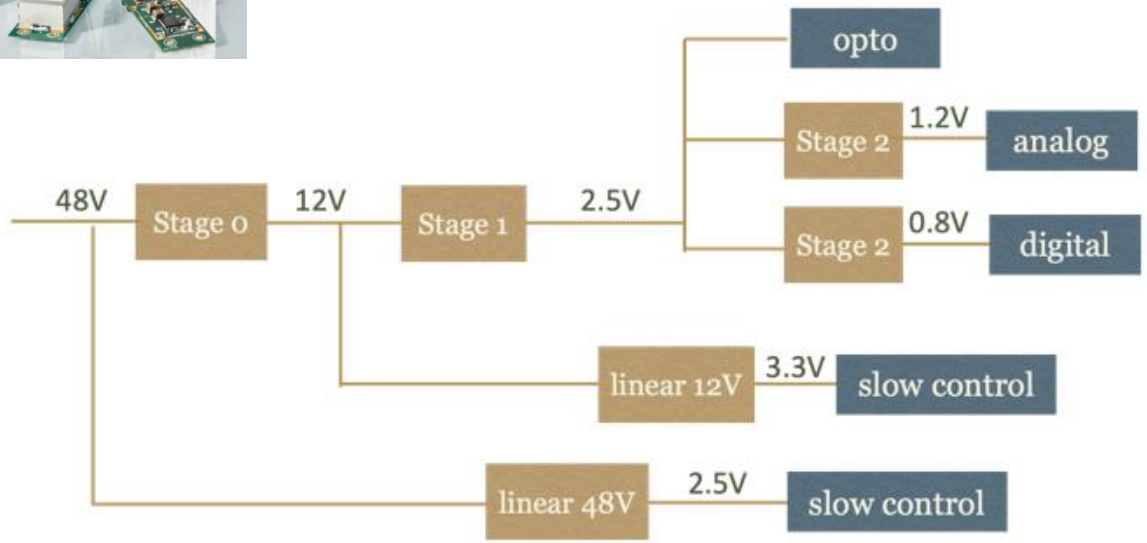
- xTCA
  - xTCA interest group
  - ATCA common infrastructure procurement framework & support
  - IPMC design, production and support
- SoC
  - Interest Group
    - Large community.
    - SoC usage: x10 between LS1 and LS3
    - Sharing experience in HW & SW,
    - Lobbying to get ARM supported at CERN.

Common Projects: 2. Power

ON DETECTOR ELECTRONICS (FRONT-END)

OFF DETECTOR ELECTRONICS (BACK-END)

EP-ESE has developed a family of components allowing the assembly of a flexible power distribution system. These components are represented in this example distribution scheme.



- Low and high voltage supplies for detectors

Common Projects: 2. Power

Radiation Tolerant DC/DC converters

This table presents the components that are or will soon be available for power distribution

Nomenclature XYYYz	x = buck, resonant, linear, driver YYY=POL(Point Of Load) or GaN z = input voltage rating (48V, 12V, 2V5, etc.)

	Name	Type	Vin max	Iout max	Technology	Radiation specs	Package	Availability
Stage0	bPOL48V	DCDC buck (controller + commercial GaN power stage)	48V	15A	350nm CMOS with High Voltage extension at 80V (controller)	>50Mrad (limit TBC) 5e14 n/cm² (TBC) SEE "immune"	Controller in QFN32 + commercial GaN power stage with bumps for flip-chip	Close to production readiness
Stage1	FEAST2	DCDC buck	12V	4 A	350nm CMOS with High Voltage extension at 80V	150Mrad 5e14 n/cm² SEE "immune"	QFN32	Being phased out and replaced by bPOL12V
	bPOL12V	DCDC buck	11V or 12V (TBD)	4 A	350nm CMOS with High Voltage extension at 25V	150Mrad 2e15 n/cm² SEE "immune"	QFN32	Close to production readiness
Stage2	bPOL2V5	DCDC buck	2.5V	3 A	130nm CMOS	150Mrad 7e15 n/cm² SEE "immune"	Naked chip with bumps for flip-chip	✓
	rPOL2V5	DCDC resonant switched capacitor	2.5V	3 A	130nm CMOS	150Mrad 7e15 n/cm² SEE "immune"	Naked chip with bumps for flip-chip	Final phase of R&D
Linear	linPOL48V	Linear regulator	48V	200mA	350nm CMOS with High Voltage extension at 80V	150Mrad 5e14 n/cm² (TBC) SEE "immune"	DFN8	Close to production readiness
	linPOL12V	Linear regulator	12V	80 mA	350nm CMOS with High Voltage extension at 25V	150Mrad 2e15 n/cm² SEE "immune"	DFN8	✓

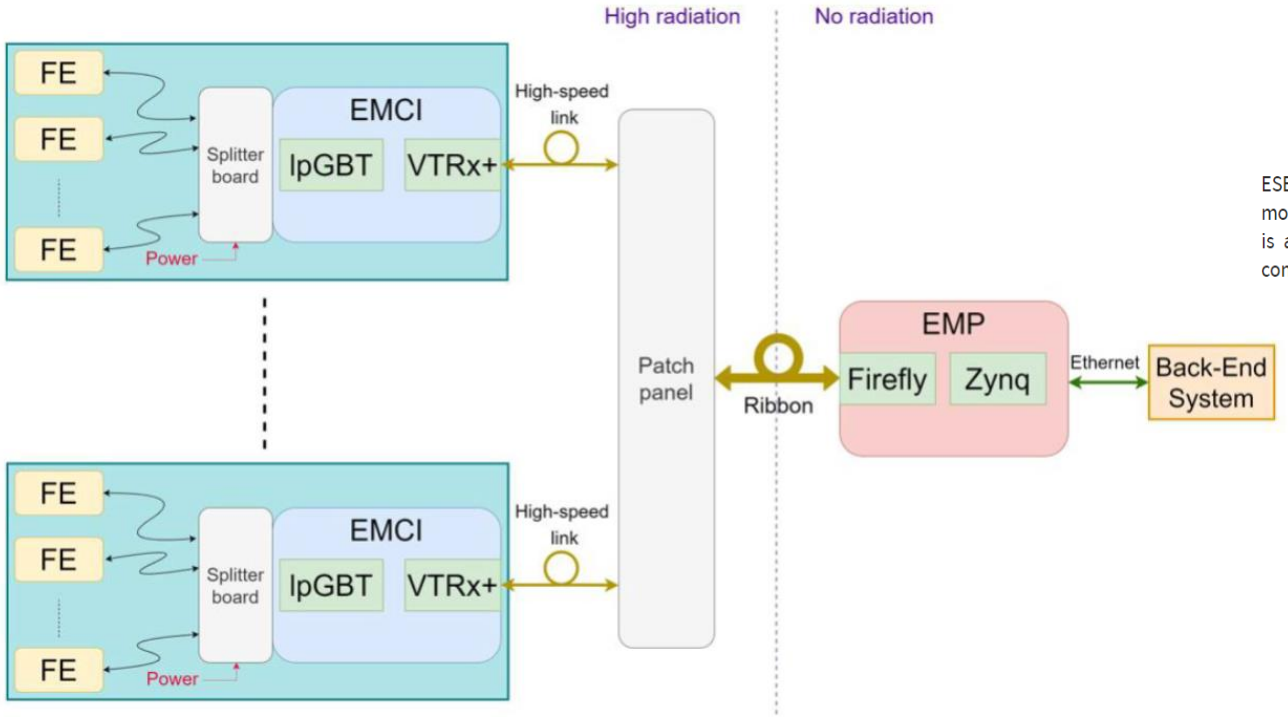
Information and datasheets available at: https://espace.cern.ch/project-DCDC-new

Common Projects: 3. Control/Monitoring

ON DETECTOR ELECTRONICS (FRONT-END)

OFF DETECTOR ELECTRONICS (BACK-END)

ESE is now designing a new system consisting of the Embedded Monitoring and Control Interface (EMCI) and the Embedded Monitoring Processor (EMP). The goal is to provide a scaleable interface for slow-controls and monitoring between the front-end electronics and the detector control system. The EMCI uses radiation-hardened components and will thus tolerate much higher levels of radiation than the ELMB2. The concept is illustrated below.



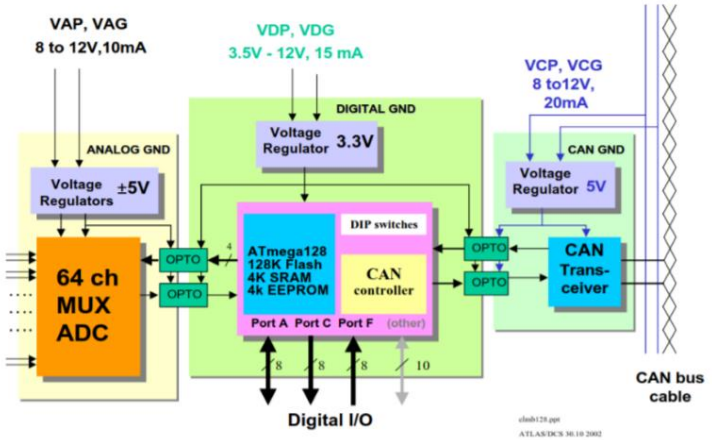
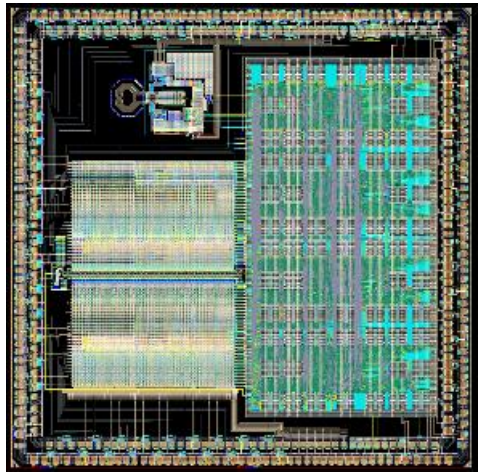


Figure 1: Architecture of the ELMB

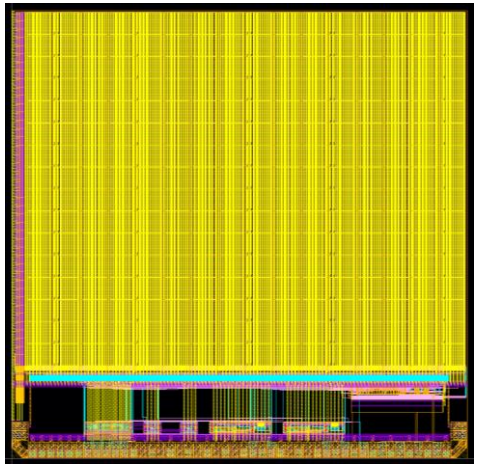
ESE has designed, tested and produced the **E**mbedded **L**ocal **M**onitor **B**oard **2** *(ELMB2)*. This is a general purpose plug-on I/O module for the monitoring and control of sub-detector front-end components, and uses commercial-off-the-shelf components. It is a replacement for the obsolete ELMB and tolerates higher levels of radiation than its predecessor. The ELMB2 is fully compatible with the infrastructure of the ELMB (motherboards, power, CAN-bus interface).

Other ESE projects of possible interest to BI (?)

picoTDC
Final version at packaging stage

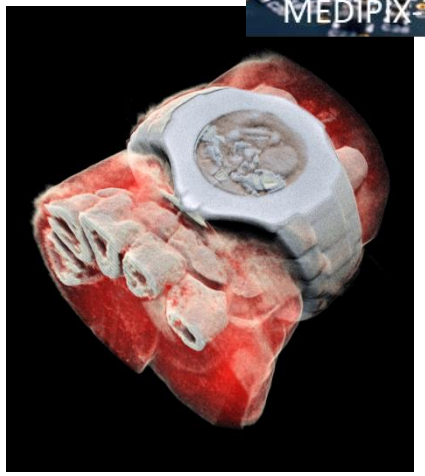


Monolithic CMOS pixel detectors
ALPIDE
MALTA
CLICTD



Hybrid pixel detectors
Medipix
First spectroscopic image of living human using Medipix3

2020> Timepix4



Medipix Timepix family

Collaboration	2003	2006	2013	2014	2017	2018	2020	2021	2023?
Medipix2	Medipix2	Timepix				Timepix2			
Medipix3			Medipix3	Timepix3					
Medipix4							Timepix4	Medipix4	
LHCb					VELOpix				VELOpix2

- Medipix chips aim at energy sensitive photon counting and typically use frame-based readout
- Timepix chips are more oriented towards single particle detection

Medipix Timepix family

	Timepix	Timepix2	Timepix3	Timepix4
Tech. node (nm)	250	130	130	65
Year	2005	2018	2013	2019
Pixel size (μm)	55	55	55	55
# pixels (x x y)	256 x 256	256 x 256	256 x 256	448 x 512
Time bin (resolution)	10ns	10ns	1.5ns	200ps
Readout architecture	Frame based (sequential R/W)	Frame based (sequential or continuous R/W)	Event driven or Frame based (sequential R/W)	Event driven or Frame-base (sequential or continuous R/W)
Number of sides for tiling	3	3	3	4

Timepix 4 specifications

			Timepix3 (2013)	Timepix4 (2018/19)
Technology			130nm – 8 metal	65nm – 10 metal
Pixel Size			55 x 55 µm	55 x 55 µm
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448
Sensitive area			1.98 cm^2	6.94 cm^2
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA	
		Event Packet	48-bit	64-bit
		Max rate	<80 Mhits/s	<715 MHz/cm^2/s
		Max pix rate	1.3kHz/pixel	10.6kHz/pixel
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr) CRW (8-bit / 16-bit) Up to 44 KHz frame @8b
		Max count rate	82 Ghits/cm^2/s	~800 Ghits/cm^2/s
TOT energy resolution			< 2KeV	< 1Kev
Time resolution (bin size)			1.56ns	~200ps
Readout bandwidth			≤5.12Gb (8 x SLVS@640 Mbps)	≤163 Gbps (16 x 10.24 Gbps)
Target global minimum threshold			<500 e^-	<500 e^-