BGI projects status and outlook

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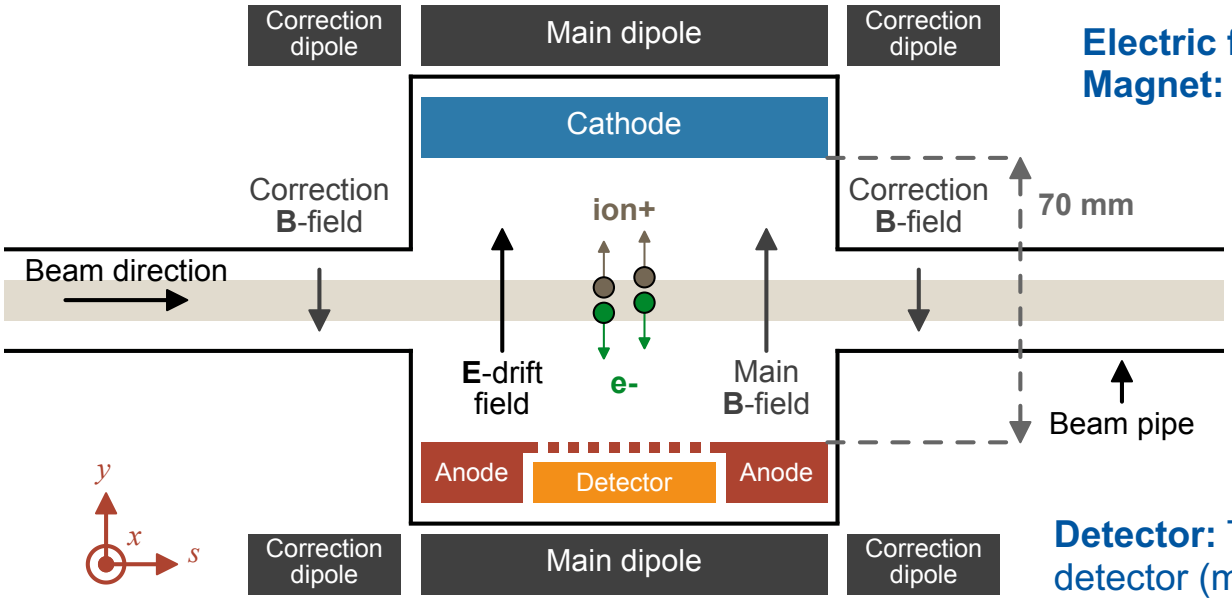
EP-ESE/SY-BI Collaboration Seminar, https://indico.cern.ch/event/1036823

What is a BGI?

Beam gas ionization profile monitor (BGI) - measures the transverse beam profile



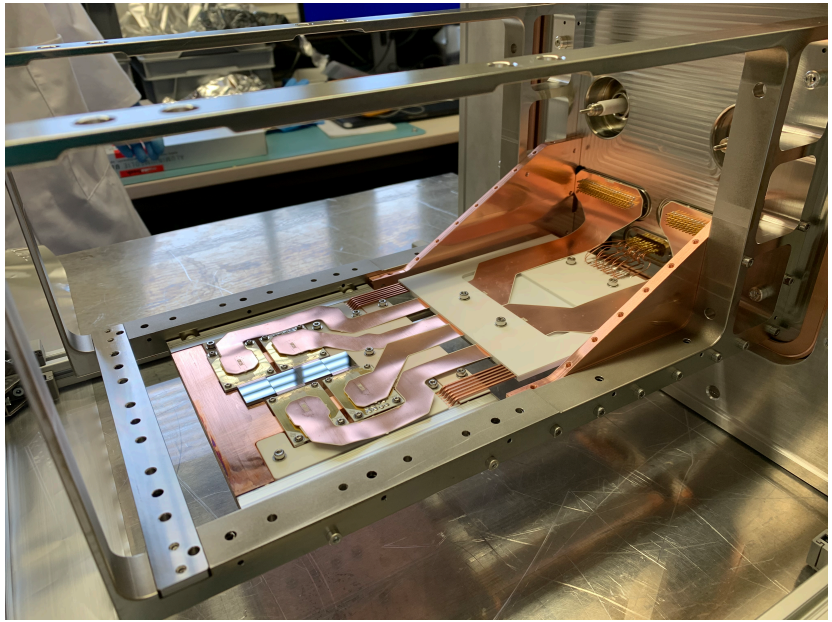
Electric field: 280 kV/m
Magnet: 0.2 T

Detector: Timepix3 hybrid pixel detector (medipix.web.cern.ch)

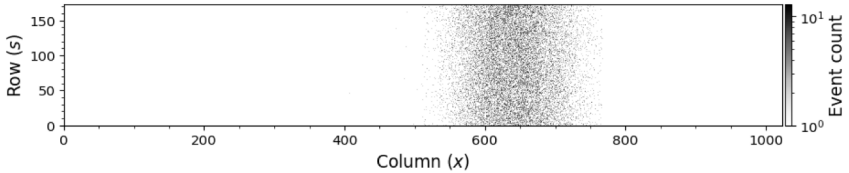
More info on: bgi.web.cern.ch

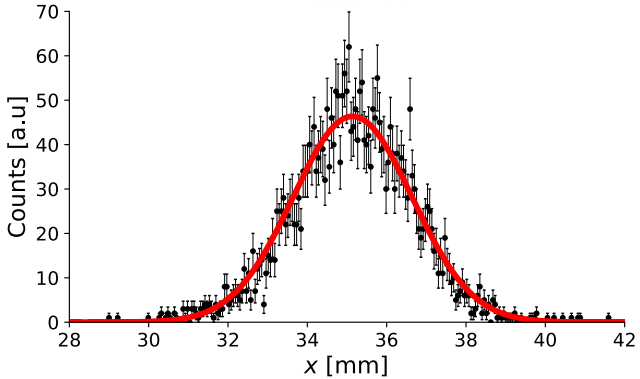
Beam profile monitoring with Timepix3

Timepix3 (EP-ESE) used inside the ultra-high vacuum of the PS, ~35 mm below the beam



4x Timepix3 detectors side-by-side

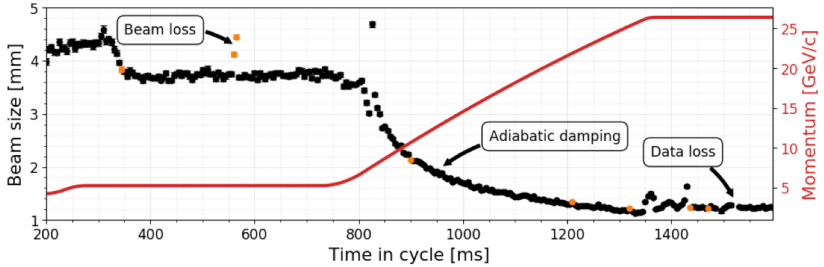




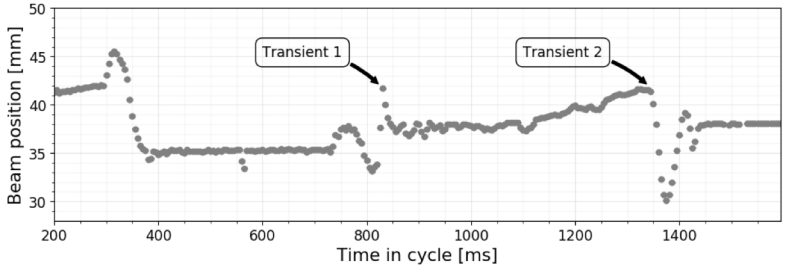
Thanks to Xavi, Michael and Jerome from the Medipix group (EP-ESE) for their help and support!

Measured beam size/position/losses evolution

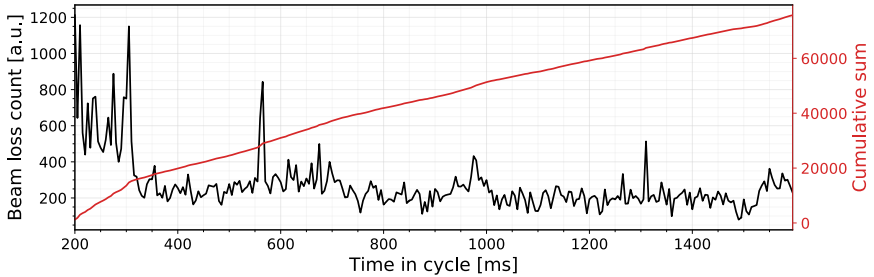
Size



Position



Losses at one location in the PS (SS82)



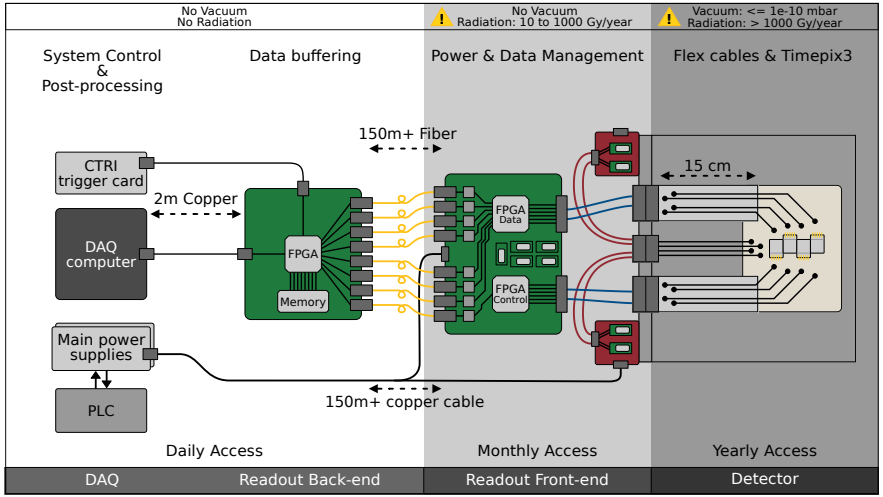
- This is a single LHC INDIV cycle in the PS
- The beam is measured at a rate of 200 kHz
- ~4000 detected ionization electrons per point
- With the PS-BGI instrument we can resolve the evolution of the beam size, position and the losses at the location of the instrument

- Losses shown here are a count of the events, can further refine by categorizing into cluster size and energy (particle identification)

Current BGI readout system

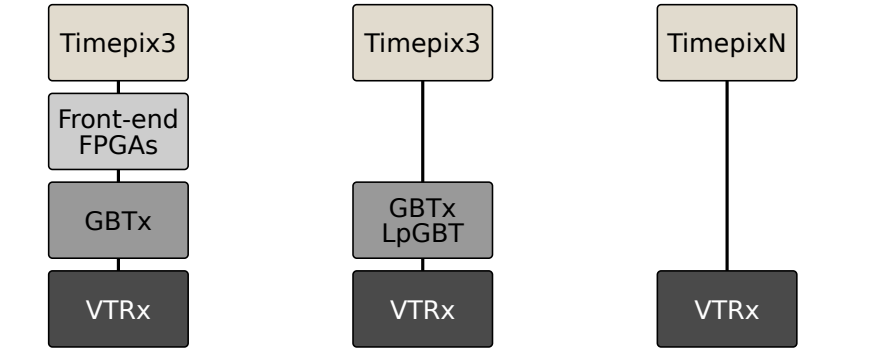
Built around EP-ESE components:

- Timepix3
- GBTx
- GBT-SCA
- FEASTMP
- VTRx
- GBT-FPGA



- The front-end FPGAs send commands to the Timepix3 detectors and synchronize the event packets that are produced
- The packets are routed to 8 optical GBT-links to the back-end FPGA
- The back-end FPGA process and store the events it receives over the links in a buffer memory that is read out by the computer
- A PLC controls all the power supplies and cooling for the in-vacuum Timepix3

Future BGI detector and front-end readout



(a) Current readout (b) Direct connection to GBT transceiver chip (c) Direct connection to optical link

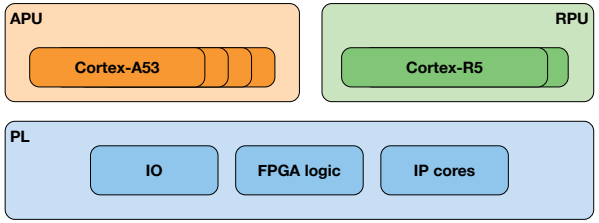
- Option (b) now under study to have a direct connection between Timepix3 and GBTx for improved radiation hardness (no FPGAs in the tunnel) and reduced complexity
- LpGBT, CWDM SM-VTRx and Timepix4 under study for future LHC-BGI
- Timepix3 -> Timepix4 improvements[1]:
  - 3.5x area
  - 8x hit rate
  - 1.5625 ns -> 195 ps time binning
  - 4x time-of-arrival (ToA) dynamic range

[1] https://indico.cern.ch/event/876275/contributions/3729426/

Future BGI back-end readout

Study just started for using Xilinx Zynq UltraScale+ MPSoC in the back-end

- 4x Application processors (APU)
- 2x Real-time processors (RPU)
- Programmable logic (PL)



Primary application is the BGI but could be used a common (CERN wide) Timepix3 readout:

- Two hardware interfaces to Timepix3: 1) remote GBT optical link or 2) local direct connection
- Two software/user interfaces: 1) Standalone operation (Linux OS on the APUs) or 2) API over Ethernet for communication with other computers (e.g. FEC)
- Potential for common (CERN wide) software for testing, calibration, configuration & data acquisition of Timepix3 detectors

See 2021 SoC workshop for more SoC applications at CERN: https://indico.cern.ch/event/996093
BGI Back-End Readout Planning document: https://edms.cern.ch/document/2561212

Questions and comments?